TWEPP 2015 - Topical Workshop on Electronics for Particle Physics



Contribution ID: 148 Type: Plenary

DARE platforms: Past, present, future

Friday, 2 October 2015 10:10 (25 minutes)

Imec has been developing radiation hardened-by-design libraries with additional functionality using different CMOS technologies (.18 UMC and beyond). These DARE (Design Against Radiation Effects) platforms allow re-use, lower development times and risk of the design of circuits that need to withstand radiation. The paper gives an overview of the currently available platforms and their metrics and gives a view on plans for the future

Summary

At the turn of the century imec, building on knowledge built in previous projects with CERN and ESA, started development of radiation hardened-by-design (RhbD) libraries in .18 UMC technology. ESA sponsored this work because the European rad-hard foundries were leaving the market.

Why are we doing this?

Imec is supporting the research community with technology and library solutions since it was founded. Currently imec e.g. is supporting the CERN community in the use of 65nm TSMC technology. Imec's RhbD solutions are open for use by all parties that want to use them in a peaceful manner. We provide the information others need to create their RhbD ASICs.

The solutions are called DARE (Design Against Radiation Effects) Platforms. DARE platforms exist for several technologies in different stages of maturity.

The start: UMC .18

A proof-of-concept project including test chip irradiation allowed defining what a library for .18 UMC technology should look like. UMC .18 being the most advanced technology imec could provide access to via its Europractice activities at that point in time.

A digital core library, I/O library and a single port RAM compiler were created. Since then this platform has been enhanced with additional functionality: clock gating cells, a dual port RAM compiler and analog IP blocks.

Current activities

Imec is supporting the UMC .18 DARE platform in several ASIC designs, including imagers.

UMC .18 doesn't support high voltages and Non-Volatile Memory is unavailable for small volume projects. Creation of an XFAB .18 XH DARE platform is well underway. Test chip design and test is planned.

Radiation hardening goals for this platform were set at a different level than those for UMC DARE; resulting in different power and size metrics.

In cooperation with CERN a 65nm RAM compiler and a comparable solution for 130nm are developed.

Imec created an ADK for I3T80. An ADK is an addition to a PDK supporting RhbD design. The concept will be explained in the full paper.

Future activities: I3T80 & 65nm

Imec is planning to develop a digital library solution of I3T80. Work is going to start on the creation of a 65nm DARE solution. Both of these activities will be performed with ESA funding.

The benefits

 ${\it DARE\ platforms\ are\ radiation\ hardened-by-design\ library\ and\ IP\ block\ solutions\ allowing\ re-use.}$

Re-use

- allows saving money in the design stage, but also in the test and qualification phase, for known-good building

blocks are being used;

- means a lower development time and being able to tap into the specialist capabilities of other teams that you might not have readily available in your team;
- decreases the risk there is in the design in standard CMOS technologies of circuits that need to withstand

DARE platforms are flexible; allowing addition of new elements then becoming part of the platform. Building platform legacy benefits all. Sharing radiation data and design methodology data increases the confidence in the success of the next ASIC.

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Presenter: REDANT, Steven (imec) **Session Classification:** Plenary