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QIE12: A New High-Performance ASIC For the ATLAS TileCal Upgrade

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We present results on the QIE12, a custom ASIC, being developed for the ATLAS TileCal Phase 2 Upgrade. The design features 1.5 fC sensitivity, more than 17 bits of dynamic range with logarithmic response, and an on-chip TDC with one nanosecond resolution. It has a programmable shunt output for monitoring the integrated current. The device operates with no dead-time at 40 MHz, making it ideal for calorimetry at the LHC. We present bench measurements and integration studies that characterize the performance, radiation tolerance measurements, and the design for the ATLAS TileCal detector for the Phase 2 Upgrade.

Summary

The QIE12 is the newest version in the family of QIE devices designed at Fermilab. It integrates and digitizes charge pulses in 25 nS time slices with no dead time. This is accomplished by splitting the input charge onto four different integrator ranges. One of the ranges is selected for digitization based on the signal size, and is digitized using an on-chip, pseudo-logarithmic, 7-bit FADC. The operations are pipelined to achieve no dead time. The output is a floating point value consisting of 7 bits of mantissa, 2 bits of exponent, and a 2-bit "CapID" code to indicate which phase is associated with each result. The resolution is held between 0.7% and 1.4% over the entire dynamic range of the QIE, which is in excess of 17 bits. The device also contains an on-chip TDC with 1 nS resolution. The output code is 16 bits for each crossing, provided by 8 output lines double clocked on each edge of the 40 MHz clock.

This newest version of the QIE has several new features. The addition of a 7th mantissa bit increases the electronics resolution, which is important for the TileCal detector. The TDC resolution was reduced to 1 nS to accommodate the extra mantissa bit. The programmable shunt splits a fraction of the input current and makes it available as an output, which will be used in an external current integrator for continuous current monitoring. The slow control interface has been changed to standard SPI, which will make it more easily integrated into the system. The chip is designed in the AMS 0.35u SiGe BiCMOS process, which provides good radiation-hardness performance.

We currently have fully-functional devices that we have tested at the bench, and have also begun studies with detectors and integration into read-out systems. We have performed radiation tolerance studies, including single-event upset, with more planned over the summer. We are currently beginning the design of a front-end board, which we plan to have functional by the time of the TWEPP meeting. A goal is a full system test in a test beam at CERN in the spring of 2016. Virtues of the front-end design include simplicity and reduced part count, which will contribute to better performance and reliability. We will present the status of the project, including the front-end board design, and our plans going forward.

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