A New ATLAS Muon CSC Readout System with System on Chip Technology on ATCA Platform

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Outline

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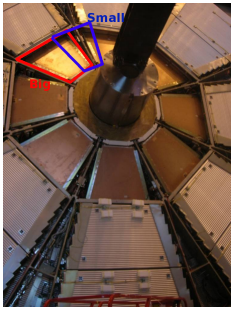
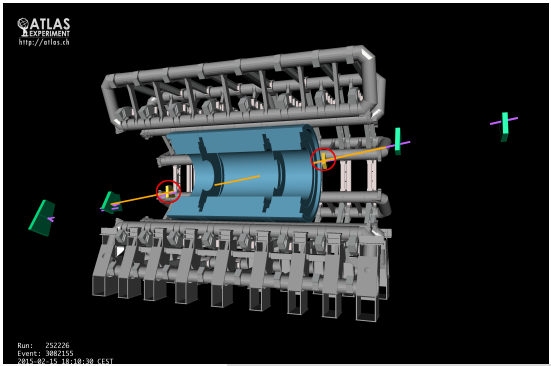
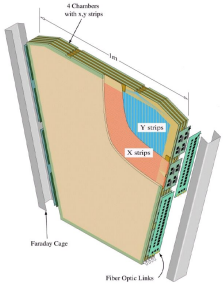
CSC

- Multiwire proportional chambers designed to detect muons in the high pseudorapidity region:
$$2.0 < |\eta| < 2.7$$
- 2 endcaps, with 16 chambers on each side (8 big, 8 small chambers for seamless coverage), each has:
  - 4 precision (η) layers with 768 strips
  - 4 transverse (ϕ) layers with 192 strips
- Very close to interaction point, thus high rate of muons going through

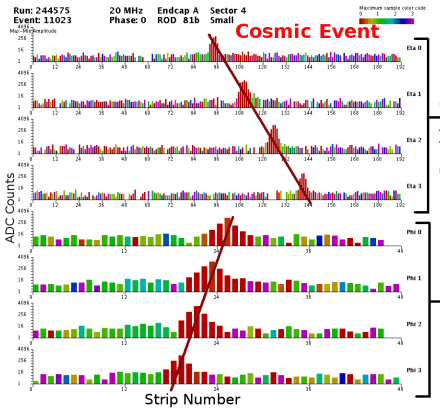


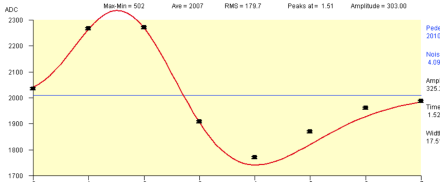




CSC ON DETECTOR ELECTRONICS

- 5 Amplifier Storage Module (ASM)-II board for each chamber
- ASM-II board handles 192 channels, each connected to a preamplifier and shaper
- Bipolar pulse with 140ns shaping time
- Pulses are sampled every 50 ns and stored on a 144 cell analog memory Switched Capacitor Array (SCA)
- Each sample is digitized to 12 bits of data
- For standard readout, 4 samples are sent to off-detector readout system, so called Readout Driver (ROD) with high speed fiberoptic G-Links
  - 10 G-Links per chamber, each carrying data of 96 channels
  - 5.76kB per event, per chamber
  - At L1 Rate of 100 kHz, input to ROD: 4.4GBits/sec per chamber
- ROD must perform threshold cut, cluster finding
  - Data reduction from $1 \rightarrow 1/6$ to $1 \rightarrow 1/60$ depending on luminosity

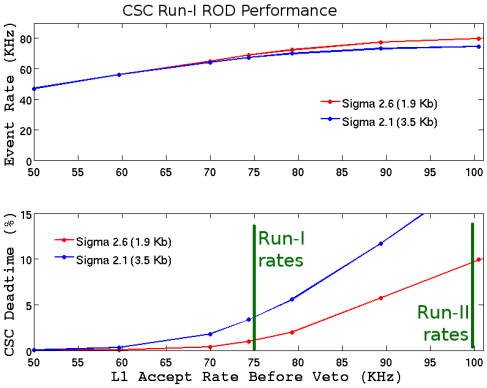




Outline

Motivation

- ATLAS Run-I conditions:
  - Bunch spacing: 50ns
  - Level 1 (L1) trigger rate: 75 kHz
  - Peak Luminosity: $8 \cdot 10^{33} \mathrm{cm}^2\mathrm{s}^{-1}$
  - Peak number of interactions per beam crossing (μ) ≈ 35
- ATLAS Run-II conditions:
  - Bunch spacing: 25ns
  - Level 1 trigger rate: 100 kHz
  - Expected Luminosity: $1.6 \cdot 10^{34} \mathrm{cm}^2\mathrm{s}^{-1}$
  - Number of interactions per beam crossing (μ) ≈ 50
- Run-I ROD:
  - Functional and robust
  - Had high deadtime for L1 trigger rates higher than 75 kHz
- In Run-II, a better performing ROD was needed to cope with higher L1 rate and luminosity, thus higher number of interactions per crossing



Outline

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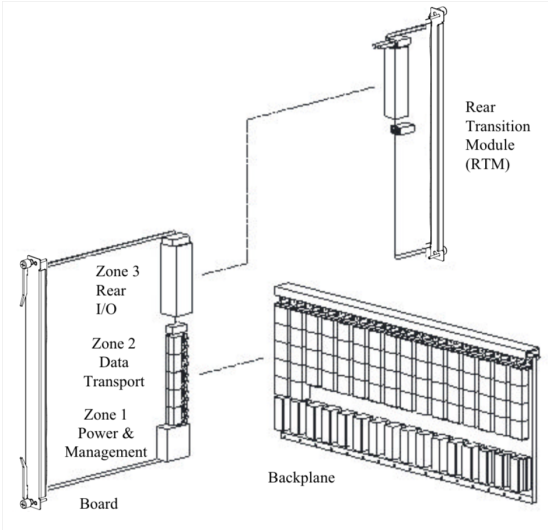
Advanced Telecommunication Computing Architecture

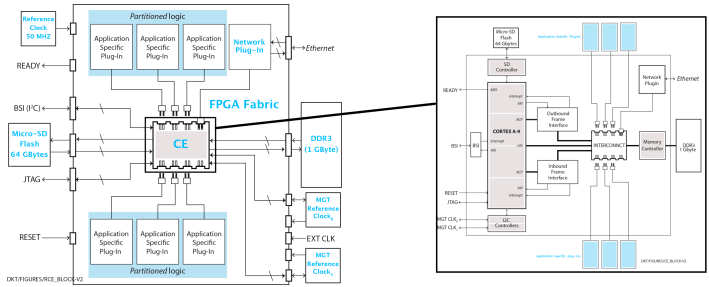
- From PICMG
- Developed for telecommunication industry
- Features
  - High Availability
  - Redundancy
  - Hot Swap
  - IPMI based shelf management infrastructure
- High-speed, protocol agnostic backplane
- Separates physical data interface from processing with Rear Transition Module (RTM)



Outline

Reconfigurable Cluster Element (RCE)

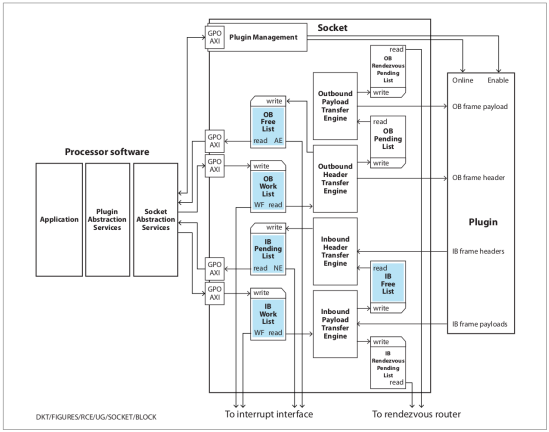
- RCE is developed by the detector R&D program at SLAC
- Based on System-On-Chip (SoC) technology (Processor-centric Xilinx ZYNQ)
- Provides a processing component that includes both firmware and software
- Large FPGA fabric, high speed I/O channels and large memory banks
- Strong internal interconnect to allow the CPU to conveniently access all resources at high speed
- The Cluster Element (CE) is the heart of RCE
  - Dual-core (A-9) ARM processor (@ 800 MHZ)
  - 1 GB of DDR3 RAM, up to 64 GB of flash
  - Memory subsystem has $>$ 6 GB/sec of I/O capacity
- Choice of OS: Real-Time Executive for Multiprocessor Systems (RTEMS), Linux or bare metal



Protocol Plug-In (PPI) Model

Defined as an arbitrary set of application specific logic, coresident with an RCE's FPGA fabric which requires the exchange of information with its CE.

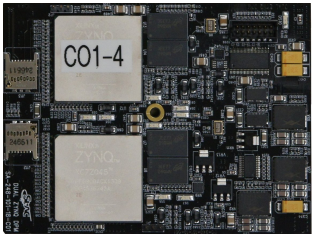
- Application specific plug-ins with plug and socket model
- User wraps the logic in a common way. Wrapper is the plug
- Wrapped logic can be plugged into 8 predefined sockets on RCE
- Application specific plug-ins can
  - Act as an Input/Output device (such as receiving data from detector and sending it to Readout System)
  - Take advantage of Digital Signal Processing (DSP) tiles and combinatoric logic of the FPGA for data manipulation



RCE types

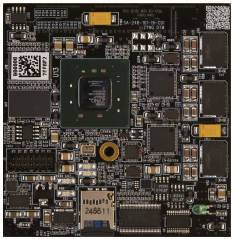
Data Processing Module (DPM)

- Contains 2 RCEs
- ZYNQ : XC7Z045-2FFG900E with 16 MGT
- DPM performs task related to data manipulation/ feature extraction (FEX)



Data Transfer Module (DTM)

- Contains 1 RCE
- ZYNQ : XC7Z030-2FBG484E with 4 MGTs
- Manages the networking between RCEs on COB and to external world



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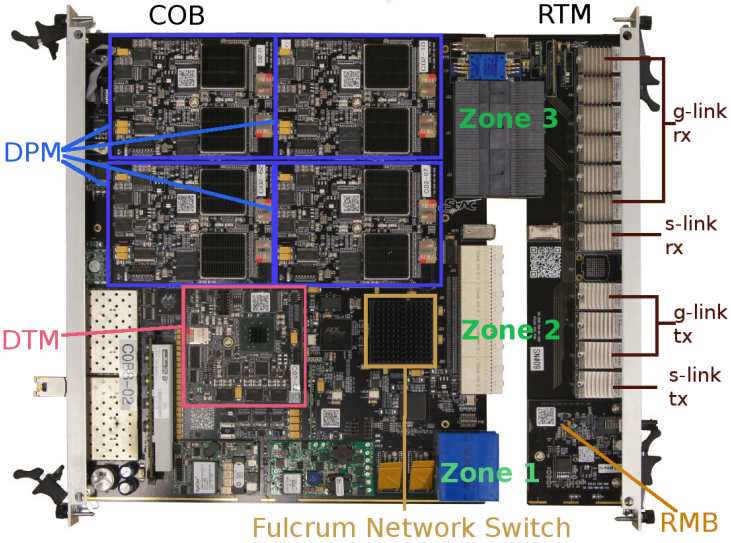
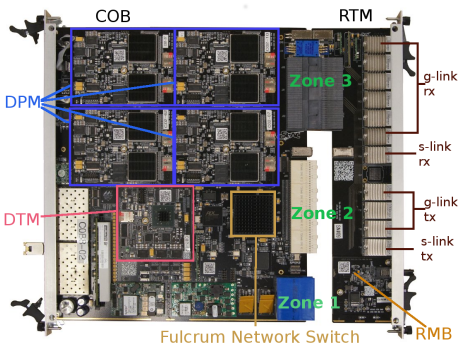
The Cluster On Board



The Cluster On Board

- Carrier board developed to hold 9 RCEs
  - 4 DPM bays (8 RCEs)
  - 1 DTM bay (1 RCE)
- Cluster Interconnect: on-board 24-port 10GbE low latency switch (Fulcrum)
- Coupled with application specific Rear Transition Modules (RTM) with Rear Mezzanine Board (RMB) for Trigger Timing and Control (TTC) interface
- 3 Zones and connectors
  - Zone 1: Power and management
  - Zone 2: Data transport interface for communication between boards
  - Zone 3: Connectivity with RTM in a 96 channel high density connector



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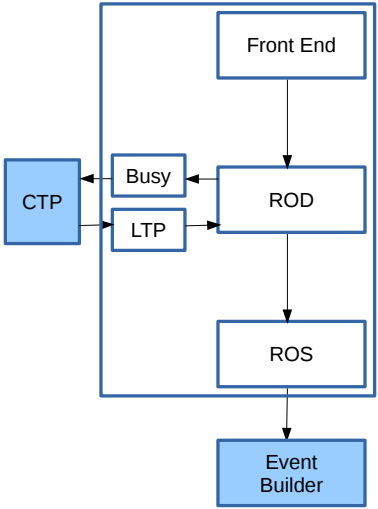
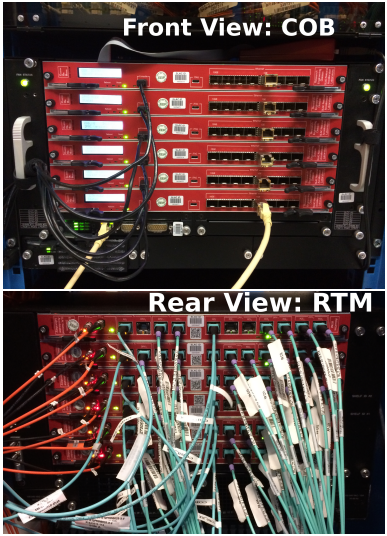
ATLAS Trigger and Data Acquisition Concepts

- Read out Driver (ROD) : Part of the off-detector readout system that process data of front-end electronics
- Local Trigger Processor (LTP): Propagates trigger signal from ATLAS Central Trigger Processor (CTP) to ROD
- Busy Module: Propagates busy from ROD to CTP
- Read out System (ROS) : Stores event fragments that are processed in ROD, sends them for event building depending on the decision of High Level Trigger (HLT)
- Complex deadtime: Burst protection using a leaky bucket model (Run-II Settings: 15/370, 42/381, 9/351, 7/350)



Overview of the System

- Standard 6-slot ATCA Shelf populated with COB+RTM
- COB hosts RCEs that provide feature extraction and data formatting
- On each COB, there are up to 3 DPMs (4-6 RCEs) and 1 DTM (1 RCE)
- RTM: Provides physical interface to chambers and the central Trigger and Data Acquisition (TDAQ) system
  - The data fibers from/control fiber to on-detector electronics (G-Links)
  - Read Out Links (ROL) to ROS (S-Links)
  - Connections to Busy Module, and LTP



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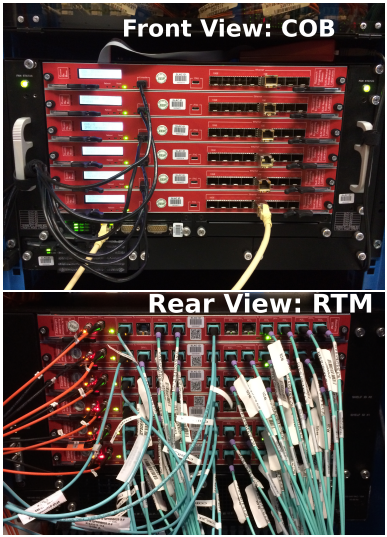

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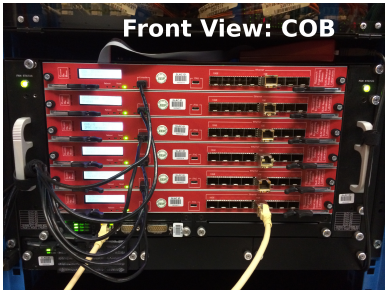

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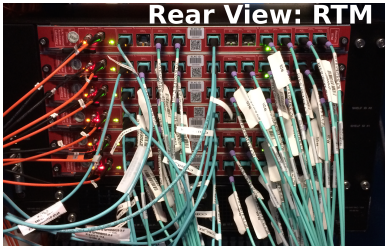

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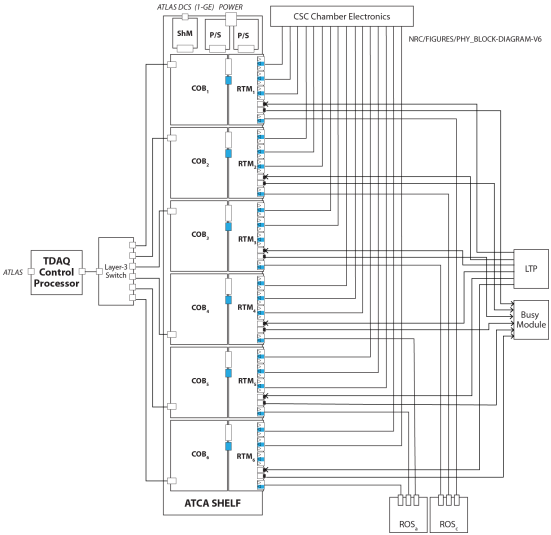
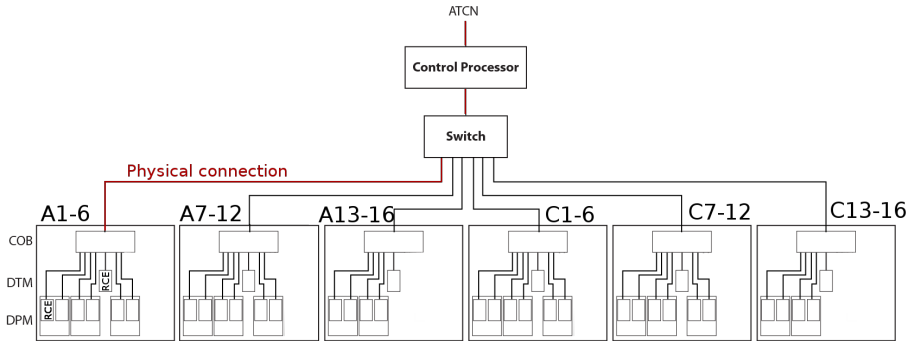


Overview of the System

- Control Processor (CP) is used to interact with the RCEs and ATLAS
  - CP connects to RCEs via a dedicated switch, and to ATLAS Technical Network (ATCN)
  - Internal network assignment of the COBs done in the ATCA fabric



DPM and DTM in CSC COB

DPM

- Equivalent of Read Out Driver (ROD) in ATLAS systems
- Each RCE handles a single chamber
  - 10 G-Links as input, 1 S-Link as output
- Runs RTEMS as OS
- Processes 4 or more time slices from the Front-End per event
- Feature extraction, zero suppression
- Samples into event fragments
- Sends formatted data to ROS via ROL

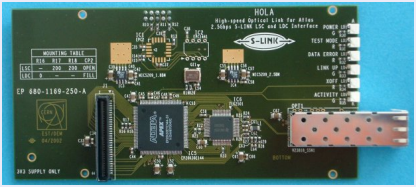
DTM

- Runs Arch Linux as OS
- Handles TTC distribution directly communicating with Local Trigger Processor (LTP) (No intermediate agent like TTC Interface Module (TIM)).
- Manages network traffic
- TTC emulator available for Local Trigger Processor (LTP) functionality

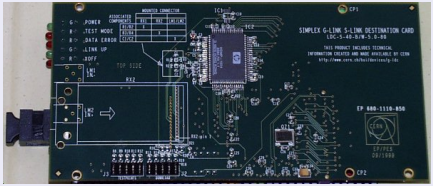
Firmware Solutions Replacing Hardware

Traditional hardware solutions are implemented in firmware of the SoC, causing smaller footprint and lower power consumption

- TTC handling: DTM firmware eliminated need for intermediate distribution module (TIM)
- Connection to ROS: S-link High-speed Optical Link (HOLA) card replaced by firmware
  - Typical 9U VME board has space for 3 HOLAs, while a CSC COB can host 8 S-Links

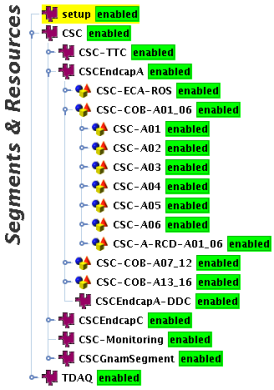


- Connection to Front-End: G-link ASIC (HDMP) implemented in firmware (In Run-I CSC ROD, G-link ASIC was implemented in the CSC Transition Module (CTM) in Xilinx Virtex-II pro FPGA)

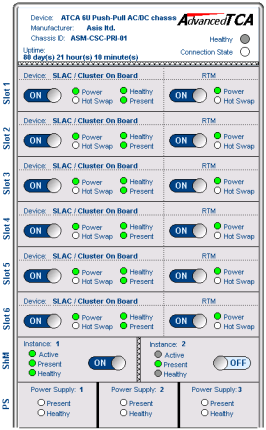


Outline

Integration with ATLAS TDAQ



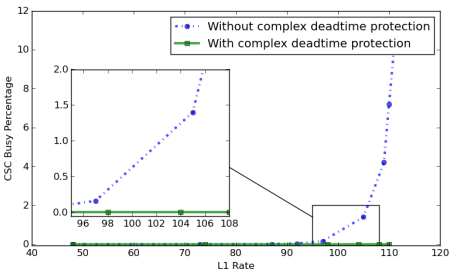
- Control Processor
  - Interacts with the TDAQ infrastructure
  - Interacts with RCEs in a client/server model
  - Each RCE is represented by a separate process in the CP
- Automatic recoveries to recover a crashed RCE deployed
- All firmware registers are periodically dumped to Information Services (IS) for diagnosis
- In situ fast calibration by doing histogramming on the ROD
- ATCA shelf is controlled and monitored via Detector Control System (DCS) using IPMI interface

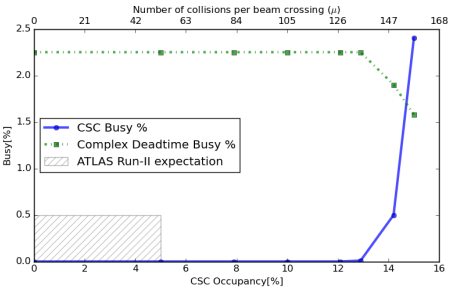


Outline

Performance

- Performance has few layers: Configuration, Front-End, Feature Extraction, data transfer to ROS
- Fast configuration due to the parallel operation on each RCE
- G-Link bandwidth has not changed, and it is limited to 111 kHz at 4 samples (lower rate at > 4 samples)
- High performing FEX code using On-Chip Memory (OCM) deployed
- Increased bandwidth to ROSes by doubling the number of S-links compared to Run-1
- Performance tests show
  - 0% deadtime up to L1 rate of 110 kHz with Run-II occupancy, while protected by complex deadtime
  - At 100 kHz input rate, no busy until 13% occupancy (Maximum expected in Run-II for CSC $\approx 5\%$)
- System is able to handle the Level-1 trigger rate of 100 kHz and the higher luminosity of Run-II



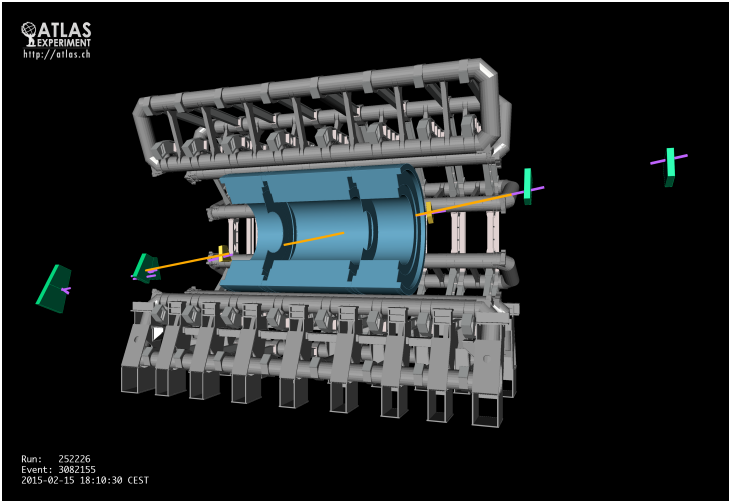


Outline

Concluding Remarks

- With Run-II upgrade, ATLAS L1 trigger rate and luminosity increased
- The CSC Run-I off detector readout system would not be able to cope with Run-II conditions
- The CSC Run-II off-detector readout system was developed with this goal using modern DAQ technologies
- It is the first deployment of a ATCA and RCE based DAQ system in ATLAS
- Additional functionality compared to old ROD such as automatic recoveries, IS monitoring, high statistics pedestal calculation on the RCE
- Large FPGA fabric allows to implement hardware solutions in the firmware with much smaller footprint and lower power consumption
- System running stably since start of Run-II
- Performance tests show we accomplished main goal of 100 kHz L1 rate at Run-II occupancy with significant margin

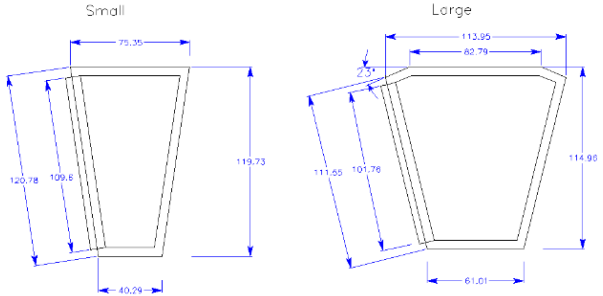
Obrigado pela atenção



OUTLINE

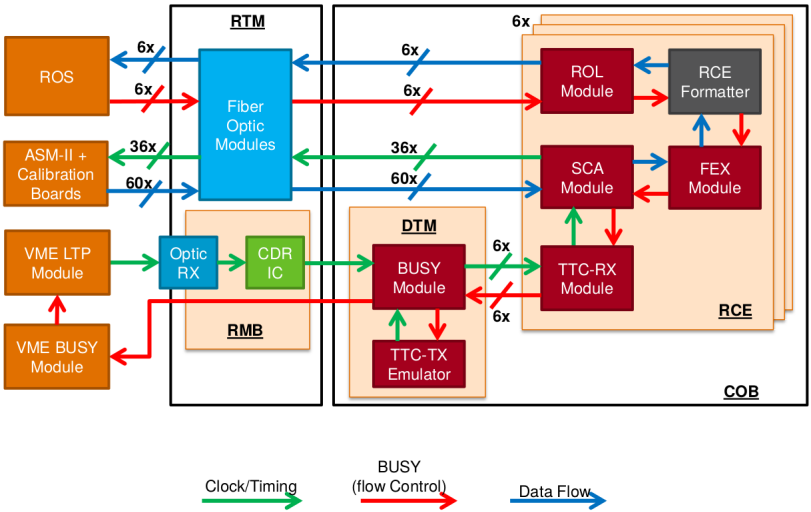
ATLAS CSC

- Strip pitch for precision layers:
  - Big chambers: 5.567 mm
  - Small chambers: 5.308 mm
- High spatial resolution (60μm) and high counting rate capability
- Good two-track separation, 40% of the readout pitch
- Short electron drift time ($<$ 45ns), and good timing resolution ($\approx$ 7ns)
- Low neutron sensitivity, ($\varepsilon_n < 1\%$)
- Low photon sensitivity, ($\varepsilon_\gamma \approx 1\%$ for $E_\gamma = 1$MeV)

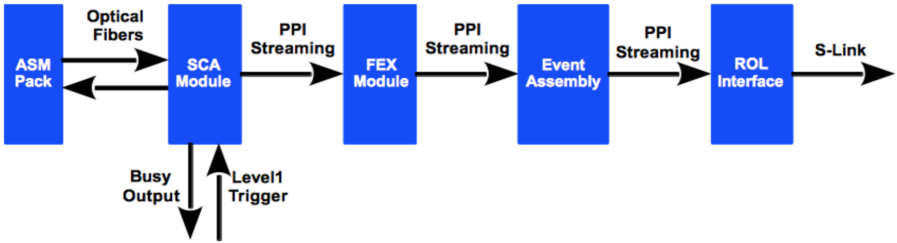


COB DIAGRAM

For single ATCA slot



DATAFLOW DIAGRAM



RACK INFRASTRUCTURE

ead Rod - New Rod

TTC Crate