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A low jitter PLL frequency synthesizer for high resolution TDCs in 65nm CMOS technology

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PLL synthesizer
Application

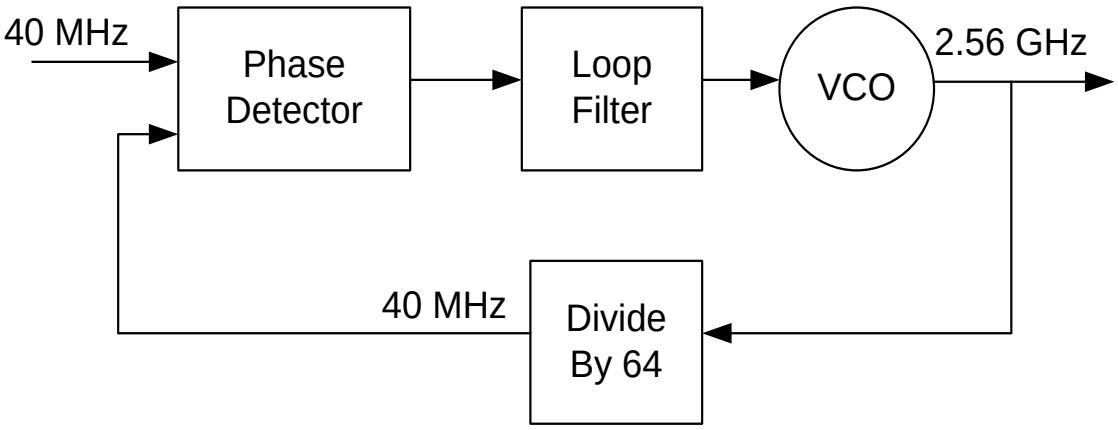
- High resolution Time-to-Digital converter PicoTDC SoC (1)
  - 3 ps LSB
  - 64 Channels
- 2.56 GHz based TDC timing generator
  - TDC requires high speed clock
  - Locked to 40 MHz – 50 MHz reference

- x 64 PLL required
  - Low additive jitter/phase noise
  - Jitter reduction

[1] Prague 2015, M. Horstmann, J. Prinzie, J. Christiansen

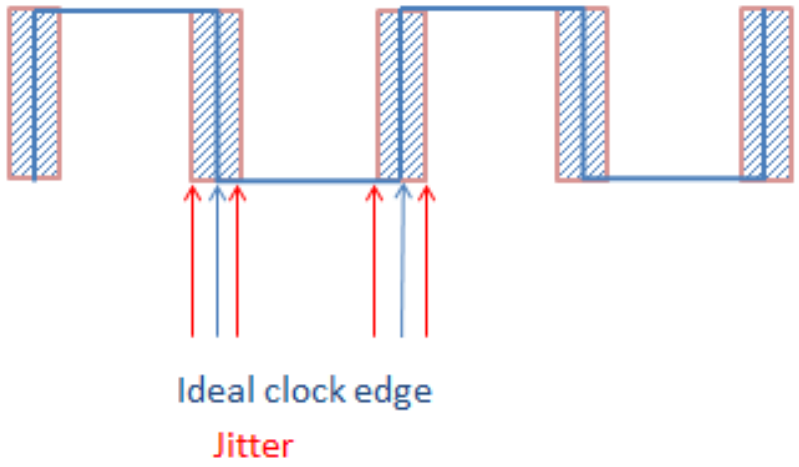
PLL synthesizer
Application

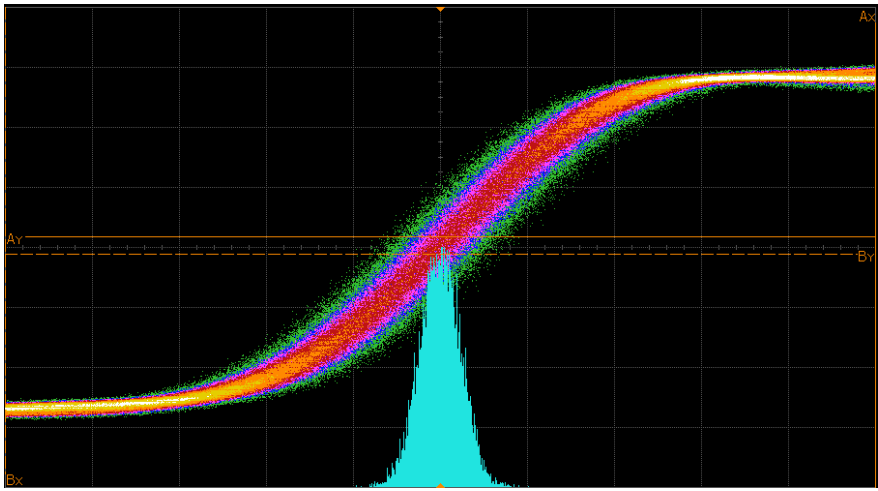
- Negative feedback loop
- Phase detector compares VCO clock with reference
  - Aligns VCO phase with reference phase
  - $\Phi_{in} = \Phi_{out}$ (phase lock)
- Adjusts VCO frequncy with error signal



PLL synthesizer
Application

- Random timing noise
  - Jitter < 1 ps RMS
- Phase noise
  - $\sin(\omega t + \Phi(t))$
  - $PN = F(\Phi(t))$
- Reference clock noise
  - Low pass filter
- VCO clock noise
  - High pass filter





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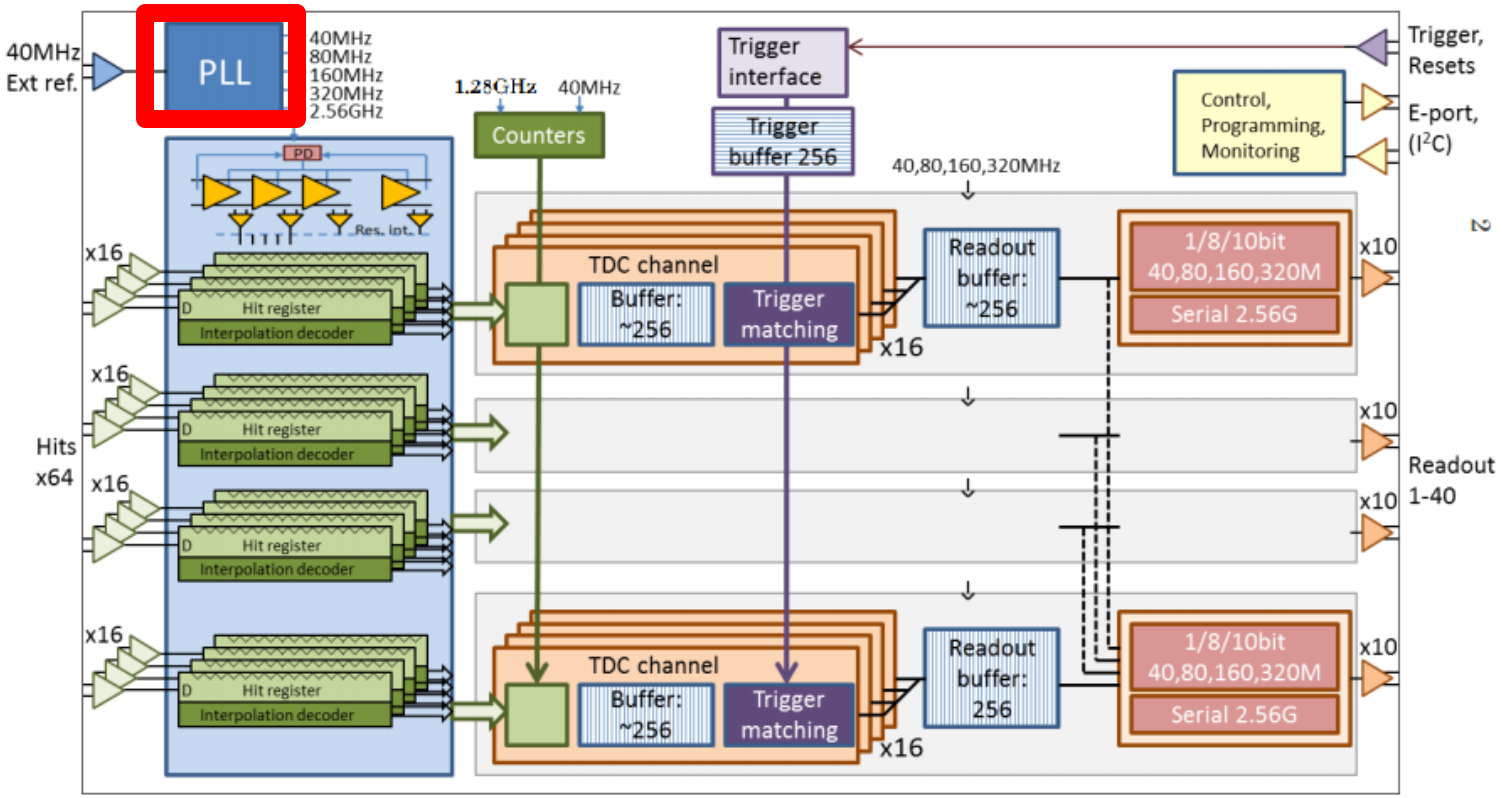
PLL synthesizer

Application



64 channels, 3ps or 12ps time binning

64 channels, 3ps: ~1W

64 channels, 12ps: ~0.4W

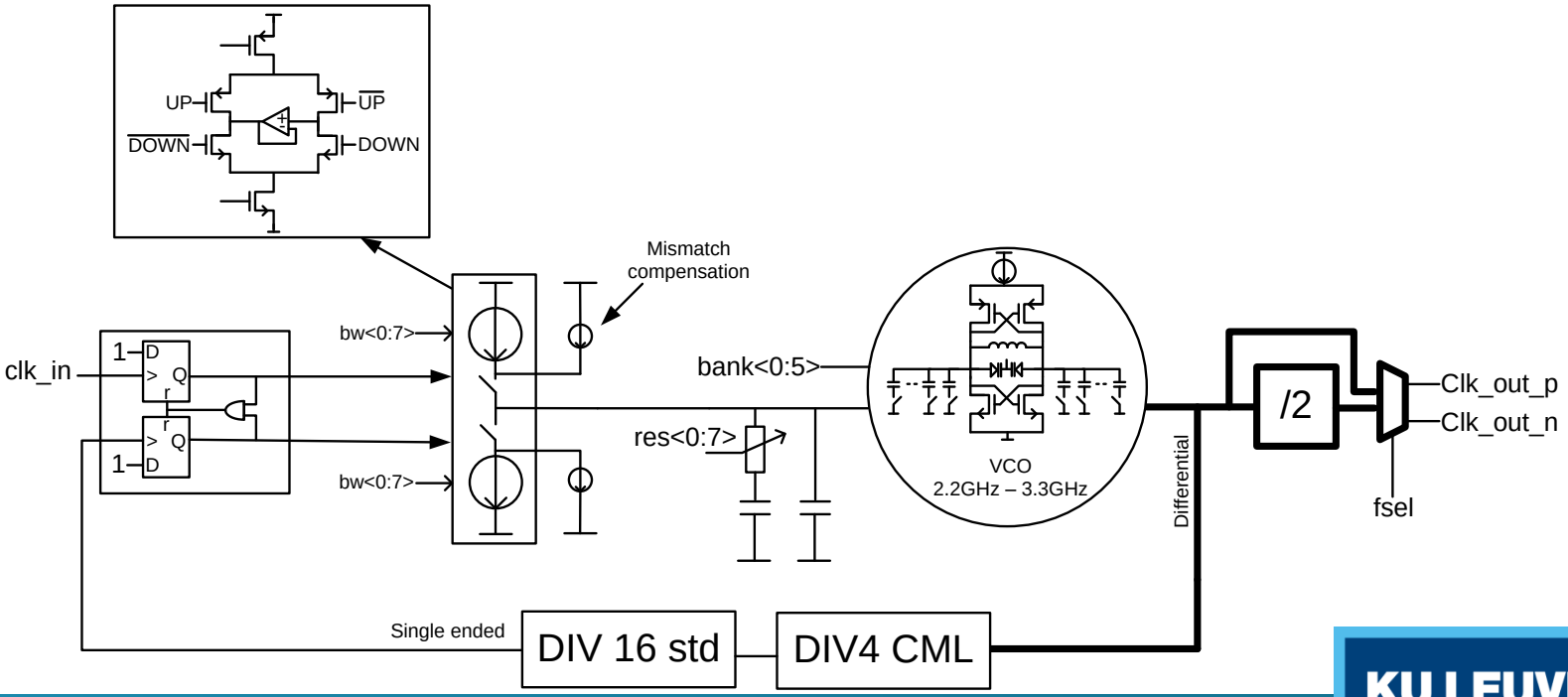
32 channels, 12ps: ~0.2W

PLL synthesizer
LJPLL Specs

- Additive jitter < 1 ps rms
- Power consumption < 100 mW
- Reference clock: 40 MHz – 50 MHz
- SEU aware design
- Configurable bandwidth (100 kHz – 2 MHz)
- Easy configuration (corner aware)

PLL synthesizer
Architecture

- LC based low noise oscillator
- /64 TMR divider
- TMR phase detector
- Configurable charge-pump/Filter



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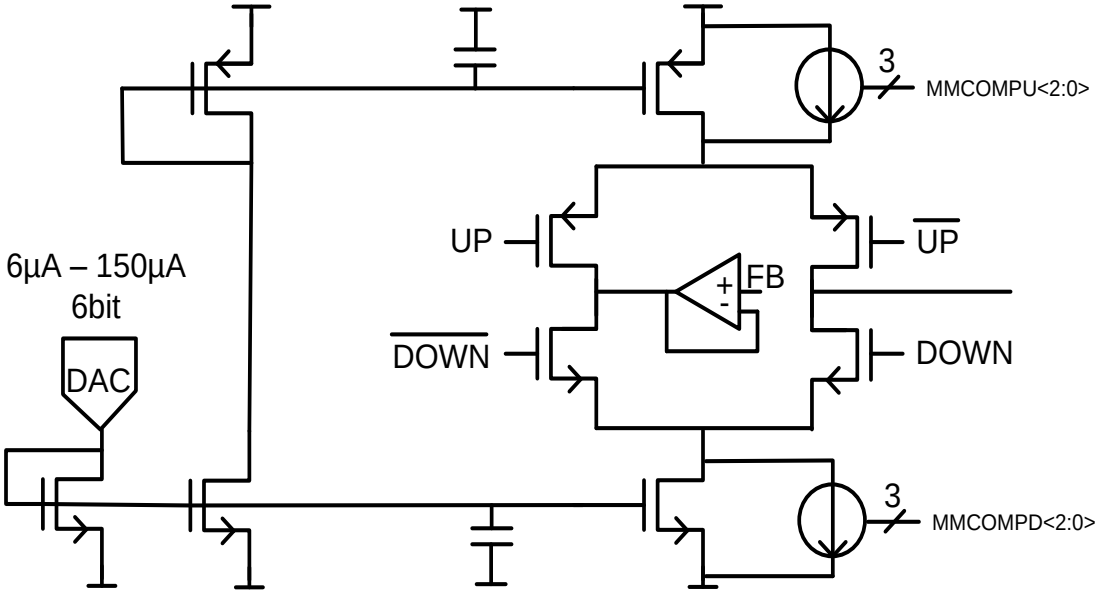
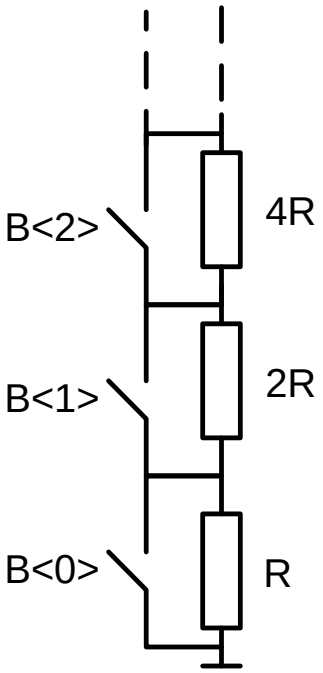
PLL synthesizer
Charge pump

- 100 kHz – 2 MHz bandwidth
- Tunable charge pump current with on-chip reference
- Bias decoupling for SET protection
- Adjustable loop resistor





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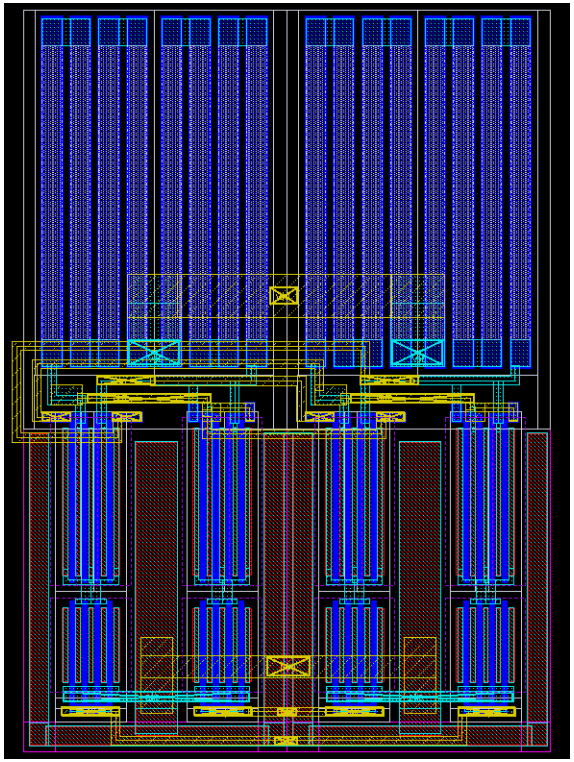
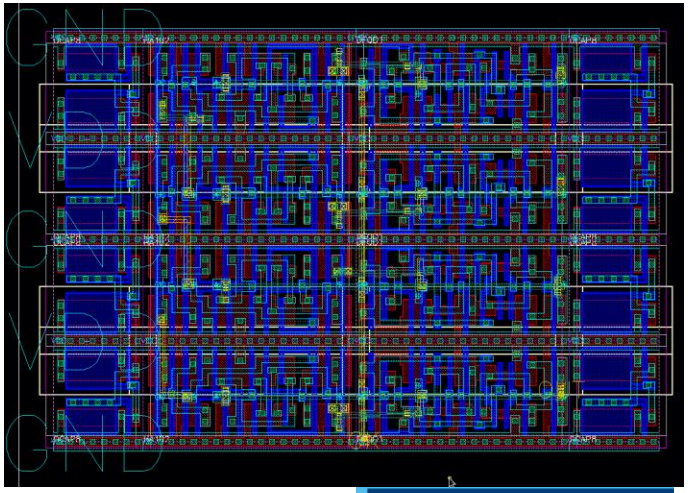
PLL synthesizer
Divider

- High speed CML prescaler (DIV4)
  - 1.5 mA current
- Low speed divider (DIV16)
  - Protection with TMR for SET
  - Standard cell design
  - Custom routed
- Fixed division ratio

- Selectable DIV2 at output
  - 2.56 GHz or 1.28 GHz





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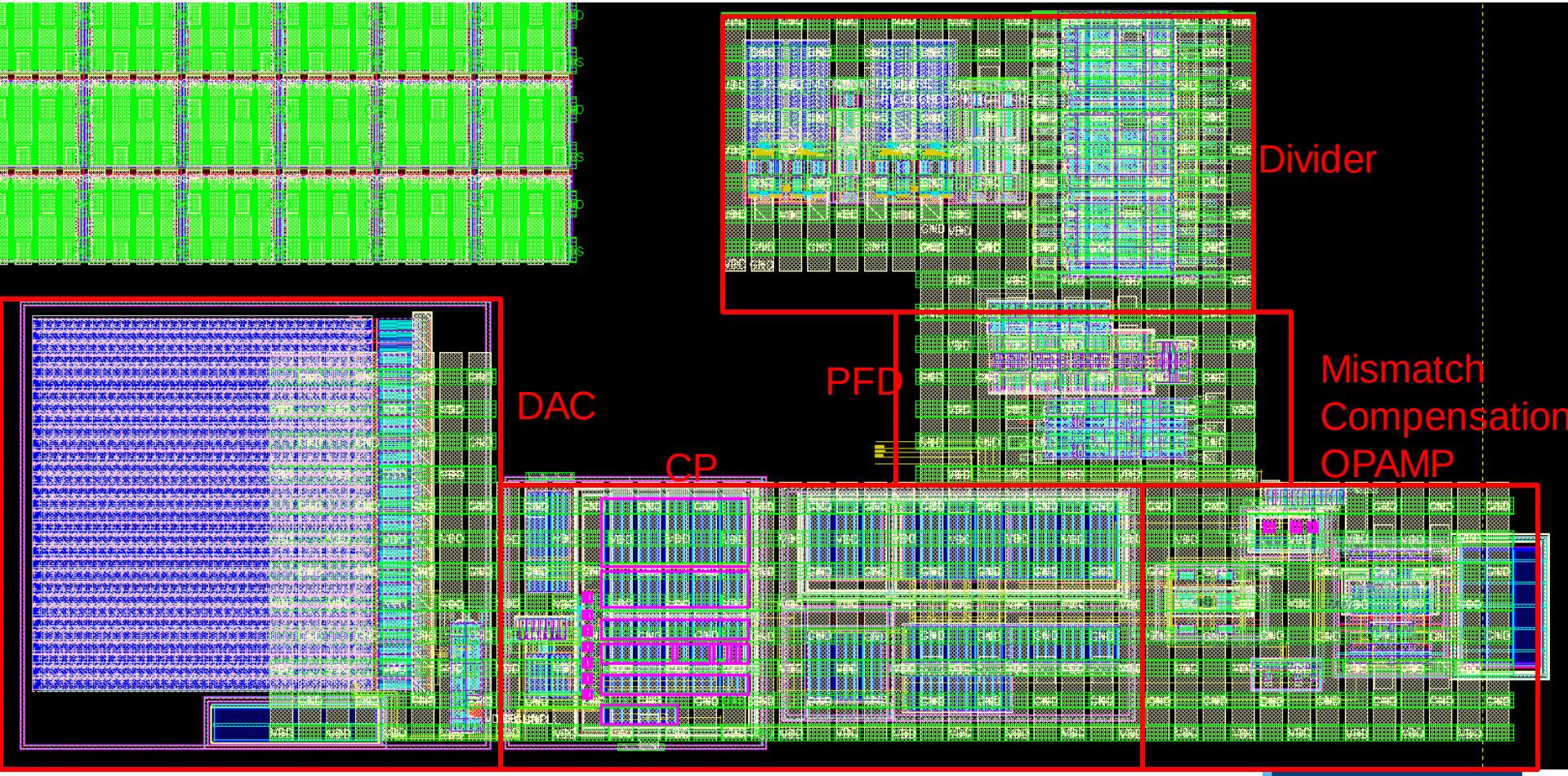
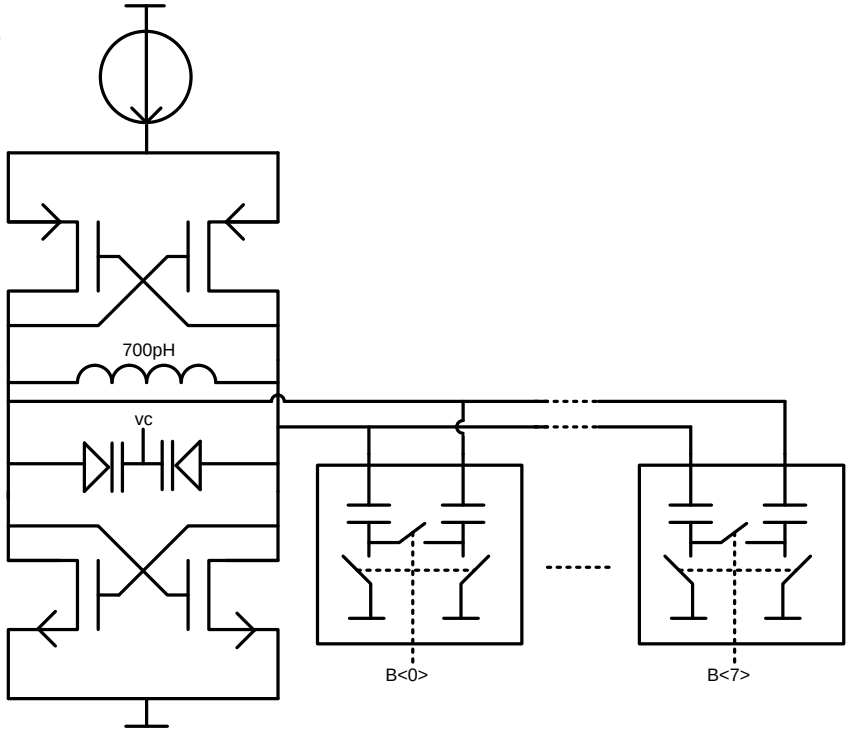
180 µm x 90 µm



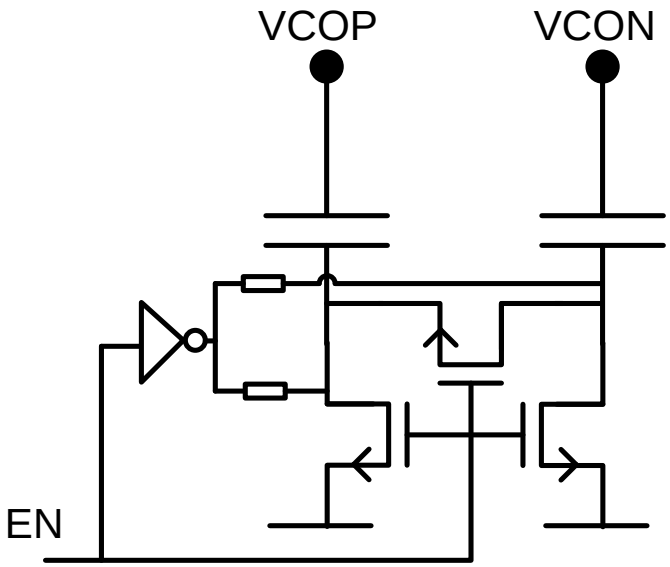
PLL synthesizer
VCO

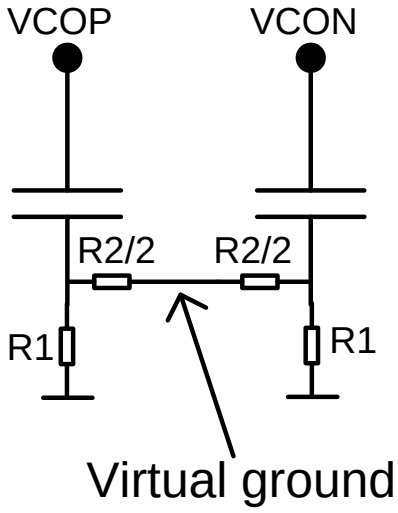
- LC tank oscillator
- Optimized for low phase noise
  - Low tank Rs
- 700 pH inductor
  - Q=16
- PMOS current source
  - Lower 1/f noise
- 8 programmable capacitor banks
- 2.2 GHz – 3.5 GHz
- < -124 dBc/Hz @ 1 MHz phase noise
- 5 mA



PLL synthesizer
VCO

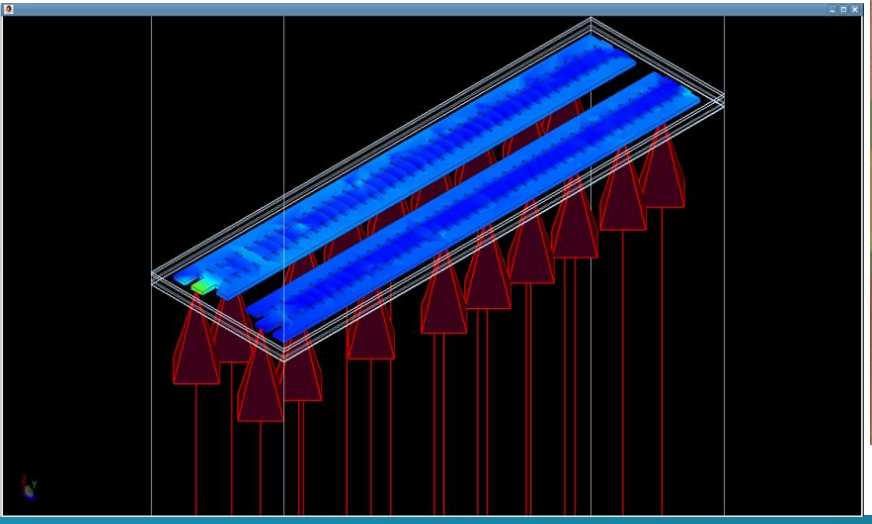
- High Q switched capacitors needed
- MOMCAP with Q > 35
- Q limited by switch
- Virtual grounded switch to improve Q→ Better phase noise
- MOMCAP have high variability (bad)

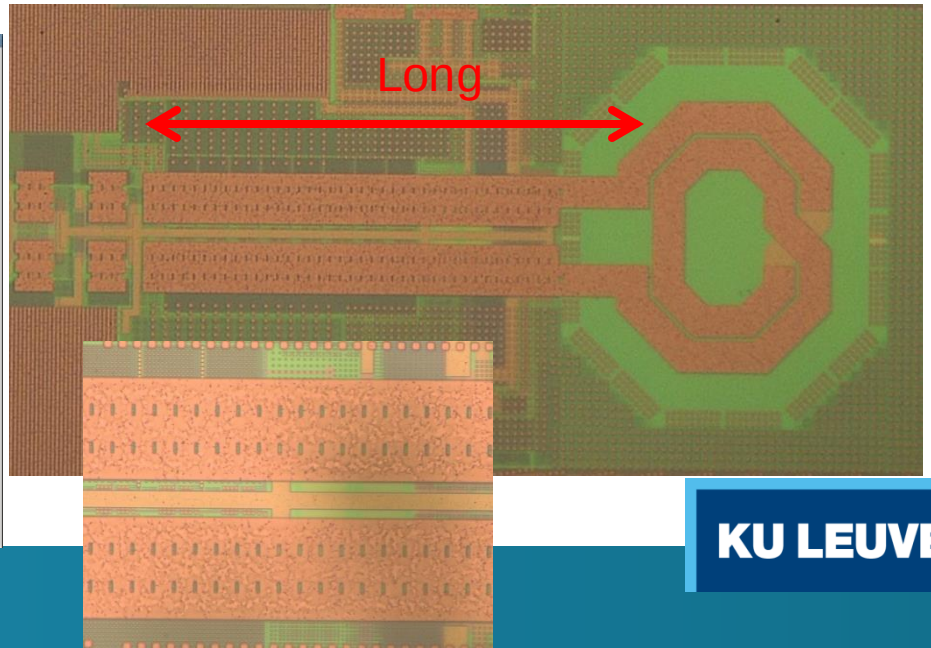




PLL synthesizer
VCO

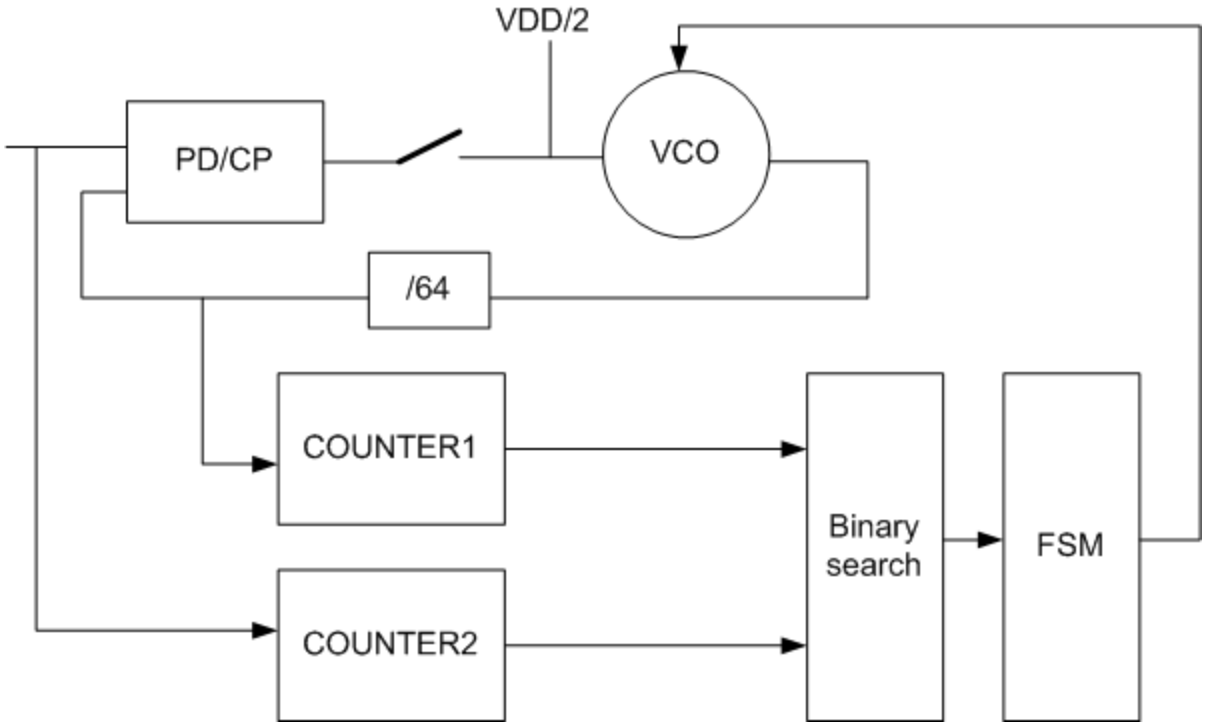
- Distributed track to capacitor bank is relatively long
- EM simulations necessary for equivalent inductance (L-M)
- Lowers the tank's Q
- Optimized shape for good M
- 1 pH/µm → 250 fH/µm (equivalent, s-parameter matching)

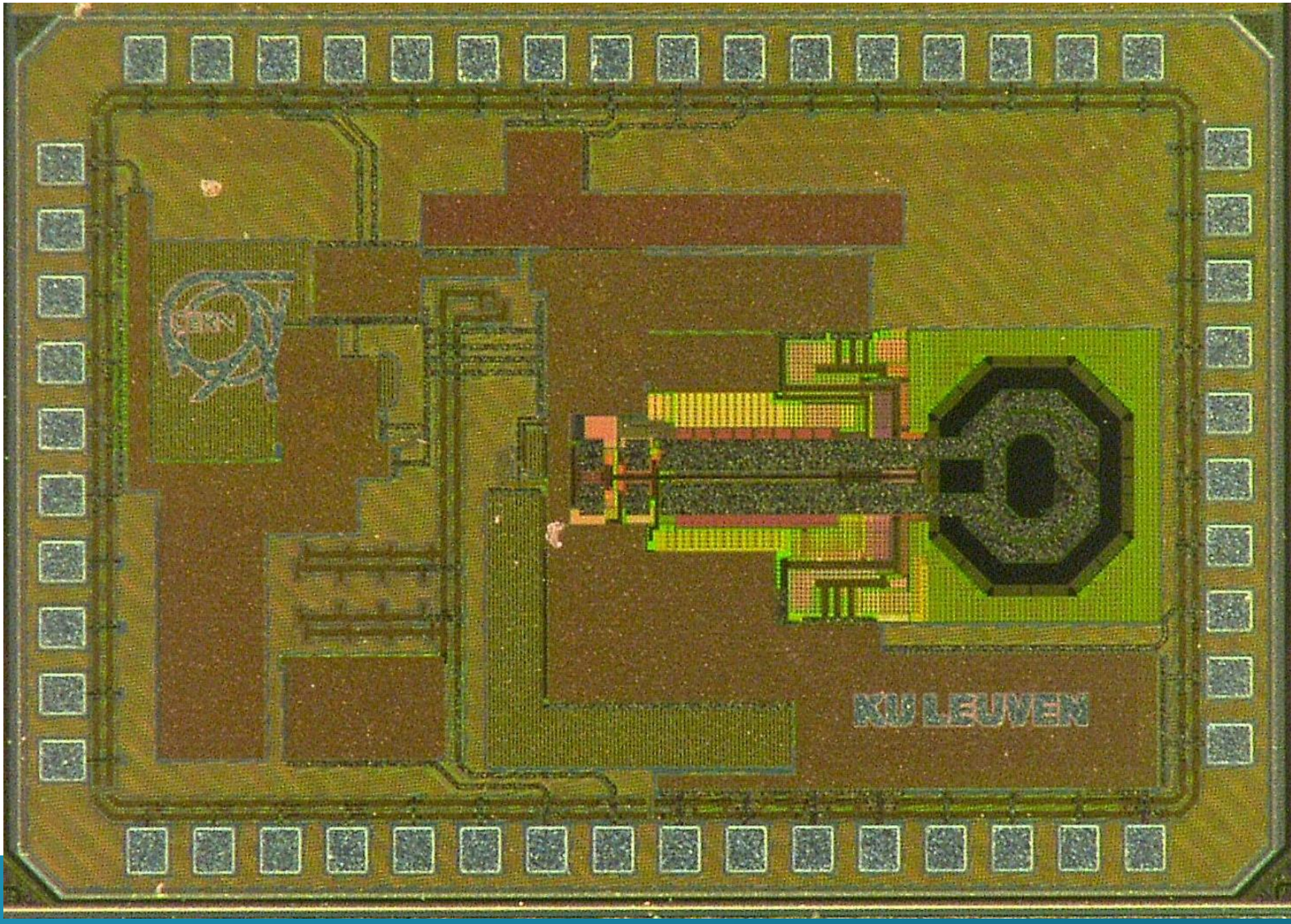




PLL synthesizer
VCO

- Automatic band selection required (MOMCAP variation)
- Digital binary search algorithm
- Fully TMR




ESAT
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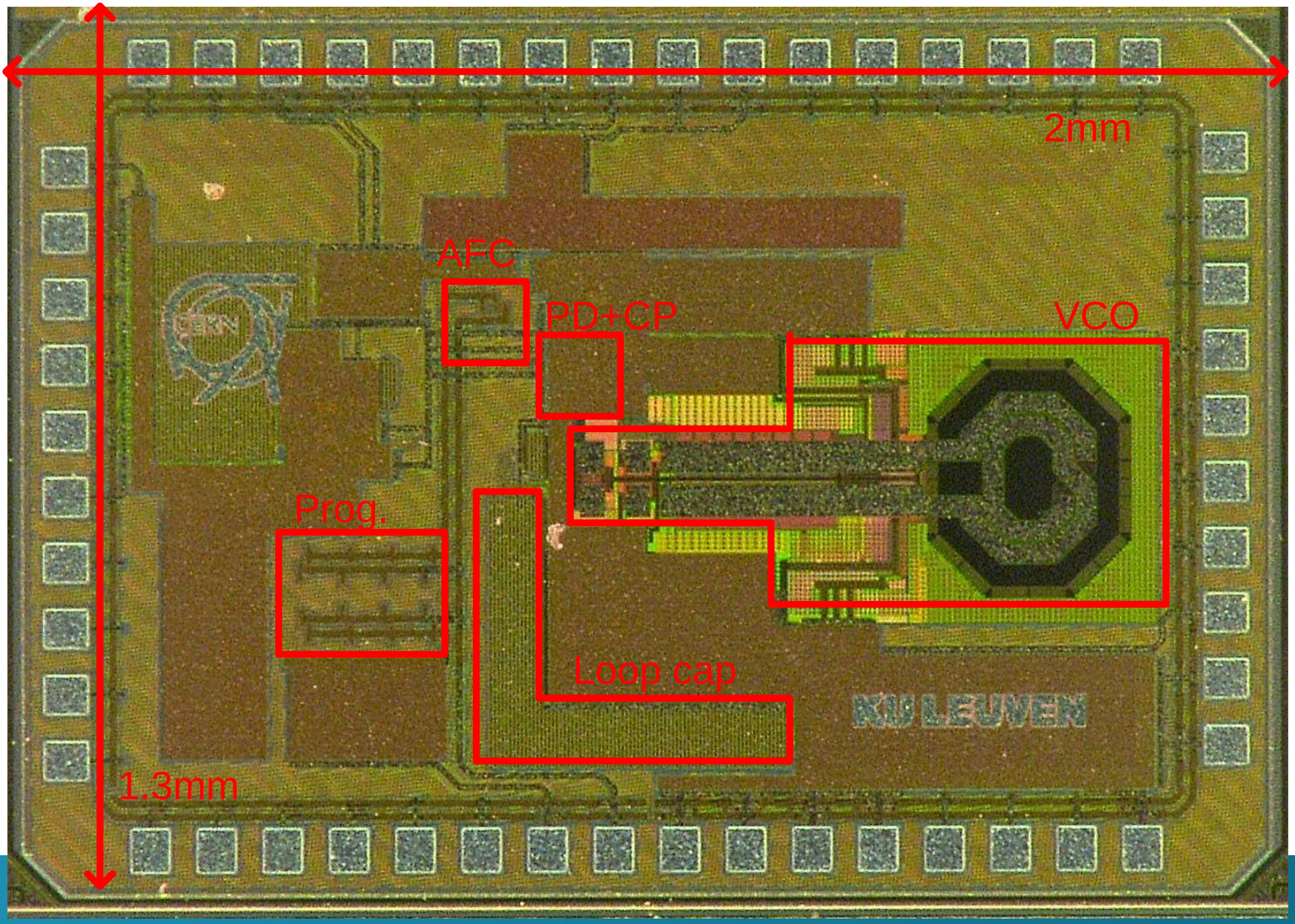
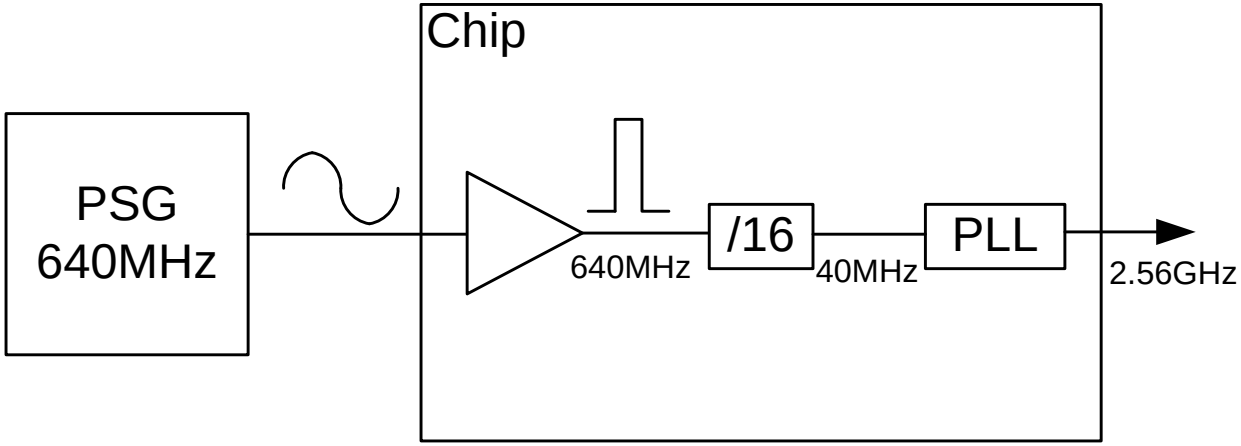

2mm
AFC
PD+CP
VCO
Prog.
Loop cap
KU LEUVEN
1.3mm

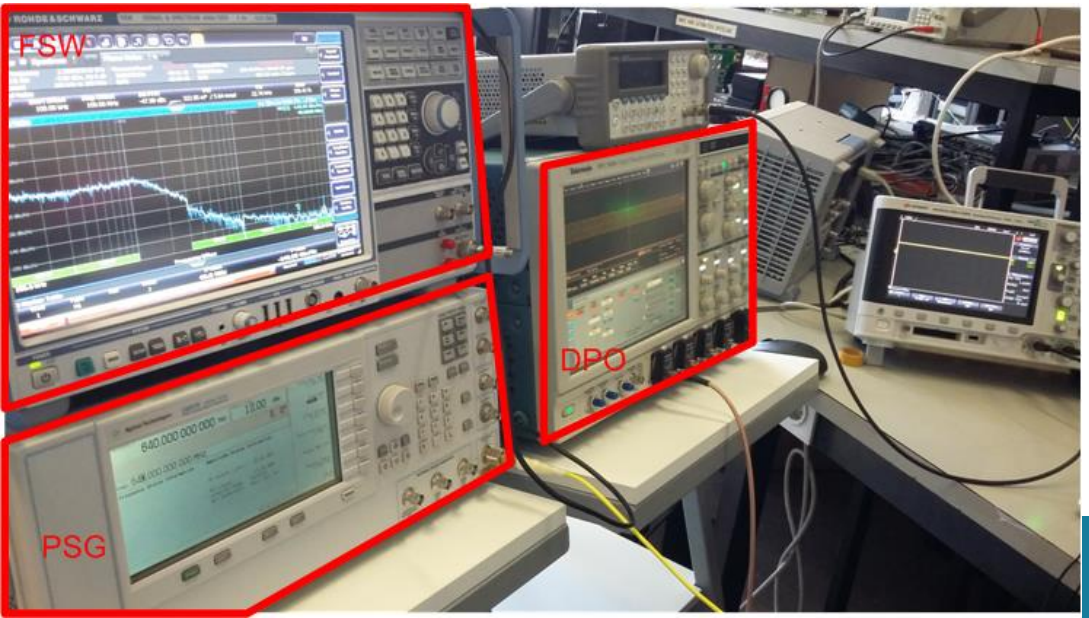
Measurements

- Characterizing PLL
  - Ultra low noise reference
- Agilent PSG signal generator
  - Only sine wave (~100 fs rms jitter)
  - 40 MHz at input buffer kills jitter
- 640 MHz reference → /16 on chip prescaler



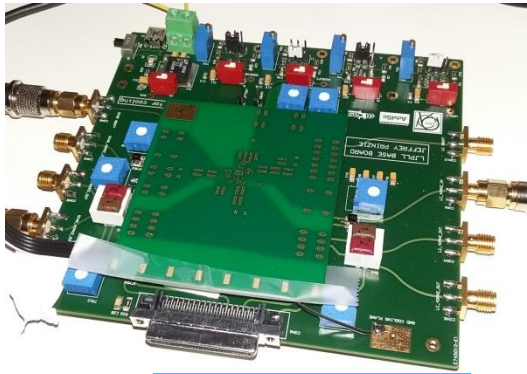
Measurements

- R&S FSW PN-analyzer
  - Ideal noise floor
  - No histograms
  - Frequency domain analysis
- Tektronix DPO7000 sampling oscilloscope
  - Closed loop sampling
  - Worse noise floor (290 fs internal jitter)
  - Time-domain analysis
  - Histograms

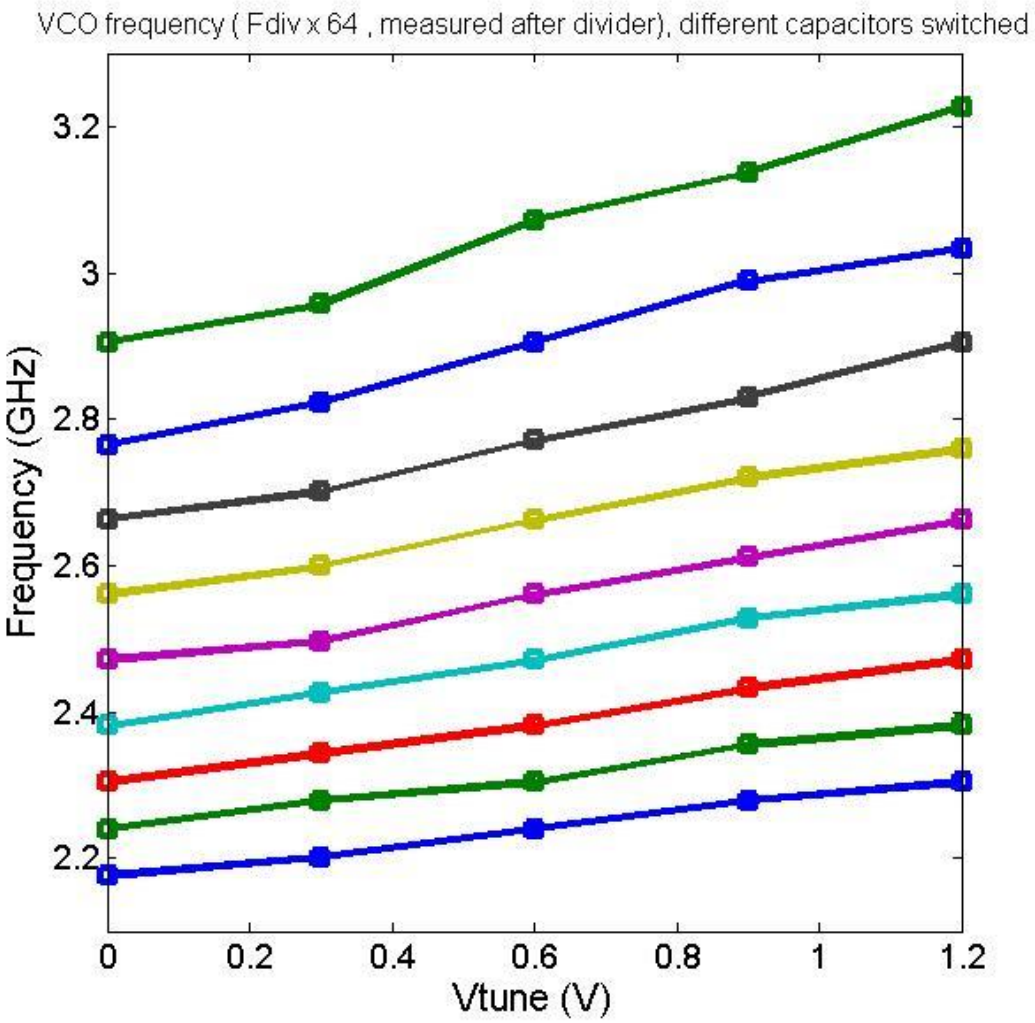


1.2 V V_{DD}

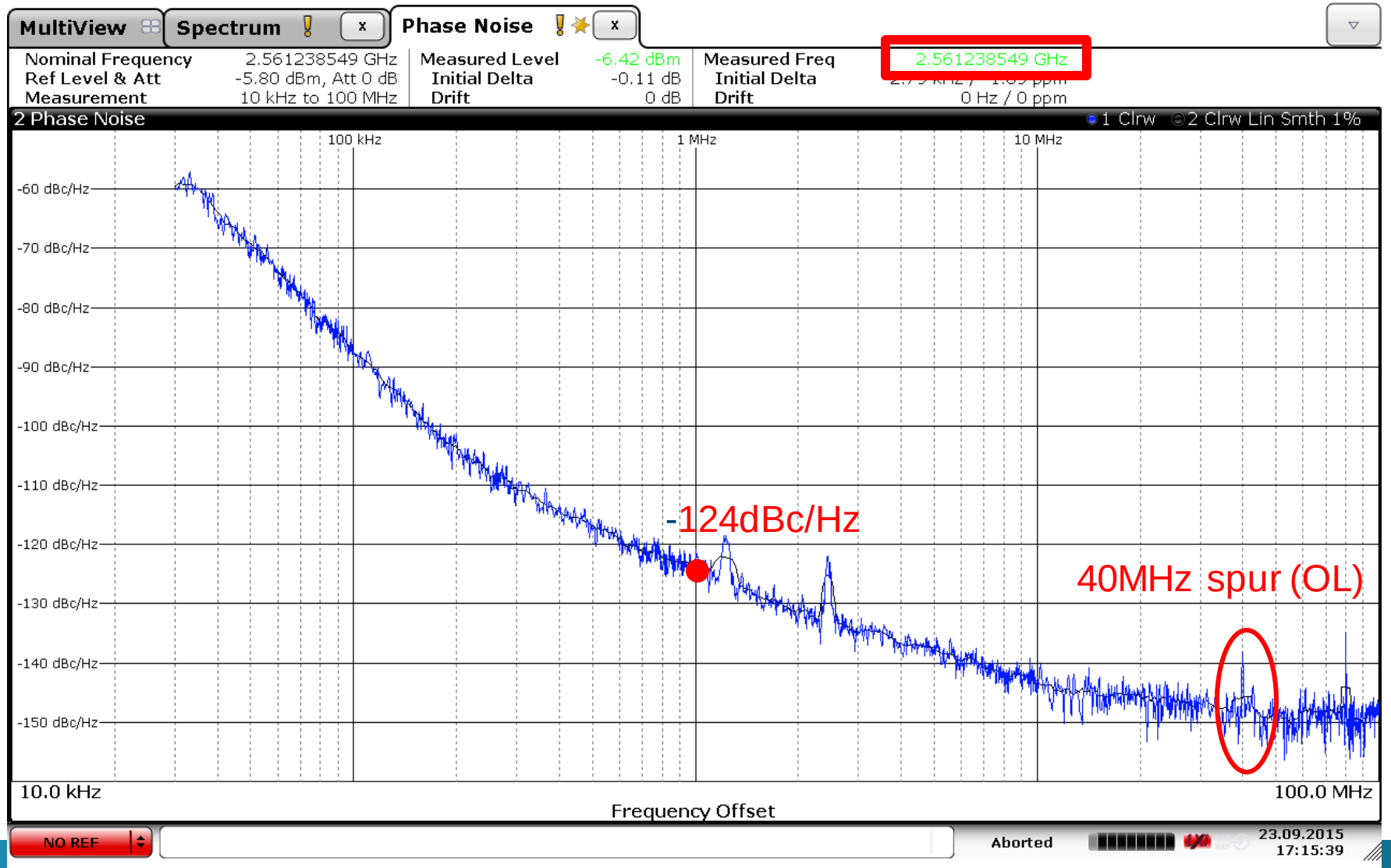
25 °C



Open loop VCO



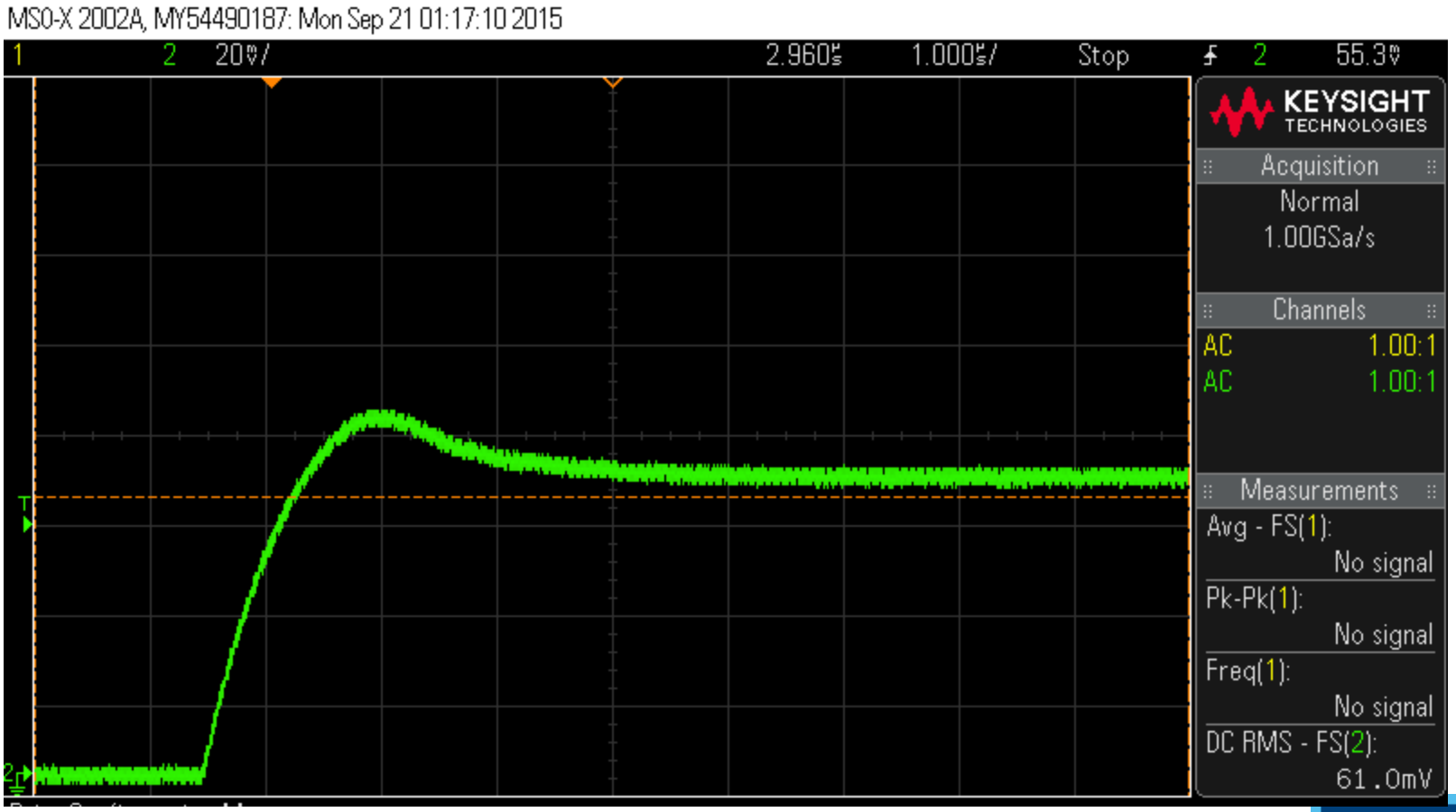
Open loop VCO



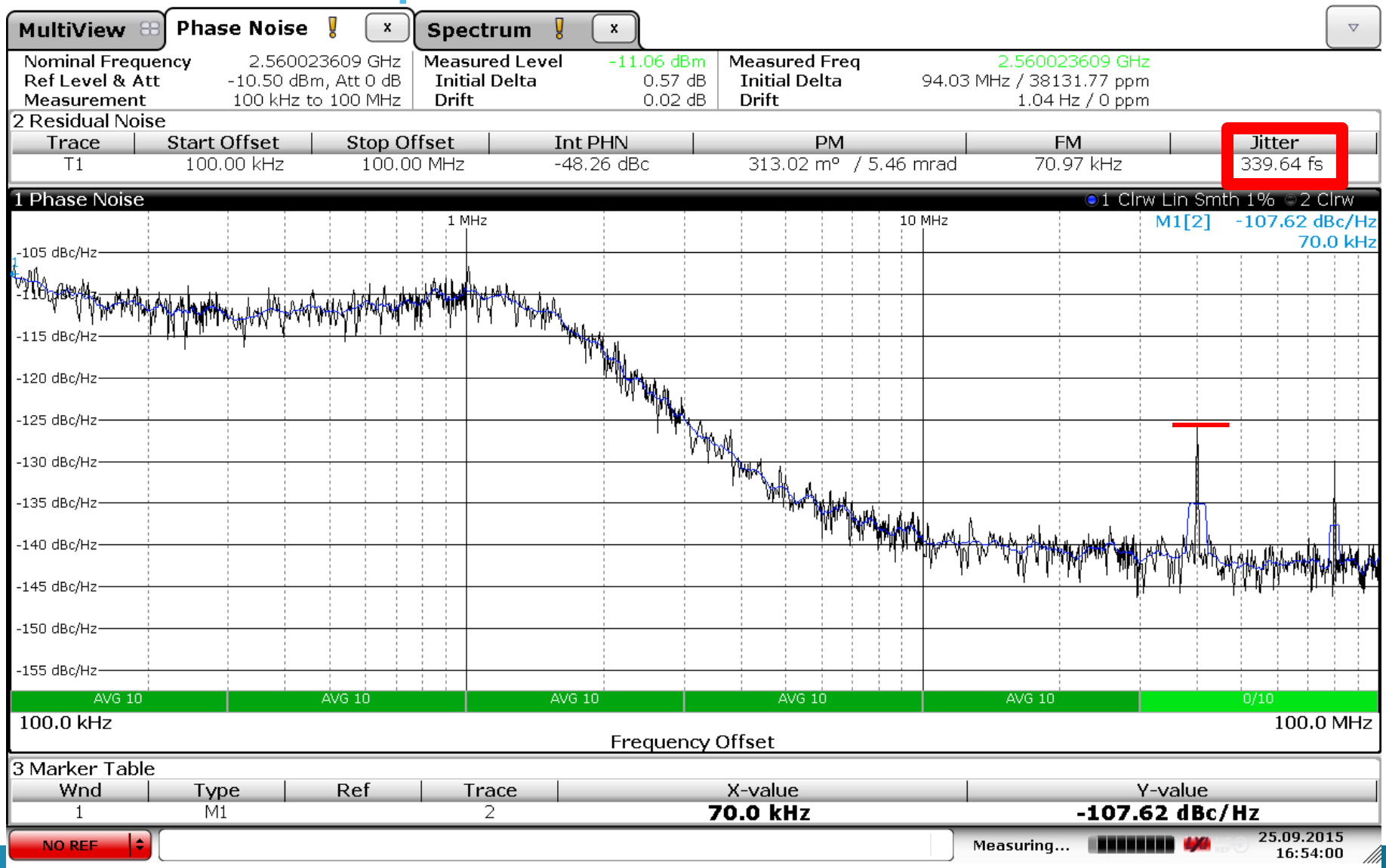
Date: 23.SEP.2015 17:15:39

Closed loop PLL

- Phase step to verify damped system

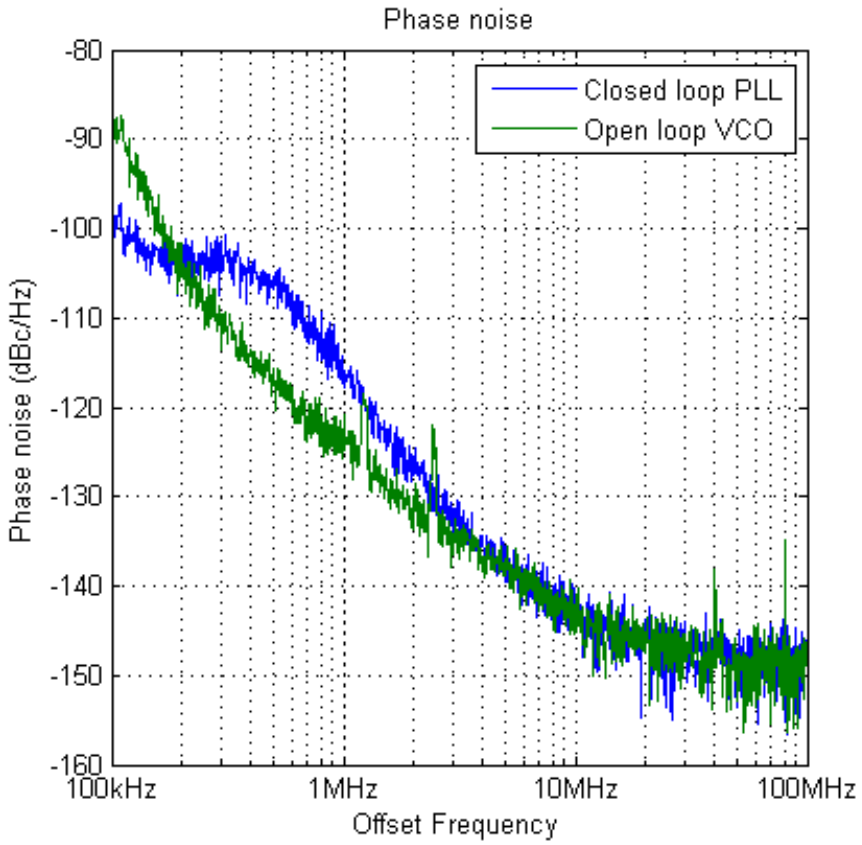


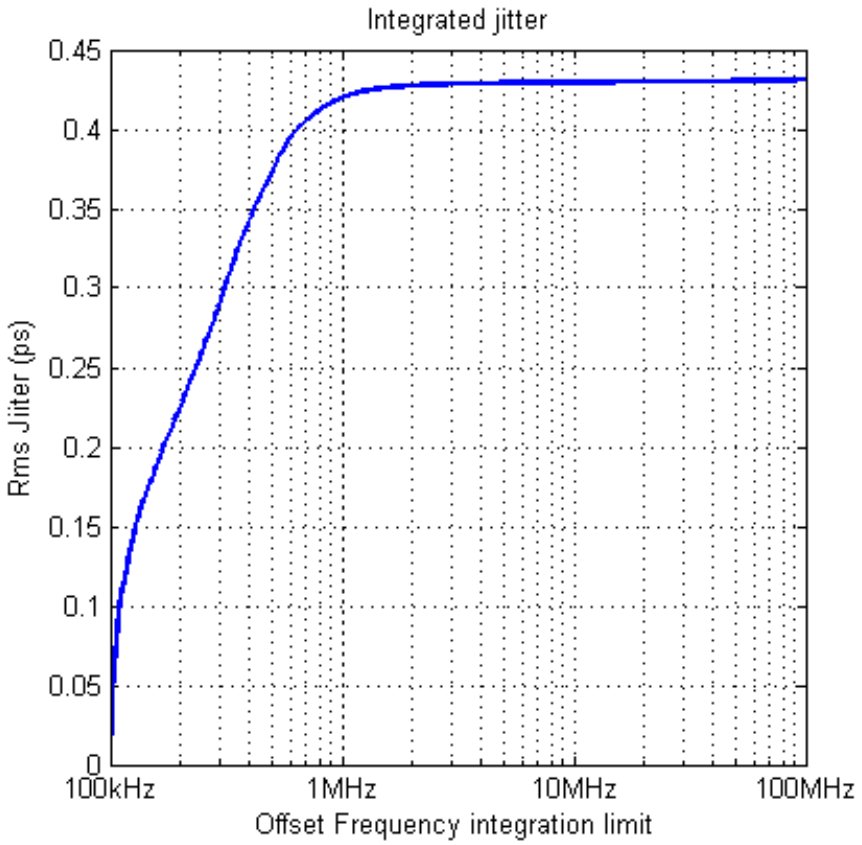
Closed loop PLL



Date: 25.SEP.2015 16:54:00

Closed loop PLL





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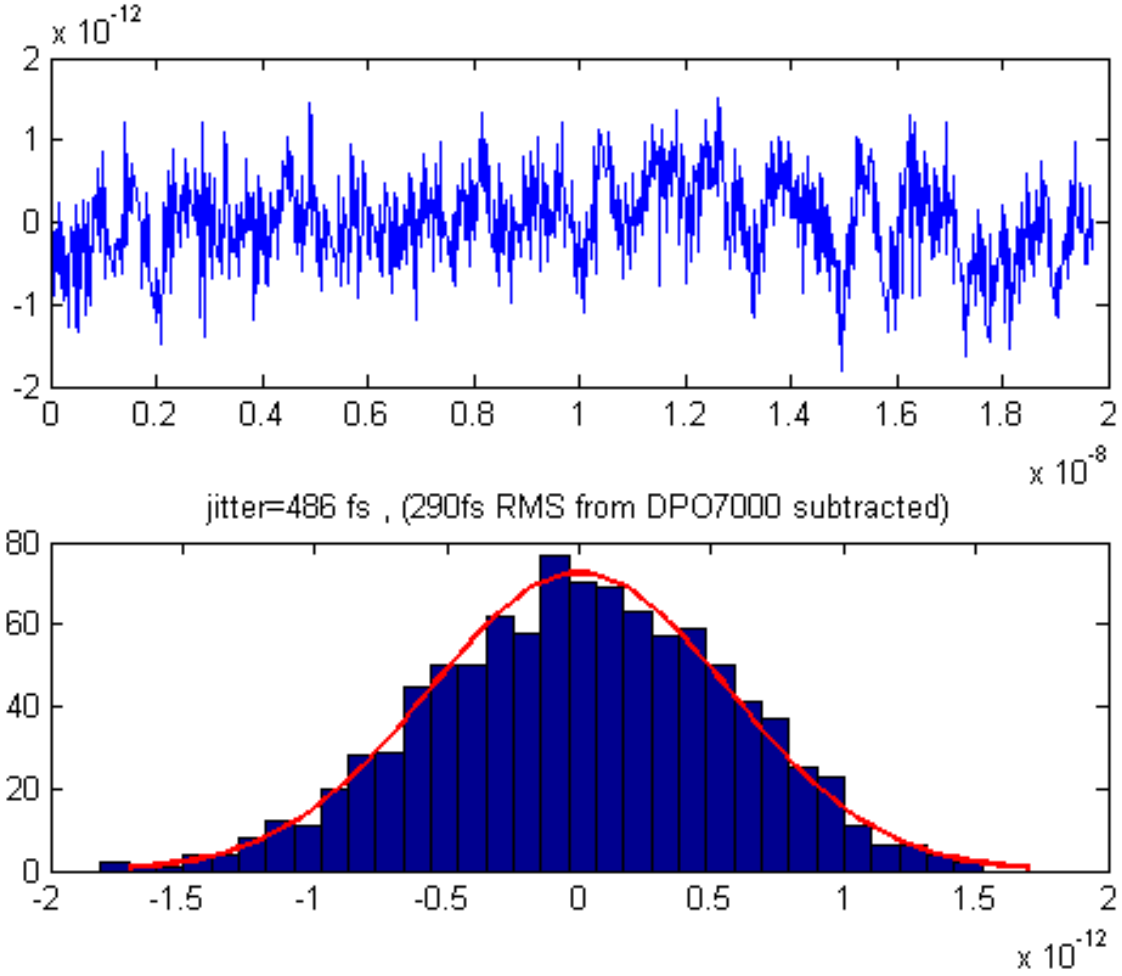
Closed loop PLL (DPO7000)



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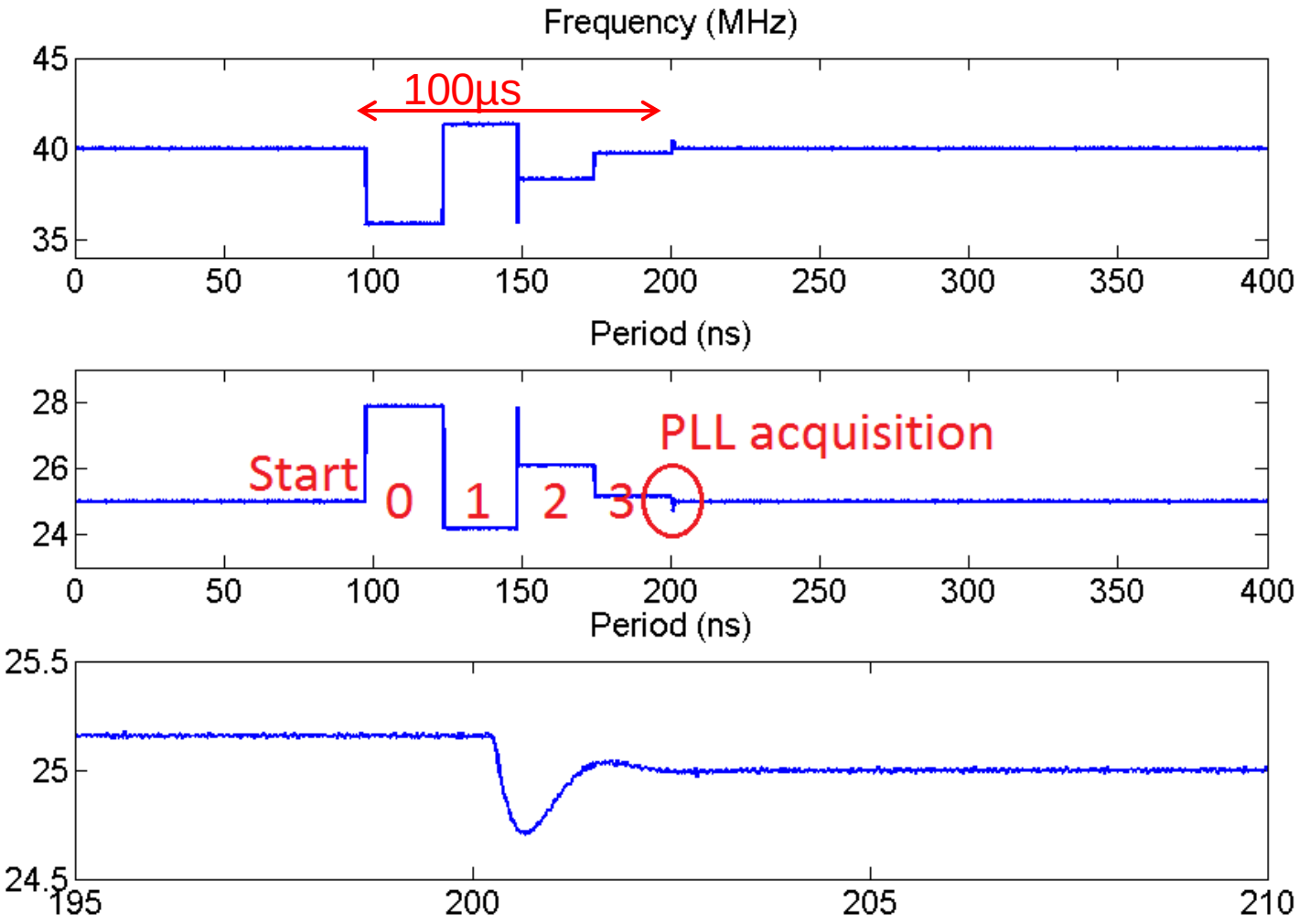
AFC calibration



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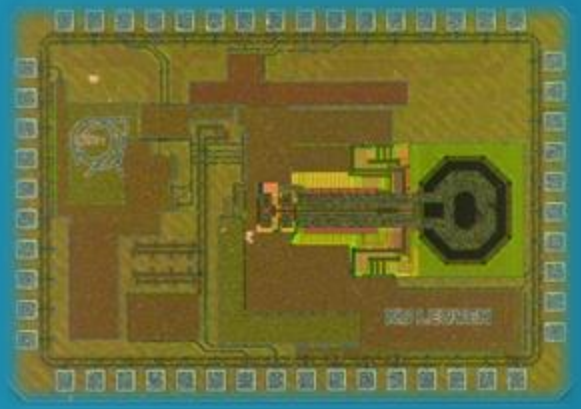
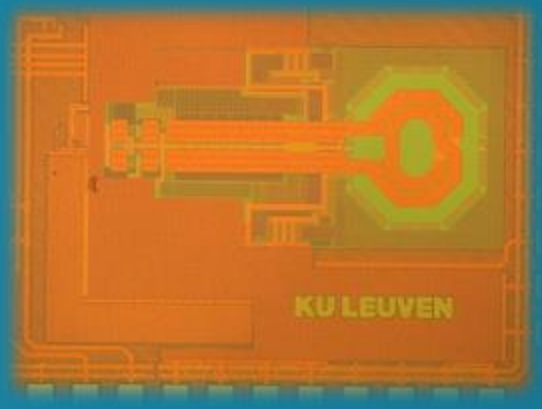
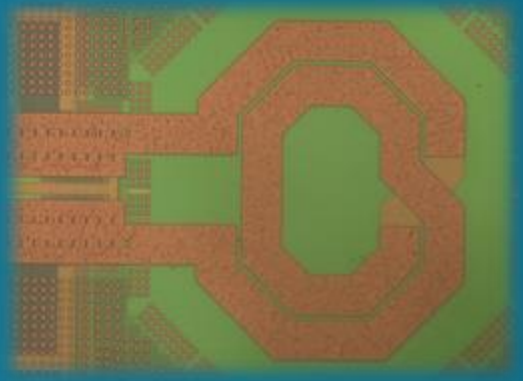
Summary

- Designed and tested LJPLL chip
- LC oscillator based clock generator
- 350 fs rms jitter measured
- <30 mW power consumption
- 100 kHz – 2 MHz programmable bandwidth
- Automatic band selection algorithm included



Thank You

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Michiel Steyaert
Jorgen Christiaensen
Paulo Moreira
Paul Leroux

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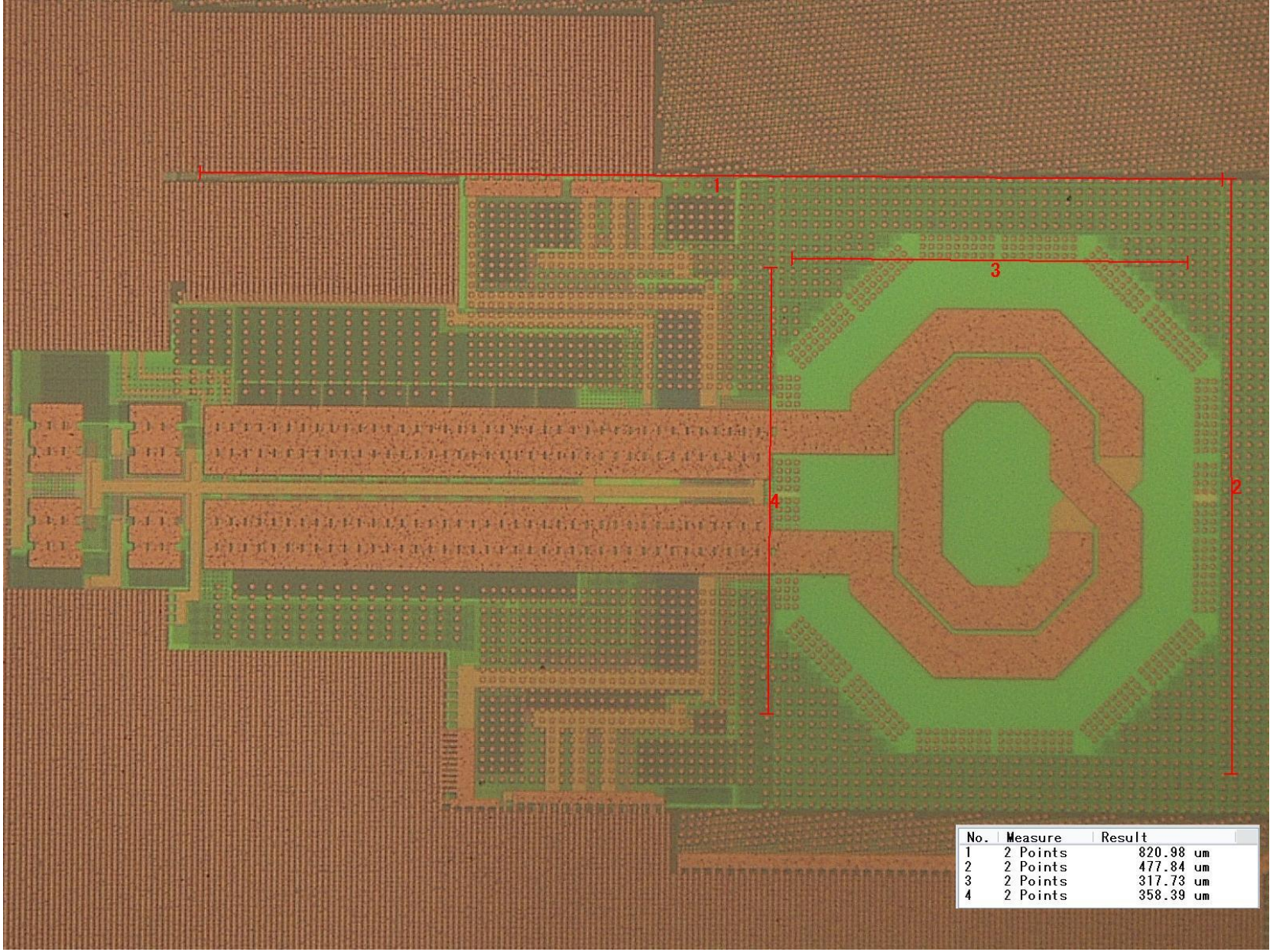
1
2
3
4
No. Measure Result
1 2 Points 820.98 um
2 2 Points 477.84 um
3 2 Points 317.73 um
4 2 Points 358.39 um