A low jitter PLL frequency synthesizer for high resolution TDCs in 65nm CMOS technology

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PLL synthesizer
Application

• High resolution Time-to-Digital converter PicoTDC SoC (1)
  o 3 ps LSB
  o 64 Channels
• 2.56 GHz based TDC timing generator
  o TDC requires high speed clock
  o Locked to 40 MHz – 50 MHz reference

• x 64 PLL required
  o Low additive jitter/phase noise
  o Jitter reduction

PLL synthesizer

Application

- Negative feedback loop
- Phase detector compares VCO clock with reference
  - Aligns VCO phase with reference phase
  - $\Phi_{in} = \Phi_{out}$ (phase lock)
- Adjusts VCO frequency with error signal
PLL synthesizer
Application

• Random timing noise
  o Jitter < 1 ps RMS

• Phase noise
  o $\sin(\omega t + \Phi(t))$
  o $\text{PN} = F(\Phi(t))$

• Reference clock noise
  o Low pass filter

• VCO clock noise
  o High pass filter
PLL synthesizer

Application

64 channels, 3ps or 12ps time binning

- 64 channels, 3ps: ~1W
- 64 channels, 12ps: ~0.4W
- 32 channels, 12ps: ~0.2W
PLL synthesizer

LJPLL Specs

- Additive jitter < 1 ps rms
- Power consumption < 100 mW
- Reference clock: 40 MHz – 50 MHz
- SEU aware design
- Configurable bandwidth (100 kHz – 2 MHz)
- Easy configuration (corner aware)
PLL synthesizer
Architecture

- LC based low noise oscillator
- /64 TMR divider
- TMR phase detector
- Configurable charge-pump/Filter

![PLL synthesizer architecture diagram]
PLL synthesizer
Charge pump

- 100 kHz – 2 MHz bandwidth
- Tunable charge pump current with on-chip reference
- Bias decoupling for SET protection
- Adjustable loop resistor
PLL synthesizer

Divider

• High speed CML prescaler (DIV4)
  o 1.5 mA current

• Low speed divider (DIV16)
  o Protection with TMR for SET
  o Standard cell design
  o Custom routed

• Fixed division ratio

• Selectable DIV2 at output
  o 2.56 GHz or 1.28 GHz
180 µm x 90 µm
PLL synthesizer vCO

- LC tank oscillator
- Optimized for low phase noise
  - Low tank Rs
- 700 pH inductor
  - Q=16
- PMOS current source
  - Lower 1/f noise
- 8 programmable capacitor banks
- 2.2 GHz – 3.5 GHz
- < -124 dBc/Hz @ 1 MHz phase noise
- 5 mA
PLL synthesizer
VCO

- High Q switched capacitors needed
- MOMCAP with Q > 35
- Q limited by switch
- Virtual grounded switch to improve Q→ Better phase noise
- MOMCAP have high variability (bad)
PLL synthesizer

VCO

- Distributed track to capacitor bank is relatively long
- EM simulations necessary for equivalent inductance (L-M)
- Lowers the tank’s Q
- Optimized shape for good M
- 1 pH/µm → 250 fH/µm (equivalent, s-parameter matching)
PLL synthesizer
VCO

- Automatic band selection required (MOMCAP variation)
- Digital binary search algorithm
- Fully TMR
VCO
Loop cap
AFC
PD+CP
Prog.
1.3mm
2mm
Measurements

- Characterizing PLL
  - Ultra low noise reference
- Agilent PSG signal generator
  - Only sine wave (~100 fs rms jitter)
  - 40 MHz at input buffer kills jitter
- 640 MHz reference → /16 on chip prescaler
Measurements

- R&S FSW PN-analyzer
  - Ideal noise floor
  - No histograms
  - Frequency domain analysis

- Tektronix DPO7000 sampling oscilloscope
  - Closed loop sampling
  - Worse noise floor (290 fs internal jitter)
  - Time-domain analysis
  - Histograms

1.2 V $V_{DD}$
25 °C
Open loop VCO

VCO frequency (Fdiv x 64, measured after divider), different capacitors switched

Frequency (GHz)

Vtune (V)
Open loop VCO

<table>
<thead>
<tr>
<th>Nominal Frequency</th>
<th>Measured Level</th>
<th>Measured Freq</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.561238549 GHz</td>
<td>-6.42 dBm</td>
<td>2.561238549 GHz</td>
</tr>
<tr>
<td>Ref Level &amp; Att</td>
<td>Initial Delta</td>
<td>Initial Delta</td>
</tr>
<tr>
<td>Measurement</td>
<td>Drift</td>
<td>Drift</td>
</tr>
<tr>
<td>-5.80 dBm, Att 0 dB</td>
<td>-0.11 dB</td>
<td>0 Hz / 0 ppm</td>
</tr>
<tr>
<td>10 kHz to 100 MHz</td>
<td>0 dB</td>
<td></td>
</tr>
</tbody>
</table>

-124dBc/Hz

40MHz spur (OL)
Closed loop PLL

- Phase step to verify damped system
Closed loop PLL

Nominal Frequency: 2.560023609 GHz
Ref Level & Att: -10.50 dBm, Att 0 dB
Measurement: 100 kHz to 100 MHz

Measured Level: -11.06 dBm
Initial Delta: 0.57 dB
Drift: 0.02 dB

Measured Freq: 2.560023609 GHz
Initial Delta: 94.03 MHz / 38131.77 ppm
Drift: 1.04 Hz / 0 ppm

Jitter: 339.64 fs
Closed loop PLL

Phase noise

- Offset Frequency

- Rms Jitter (ps)

Integrated jitter

- Offset Frequency integration limit
Closed loop PLL (DPO7000)

![Graph showing jitter and RMS values](image-url)
AFC calibration

Frequency (MHz)

100µs

Period (ns)

Start 0 1 2 3 PLL acquisition

Period (ns)
Summary

• Designed and tested LJPLL chip
• LC oscillator based clock generator
• 350 fs rms jitter measured
• <30 mW power consumption
• 100 kHz – 2 MHz programmable bandwidth
• Automatic band selection algorithm included
Thank You

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