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A low jitter PLL frequency synthesizer for high resolution TDCs in 65nm CMOS technology

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A PLL has been designed for high frequency clock generation with only 280 fs RMS jitter. The integer N PLL multiplies a 40 MHz reference clock to 2.56 GHz. The PLL uses a low phase noise LC tank oscillator that has a tuning range from 2.4 GHz to 3.7 GHz with a phase noise of only 125 dBc/Hz @ 1 MHz and a power consumption of 5.7 mW. An all-digital automatic frequency calibration circuit is included to select the optimal frequency range of the VCO.

Summary

Next generation particle detectors such as ATLAS, CMS and ALICE require high resolution Time-to-Digital Converters (TDCs), which are typically based on a high frequency DLL timing generator. This work proposes an integrated PLL synthesizer that multiplies a 40 MHz reference clock by 64 to 2.56 GHz and can be used to provide low jitter clock signals to the timing generator of the TDC channels. Since the resolution of the TDC is scaled down towards sub-picosecond ranges, the clock generation requires low timing noise.
The integer-N PLL includes an integrated low phase noise LC-tank VCO that can be used in different configurations to provide low phase noise or higher supply rejection. The tuning range of the VCO is split into 8 sub-bands and has a tuning range from 2.4 GHz to 3.7 GHz. This ensures that a reference clock ranging from 40 MHz to 50 MHz can be used to drive the PLL in all process corners.
A highly configurable charge-pump and loop filter allows flexible customization of the loop characteristics depending on the quality of the reference clock. Jitter that originates from the reference clock can be filtered by the loop depending on the configuration the filter.
The PLL includes an all-digital automatic frequency calibration (AFC) circuit to select the optimal sub-band of the VCO. The AFC is based on an FSM that uses two counters to detect the frequency difference of the divided VCO and the reference clock. The FSM uses a binary search algorithm to find the optimal VCO configuration that may depend on the process corner. This algorithm can select the optimal configuration in less than 110 µs. The AFC is implemented using a Triple-Modular Redundant (TMR) FSM to prevent single-events from disturbing the calibration cycle.

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