Session Program

28 September 2015 to 2 October 2015

TWEPP 2015 - Topical Workshop on Electronics for Particle Physics

ASICs

Lisbon
IST (Instituto Superior Técnico) Alameda Campus Av. Rovisco Pais, 1 1049-001 Lisboa Portugal

Tuesday 29 September

14:50

ASICs

Session |
Location: Lisbon, Grande Anfiteatro, IST (Instituto Superior Técnico) Alameda Campus Av. Rovisco Pais, 1 1049-001 Lisboa Portugal |
Convener: Christophe De La Taille

14:50–15:15

A High Frame Rate Pixel Chip Design for Synchrotron Radiation Applications

Speaker
Wei Wei

15:15–15:40

65 nm CMOS analog front-end for pixel detectors at the HL-LHC

Speaker
Luigi Gaioni

15:40–16:05

Front End ASIC for AGIPD, a high dynamic range fast detector for the European XFEL

Speaker
Dr Alexander Klyuev

16:05

Wednesday 30 September

09:50

ASICs

Session |
Location: Lisbon, Grande Anfiteatro, IST (Instituto Superior Técnico) Alameda Campus Av. Rovisco Pais, 1 1049-001 Lisboa Portugal |
Convener: Christophe De La Taille

09:50–10:15

Front end Optimization for the Monolithic Active Pixel Sensor of the ALICE Inner Tracking System Upgrade

Speaker
Daehyeok Kim

10:15–10:40

Charge Collection Properties of a Depleted Monolithic Active Pixel Sensor using a HV-SOI process

Speaker
Sonia Fernandez Perez

10:40

11:10

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Convener: Christophe De La Taille

11:10–11:35

Prototyping of an HV-CMOS demonstrator for the High Luminosity-LHC upgrade

Speaker
Eva Vilella

11:35–12:00

Development on CMOS MAPS devices for the ATLAS Phase-II Strip Tracker Upgrade

Speaker
Todd Brian Huffman

12:00–12:25

Prototype active silicon sensor in LFoundry 150nm HV/HR-CMOS technology for ATLAS Inner Detector Upgrade

Speaker
Piotr Rymaszewski

12:25

14:50

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Convener: Alessandro Marchioro

14:50–15:15

Design and results of a 65 nm digital readout Macro Pixel ASIC (MPA) prototype with on-chip particle recognition for the Phase II CMS Outer Tracker upgrade

Speaker
Davide Ceresa

15:15–15:40 **A 128-channel event driven readout ASIC for the R3B Tracker**

Speaker
Mr Lawrence Jones

15:40–16:05
PACIFIC: The readout ASIC for the SciFi Tracker planned for the upgrade of the LHCb detector

Speaker
Jose Mazorra De Cos

16:05

Thursday 1 October

09:50

ASICs

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Location: Lisbon, Grande Anfiteatro, IST (Instituto Superior Técnico) Alameda Campus Av. Rovisco Pais, 1 1049-001 Lisboa Portugal |
Convener: Marcus Julian French

09:50–10:15 **SAMPA Chip: a New ASIC for the ALICE TPC and MCH Upgrades**

Speaker
Marco Bregant

10:15–10:40 **FATALIC: A dedicated Front-End ASIC for the Atlas TileCal Upgrade**

Speaker
Laurent Royer

10:40

11:10

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Convener: Marcus Julian French

11:10–11:35
KLauS: A low power Silicon Photomultiplier Charge Readout ASIC in .18 UMC CMOS

Speaker
Konrad BRIGGL

11:35–12:00
A low jitter PLL frequency synthesizer for high resolution TDCs in 65nm CMOS technology

Speaker
Jeffrey Prinzie

12:00–12:25
A fast multichannel, ultra-low power 10-bit ADC for readout of future particle physics detectors

Speaker
Marek Idzik

12:25

14:50

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Convener: Mitchell Franck Newcomer

14:50–15:15
Redundant SAR ADC architecture and circuit techniques for ATLAS LAr Phase-II upgrade

Speaker
Yun Chiu

15:15–15:40

Development of a low power Phase-Locked Loop (PLL) and Delay-Locked Loop (DLL) in 130nm CMOS technology

Speaker
Miroslaw Firlej

15:40–16:05 **GBLD10+: A Compact Low-power 10 Gb/s VCSEL Driver IC**

Speaker
Tao Zhang

16:05