BND School 2015

International Summer School on Particle Physics

Tracking and Tracking Detectors

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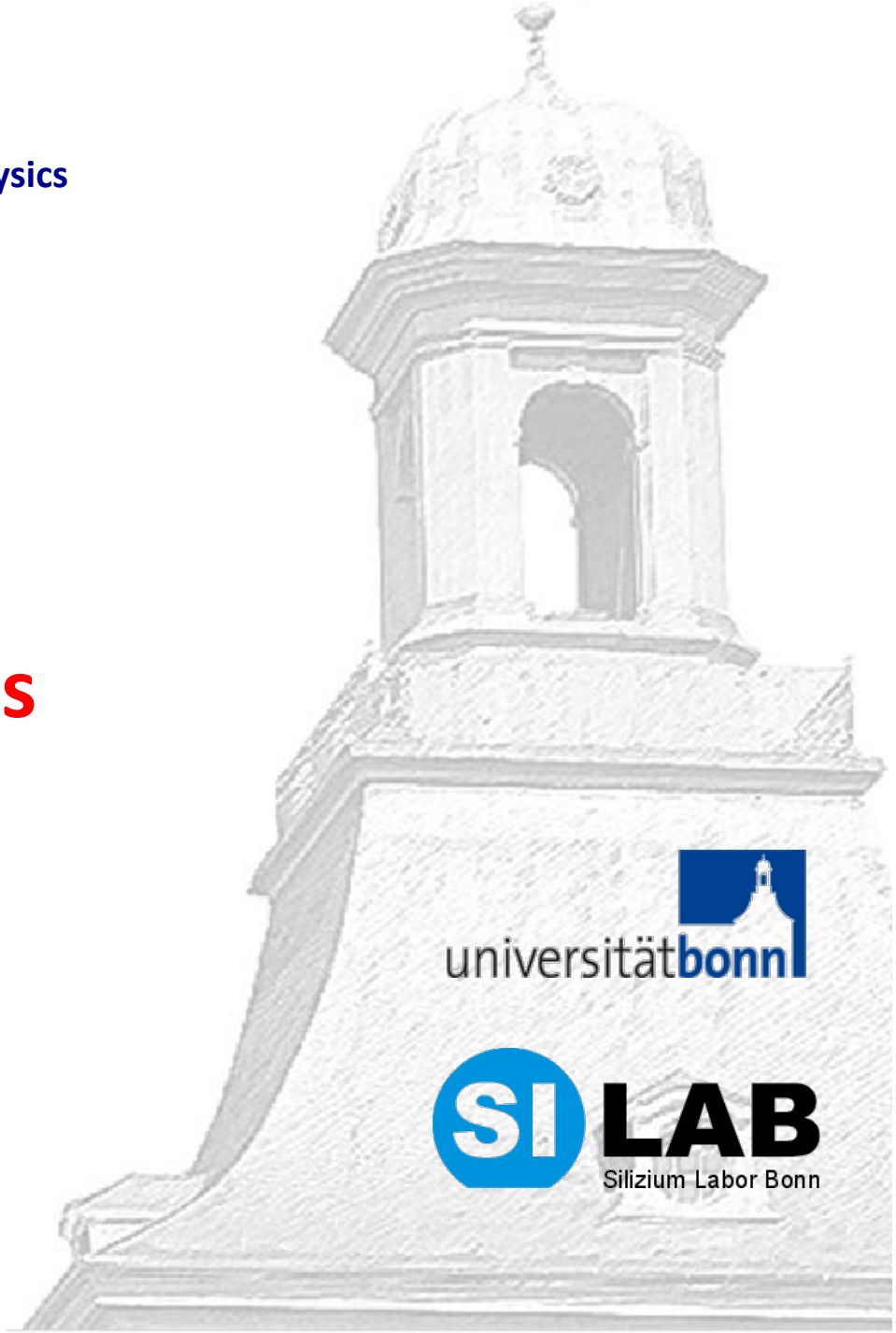

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Outline

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Lecture 1

Tracking

- momentum measurement
- vertex measurement
- influence of multiple scattering
- errors and what to do …

Lectures 2 & 3

Tracking Detectors

- the signal and the noise
- spatial resolution with structured electrodes
- gaseous detectors
- semiconductor detectors

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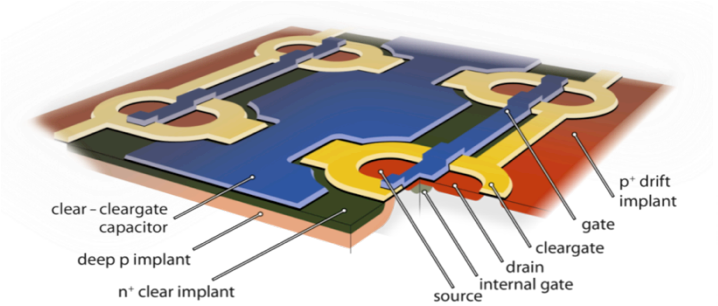
Lecture 3

Tracking Detectors (Semiconductors)



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Content Lecture 3

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- Looking back at LHC trackers
- Tasks of strip/pixel detectors
- Fundamentals of silicon detectors
  - pn and other junctions
  - single and double sided detectors
  - signal and noise
  - δ electrons
  - Ramo for strips again
  - Lorentz angle
- Hybrid Pixels
  - sensors
  - front end chips
  - amplifiers, shapers, pile-up
  - thresholds and intime thresholds
  - hybridization
  - biasing
- Large tracking detectors
- Upgrades of pixel detectors
- Radiation Damage
  - sensor damage and curing measures
  - R/O chip damage and cures
- Noise in ionization detectors
  - Don't be afraid about noise theory
  - When to care about noise?
  - Noise sources in a typical detector system
  - Calculating the noise of a pixel/strip system
- How to make things better?
  - Radiation hard sensors and electronics
- Monolithic approaches for pixels
  - DEPFET pixels
  - Monolithic pixels (MAPS)

Looking back at 3 years of LHC (25 /fb) ...

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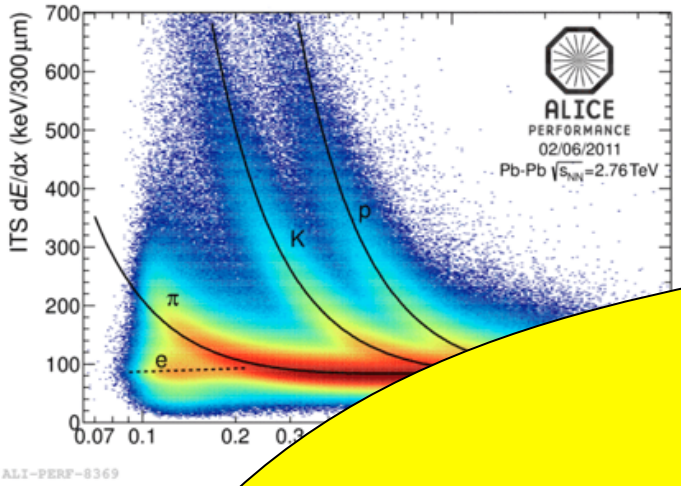
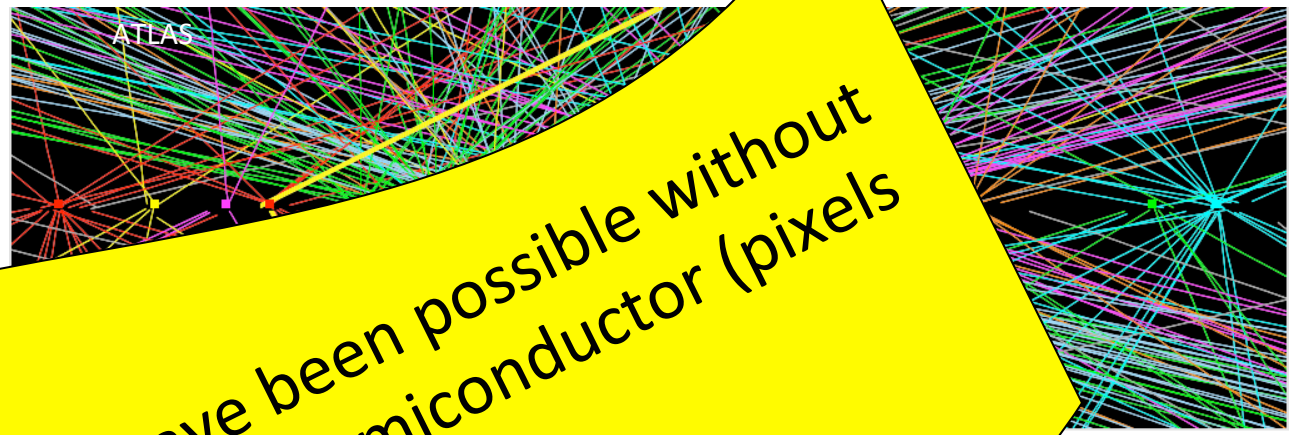
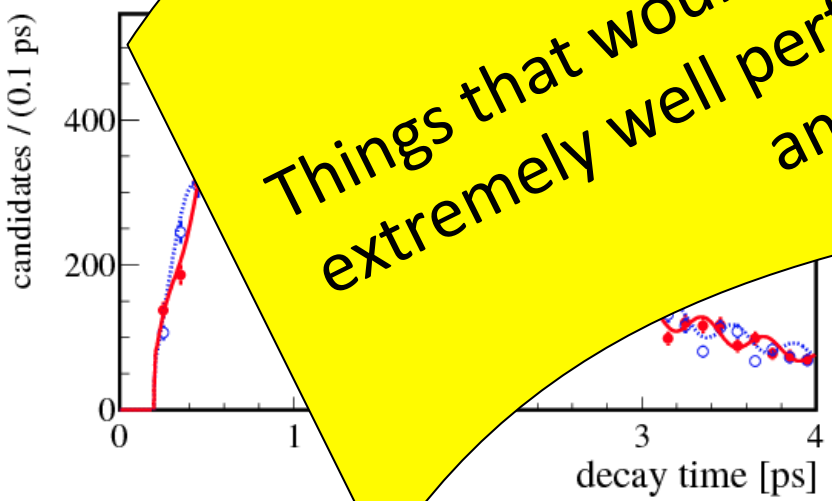
- This is a definitively a success story !

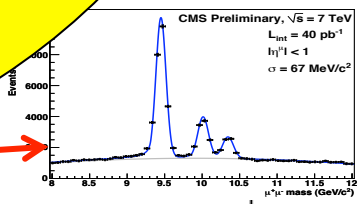
~70 interaction /BX

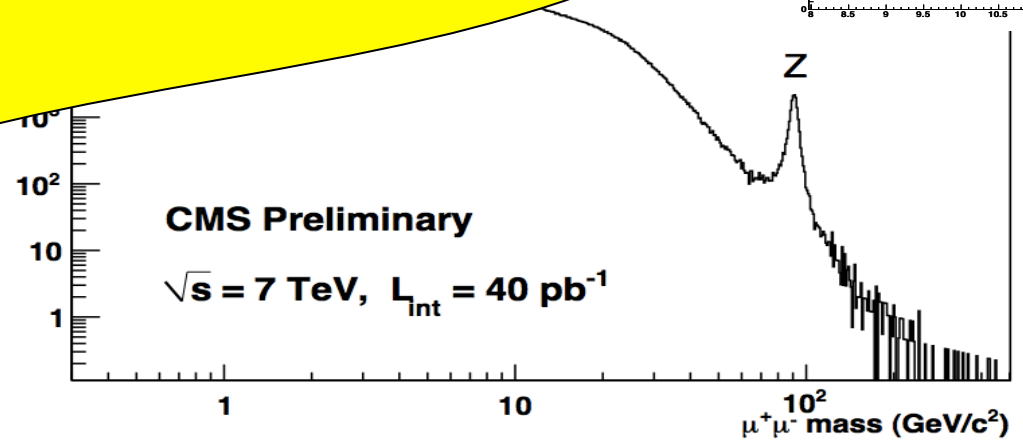




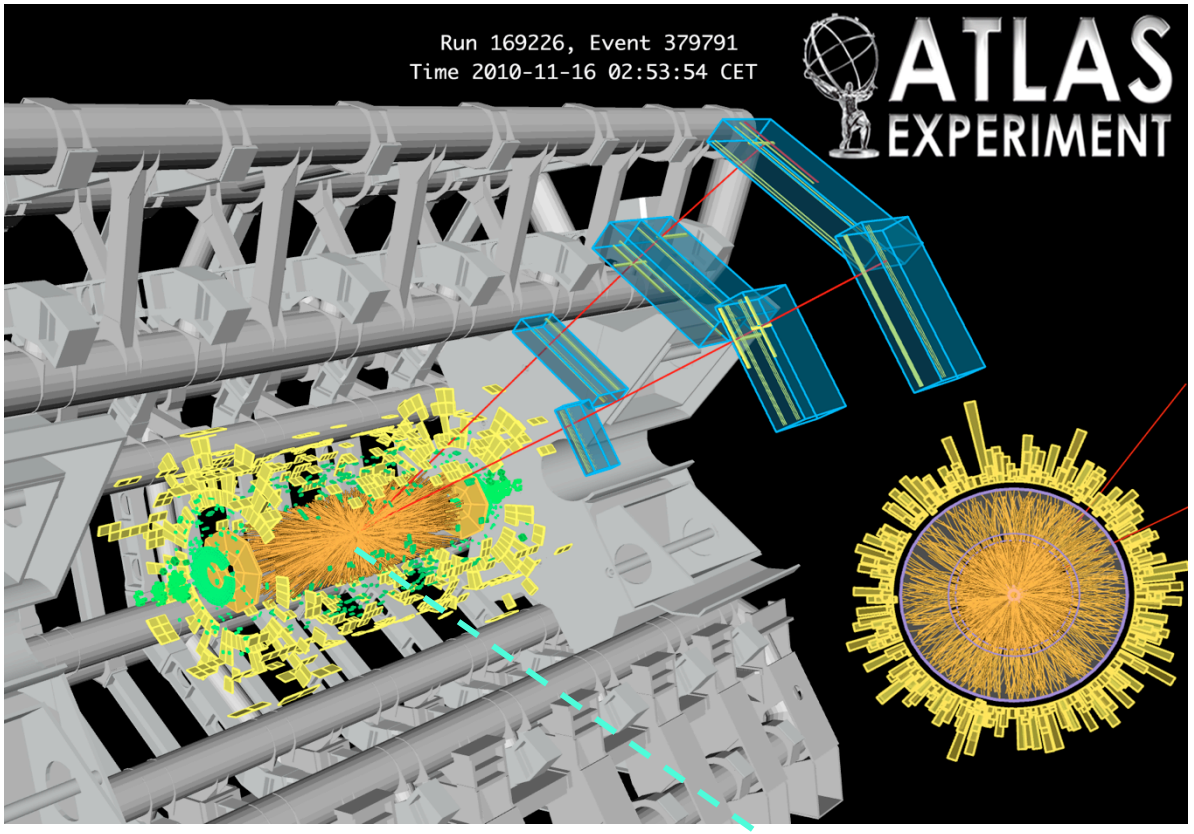
Things that would not have been possible without extremely well performant semiconductor (pixels and strips) trackers







Tracking in pp collisions at 14 TeV (LHC)



~1200 tracks every 25 ns
or ~ 10^{11} per second

⇒ high radiation dose

10^{15} n_{eq} / cm^2 / 10 yrs @ LHC

or

600 kGy (60 Mrad)
through the ionisation of
mips in 250 µm bulk silicon

position of
tracking detector (pixels, strips, straw tubes)

LHC ≅ 10^6 x LEP in track rate !

Note: LHC Upgrade (2026): HL–LHC = LHC x 10 !

Tasks of semiconductor strip and pixel detectors

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1. Pattern Recognition and Tracking
   - precision tracking points in 3D → track seeding
   - 1 pixel layer ←→ 3-4 strip layers (x,y & u,v for ambiguities)

2. Vertexing (primary and secondary vertex) [1)]
   - impact parameter resolution ~10µm (rφ), ~70µm (z)
   - secondary vertex resolution ~50µm (rφ), ~70µm (z)
   - primary vertex resolution ~11µm (rφ), ~45µm (z)
   - (life) time resolution ~70 fs

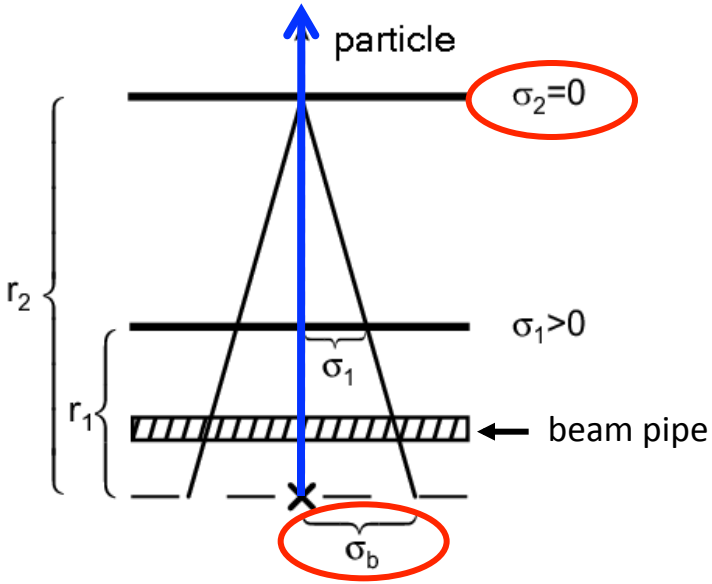
3. Momentum measurement [1)]

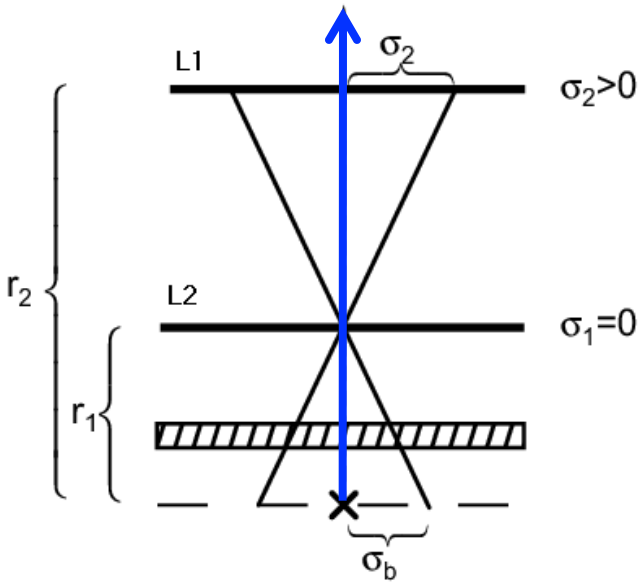
$$\frac{\sigma_{p_T}}{p_T} = 0.03\%\ p_T(\mathrm{GeV}) \oplus 1.2\%$$

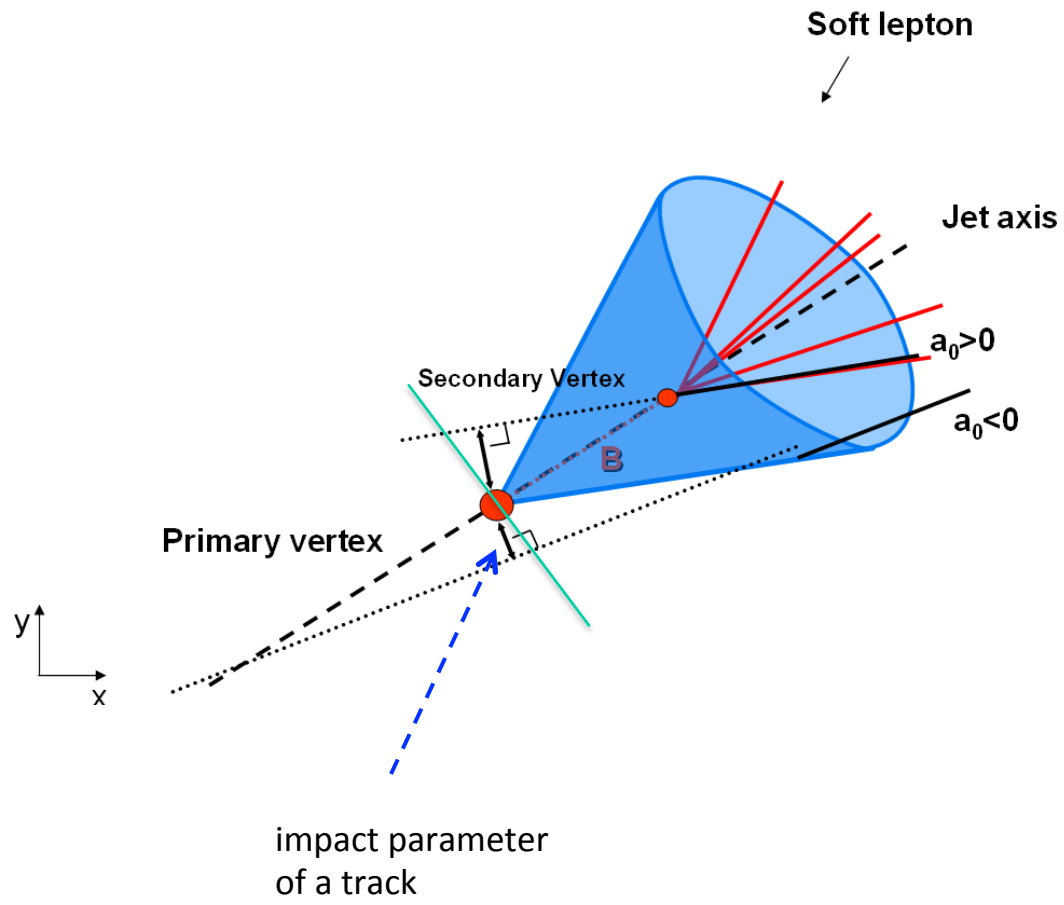
(inner detector)

[1)] values for ATLAS

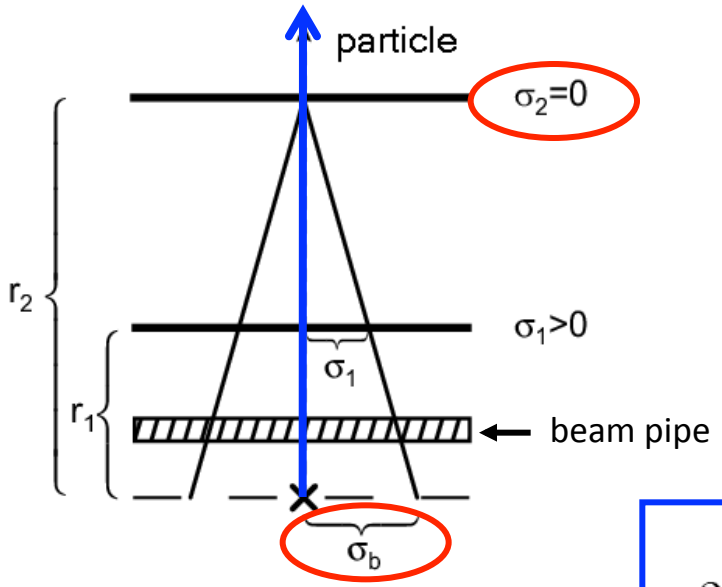
Impact parameter resolution (simplified)







Impact parameter resolution (simplified)

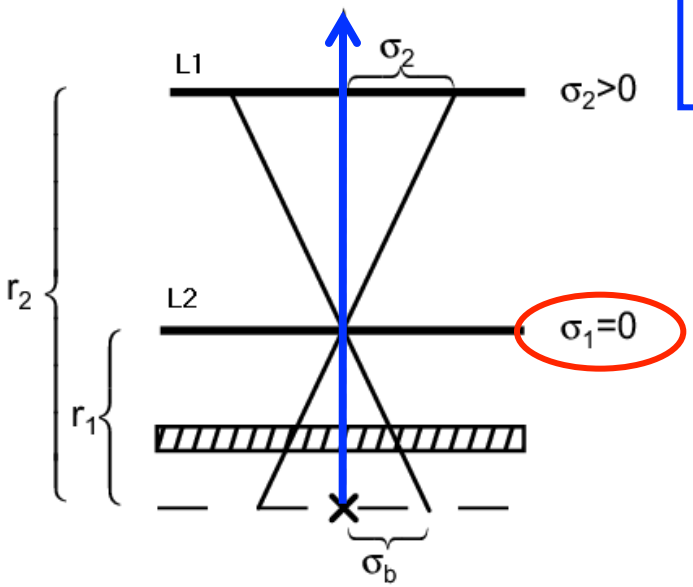


$$\frac{\sigma_b}{\sigma_1} = \frac{r_2}{r_2 - r_1}$$

small !

small !

$$\sigma_b^2 = \left(\frac{r_1}{r_2 - r_1}\,\sigma_2\right)^2 + \left(\frac{r_2}{r_2 - r_1}\,\sigma_1\right)^2 + \sigma_{MS}^2$$



$$\frac{\sigma_b}{\sigma_2} = \frac{r_1}{r_2 - r_1}$$

small x/X_0

$$\sigma_{MS} \sim \frac{1}{p}\sqrt{\frac{x}{X_0}}$$

Semiconductors suited for detectors

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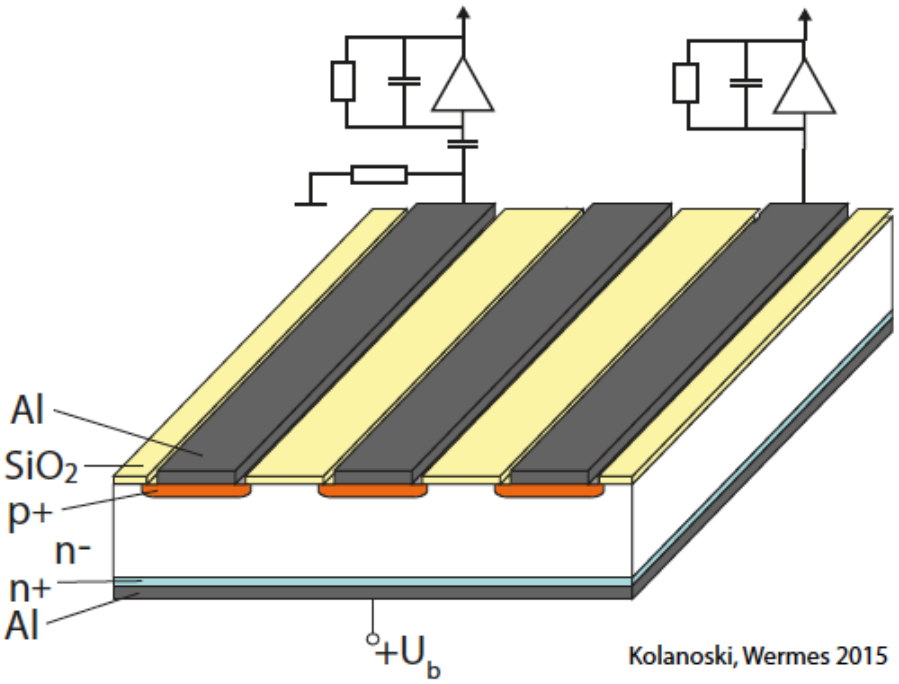
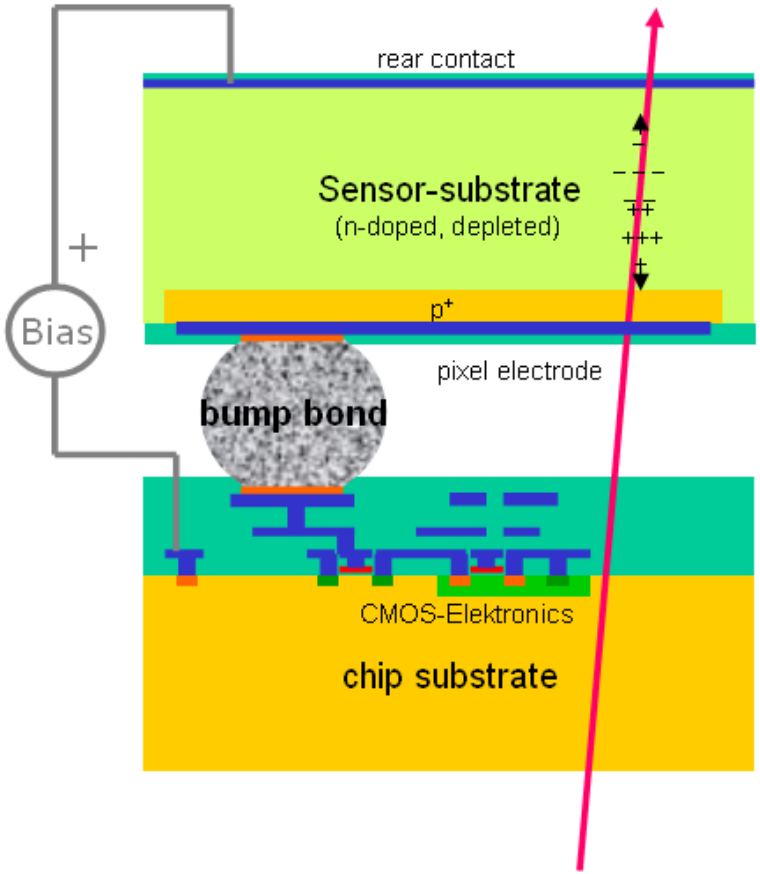
Semiconductor	band gap (eV)	intrinsic carrier conc. (cm^{-3})	average Z	w_{eh} (eV)	mobility cm^2/Vs e	h	carrier life time
Si	1.12	$1.45 \cdot 10^{10}$	14	3.61	1450	505	100μs
Ge	0.66	$2.4 \cdot 10^{13}$	32	2.96	3900	1800	
GaAs	1.42	$1.8 \cdot 10^{6}$	32	4.35	8800	320	1-10 ns
CdTe	1.44	10^{7}	50	4.43	1050	100	0.1-2 μs
CdZnTe	~1.6		49.1	4.6	~1000	50-80	~ μs
CdS	2.42		48 + 16	6.3	340	50	
HgI_2	2.13		62	4.2	100	4	~ μs
InAs	0.36		49 + 33		33000	460	
InP	1.35		49 + 15		4600	150	
ZnS	3.68		30 + 16	8.23	165	5	
PbS	0.41		82 + 16		6000	4000	
Diamond	5.48	$<10^{3}$	6	13.1	1800	1400	~1 ns

photon absorption by photo effect ~$Z^{(4-5)}$

Fundamentals of Semiconductor Detectors



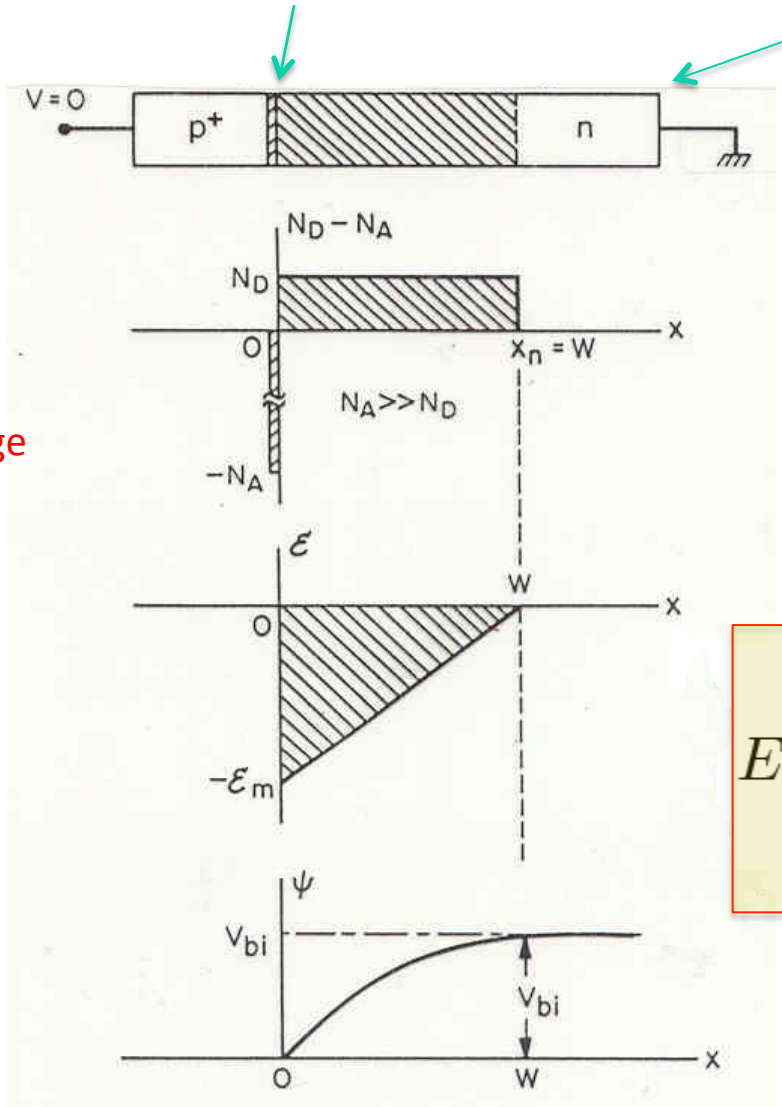
Microstrip Detector



Pixel Detector

The pn junction as a semiconductor particle detector

thin (~µm), highly doped p^+ ($\sim 10^{19}$ cm^{-3}) layer on lightly doped n^- ($\sim 10^{12}$ cm^{-3}) substrate



Space charge region (depleted of mobile charge carriers)

Electric field

Potential

reverse biased junction

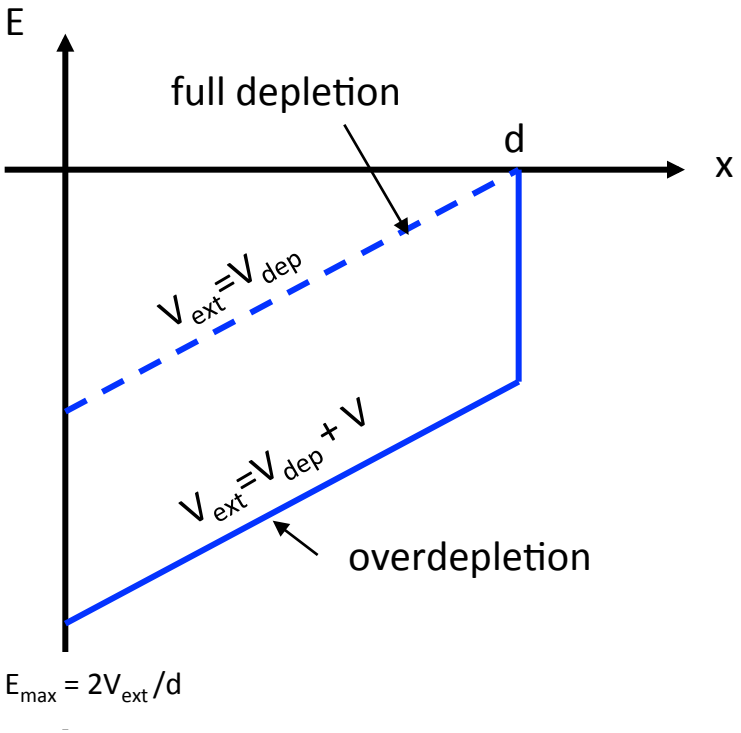
$$N_A x_p = N_D x_n$$ neutrality condition

$$\frac{dE}{dx} = \frac{1}{\epsilon}\rho(x)$$ Maxwell

$$E(x) = \begin{cases} \frac{-eN_A}{\epsilon}(x + x_p) \; ; -x_p < x < 0 \\ \frac{+eN_D}{\epsilon}(x - x_n) \; ; 0 < x < x_n \end{cases}$$

$$V_{bi} = \frac{e}{2\epsilon}\left(N_A x_p^2 + N_D x_n^2\right)$$

The pn junction as a semiconductor particle detector



$E_{max} = 2V_{ext}/d$

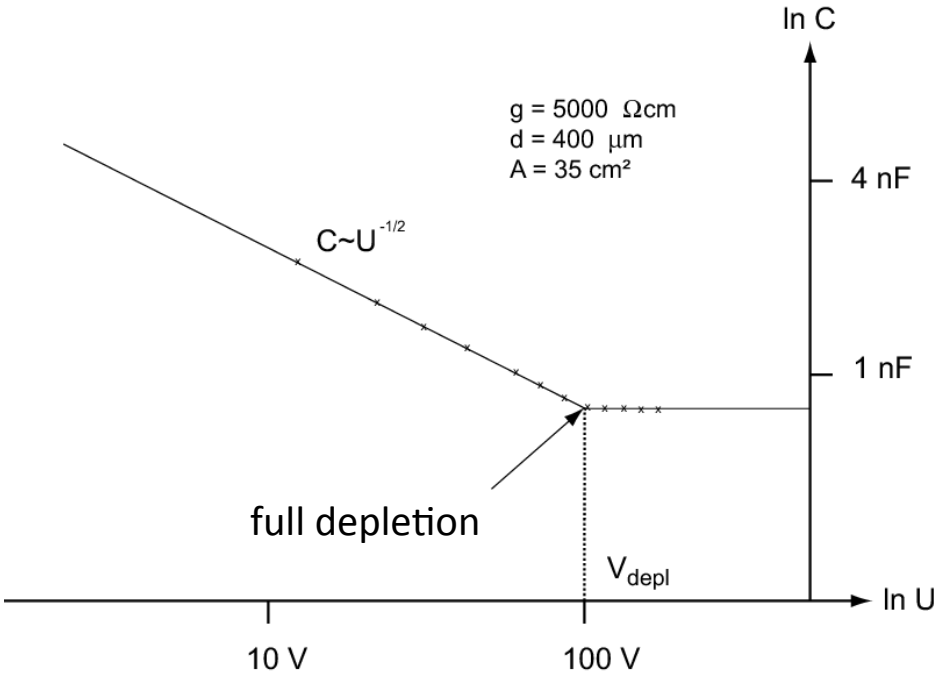
with applied external bias voltage

$$E(x) = -\frac{V + V_{dep}}{d} + \frac{2V_{dep}\,x}{d^2}$$

$$d = x_n = \sqrt{\frac{2\epsilon}{e}\frac{1}{N_D}\left(V_{bi} + V_{ext}\right)} \propto \sqrt{V_{ext}}$$

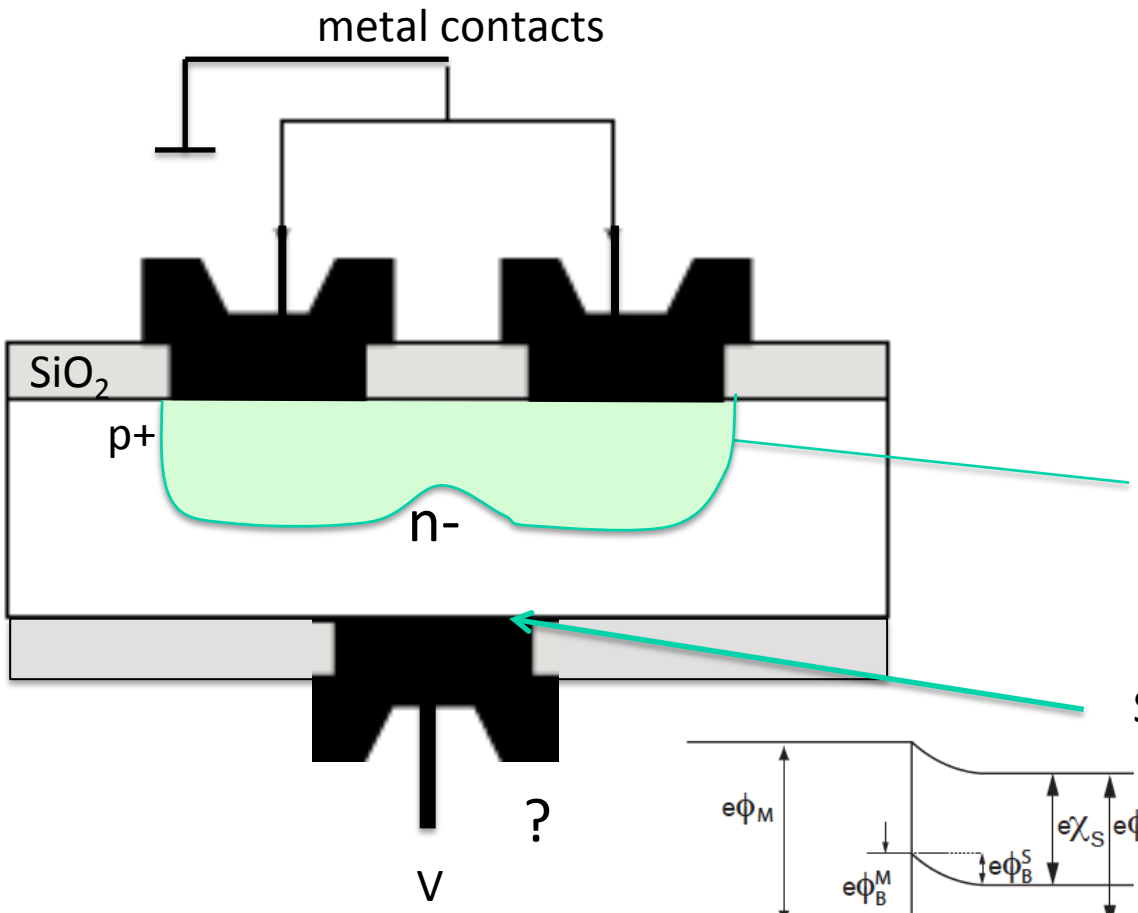
capacitance

$$\frac{C}{A} = \frac{1}{\epsilon\epsilon_0}\frac{1}{d} \propto \frac{1}{\sqrt{V_{ext}}}$$

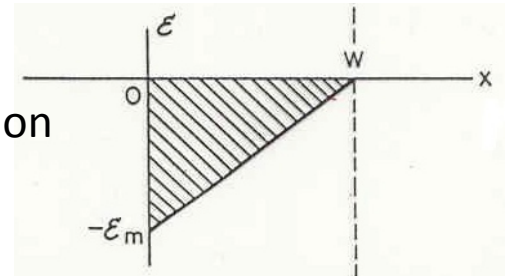


depletion zone grows from the junction into the lower doped bulk

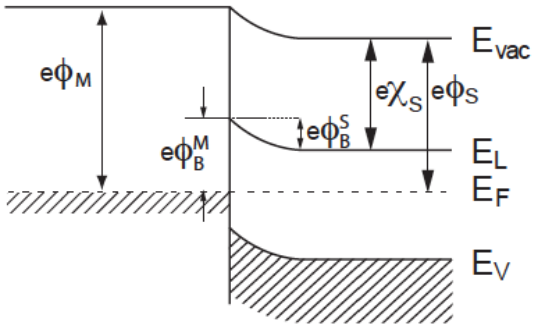
Contacts

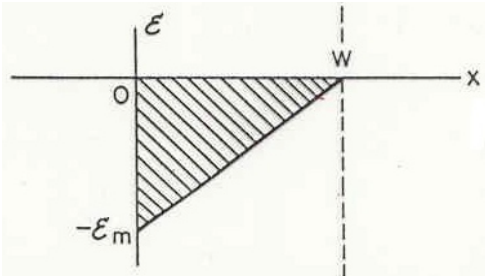


pn - junction



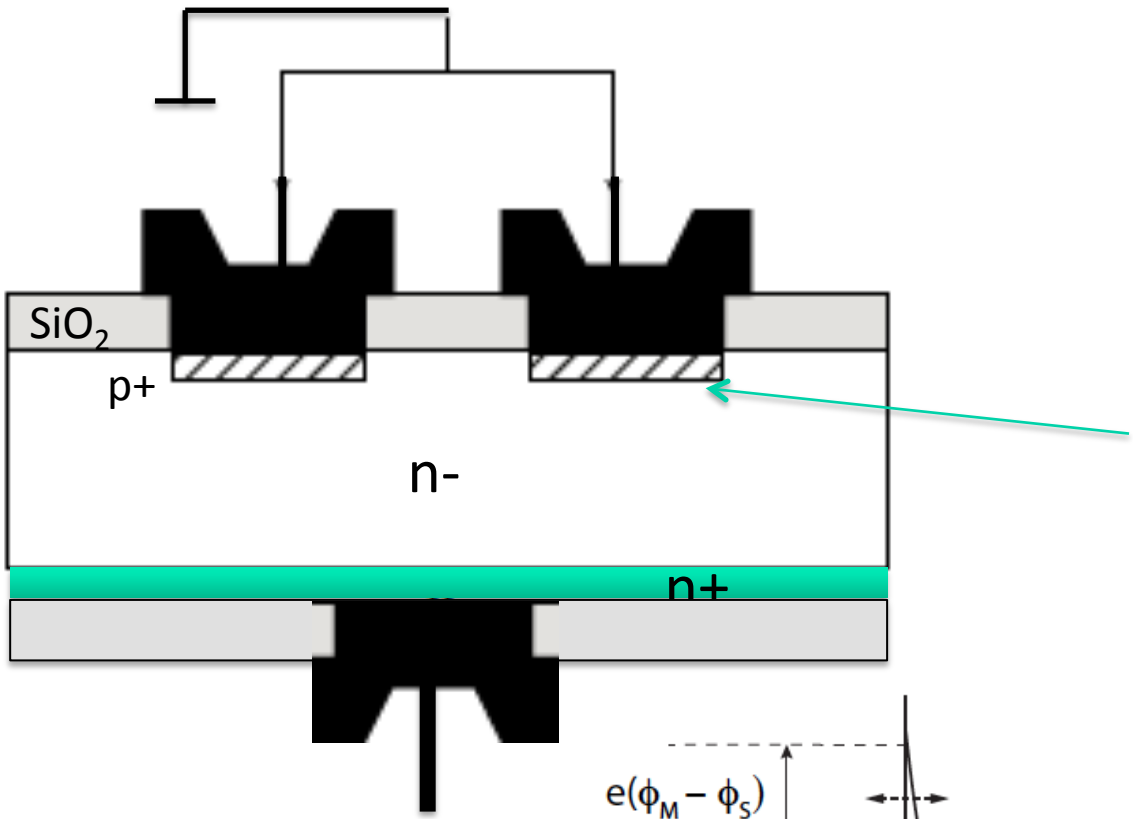
Schottky contact



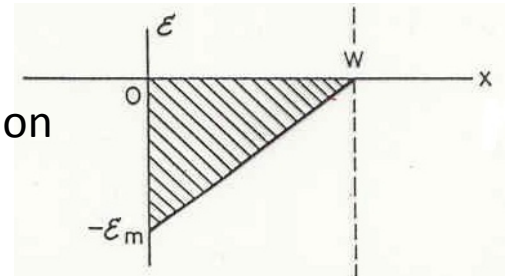


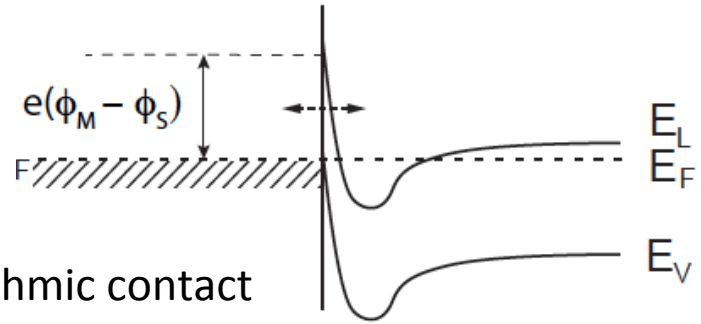
metal semiconductor

Contacts



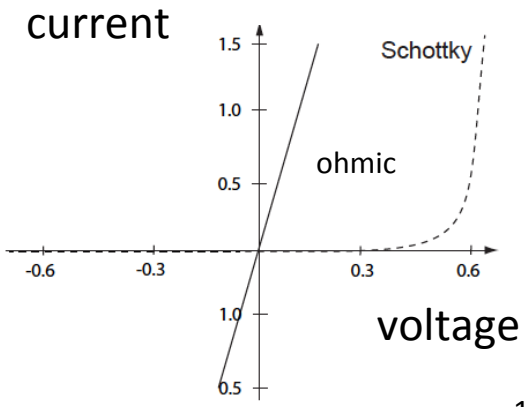
pn - junction





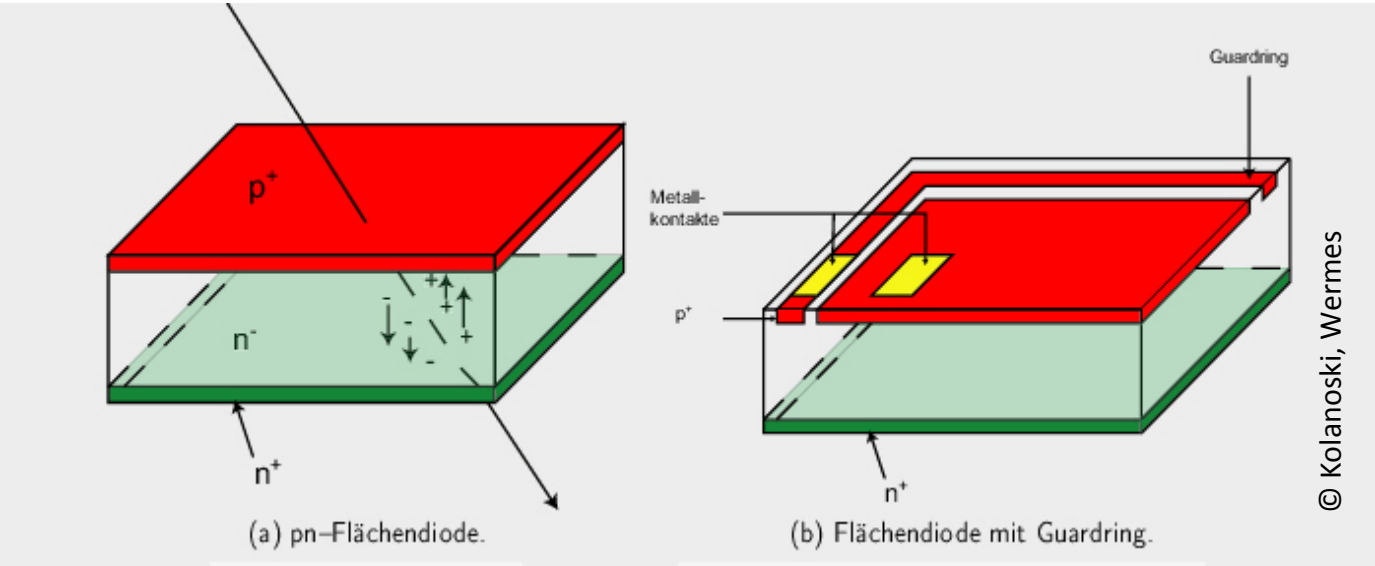
ohmic contact

current



voltage

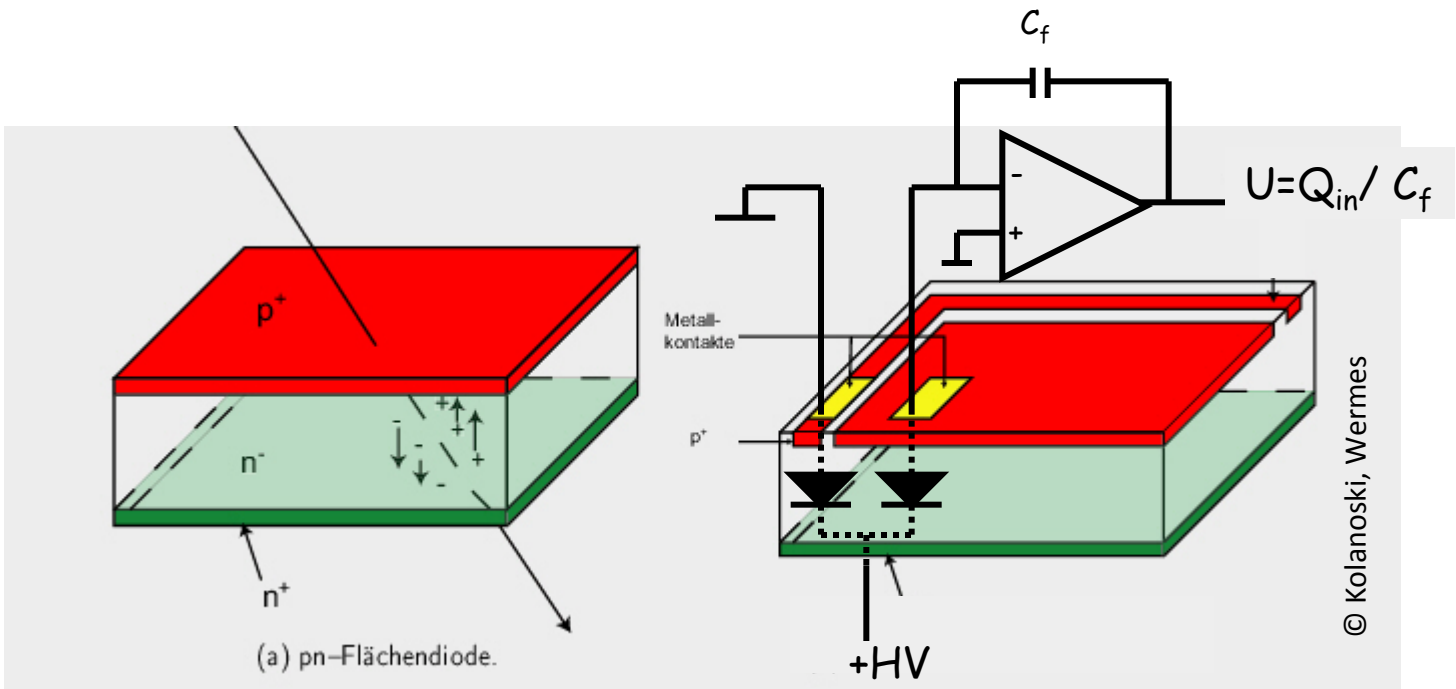
Detector shapes



pn area diode

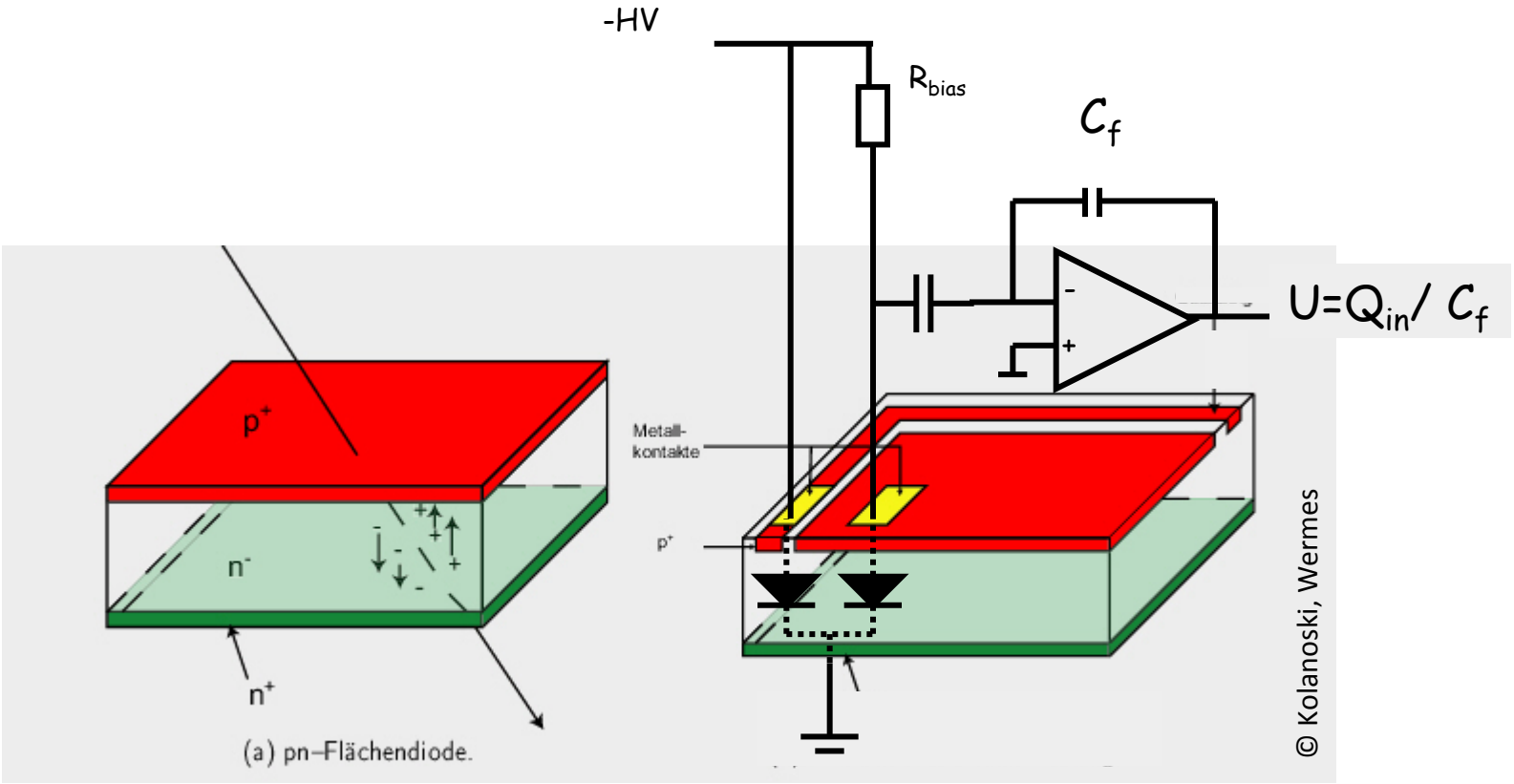
area diode w/ guard ring

Detector shapes



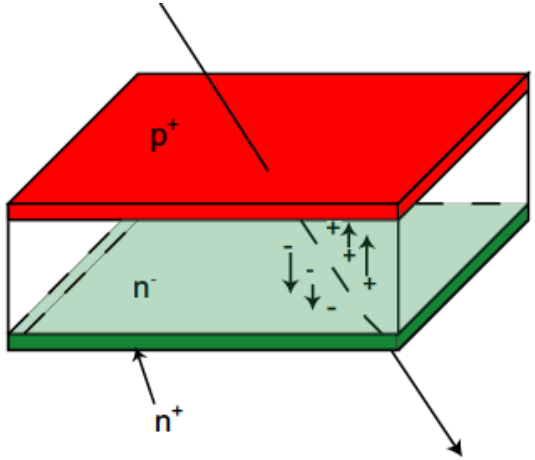
DC - Coupling

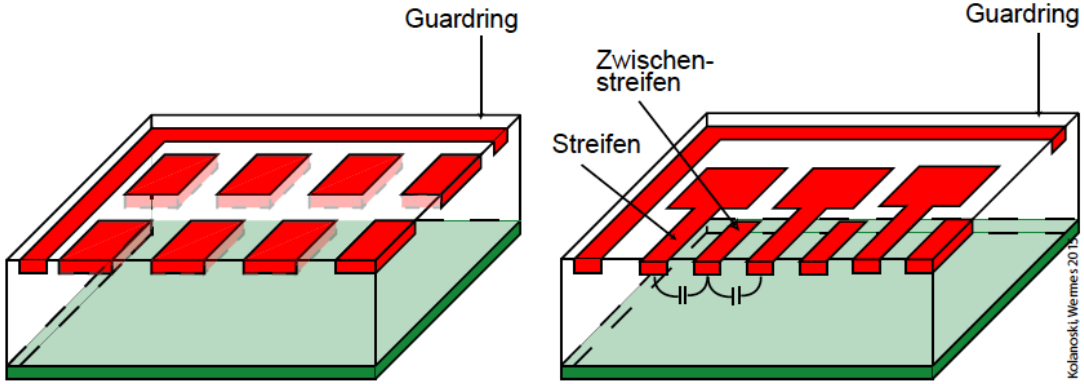
Detector shapes



AC - Coupling

The Signal in pixel detectors => particle tracks





in Si bulk fully depleted

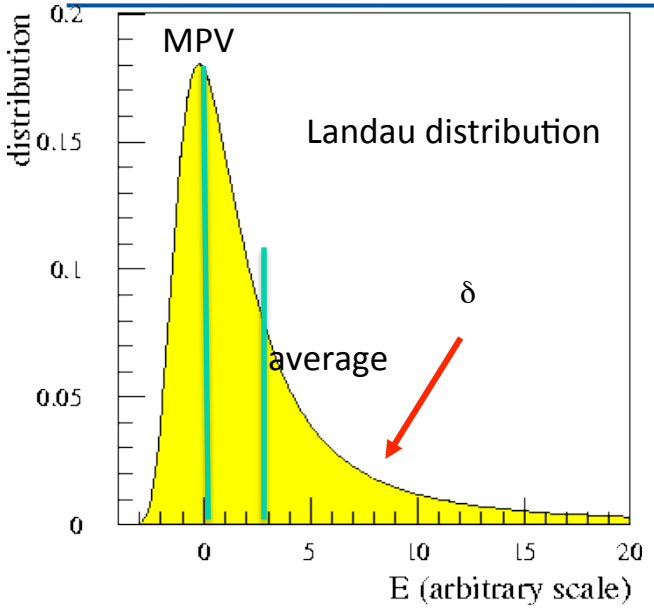
- w_i = 3.65 eV per e/h
- a high energy particle
  → ~ 80 e/h per µm
- all charge collected
- ~ 20 000 e/h per 250 µm
  = 3 fC

- radiation
  e.g. 10 keV X-ray: 3000 e/h
  ≈ 0.5 fC

- pixel or strip pattern
- typical cells: 100 x 150 µm²
  50 x 400 µm²
- charge drift in E-field
- charge diffusion σ ~ 8-10 µm
  → charge spreads over 2-3 pixels/strips

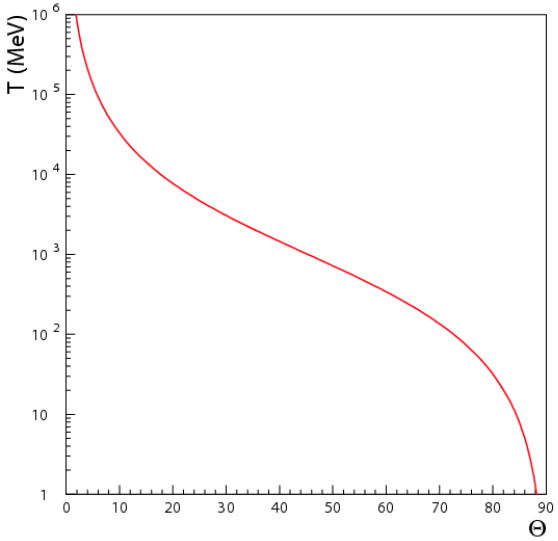
note: photo effect ~$Z^{(4-5)}$
Si → CdTe, CZT, HgI_2, …

Charge distribution and delta electrons



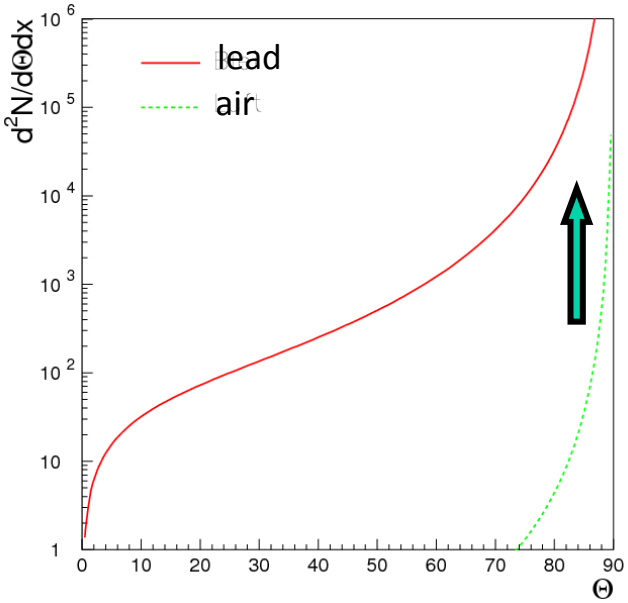
kinematics: 1-1 relation between emission angle and kin. energy

$$\Theta_e(T) = \arctan\left[\frac{1}{\gamma}\left(\frac{T_{\max}}{T}-1\right)^{\frac{1}{2}}\right] \simeq \arctan\sqrt{\frac{2m}{T}}$$



slow ones emitted at right angles
→ in $1/\beta^2$ part of BBF
→ highly ionizing

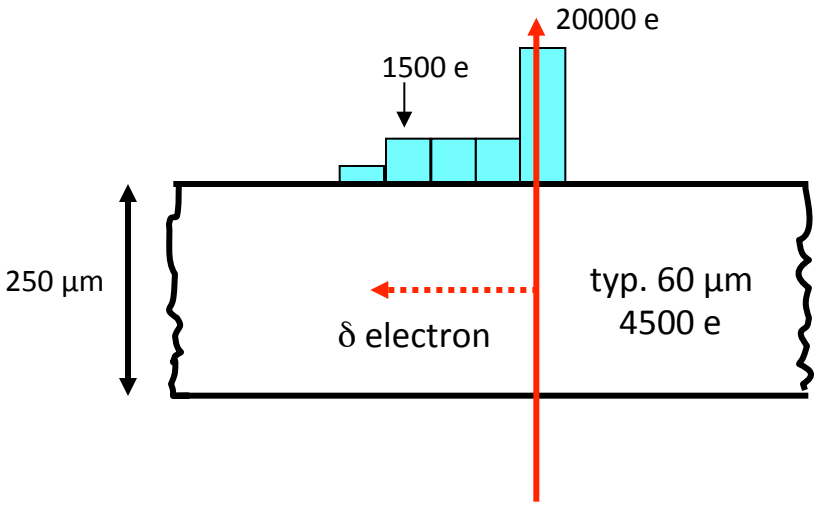
$$\frac{dN}{d\Theta} = \frac{1}{2} D z^2 \frac{Z}{A} \rho x \frac{\sin\Theta}{\cos^3\Theta}$$



for experimentalists

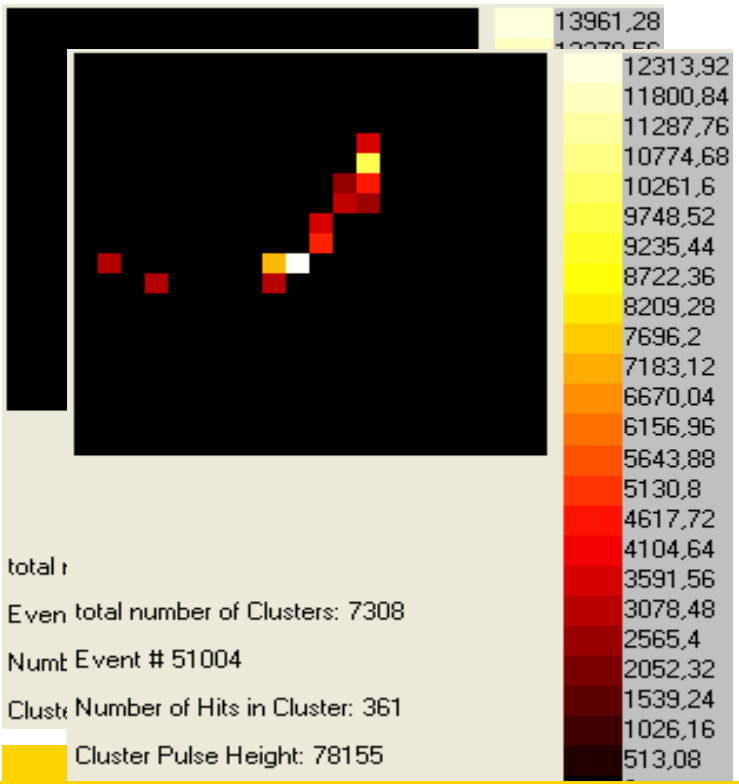
δ- electrons are "always" emitted at 90^0 and are highly ionizing

Delta electrons



effect of δ -electrons

100 keV δ-electron occurs in 300 µm Si with 6% probability and has “range” of 60 µm



δ-electron with perpendicular emission

DEPFET pixels (25 µm x 25 µm)

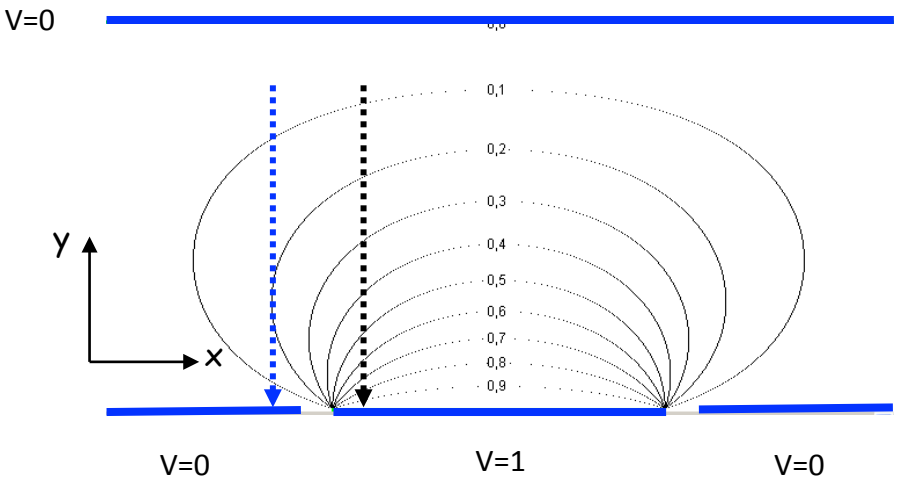
skip Lorentz angle?

Signal generation in a strip/pixel detector

reminder: weighting field and weighting potential

$$i_{e/h} = \frac{dQ_{e/h}}{dt} = q\vec{E}_W \cdot \vec{v}$$

$$dQ = q\vec{\nabla}\Phi_W d\vec{r}$$



Φ_W for a strip/pixel geometry

$$\Phi(x,y) = \frac{1}{\pi}\arctan\frac{\sin(\pi y)\cdot\sinh(\pi\frac{a}{2})}{\cosh(\pi x)-\cos(\pi y)\cosh(\pi\frac{a}{2})}$$

Signal generation in a magnetic field

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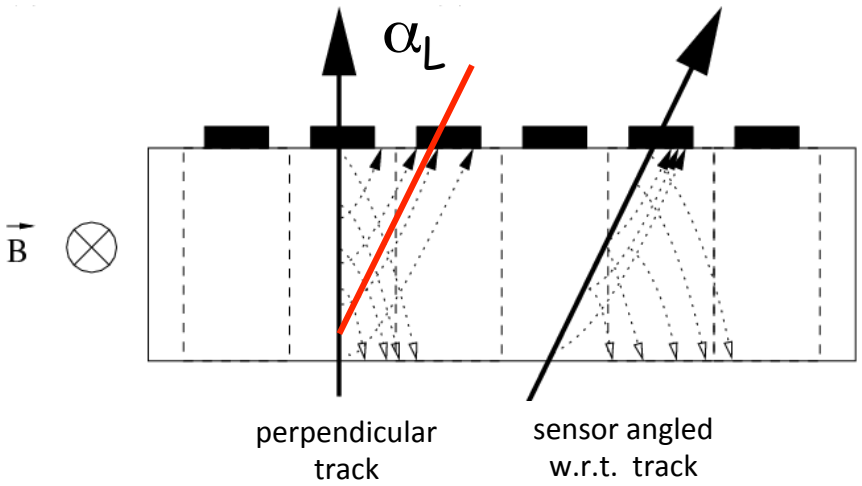
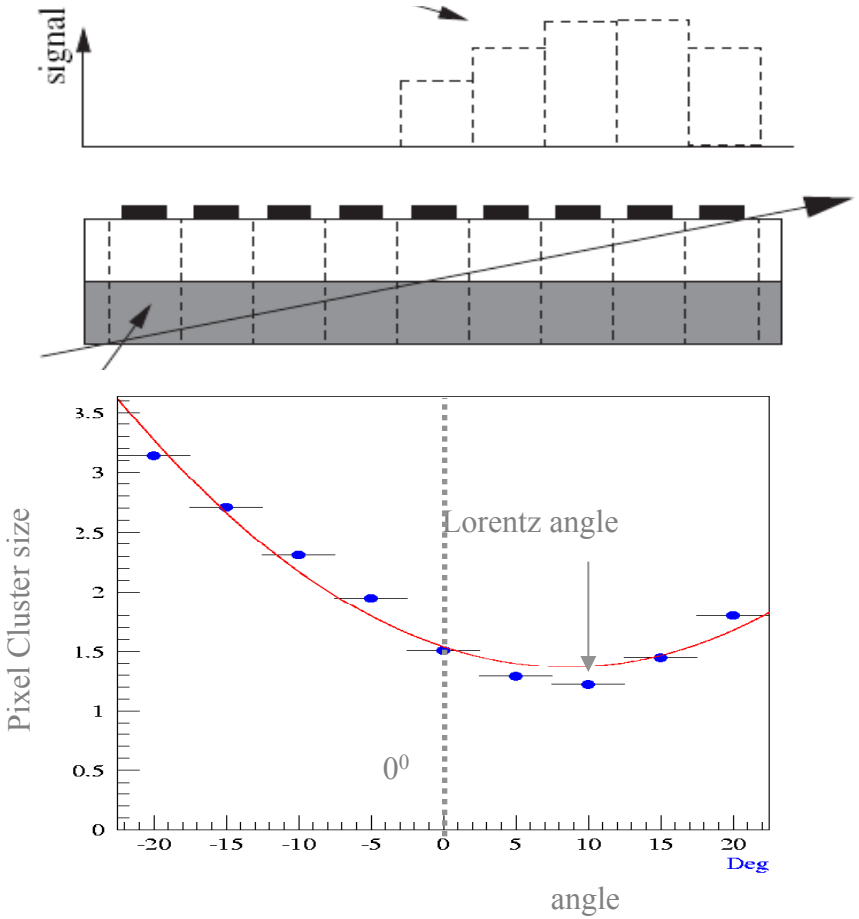
Lorentz angle (= average deviation between collisions)





$$\tan\alpha_L = \mu_{Hall} B_\perp$$

Measurement method: number of pixel hits is minimal when the particle incidence angle is equal to the Lorentz angle

I. Gorelov et al. NIM A481:204-221,2002

Hybrid Pixel Detectors

Today's "state of the art" of running detectors

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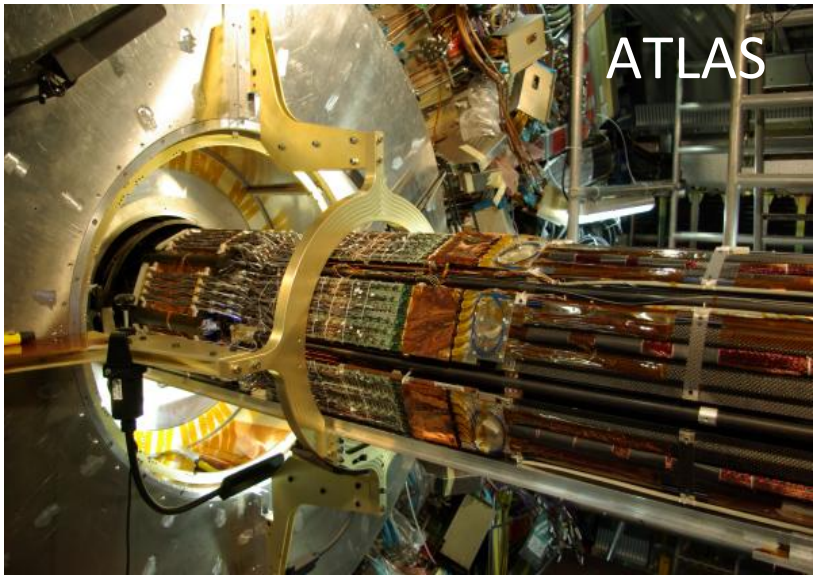
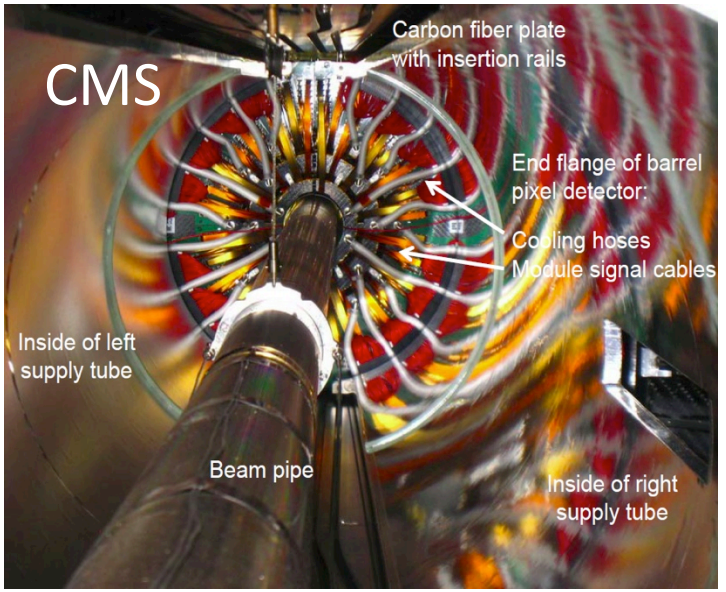
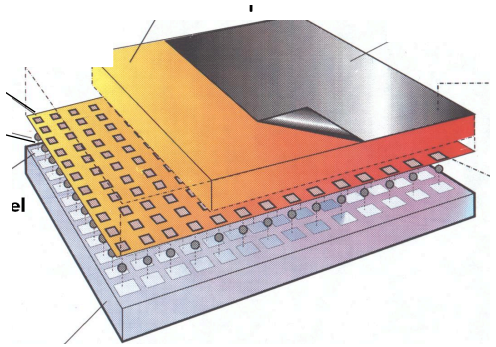
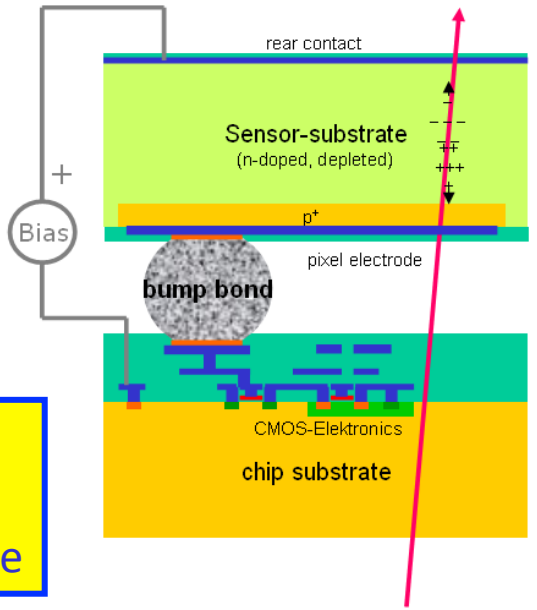


all based on
"Hybrid Pixels"







- amplification by a dedicated R/O chip
- 1-1 cell correspondence

Important: Readout Chips (ASICs)

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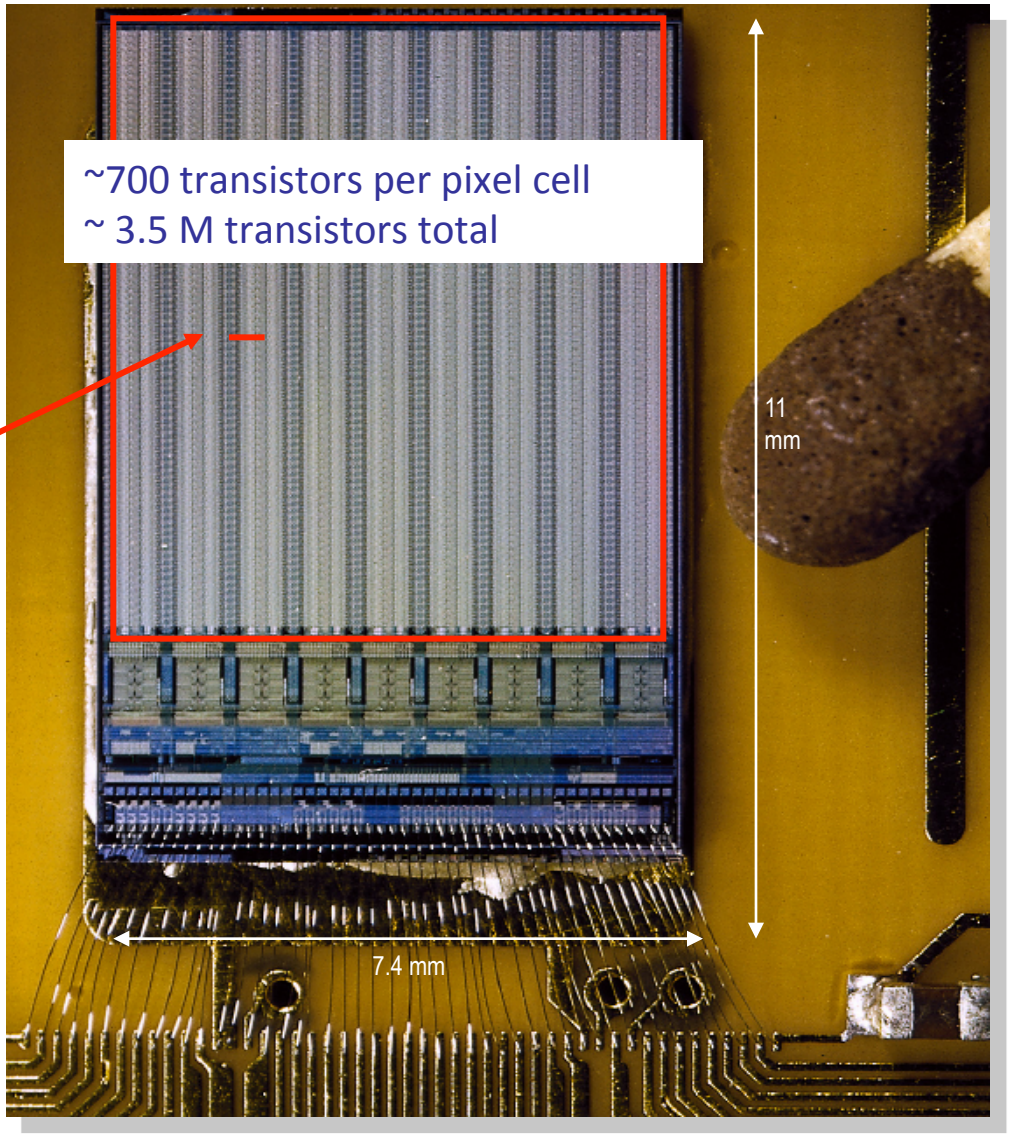
- becomes integral part of the detector
  - micro electronics
  - up to 700 million transistors so far
  - development takes typ. 10 man years

- ATLAS FE-I3
  - 0,25 µm CMOS technology
  - pixel cell size: 50 x 400 µm^2
  - 18 columns x 160 rows = 2880 cells
  - parallel processing in all cells
    - - amplification
    - - zero suppression



L. Blanquart, P. Fischer et al., NIM-A 456 (2001) 217-231

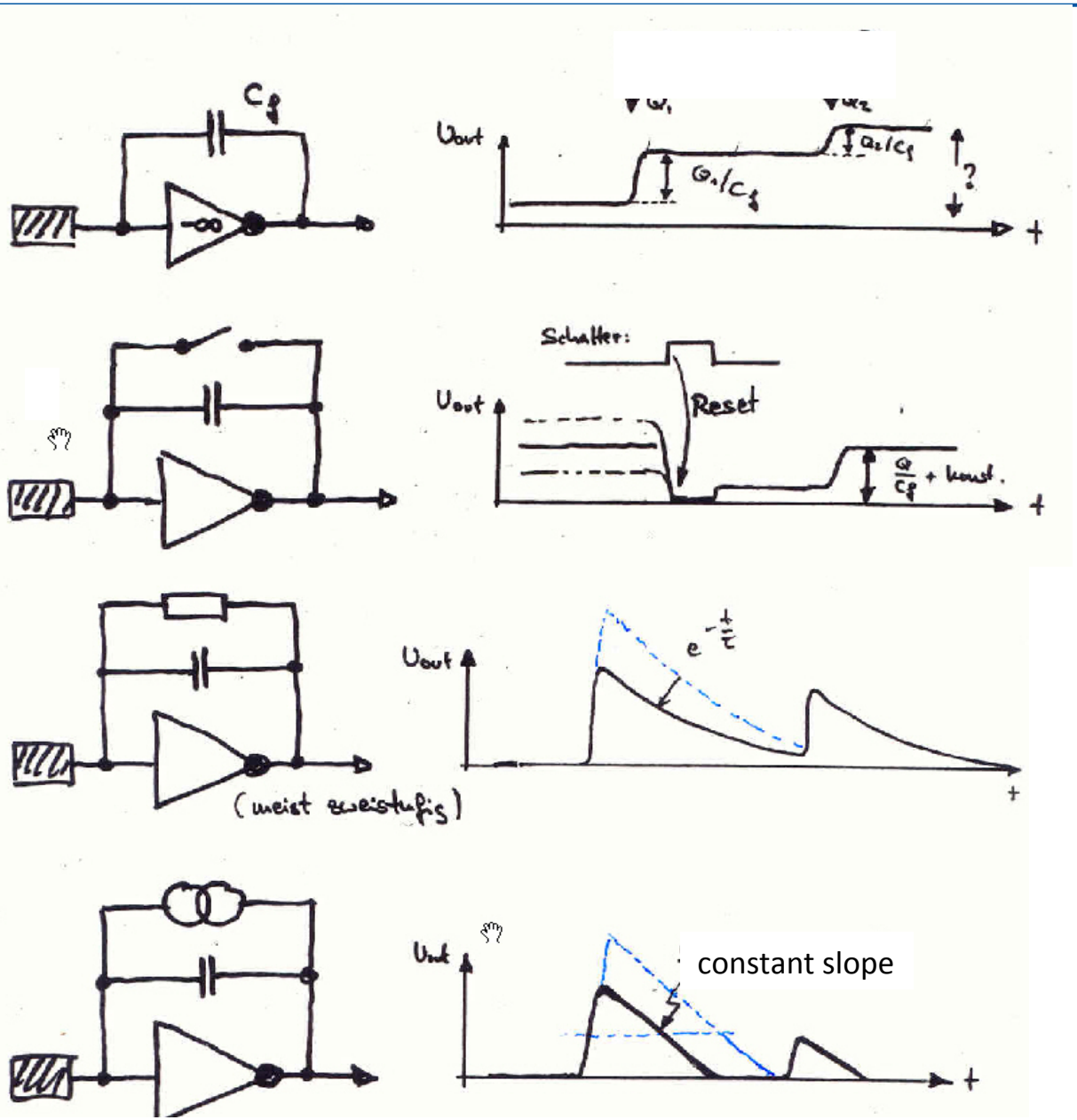
Charge Sensitive (Pre)-Amplifiers

A)

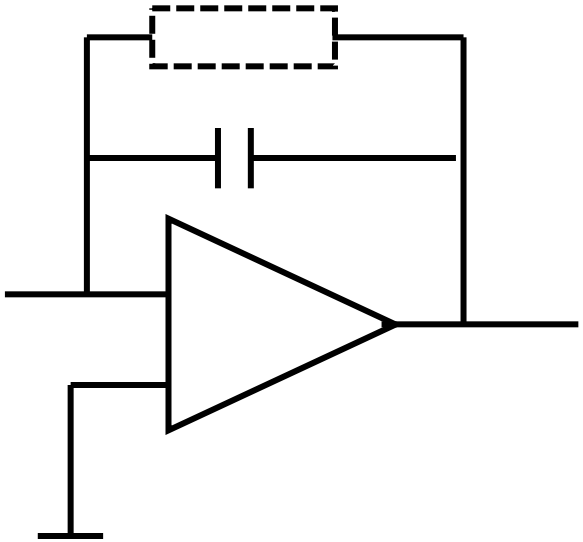
B)

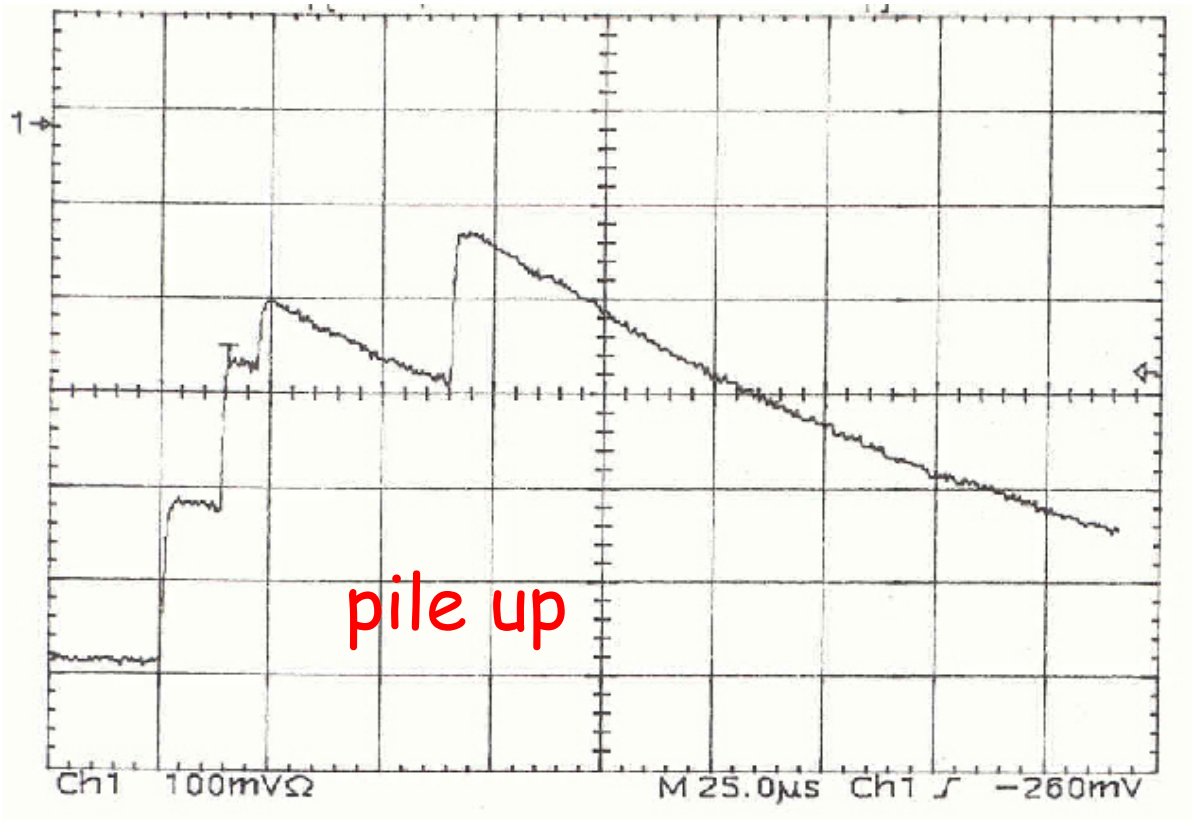
C)

D)

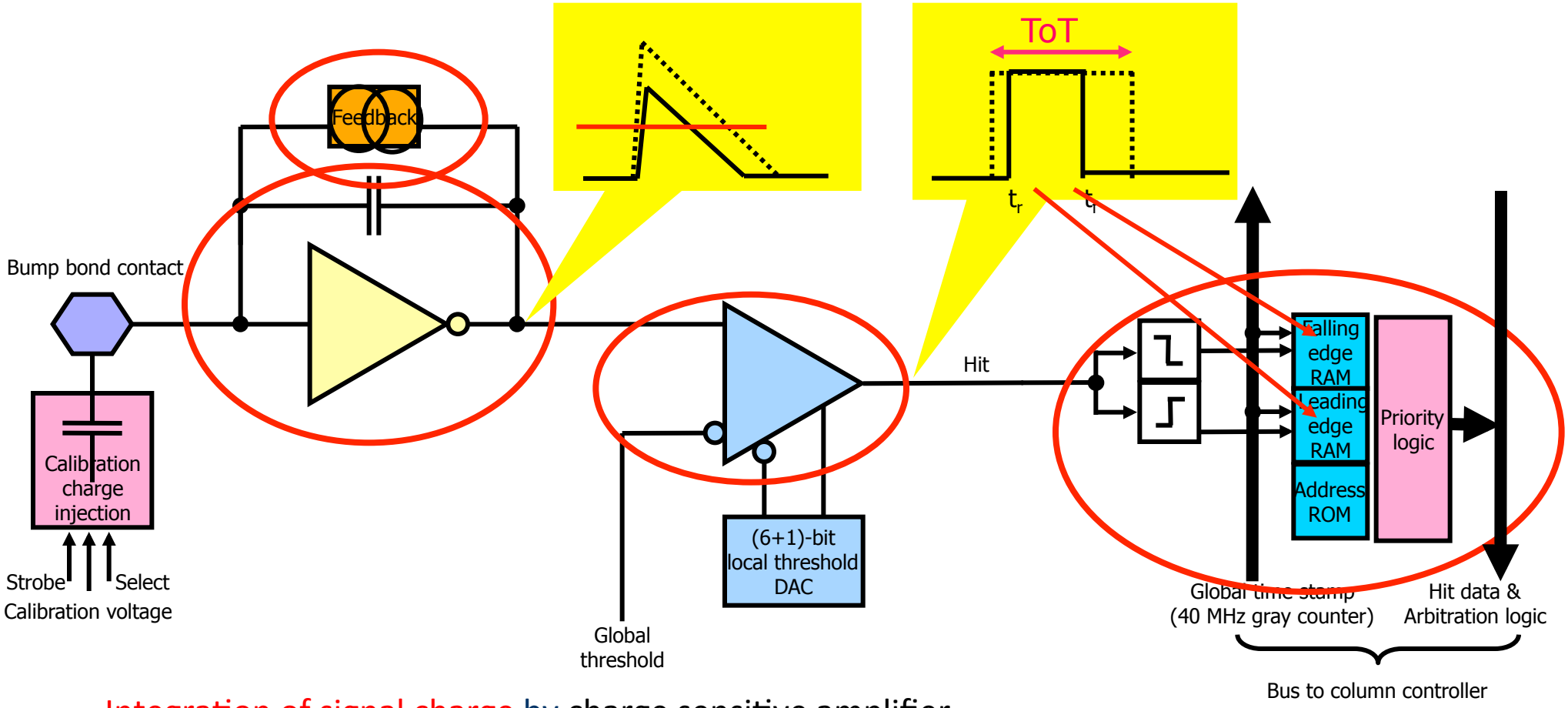


The amplifier: Charge Sensitive Amplifier (CSA)





Functions in the cell (binary readout + „poor man‘s“ analog)



- Integration of signal charge by charge sensitive amplifier
- Pulse shaping by feedback circuit with constant current feed back
- Hit detection by comparator
- ~5 bit analog information via „time over threshold“
- storage of address and time stamps in RAM at the periphery

L. Blanquart et al., NIM-A565:178-187, 2006

Pixel Frontend Chip

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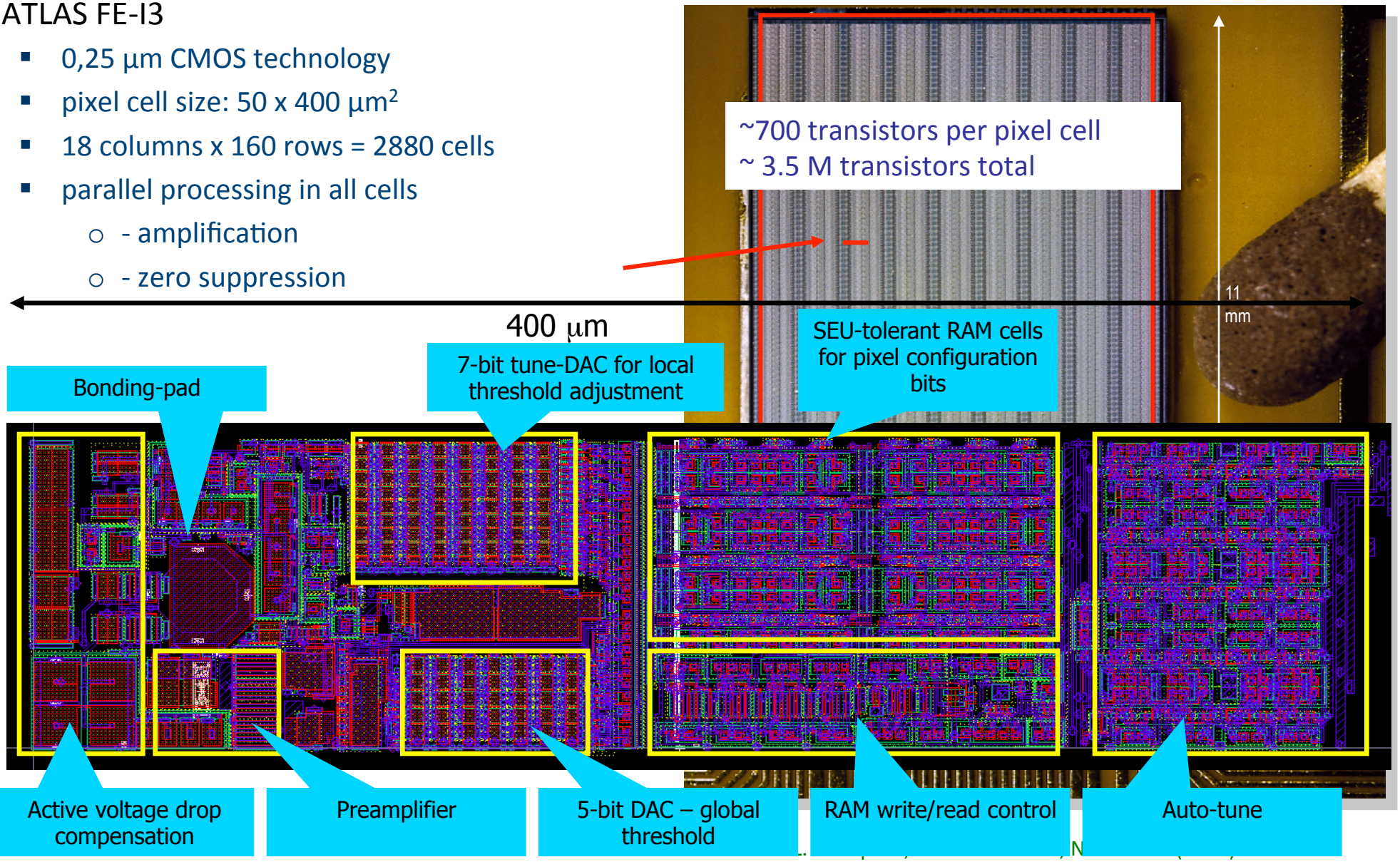
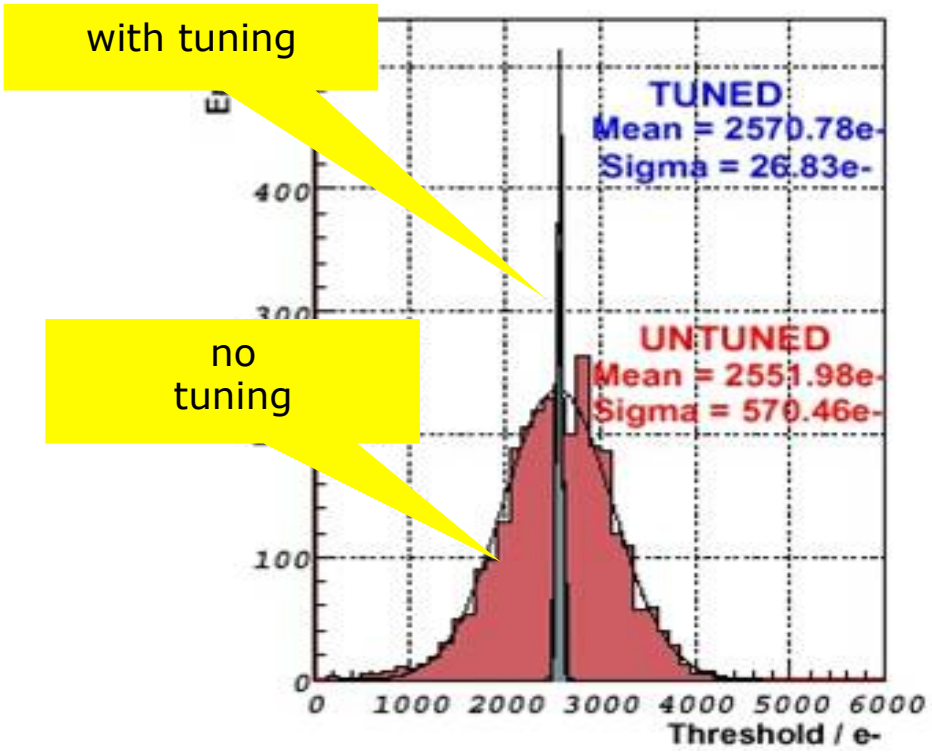
- ATLAS FE-I3
  - 0,25 µm CMOS technology
  - pixel cell size: 50 x 400 µm²
  - 18 columns x 160 rows = 2880 cells
  - parallel processing in all cells
    - - amplification
    - - zero suppression



Requirements on the electronics performance

- small noise hit rate → low noise and small threshold dispersion
- $\sigma_{noise} \oplus \sigma_{threshold}$ < ~ 600 e^- @ a threshold of 3000 e^-
- time stamp < 20 ns after BX for all signal heights



Distribution of pixel cell thresholds

Important / in-time threshold & efficiency

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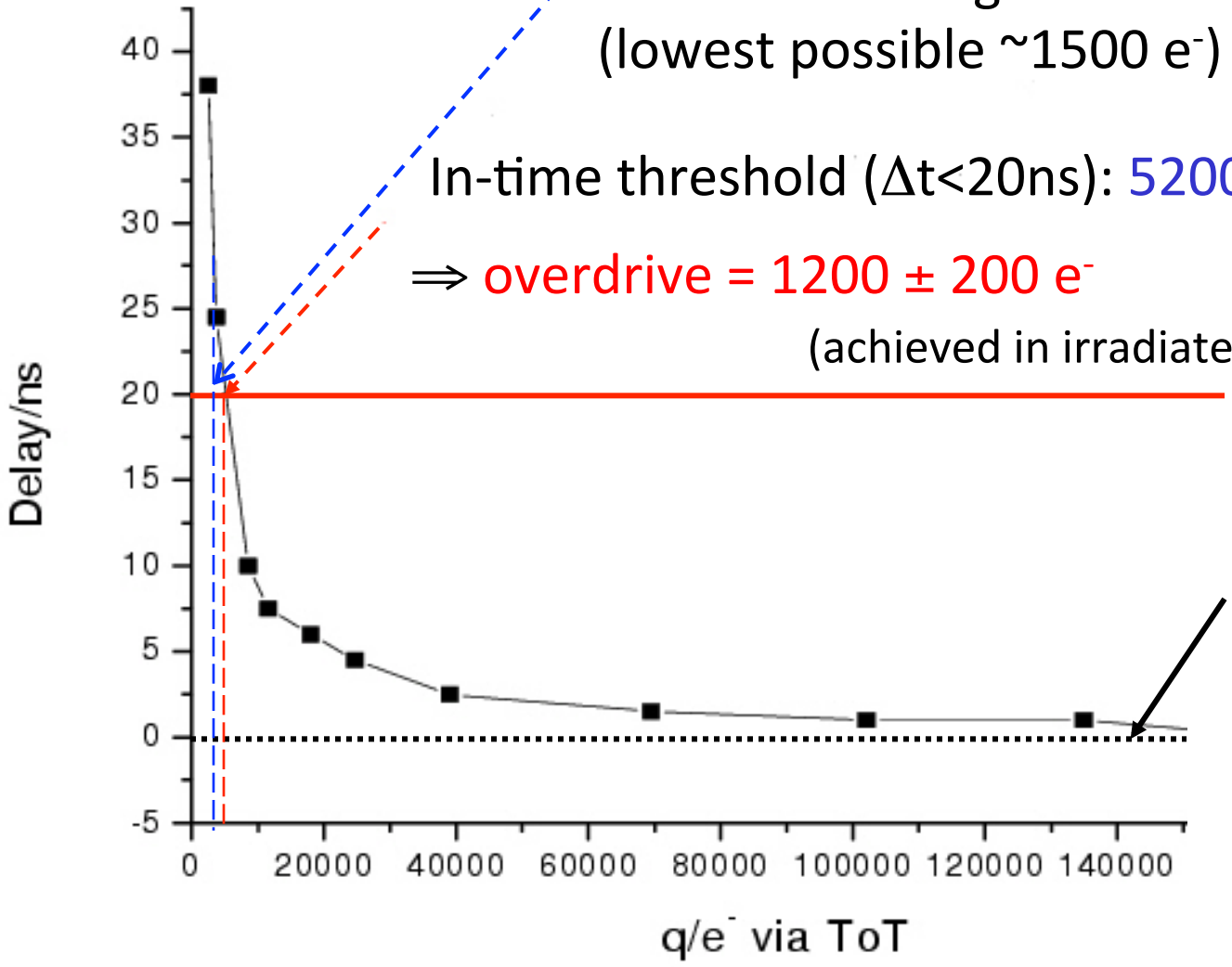
set threshold e.g. to 4000 ± 200 e^-
(lowest possible ~1500 e^-)

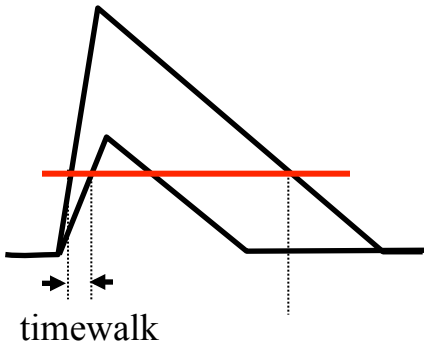
In-time threshold (Δt<20ns): 5200 ± 200 e^-

⇒ overdrive = 1200 ± 200 e^-

(achieved in irradiated assemblies)



zero time walk line
for large signals

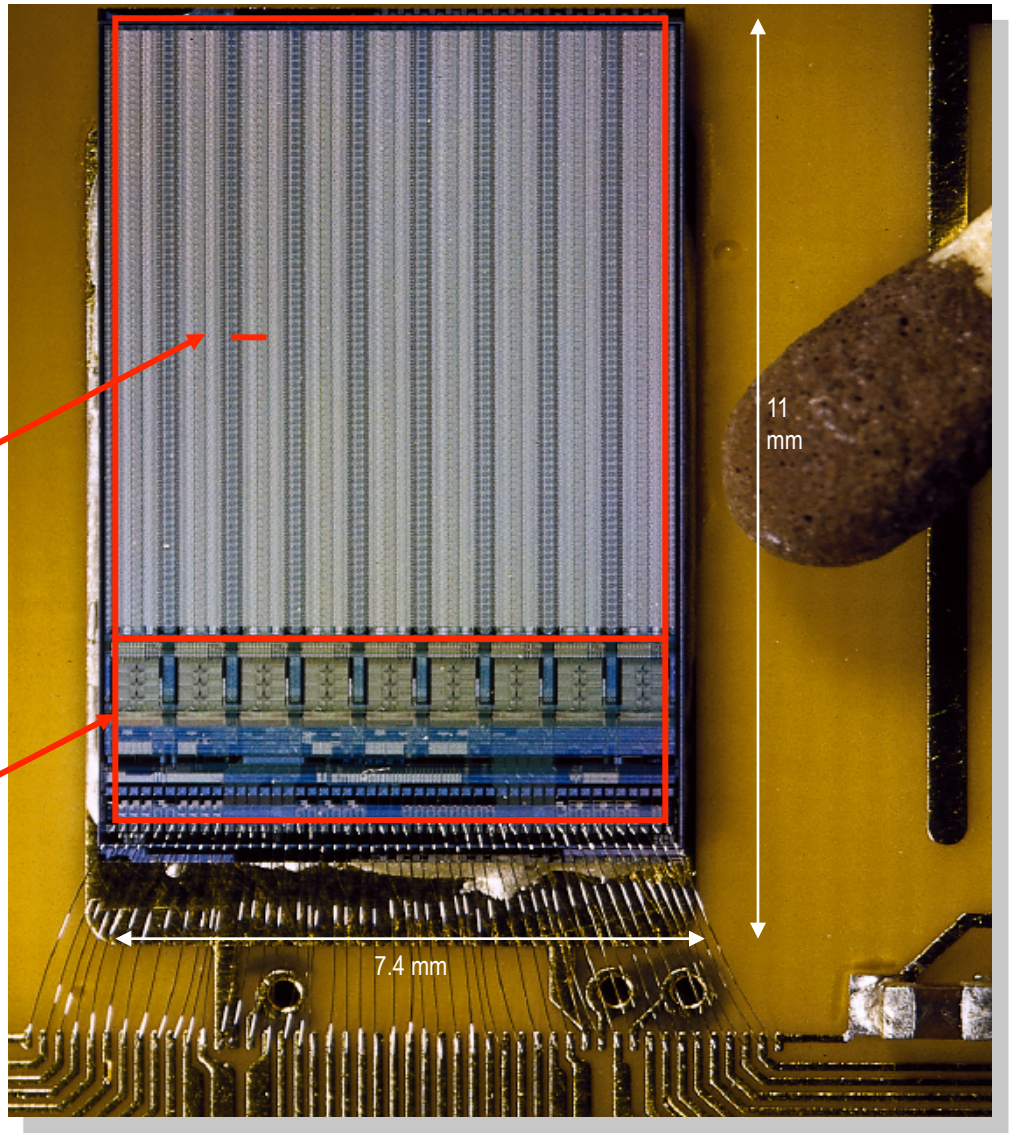


➔ in-time efficiency ~99% wanted and achieved !

ATLAS Pixel Frontend Chip

universitätbonn

- becomes integral part of the detector
  - micro electronics
  - up to 700 million transistors so far
  - development takes typ. 10 man years
- ATLAS FE-I3
  - 0,25 µm CMOS technology
  - pixel cell size: 50 x 400 µm^2
  - 18 columns x 160 rows = 2880 cells
  - parallel processing in all cells
    - - amplification
    - - zero suppression
- End of Column logic
    - storage of hit information during trigger latency (2.5 µs)
    - hit selection upon L1 trigger



L. Blanquart, P. Fischer et al., NIM-A 456 (2001) 217-231

ALTAS FE-chip readout architecture (animated)

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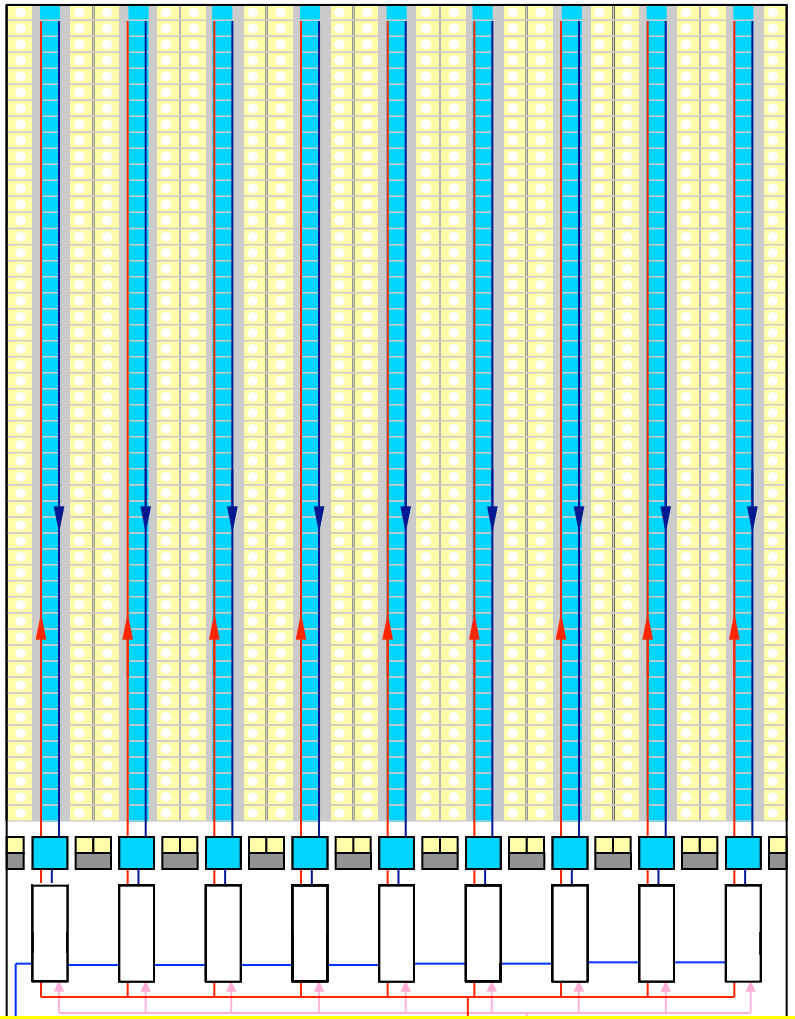
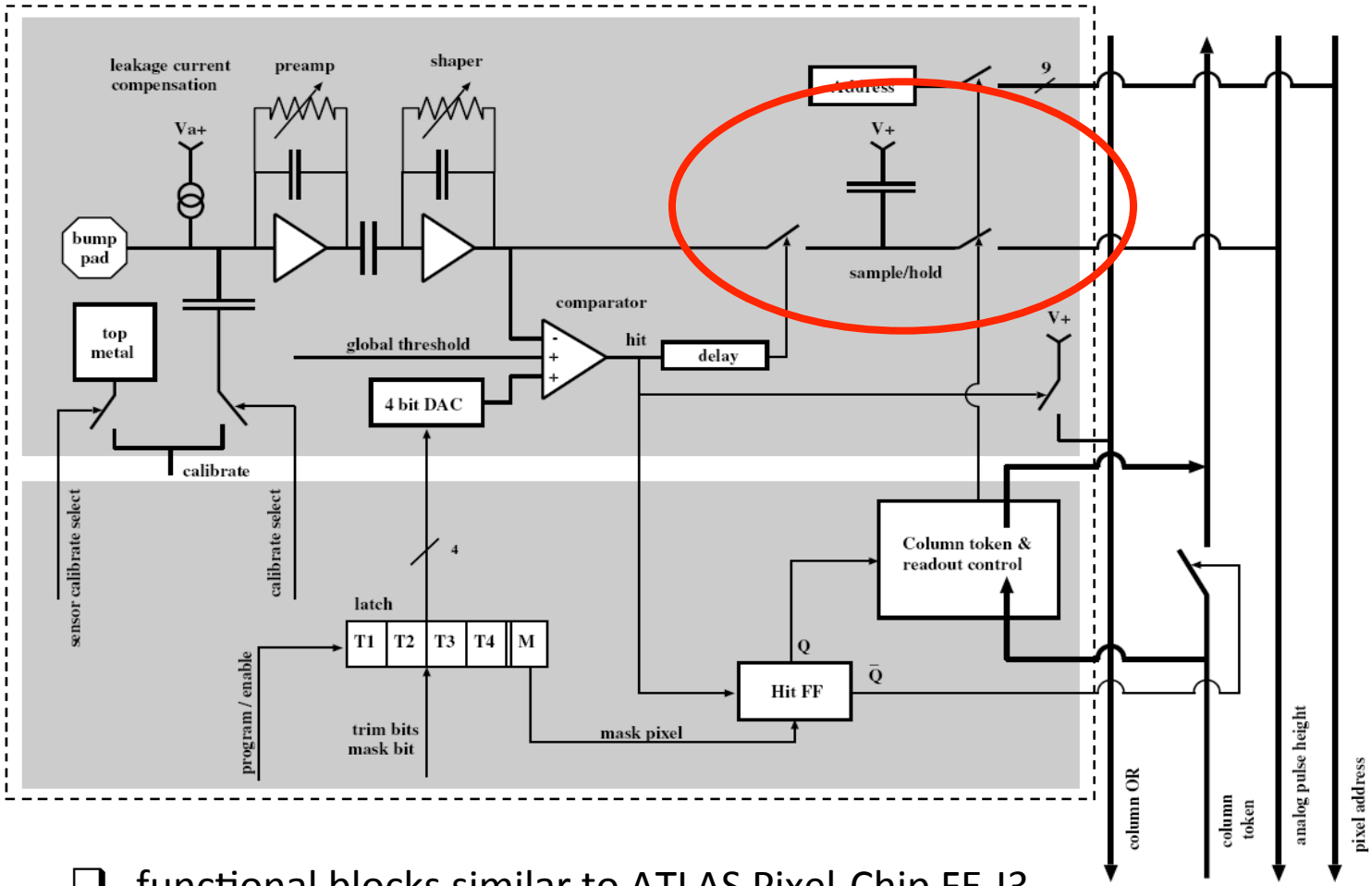
- 40 MHz Gray coded clock transmitted to all cells
- Pixel cells generate hit information (address and time stamp) which are stored at the end of column
- hits are removed if no trigger conicidence occurs
- Hit information agreeing with L1 trigger time are read out



- Analogue circuits
- Digital readout circuits
- Registers used to store configuration bits
- Time information
- Trigger

ATLAS Pixel Chip: binary hit information with additional information on signal hight via ToT measurement (~4-5 bit)

CMS pixel-chip (analog readout)



CMS Pixel-Chip PSI46V2

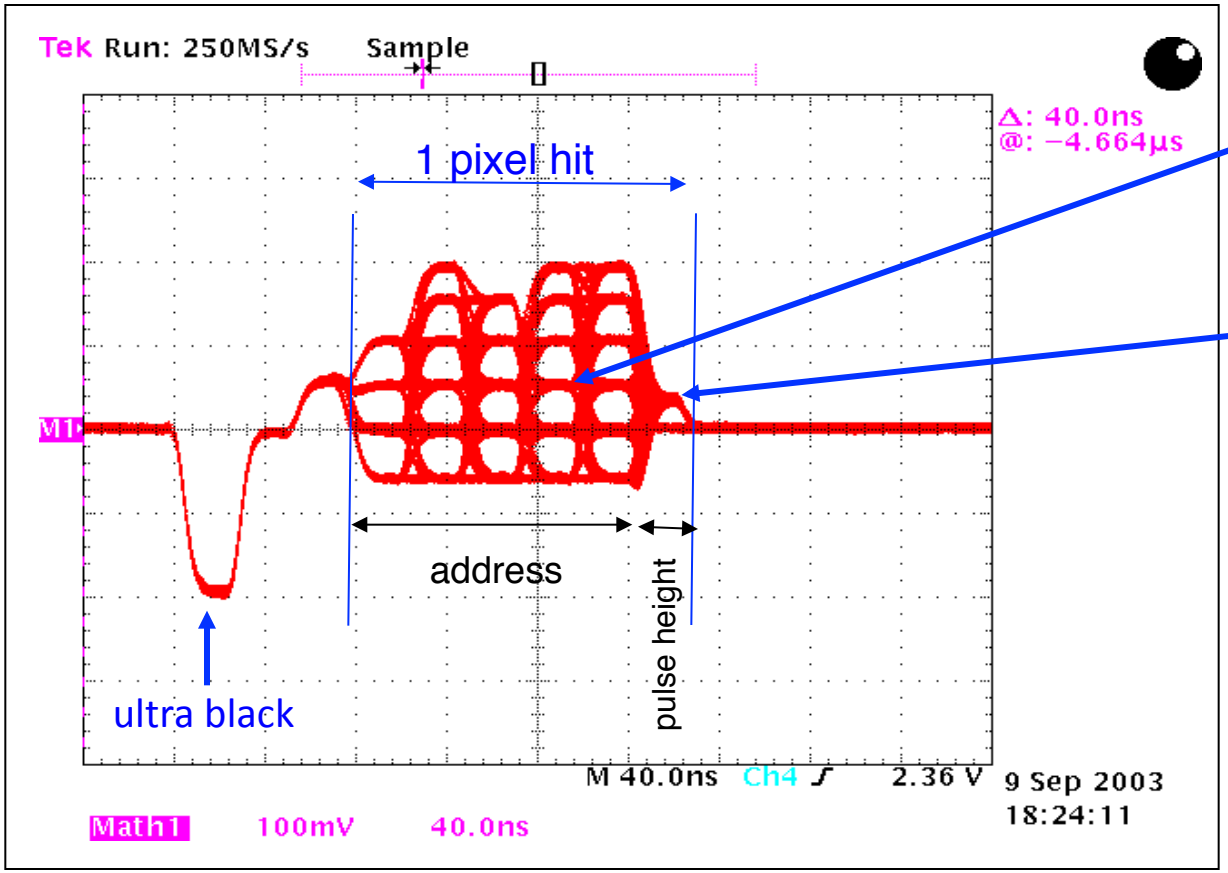
- functional blocks similar to ATLAS Pixel-Chip FE-I3
- additional storage of analog pulse height (sample/hold)
- analog output signal → amplitude + row/column address coded in analog levels

H.C. Kastli et al., e-print physics/0511166

CMS pixel-chip (analog readout)

universitätbonn

- Overlay of 4160 pixel readouts (analog coded address levels)



5 clock cycles encode 13 bits of pixel address information.

analog pixel pulse height

pixel address decoded into binary numbers for DAQ

H.C. Kastli et al., e-print physics/0511166

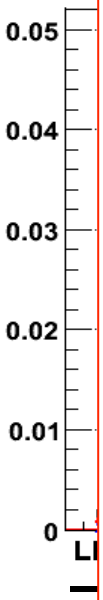
HL-LHC data rates

Hit inefficiency rises steeply with the hit rate

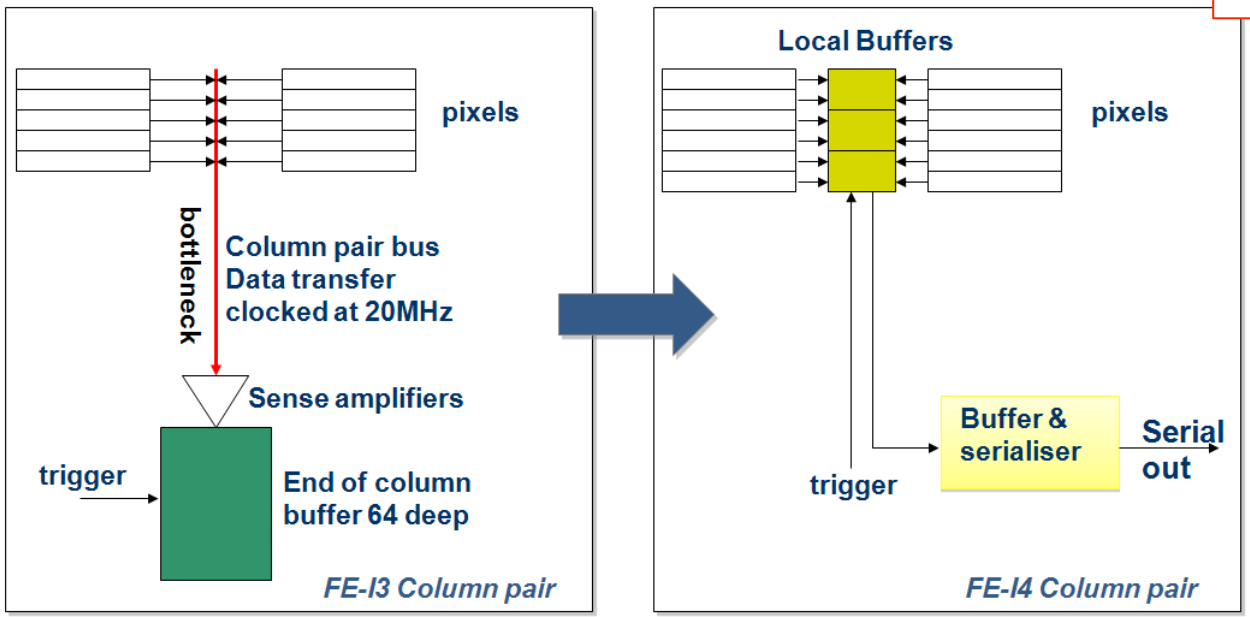
1-ε

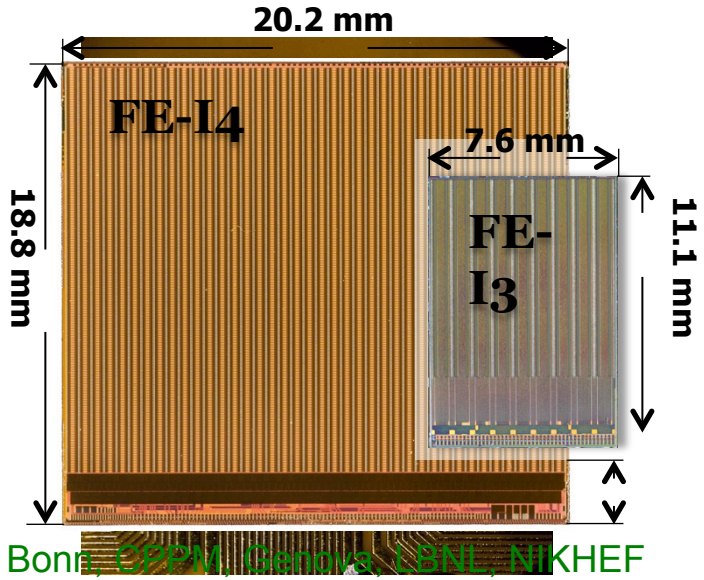
Bottleneck: congestion in (double) column readout

⇒more local in-pixel storage (250nm -> 130nm)
>99% of hits are not triggered
⇒ don't move them → no blocking



- IBM (130 nm)
- 87 Million transistors
- 26880 pixels (50 x 250 μm²)
- lower noise than FE-I3
- operation at lower thresholds
- higher rate compatibility
- radiation hard to >250 Mrad
- 3+ years of design work w/ 8 designers
- working horse for current and future pixel R&D





Bonn, CPPM, Genova, LBNL, NIKHEF

M. Garcia-Sciveres et al, Nucl.Instrum.Meth. A636 (2011) 155-159

Hybrid Pixel assembly => called „hybridization“

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Sensors

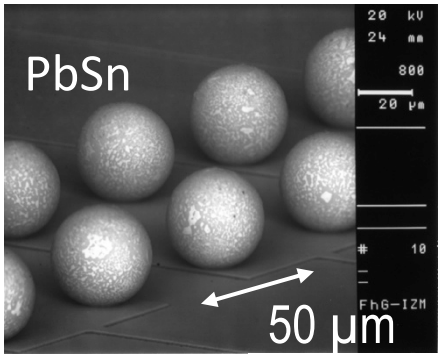
- n^+ in n (oxygenated Si)
- wafer size (Ø 10 cm)
- ~200-250 µm thick

Electronics - Chip

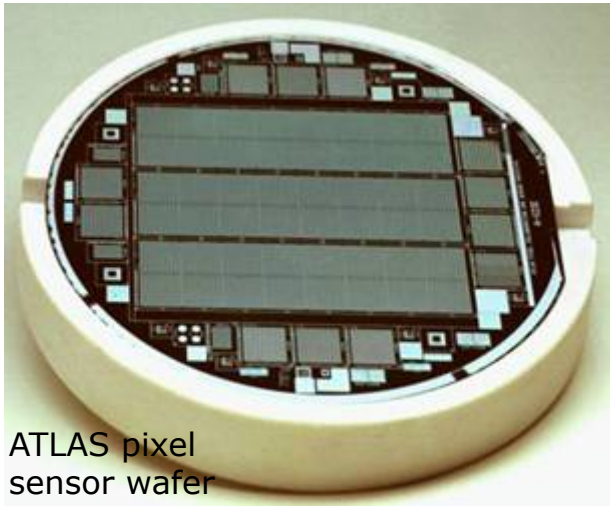
- chip size limited by yield ~1-2.5 cm^2
- wafer size (Ø 20 cm)

Hybridization

- PbSn or Indium bumps (wafer scale)
- IC wafers thinned after bumping to ~180 µm
- ‚flip-chip‘ to mate the parts
- ~3000 bumps/chip, ~50000 bumps/module



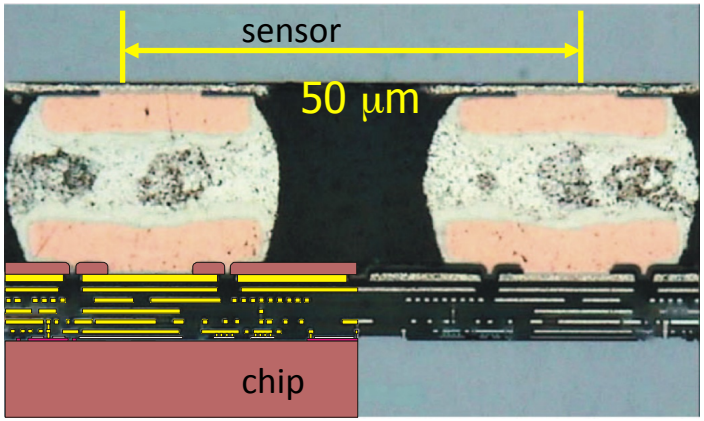
IZM,Berlin



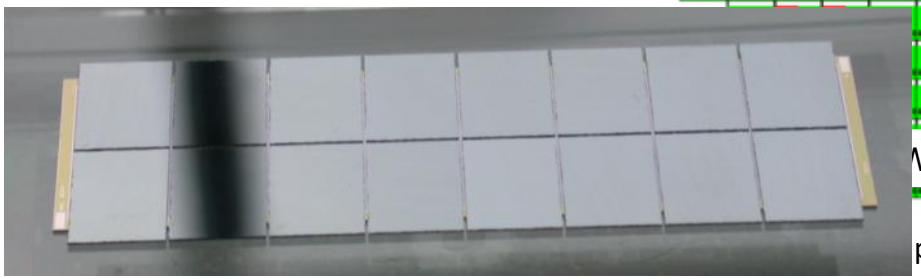
ATLAS pixel sensor wafer

Wafer

p, 82% yield

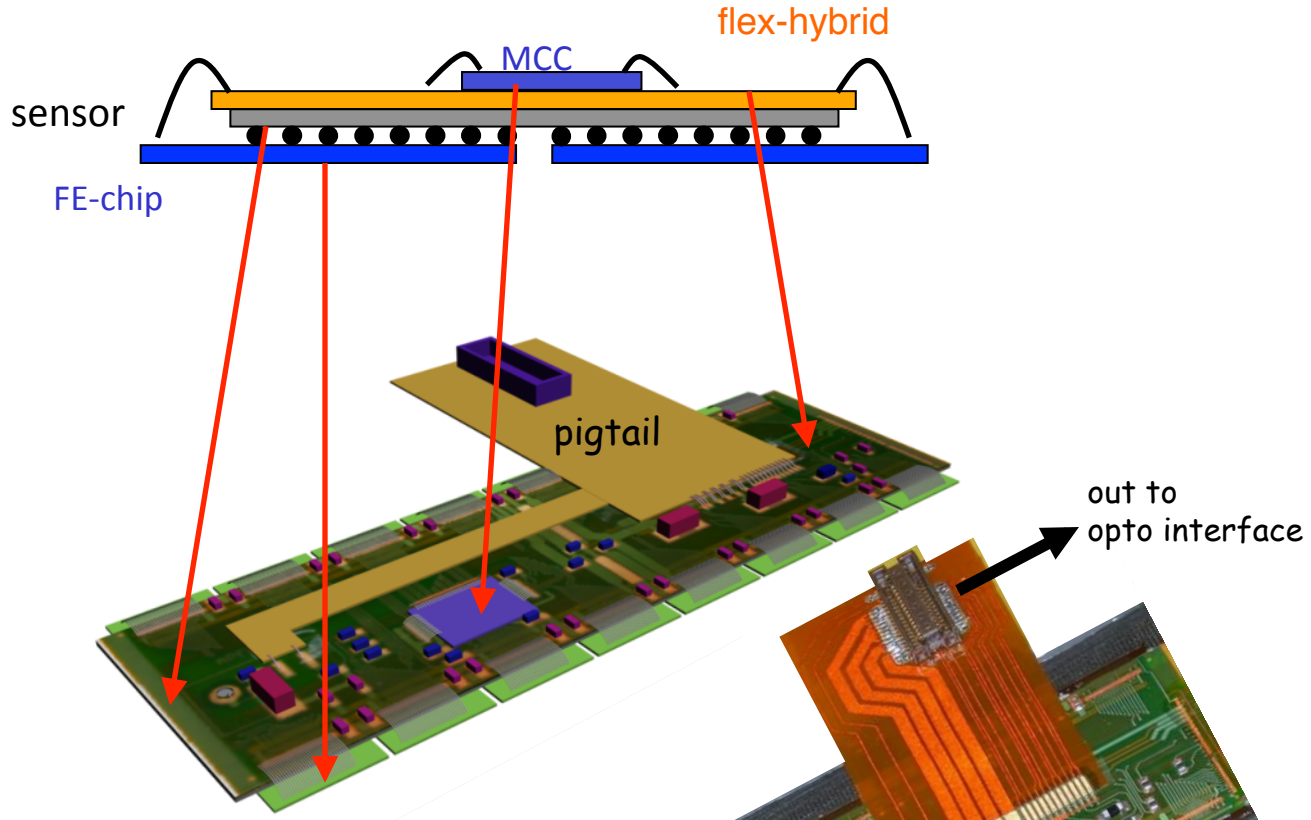


ATLAS Modul, Foto:IZM, Berlin

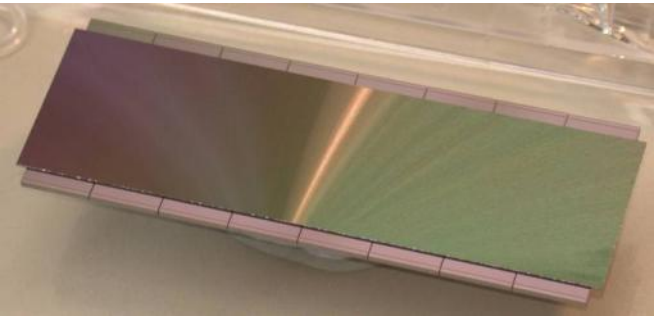


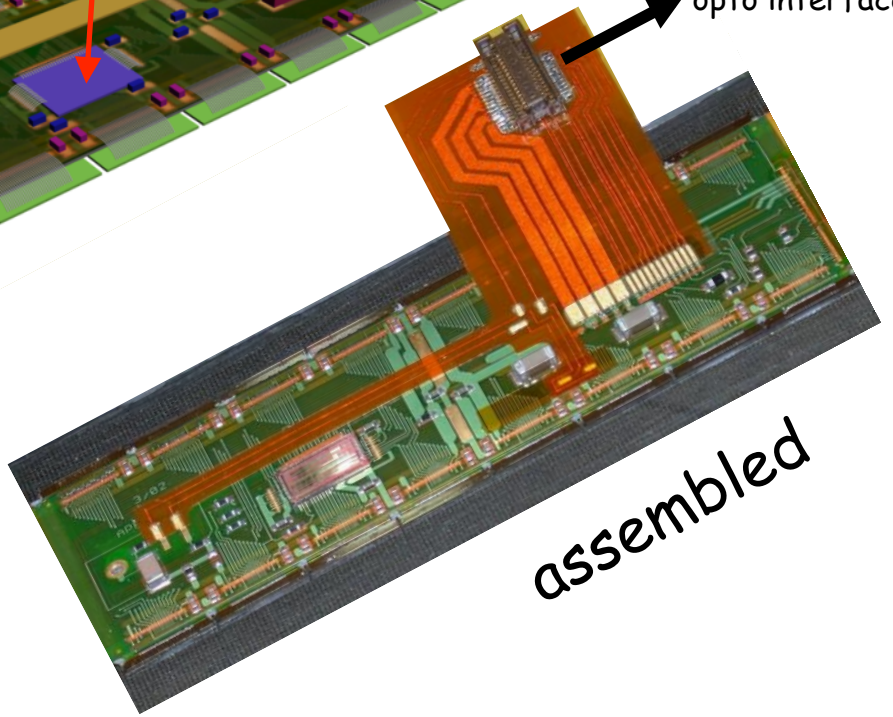
ATLAS pixel BARE module

Hybrid Pixel Assembly



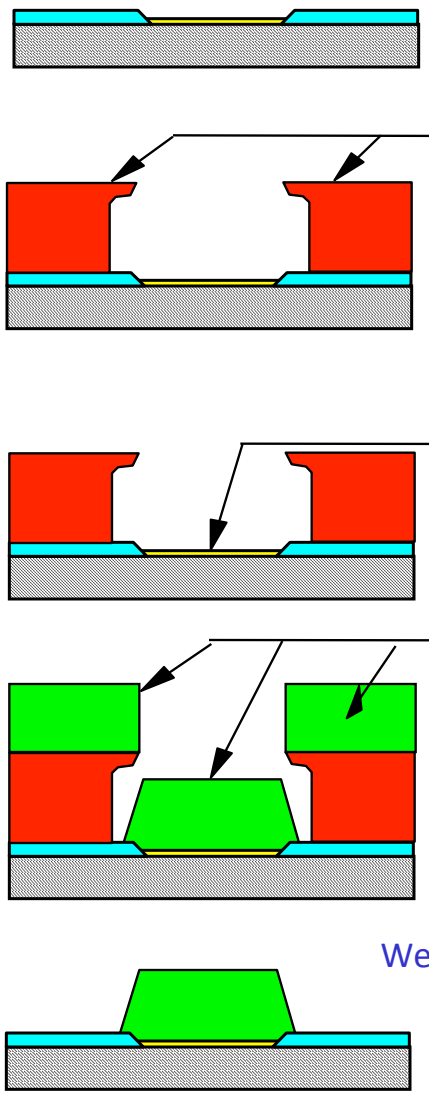
bare





assembled

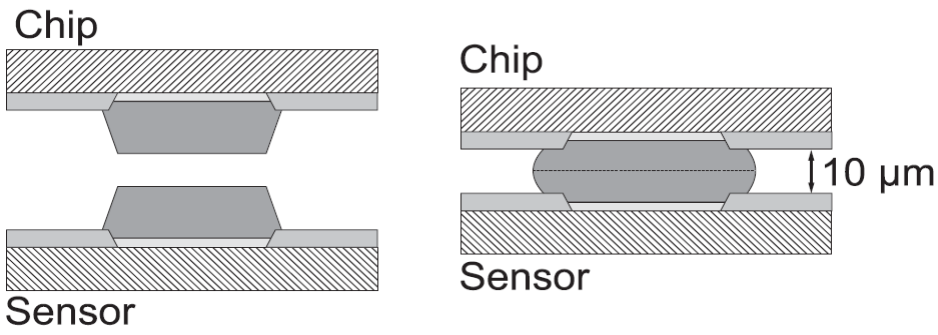
Indium bumping process



Process parameters:

- Resist Thickness: 15 μm
- Pre-bake: 30min @ 80 °C
- Deposition rate: 0.5 μm/min
- Dep. Pressure: 9 x 10^{-7} Torr
- Temp. during Dep. < 50 °C

Flip-Chip



Solder bumping & flip chip process

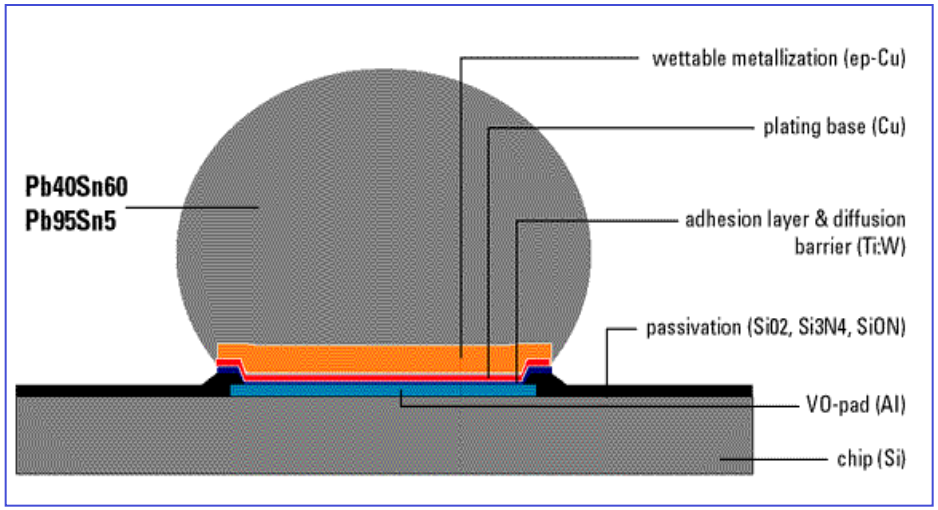
a) Sputter etching and sputtering of the plating base / UBM

b) Spin coating and printing of Photoresist

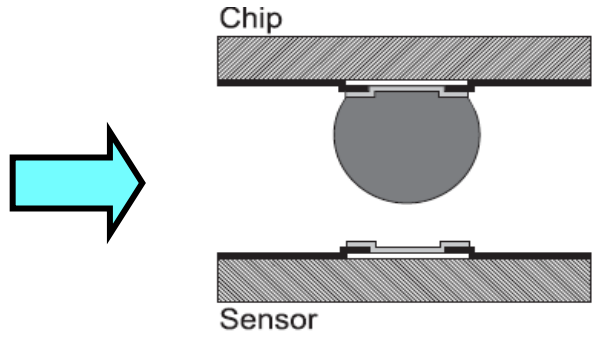
c) Electroplating of Cu and PbSn

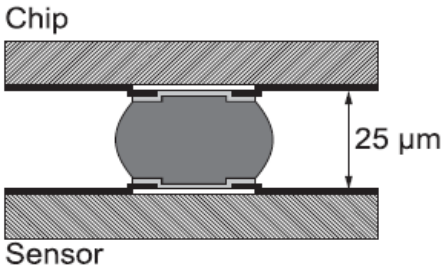
d) Resist stripping and wet etching of the plating base

e) Reflow

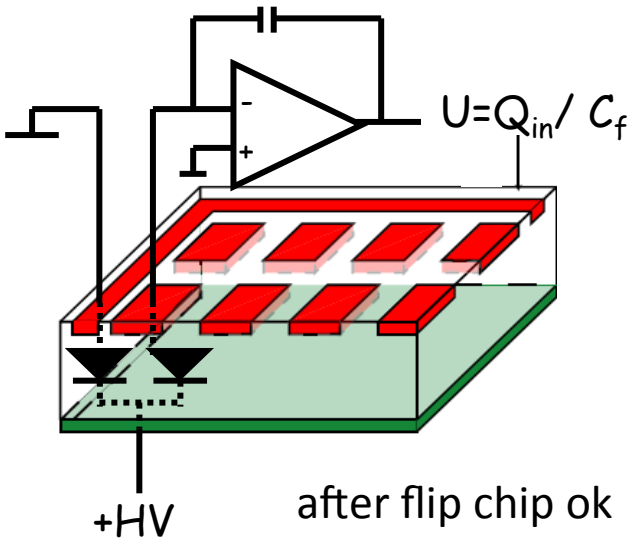


Flip-Chip

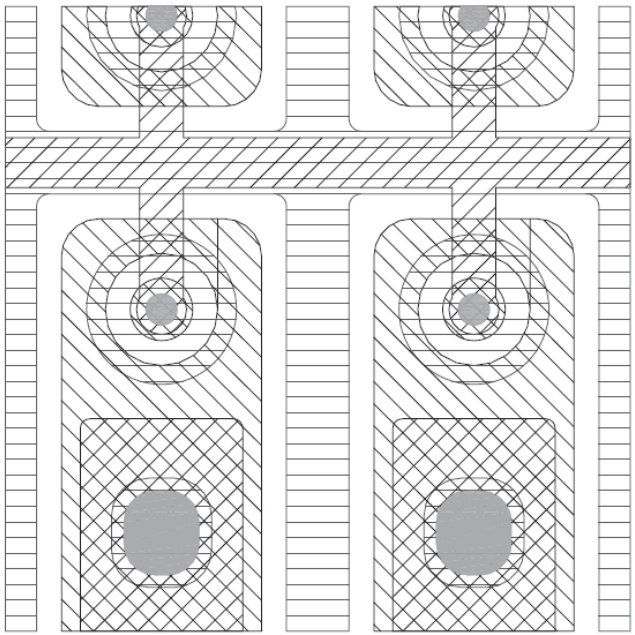


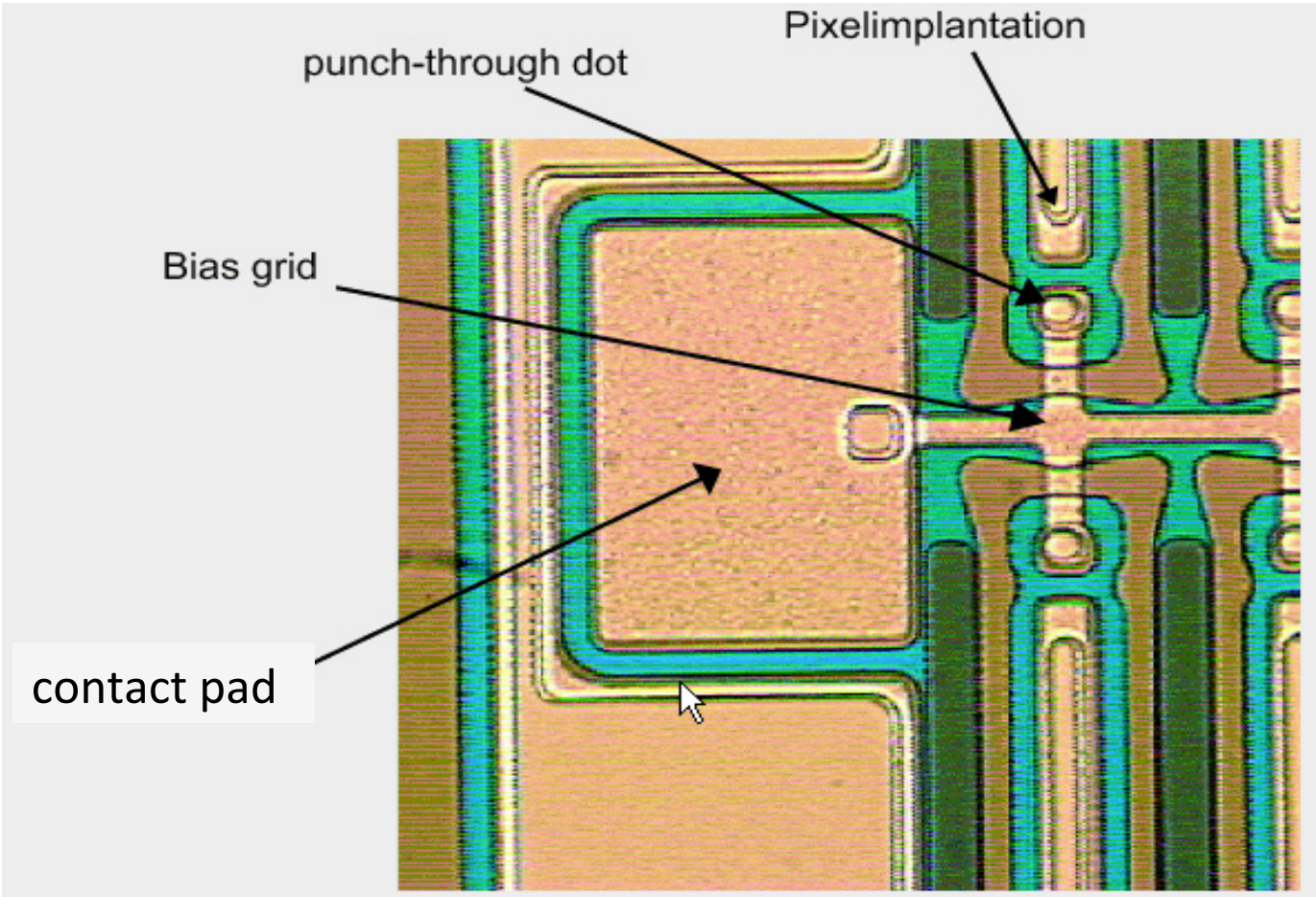


How to bias a pixel detector?



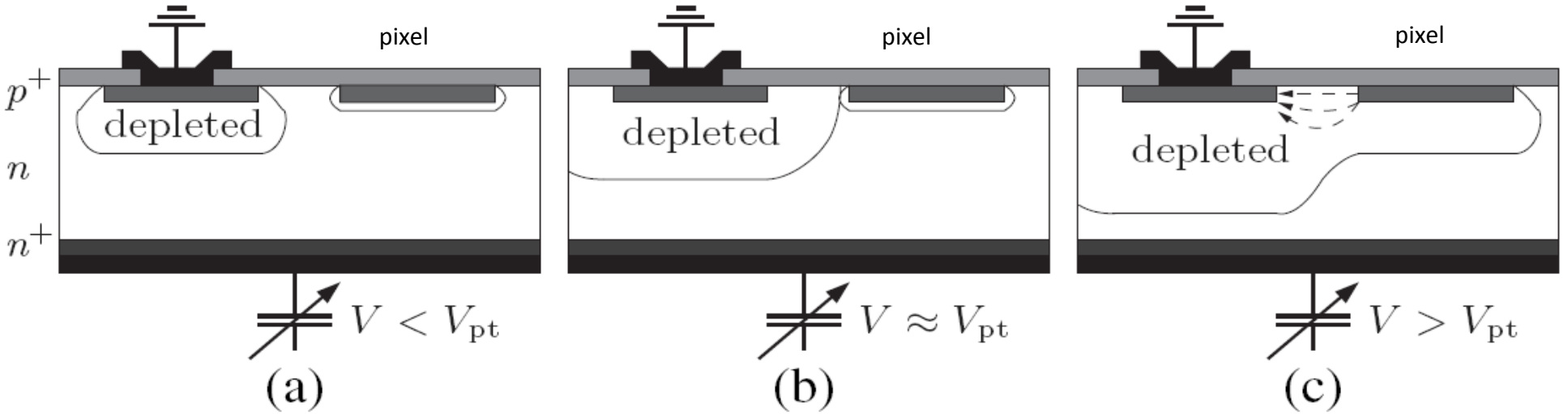
after flip chip ok





but want to test the sensor before you put 16 chips on

punch through biasing

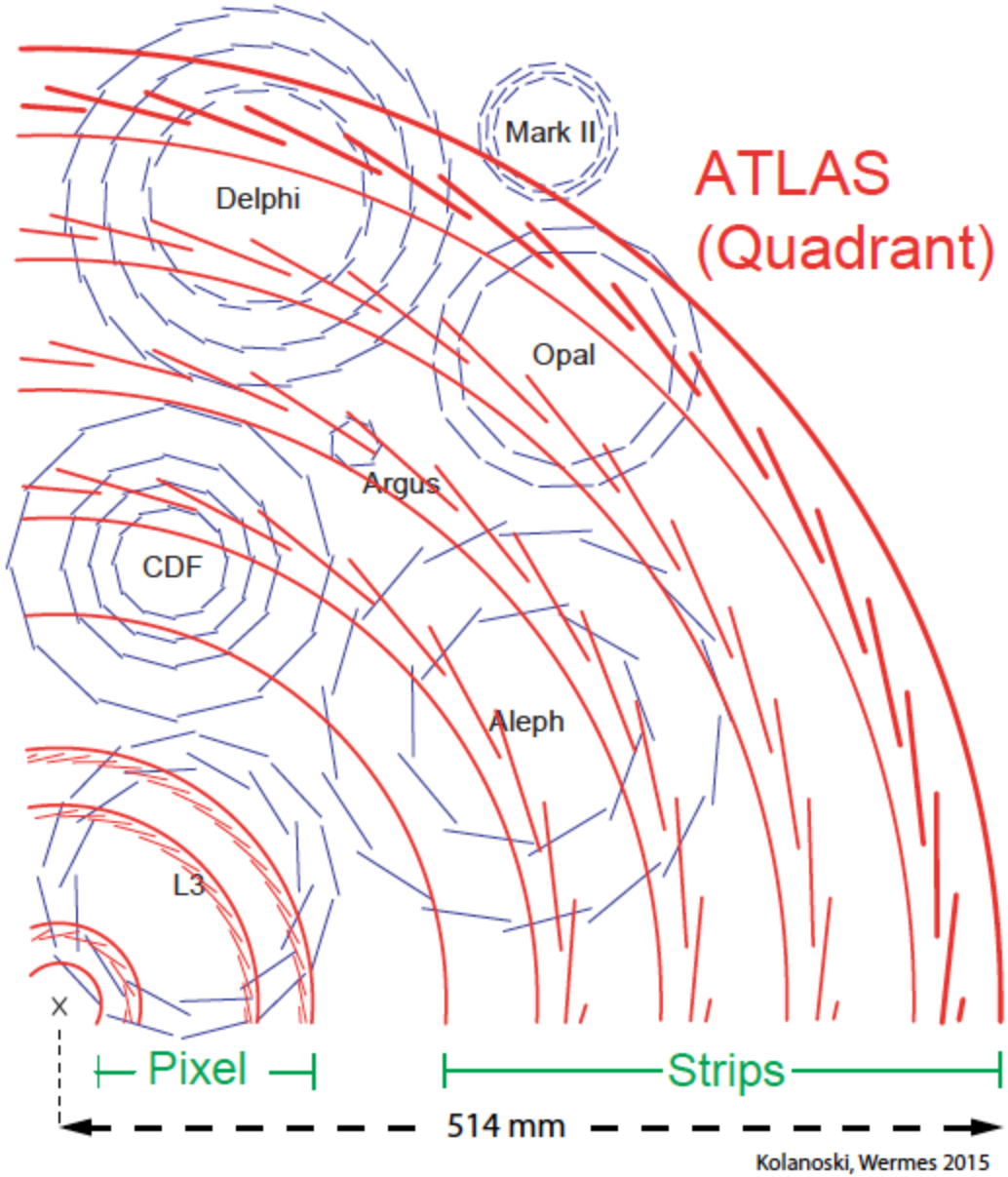


below
$V_{punch\ through}$

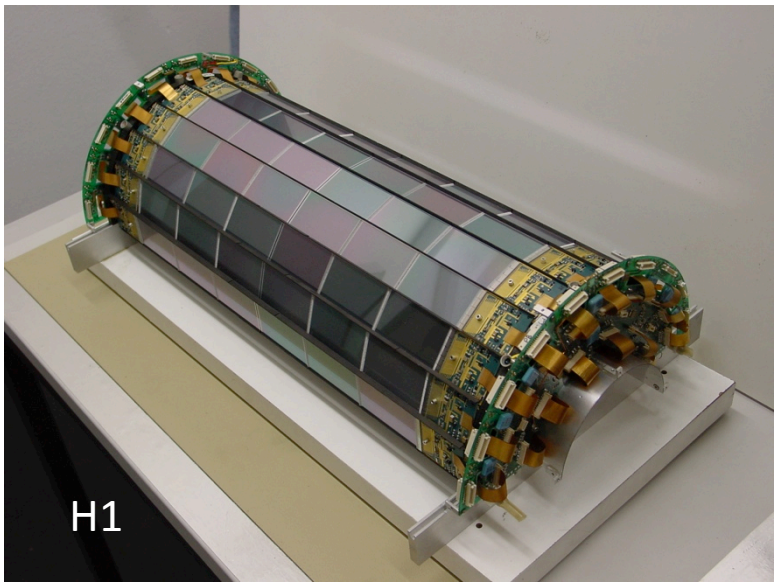
equal
$V_{punch\ through}$

above
$V_{punch\ through}$

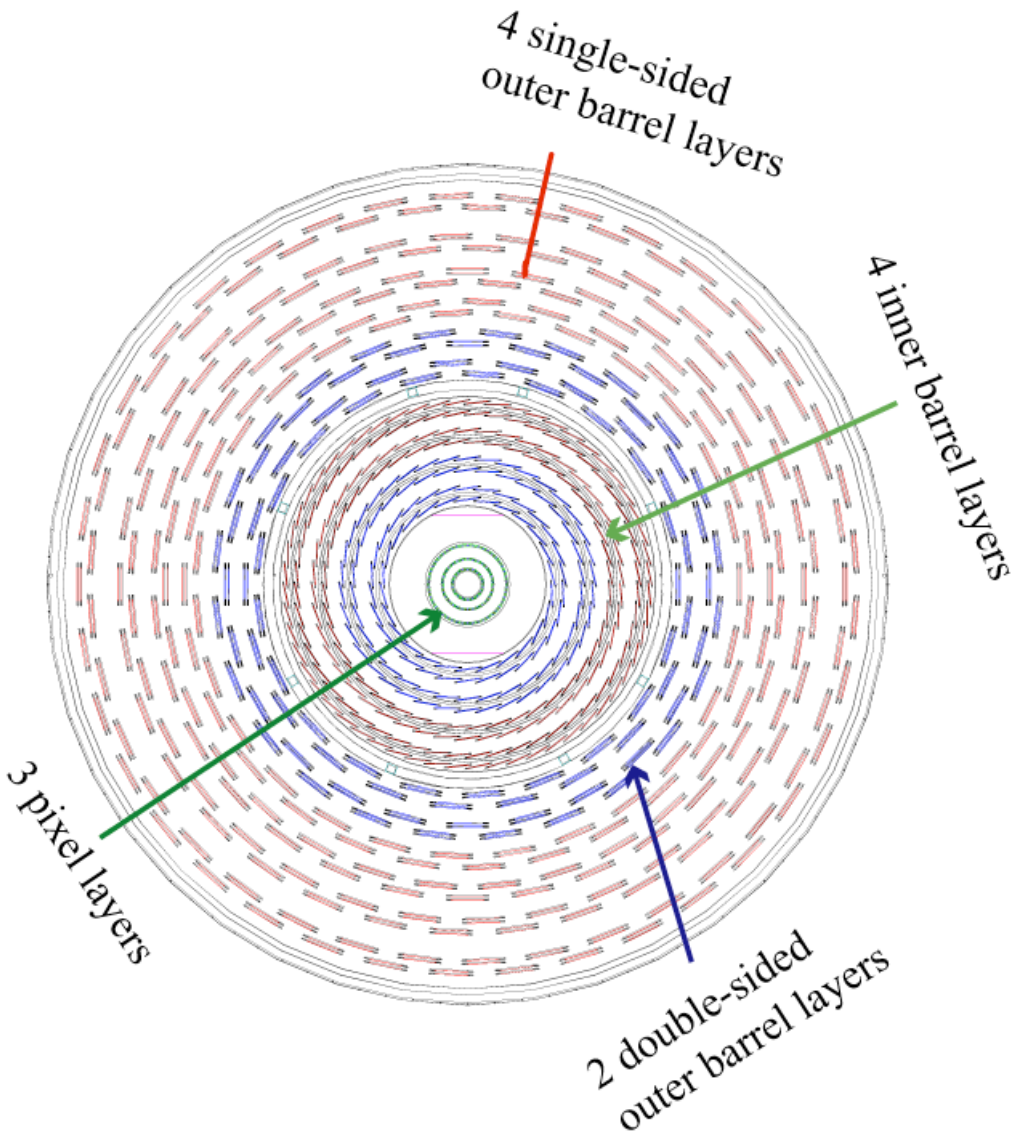
Semiconductor Tracking Detectors

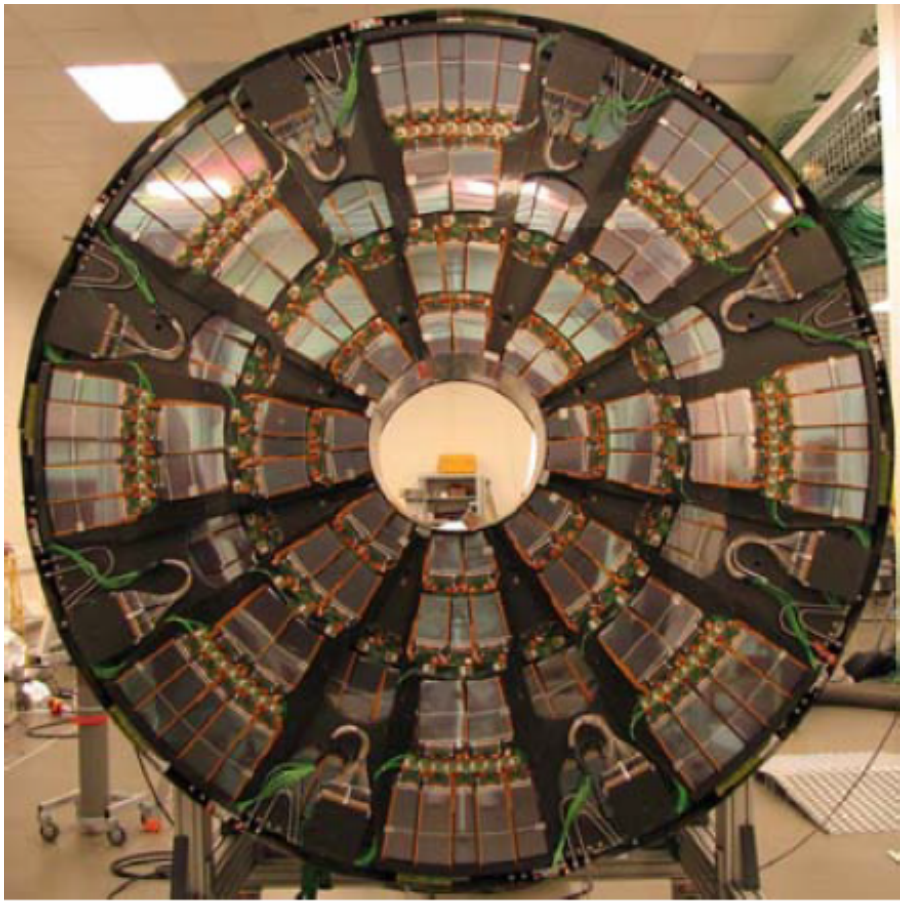


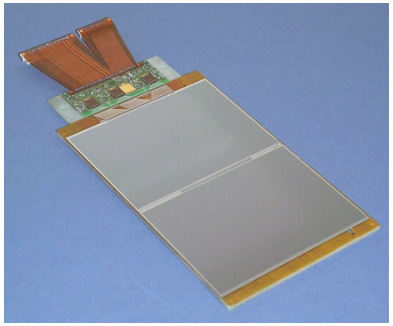
basically all
collider and vertex detectors
now possess high precision
semiconductor detectors
close to the interaction region;
often entire “trackers”



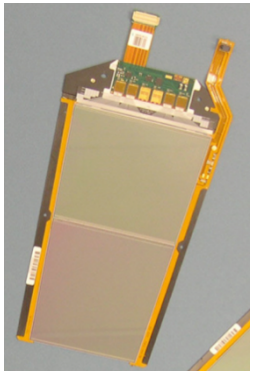
Tracking Detectors: CMS (pp collisions)







modules

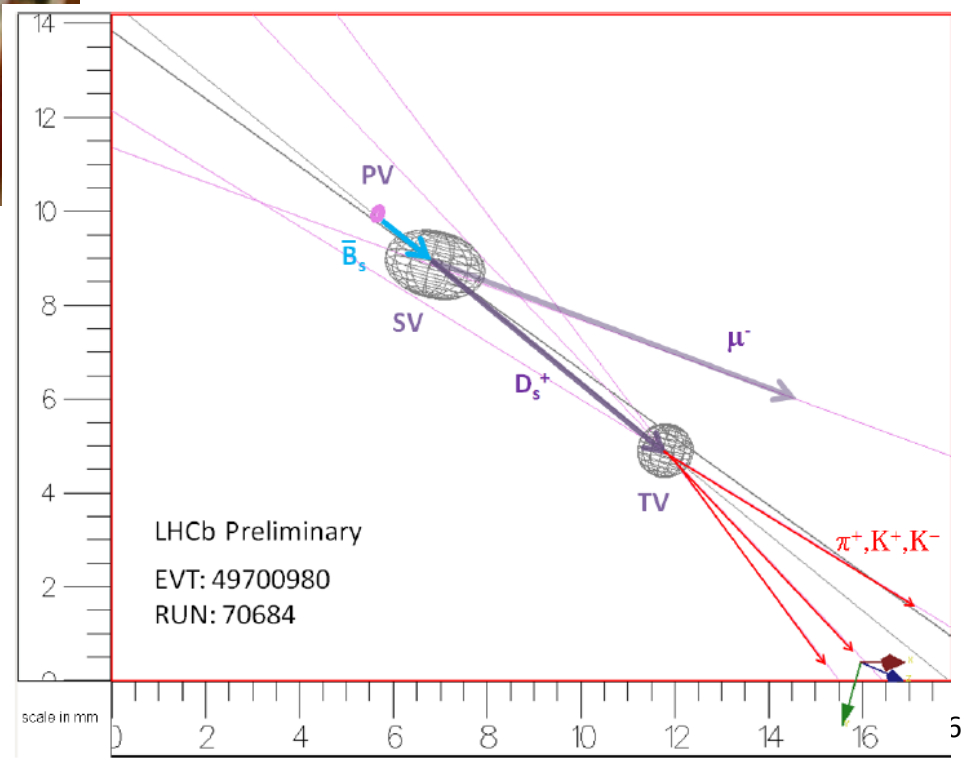


Largest Si – Detector ever (~200 m^2)

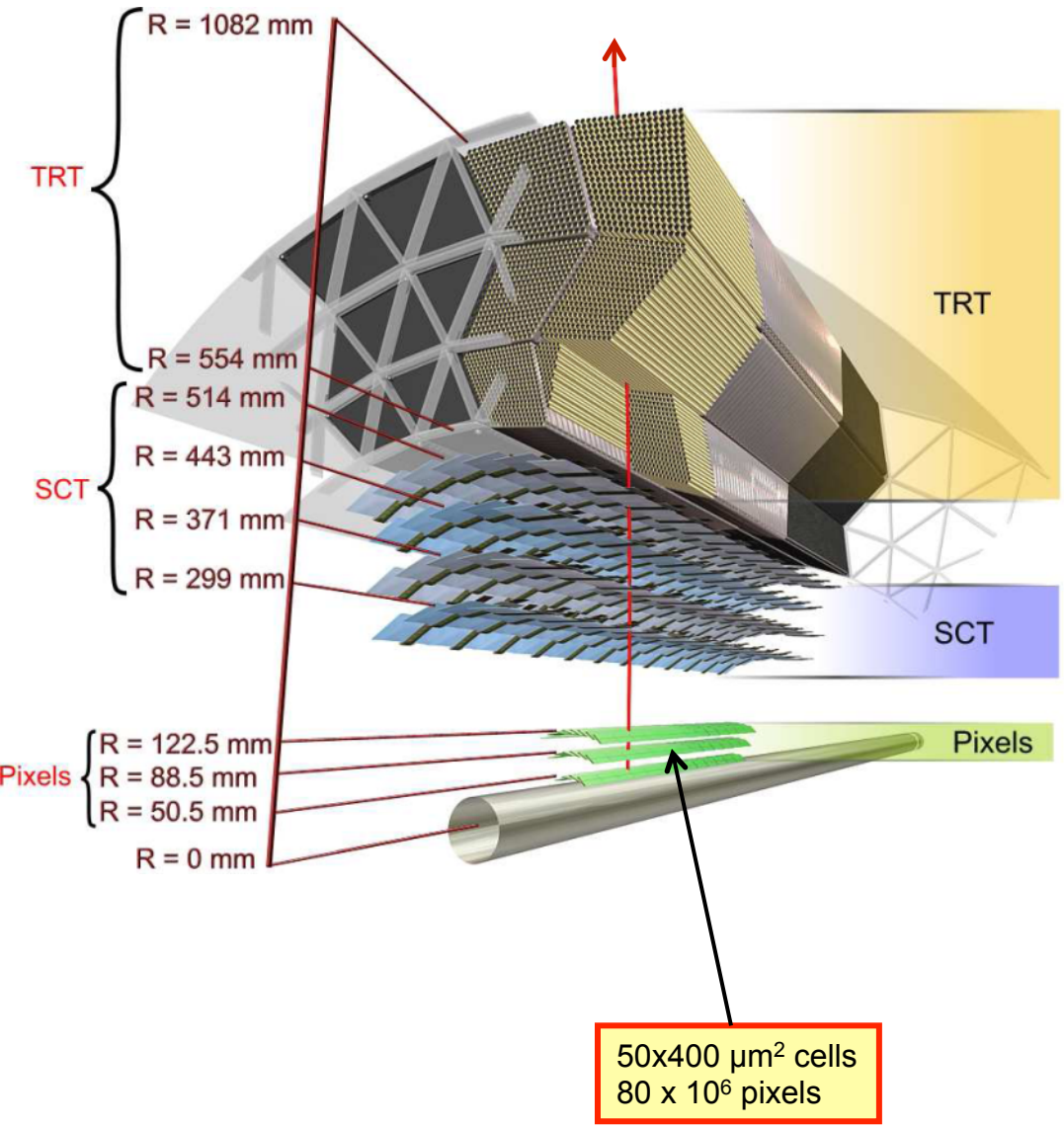
Tracking Detectors LHCb VErtex LOcator

- 42 Si strip detector elements
- 10 µm resolution
- approaches interaction point down to 7 mm

$$pp \to B_s^0 + X \to D_s^+ \mu^- \bar{\nu}_\mu + X$$
$$\to K^+ K^- \pi^+ + \mu^- \bar{\nu}_\mu + X$$



Tracking Detectors: ATLAS (pp collisions)



Transition Radiation Tracker ~ 300 m^2_{eq}

Silicon Strip Detector ~ 60 m^2

Silicon Pixel Detector ~ 1.8 m^2

	points	σ (Rφ) (μm)	σ (Rz) (μm)
TRT	36	170	-
SCT	4	17	580
PIXELS	3	10	115

ATLAS Pixel Detector

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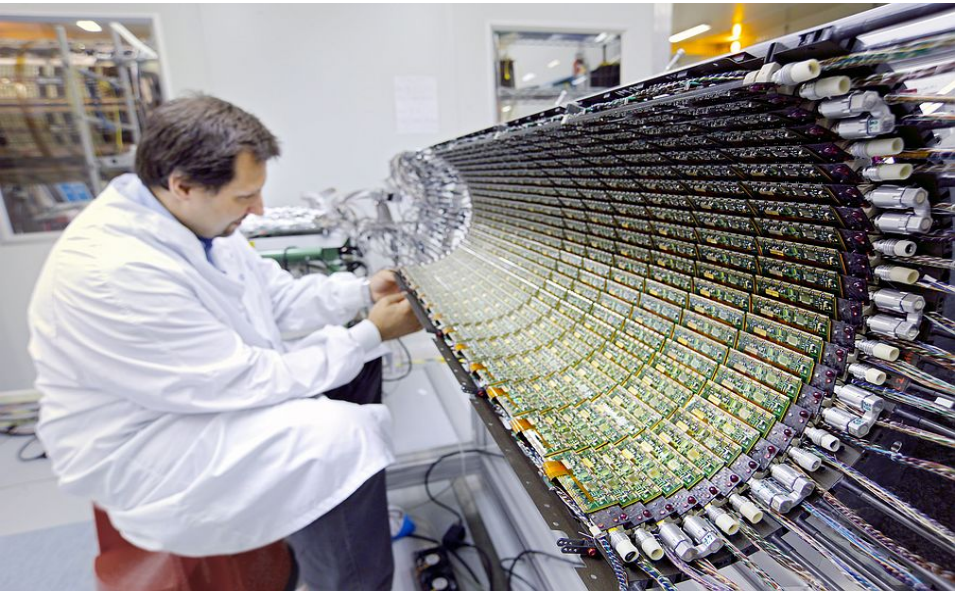

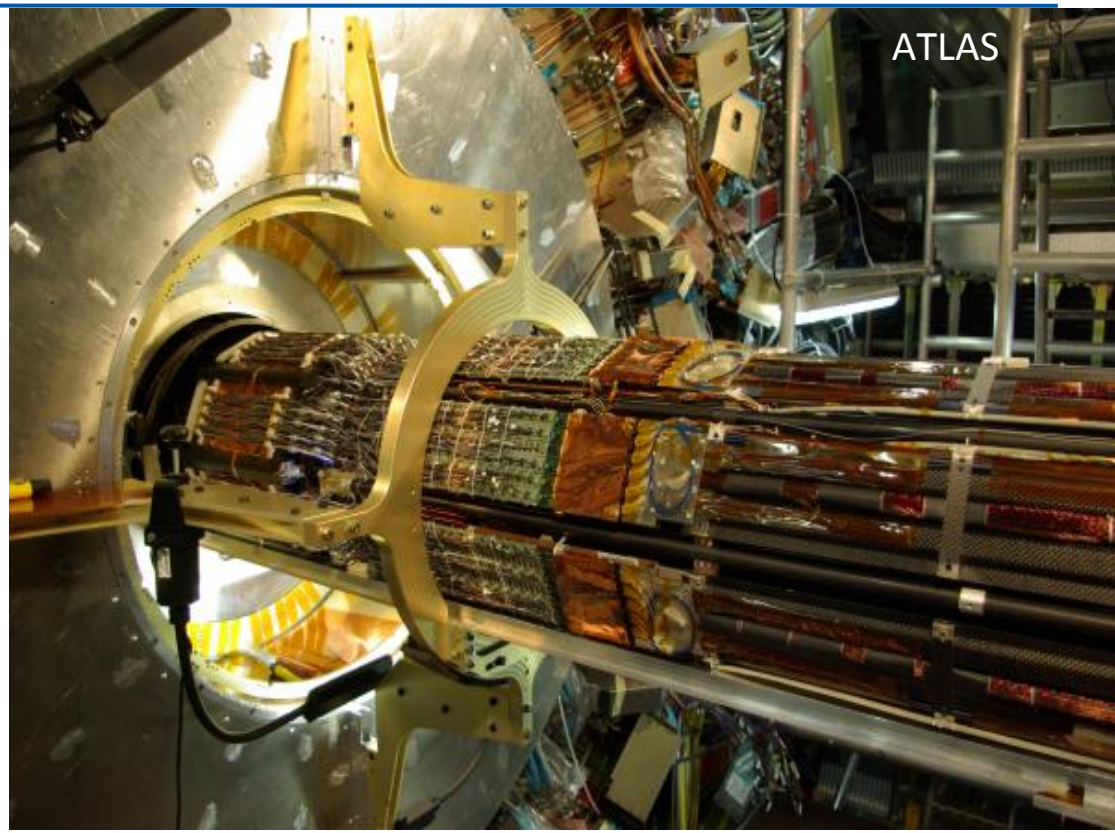

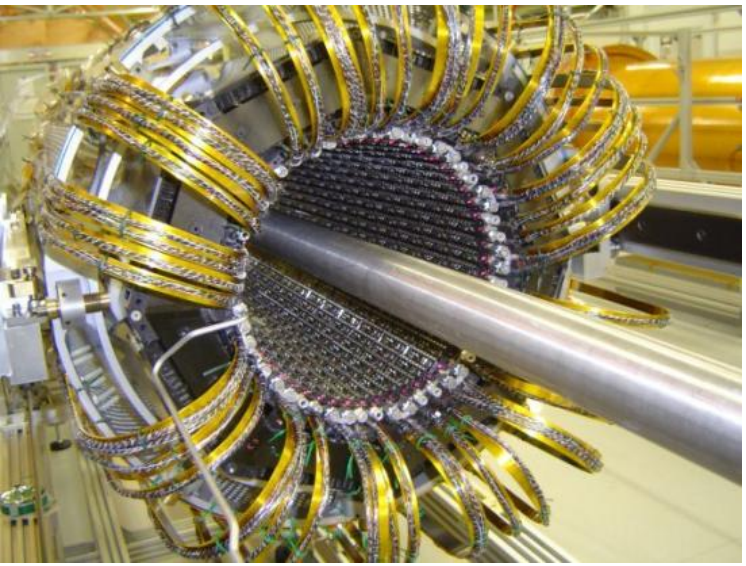

- light weight ”carbon-carbon” structures
- cooling (pumped C_3F_8 : boiling point = -25^0)
- T < -6^0 C to limit damage from irradiation

1st Upgrade … (detector in place)

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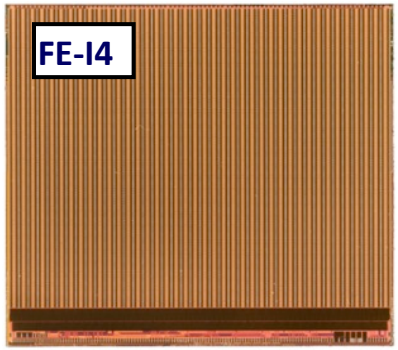
IBL = ATLAS' insertable B-Layer

- move closer to IP (5.5 cm -> 3.5 cm)
- higher rate
- higher radiation levels (~$1/r^2$)

FE-I4: larger chip
smaller feature size
higher rate capability

~0.6 × 1.1 cm²

~2 × 2 cm²



250 nm technology

pixel size 400 × 50 µm²

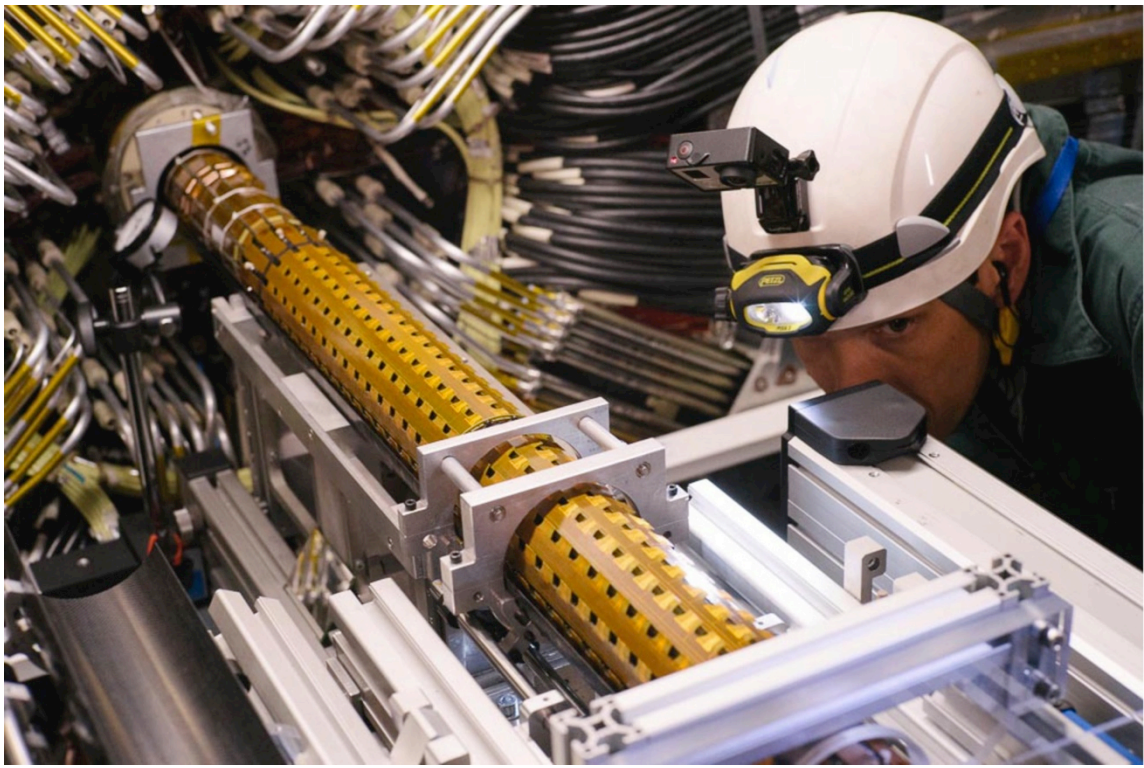
3.5 M transistors

130 nm technology

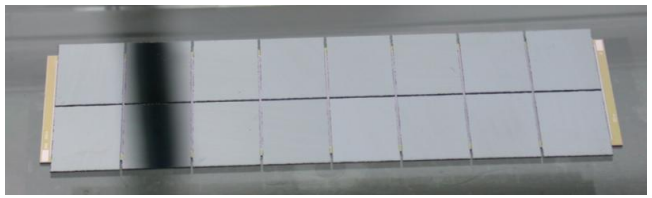
pixel size 250 × 50 µm²

87 M transistors

installed in ATLAS: May 2014

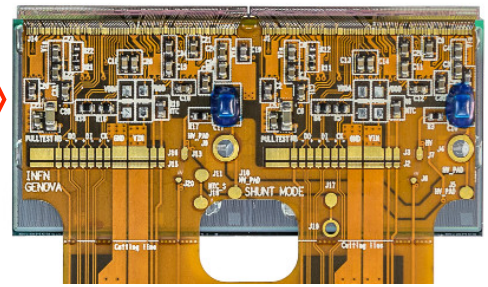


~2 × 5 cm²



ATLAS Pixel 16-chip module

~2 × 4 cm²



IBL: 2-chip module

ATLAS IBL in operation

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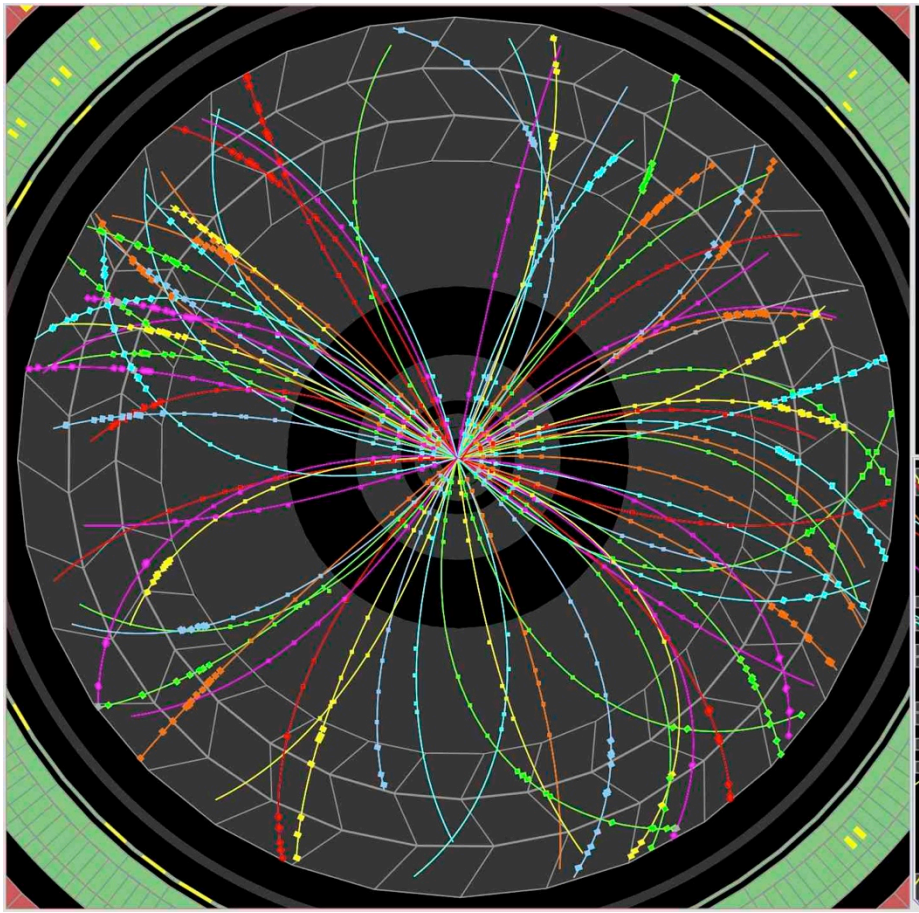
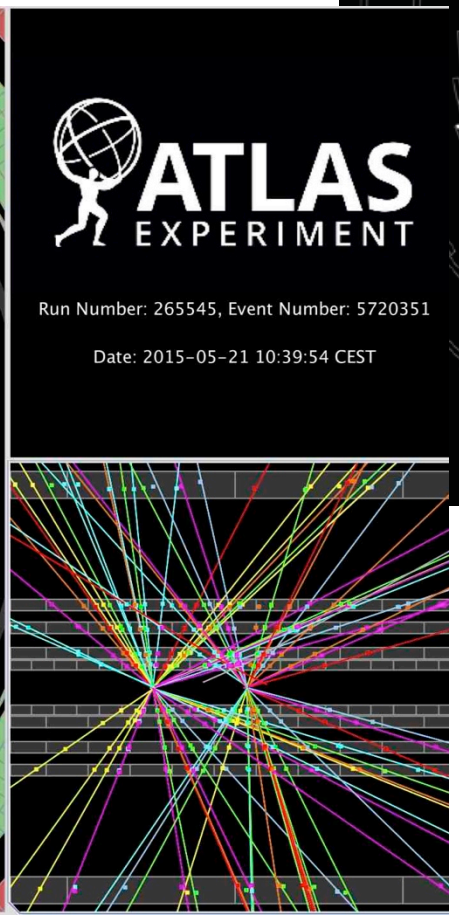
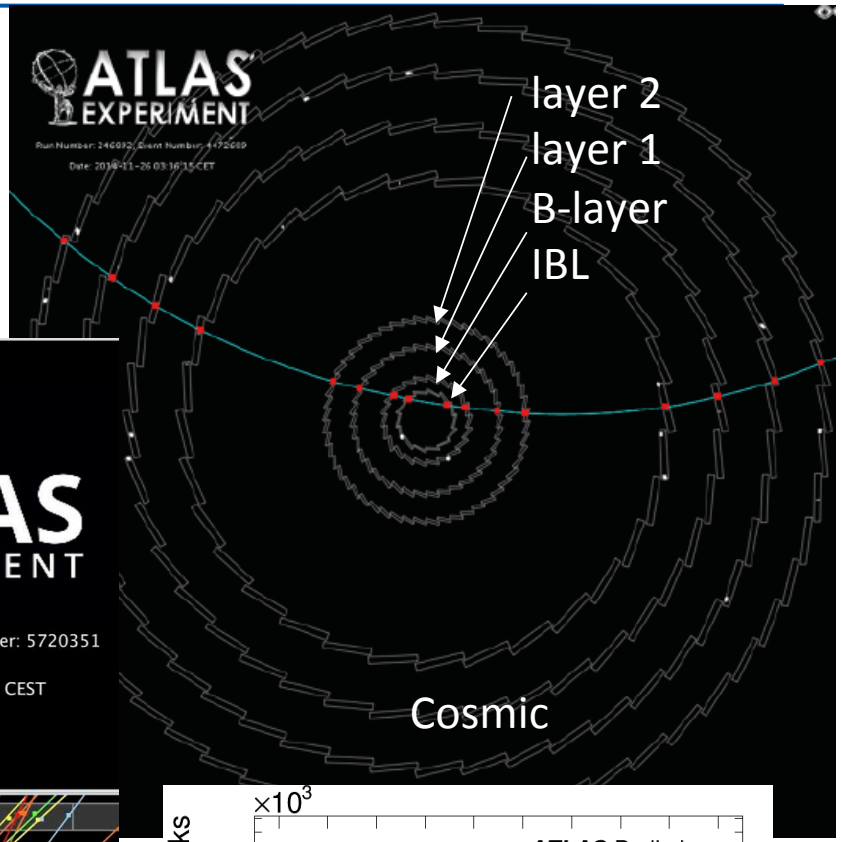
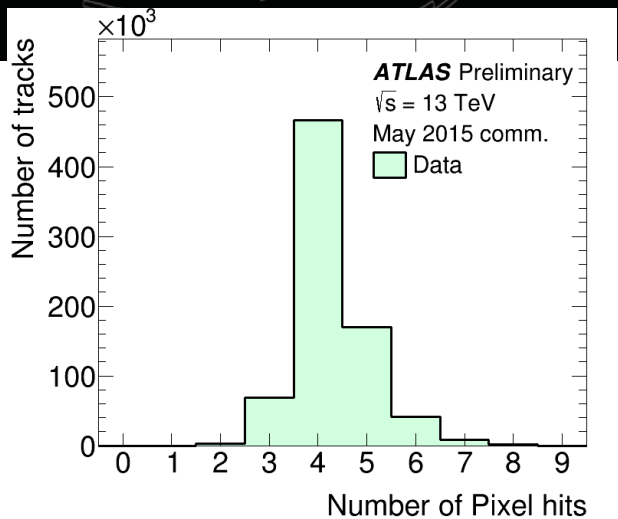
A true 4-hit pixel system!
important for b-quark tagging

13 TeV pp collision, 2 interactions

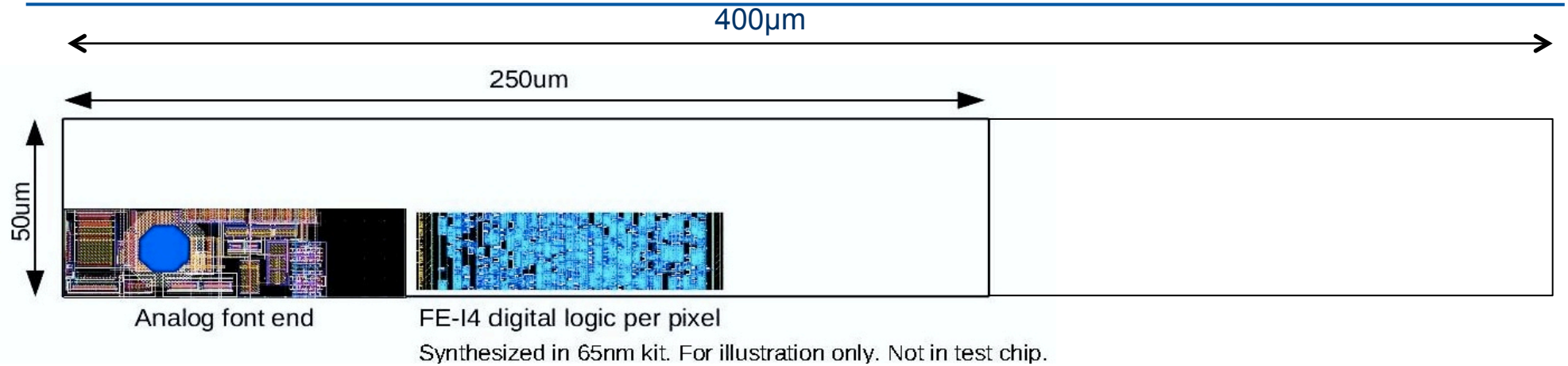








next generation based on 65 nm technology ...



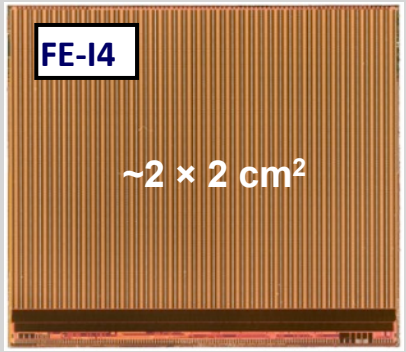
ATLAS Pixel FE chips

~0.6 × 1.1 cm²

250 nm technology

pixel size 400 × 50 µm²

3.5 M. transistors



130 nm technology

pixel size 250 × 50 µm²

87 M transistors

FE-??

hit rate **1GHz/cm²**

3.5 mW/mm²

rad hard: **2x10¹⁶/cm²**

1 Grad

65 nm technology

pixel size 50 × 50 µm²

~ 500 M transistors

addressed by CERN R&D collab.

RD53

convenors:
Jorgen Christiansen
Maurice Garcia Sciveres

65 nm prototypes of analog and digital circuits submitted and successfully tested
first large prototype submission scheduled for Sept. 2015

Radiation Damage

One of the main issues for ATLAS and CMS: Radiation damage

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- target: 10 years LHC ≅ 10^{15} n_{eq}/cm^2 (600 kGy = 60 Mrad)

- Si sensors: depletion voltage and leakage currents rise
- FE chips: threshold shifts & parasitic transistors occur
- glue: becomes hard and brittle
- mechanics: material performance degrades
- cooling: larger capacity is needed to cool more power

➔ intensive irradiation and test beam program over years including dedicated high intensity beams with LHC like rates and timing structure

Note: Plans for HL – LHC (~2023): HL-LHC = LHC x 10 => up to 1000 Mrad

Pixel Sensors in the LHC radiation environment

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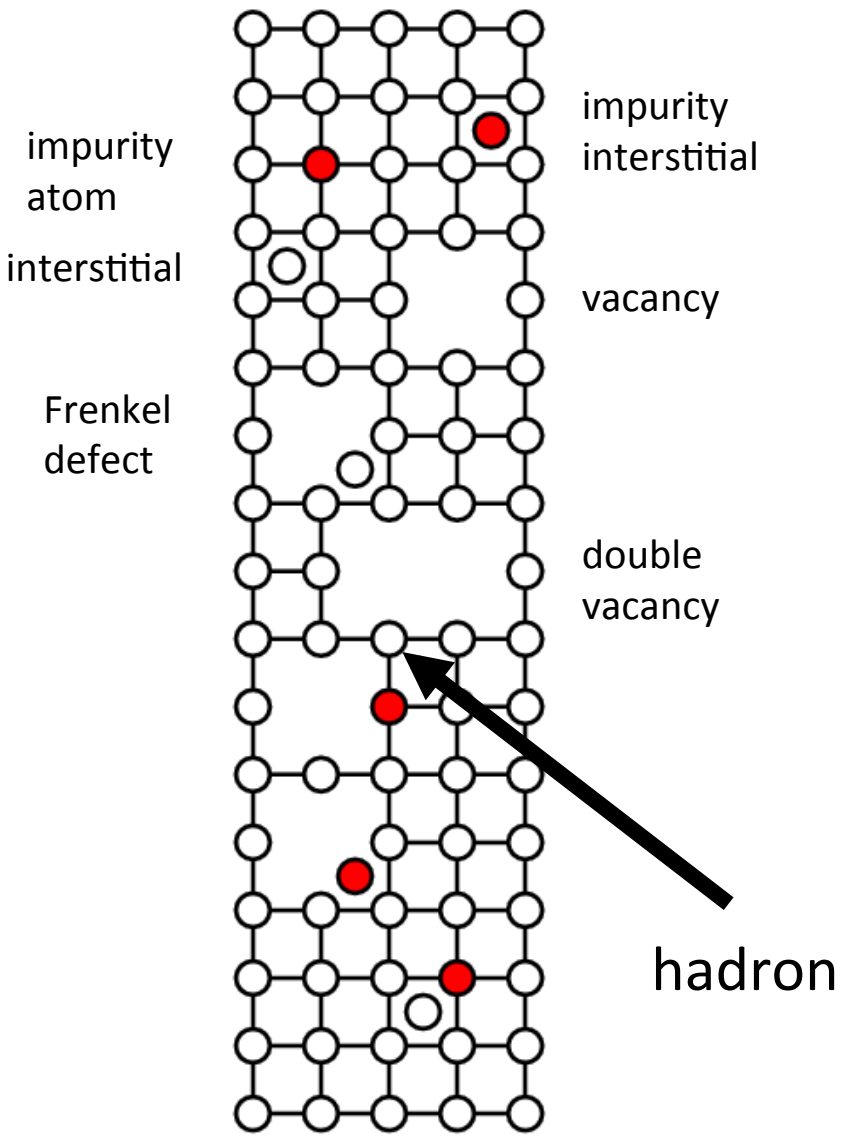
particle interactions with lattice nuclei

NIEL

non-ionizing
energy loss
(not reversible)
normalized to
1 MeV neutron damage

recoiling Si-atom can cause further defects
→ defect clusters (10nm x 200nm)

1. generation/recombination levels in band gap
   → increase of leakage current
2. change of space charge in depleted region
   → change of effective doping concentration
3. trapping centers created
   → trapping of signal charge



Pixel Sensors in the LHC radiation environment

universitätbonn

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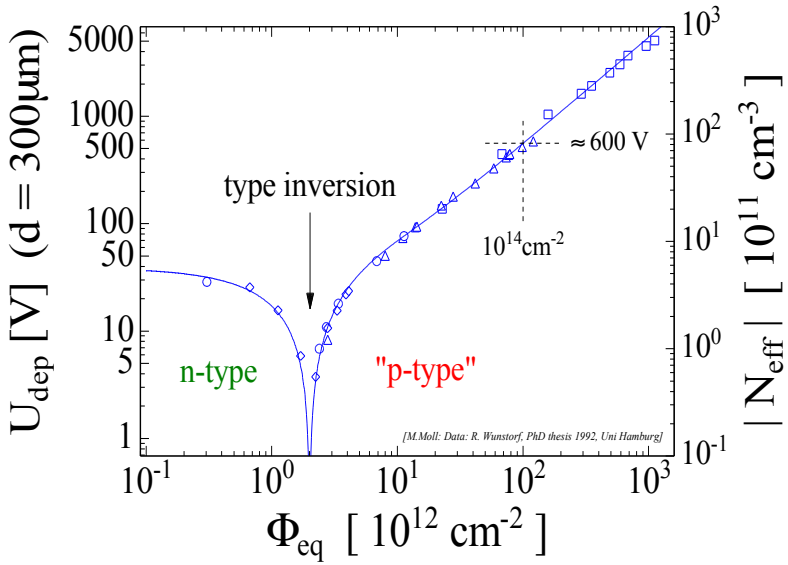
- Change of Depletion Voltage V_{dep} (N_{eff})

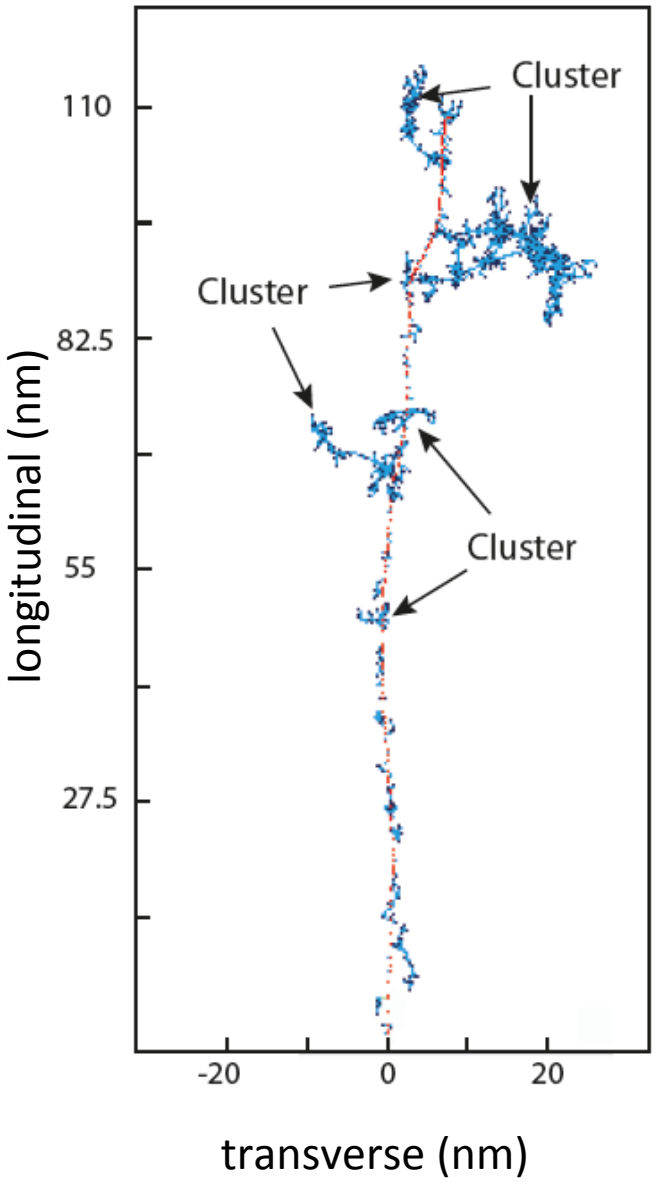
.... with particle fluence:



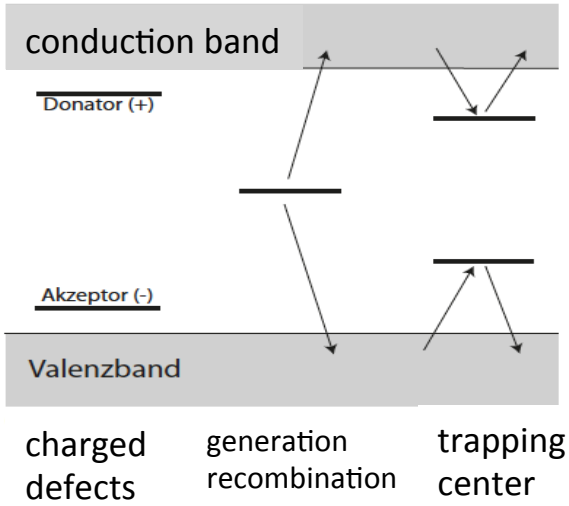
- "Type inversion": N_{eff} changes from positive to negative (Space Charge Sign Inversion)

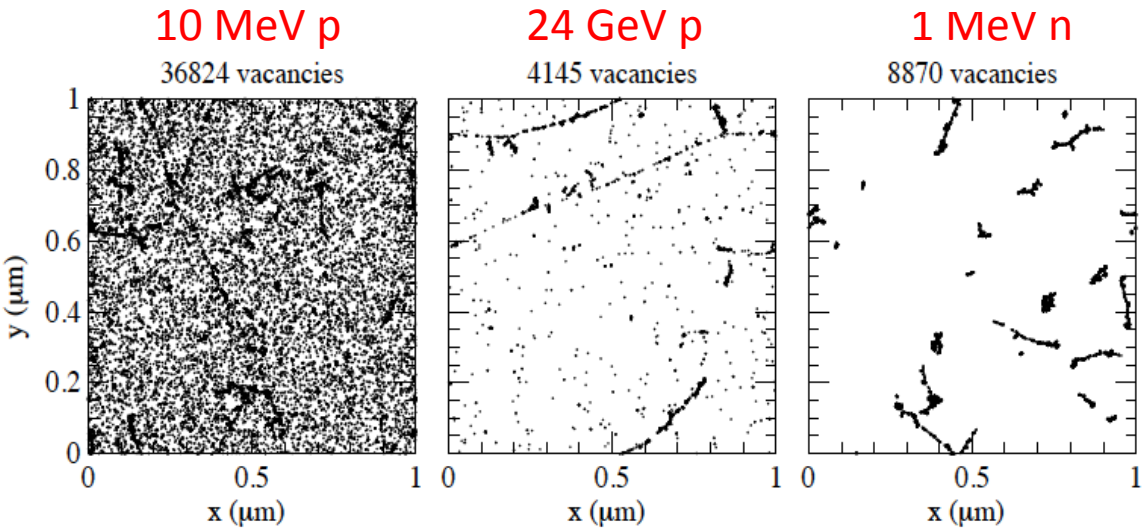
fluence (NIEL) > 10^{15} n_{eq}/cm^2
total dose > 600 kGy / 60 Mrad

Radiation Damage (NIEL)

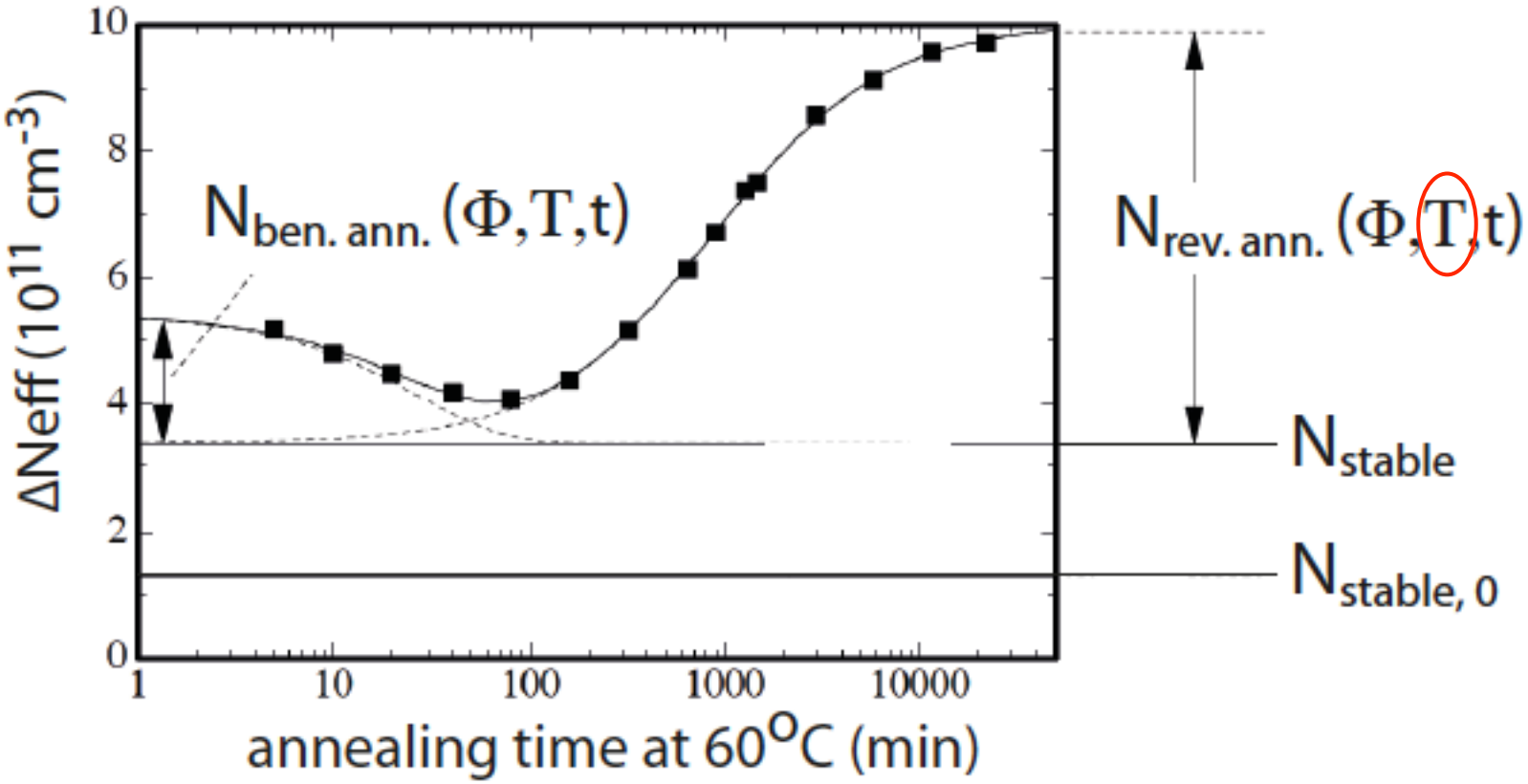


threshold energy to remove a Si-atom from the lattice:
Si - 25 eV, diamond – 43 eV





Annealing



- shaking the lattice => beneficial annealing
- too long at a high temperature => defects, that did not harm so far, become active => reverse annealing
- hence: keep detectors cool @ -5 to -10° C

Pixel Sensors in the LHC radiation environment

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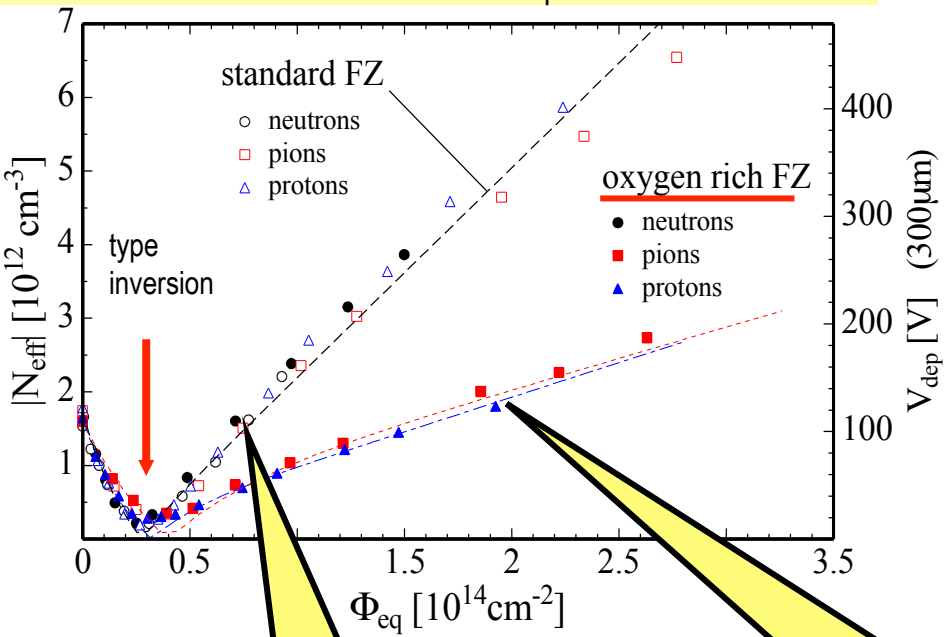
solution: oxygenated FZ silicon

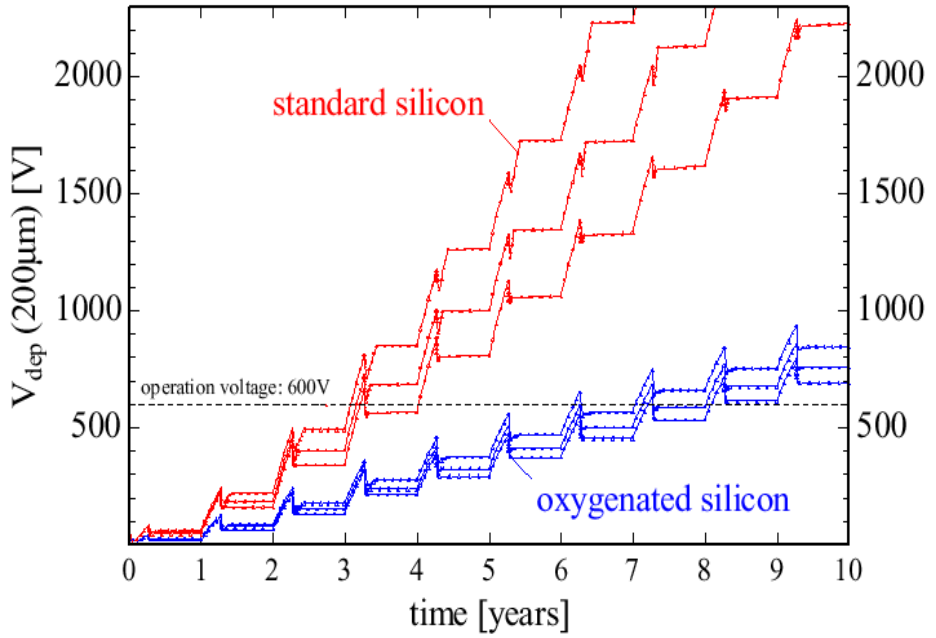
radiation tolerant to 10^{15} n_{eq} / cm^2 (600 kGy)



neutrons

protons pions

necessary voltage for full depletion



RD50, G. Lindström et al.
NIM-A 465 (2001) 60-69

reason: complex interaction of various (point+cluster) defects: V_2O interplay with a "shallow donor" that act against each other, V_2O decreases with oxygenation. For neutrons => only clusters

Pixel Sensors in the LHC radiation environment

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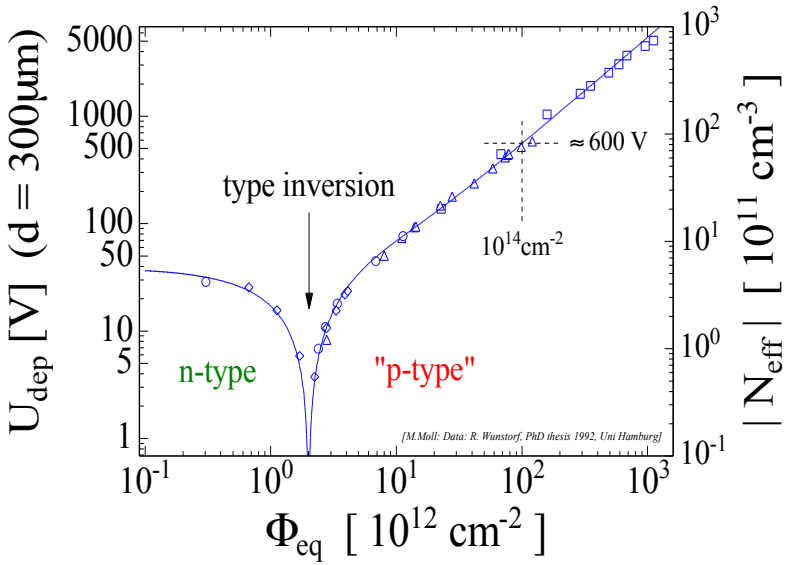
- Change of Depletion Voltage V_{dep} (N_{eff})

.... with particle fluence:



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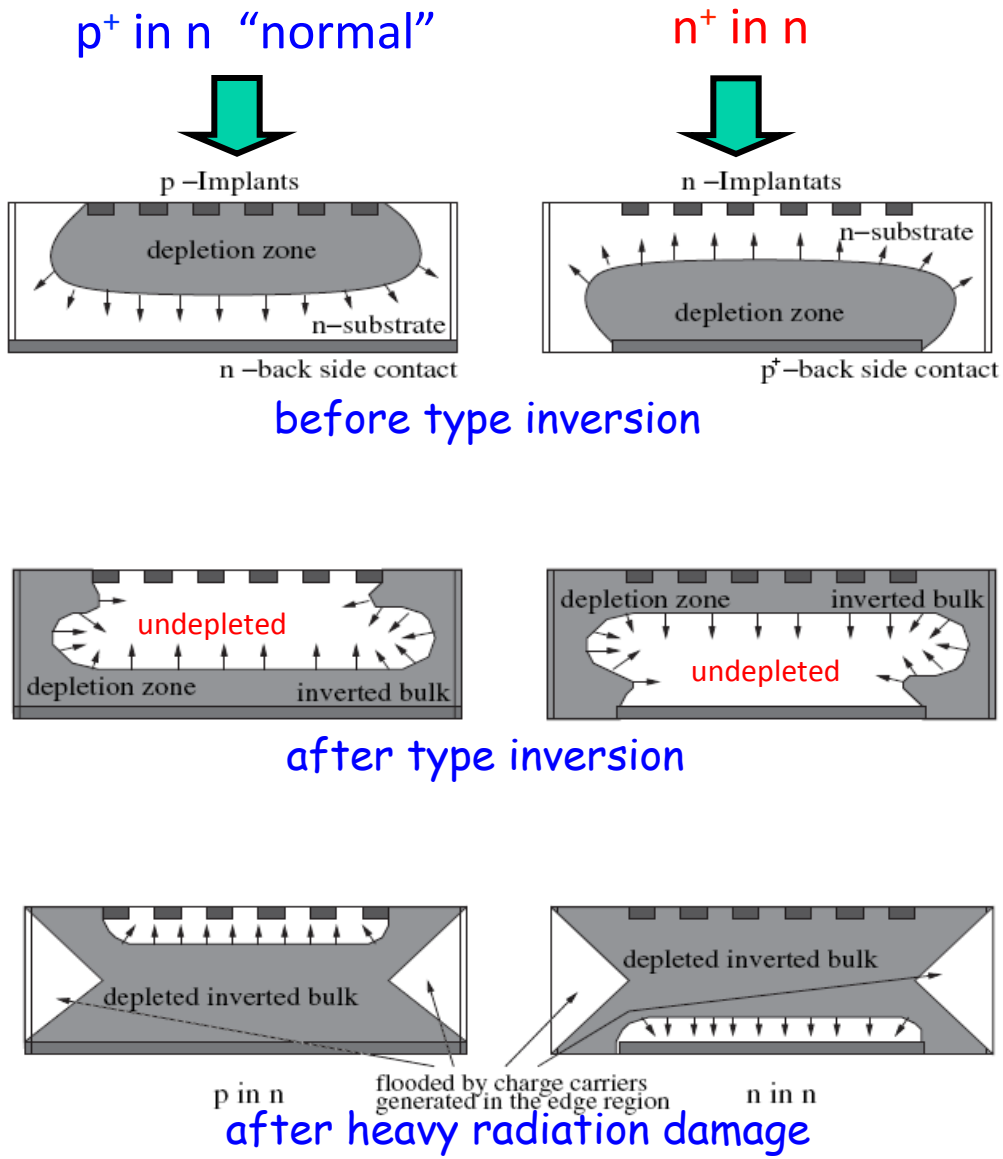
fluence (NIEL) > 10^{15} n_{eq}/cm^2
total dose > 600 kGy



L. Andricek et al, NIM-A 409 (1998) 184-193

Pixel Sensors: isolation of pixel implants

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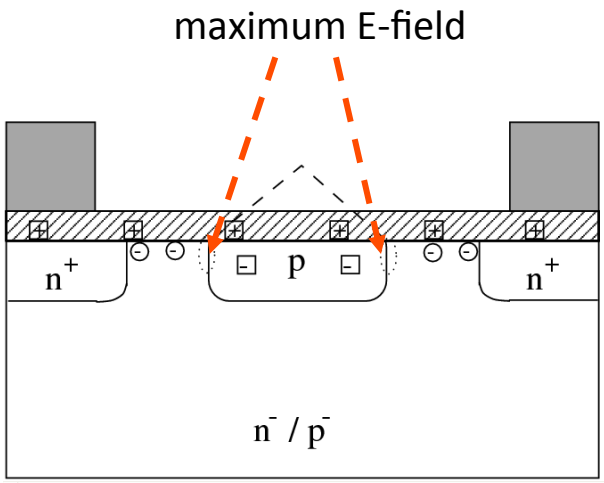
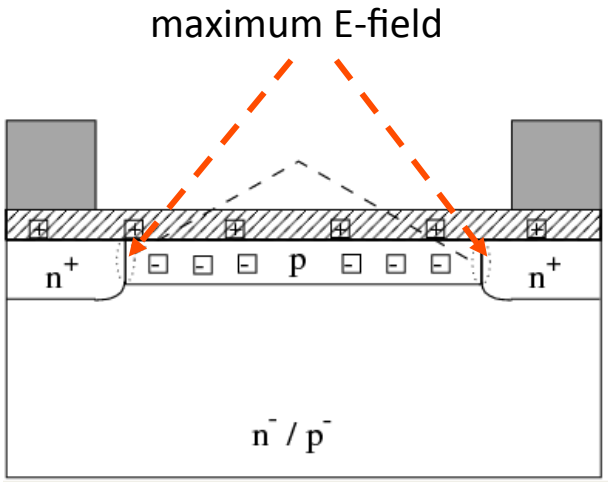
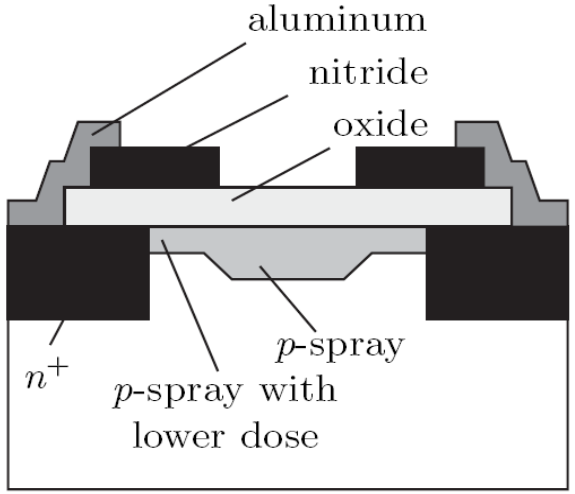
before irradiation the pn- diode is on the “wrong” side: n+ in n- contact.







p-stop

highest E-fields after irradiation

p-spray

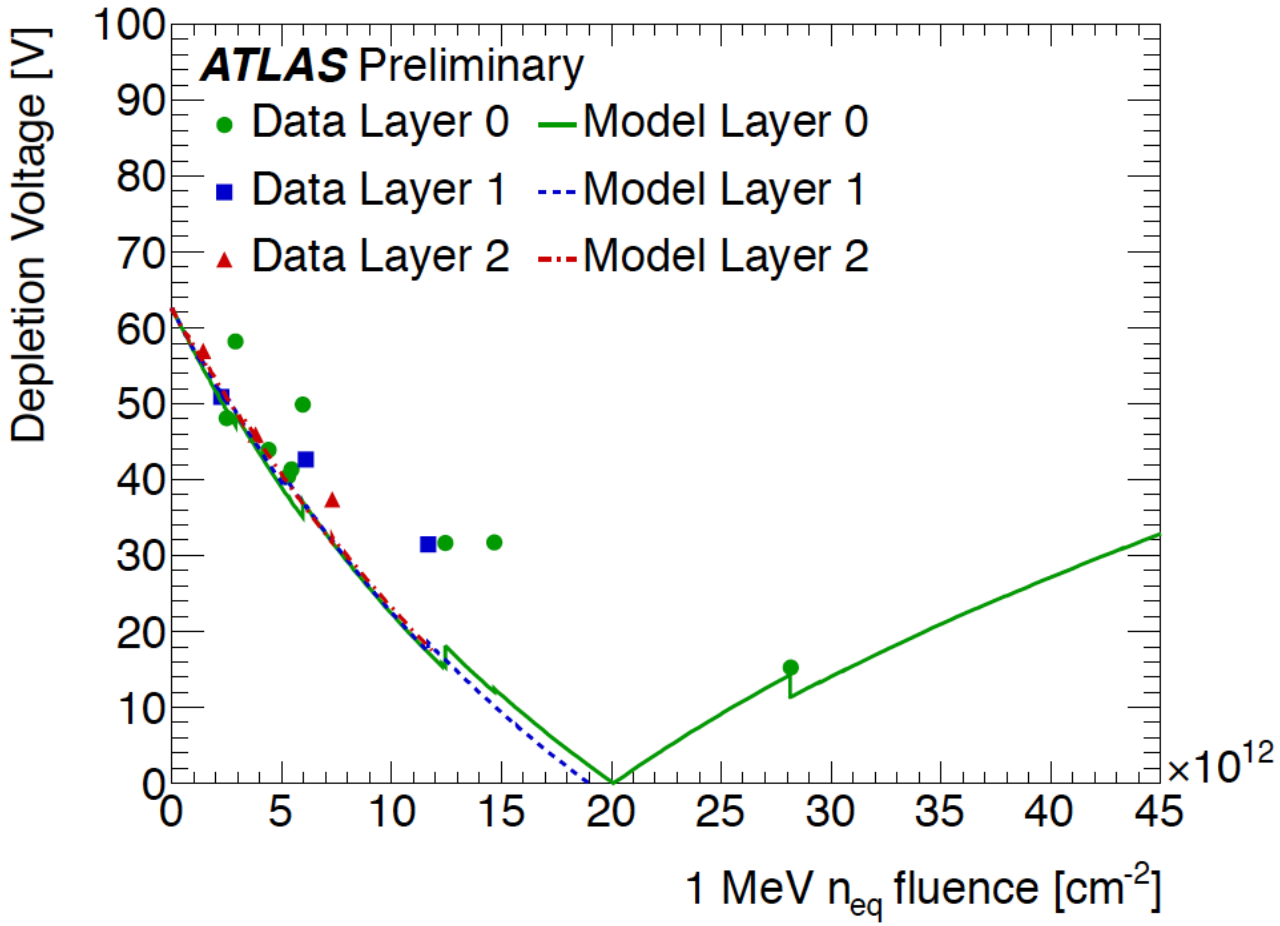
E-fields decrease with irradiation

moderated p-spray

optimum configuration
for overall voltage stability

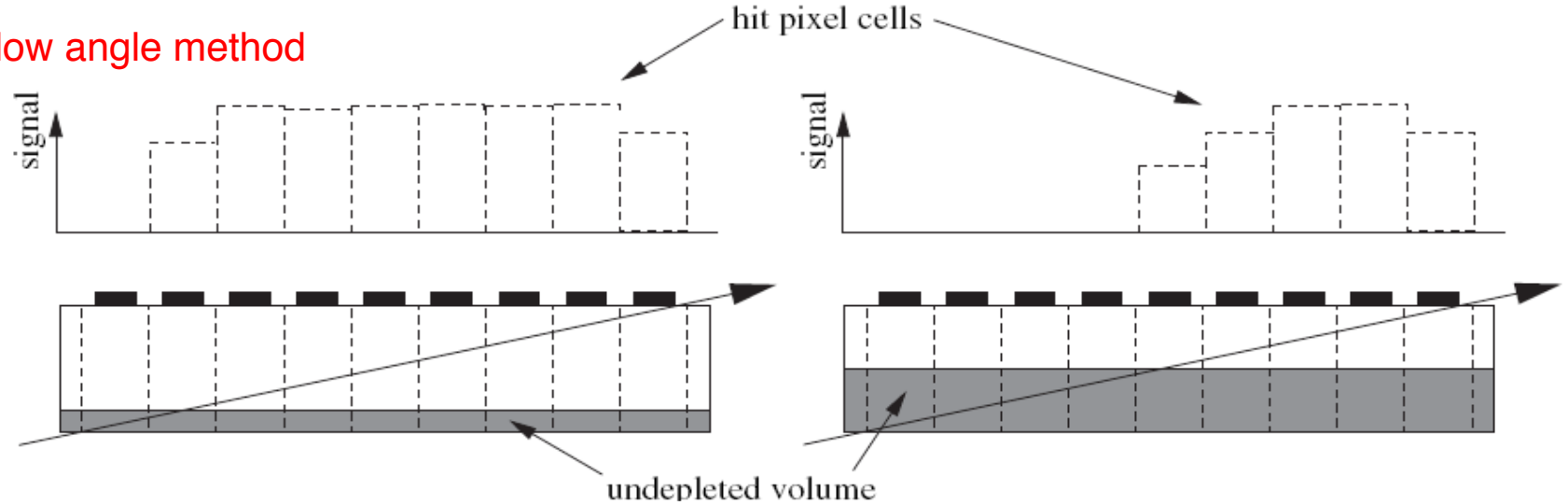
R. Richter et al, NIM-A 377 (1996) 412

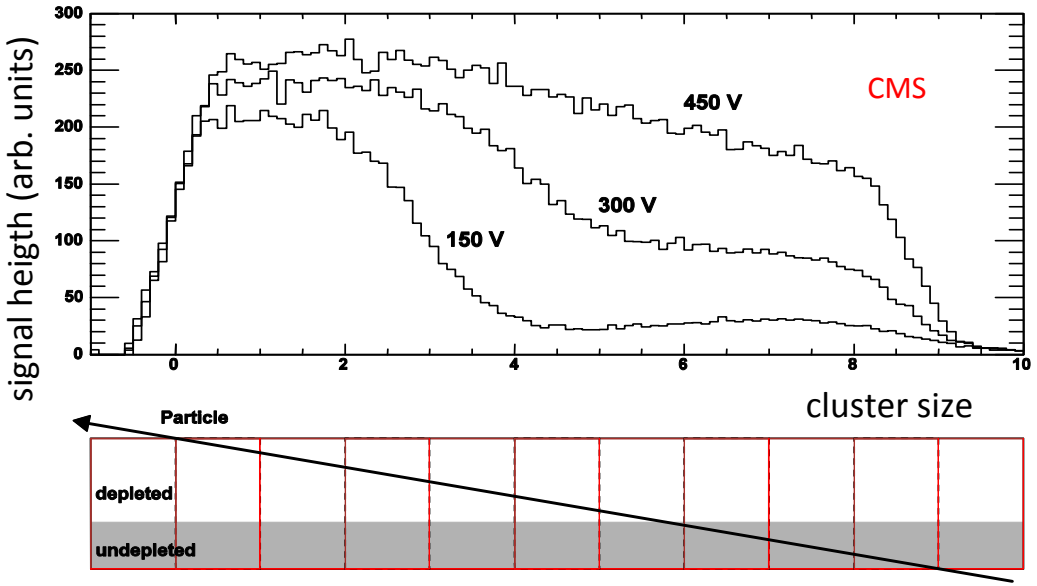
Type inversion has already been observed at LHC



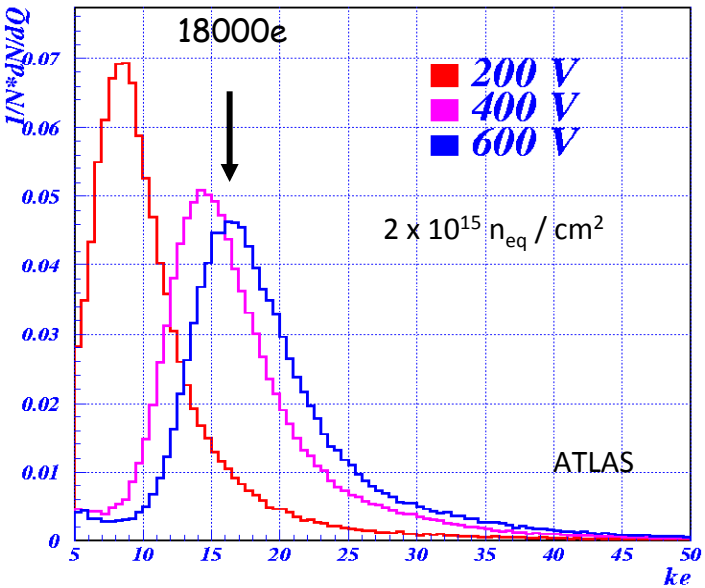
Measuring the effective depletion depth after irradiation

- Shallow angle method



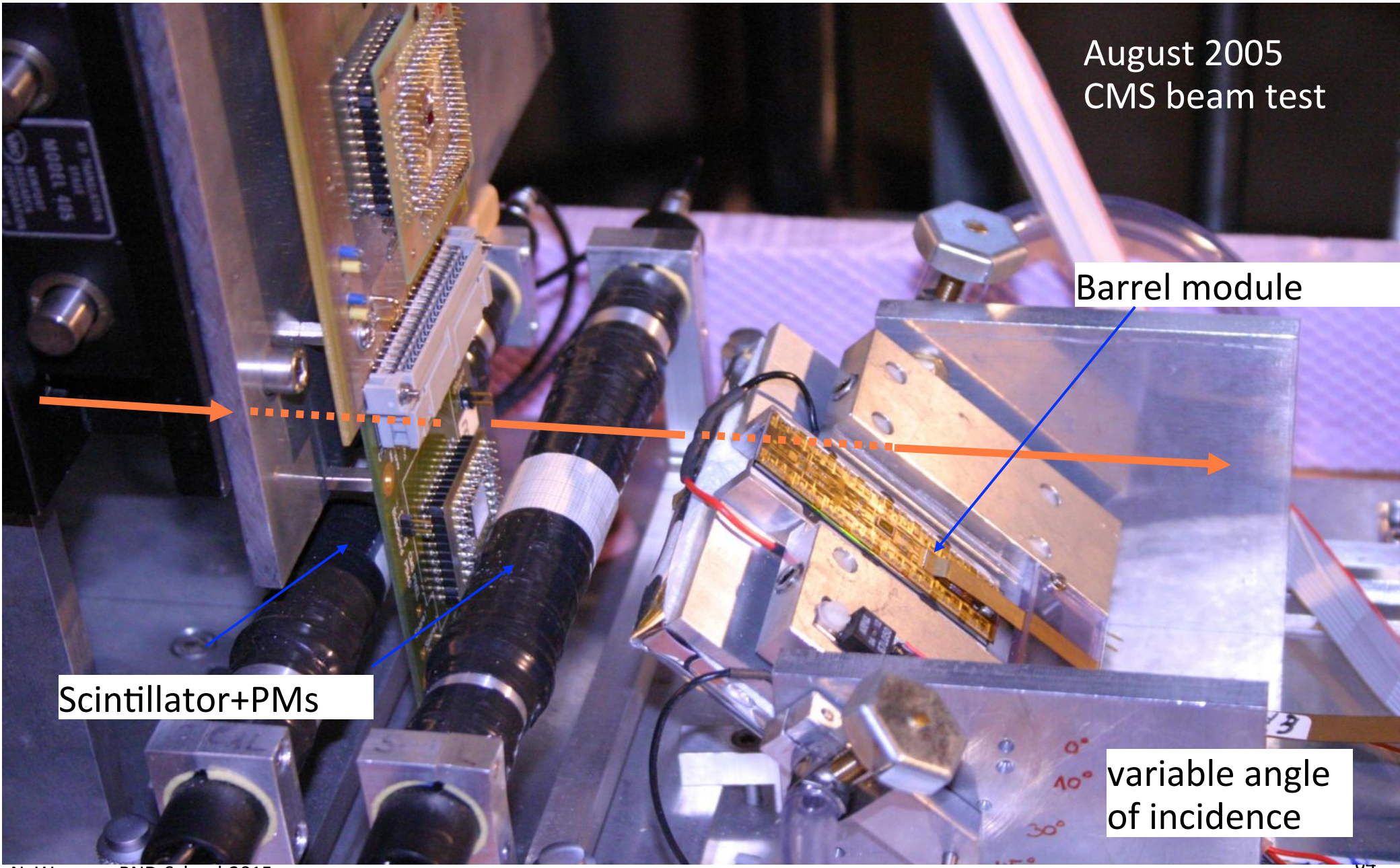


V.Chiochia, M. Swartz et al. arxiv.org/abs/physics/0409049



cluster charge

Measuring the effective depletion depth after irradiation



Radiation damage to the FE-electronics … and cure

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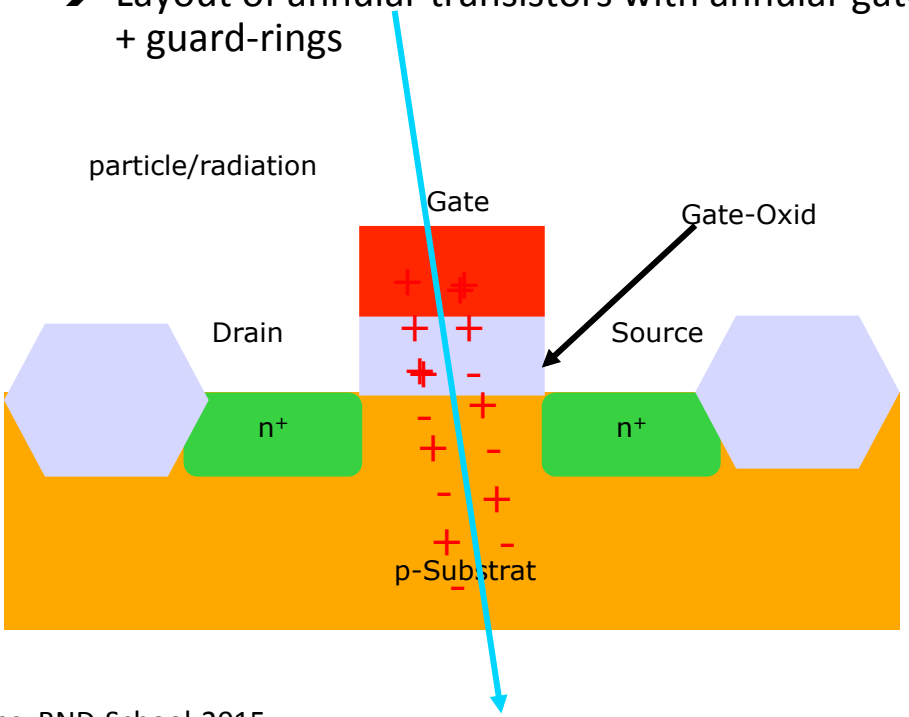
Effects: generation of positive charges in the SiO_2
and defects in Si - SiO_2 interface

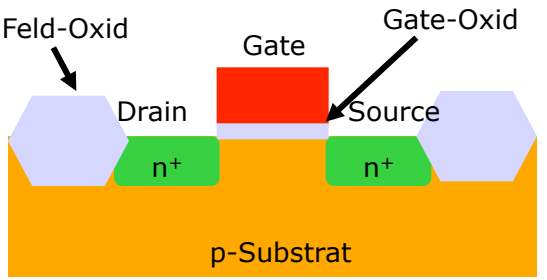
1. Threshold shifts of transistors

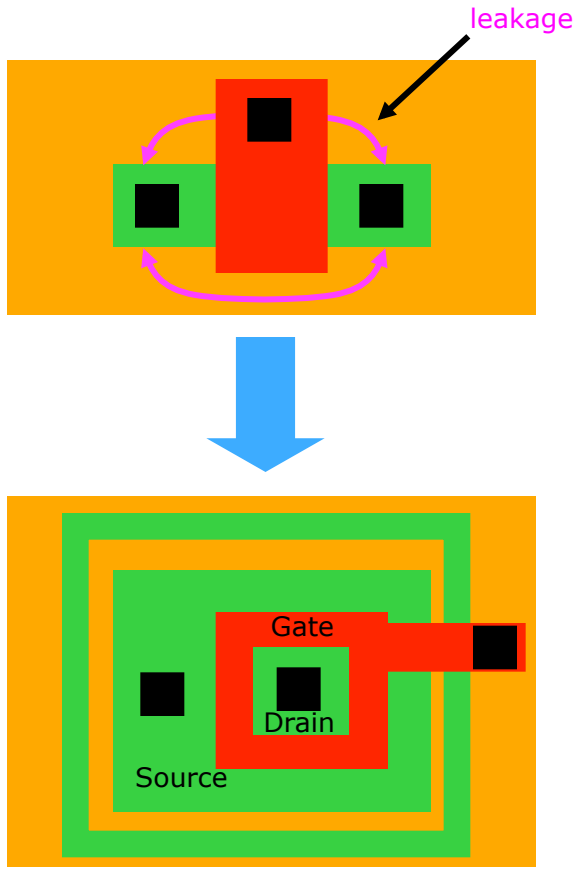
➔ Deep Submicron CMOS technologies with small structure sizes (≤ 350 nm) and thin gate oxides (d_{ox} < 5 nm) → holes tunnel out

2. Leakage currents under the field oxide

➔ Layout of annular transistors with annular gate-electrodes + guard-rings





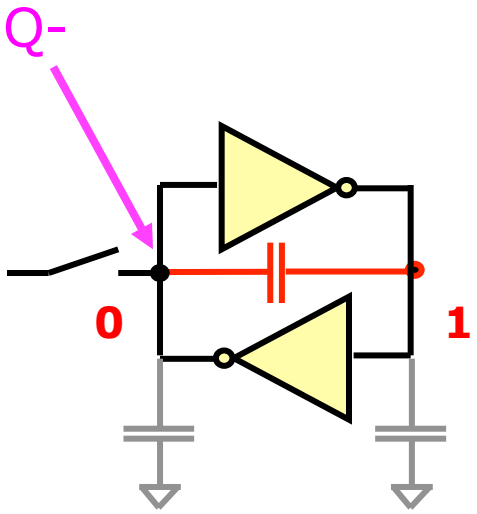


Radiation damage to the FE-electronics … and cure

radiation induced bit errors

("single event upsets" SEU)

large amounts of charge on circuit nodes
- by nuclear reactions, high track densities -
can cause "bit-flip"



standard SRAM cell

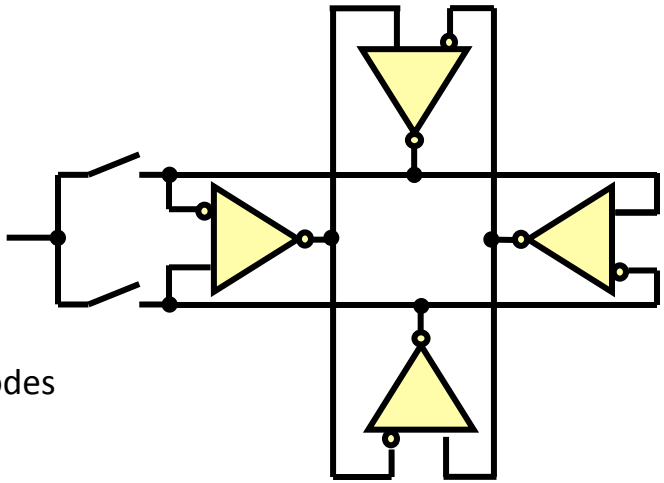
2 examples of error resistant logic cells

➔ enlarge storage capacitances in SRAM cells:

$Q_{crit} = V_{threshold} \cdot C$

➔ storage cells with redundancy (DICE SRAM cell)

information and its inverse stored on 2+2 independent and cross-coupled nodes
→ temporary flip of one node cannot permanently flip the cell.


SEU tolerant DICE SRAM cell

Irradiated Modules after 1 MGy (20 years @ LHC)

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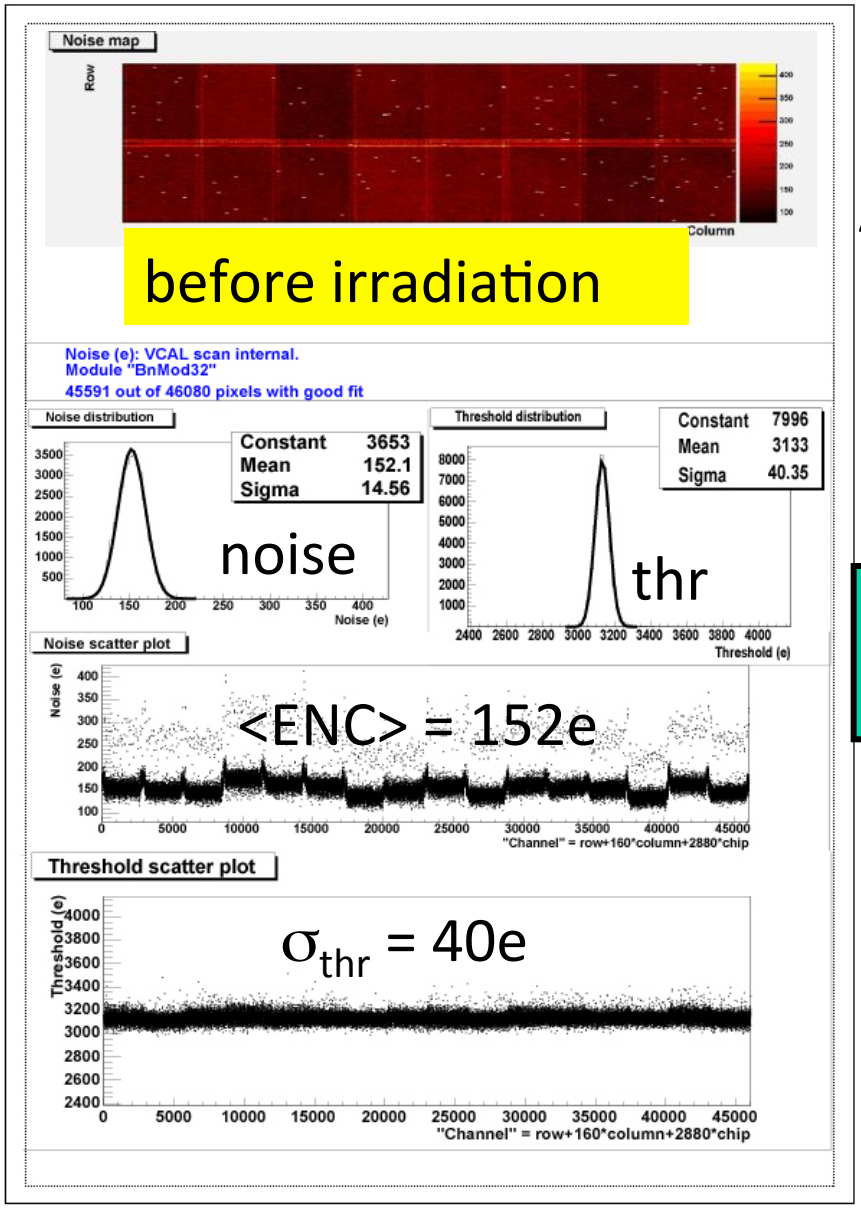
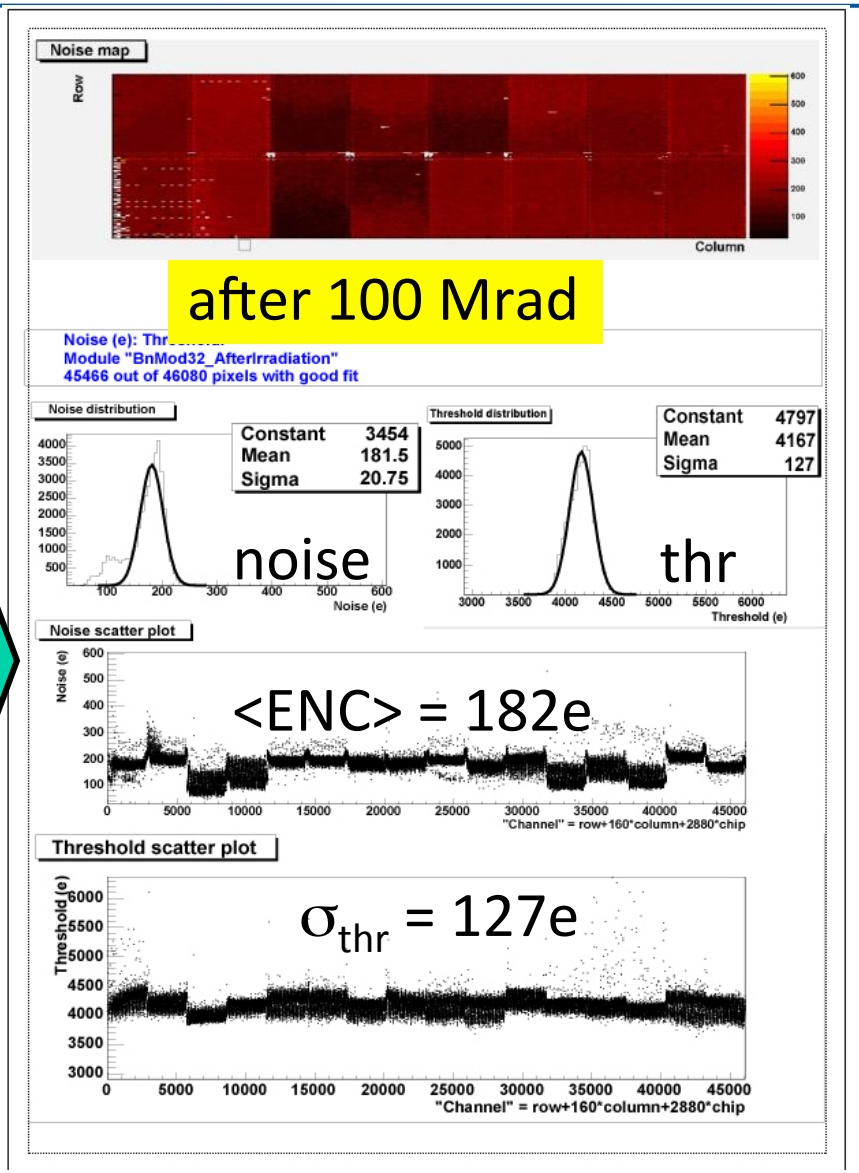


ATLAS

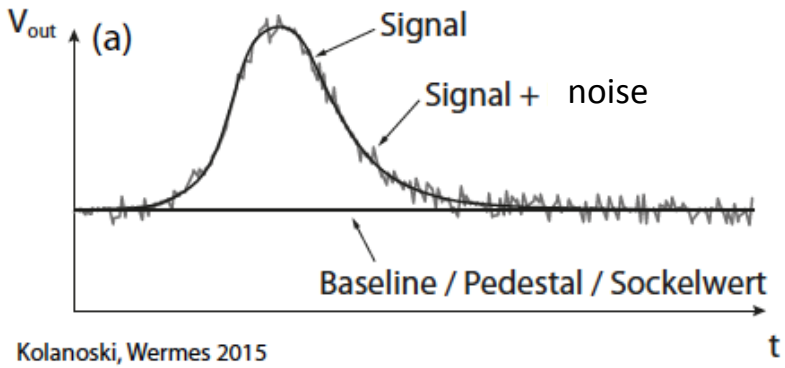
10yrs LHC

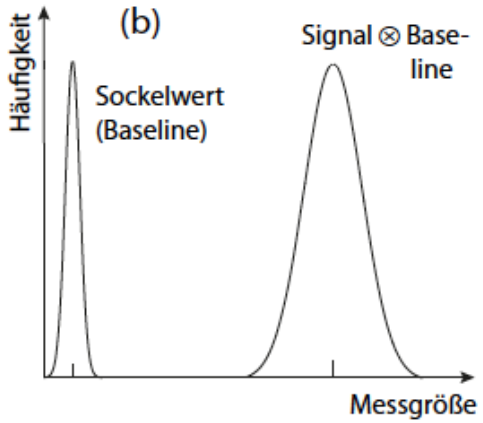


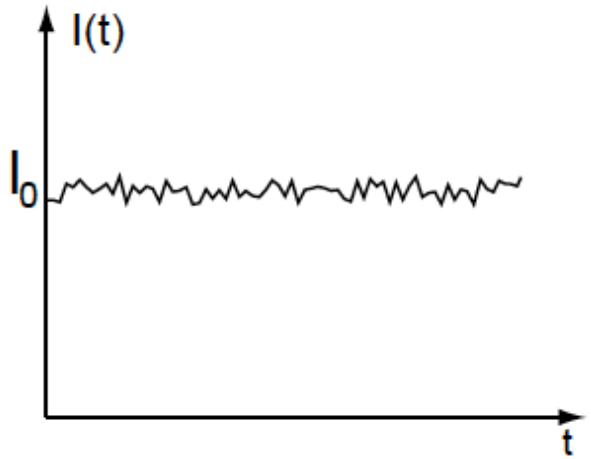
A. Andreazza NIM-A 513:103-106,2003

Noise

Noise in ionisation detectors





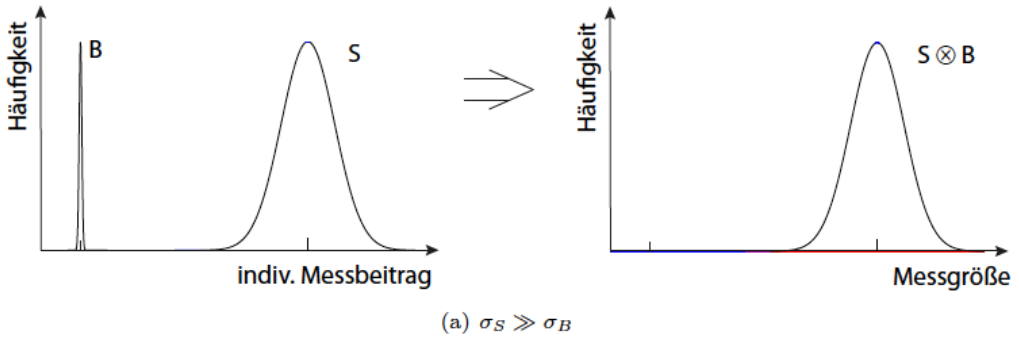


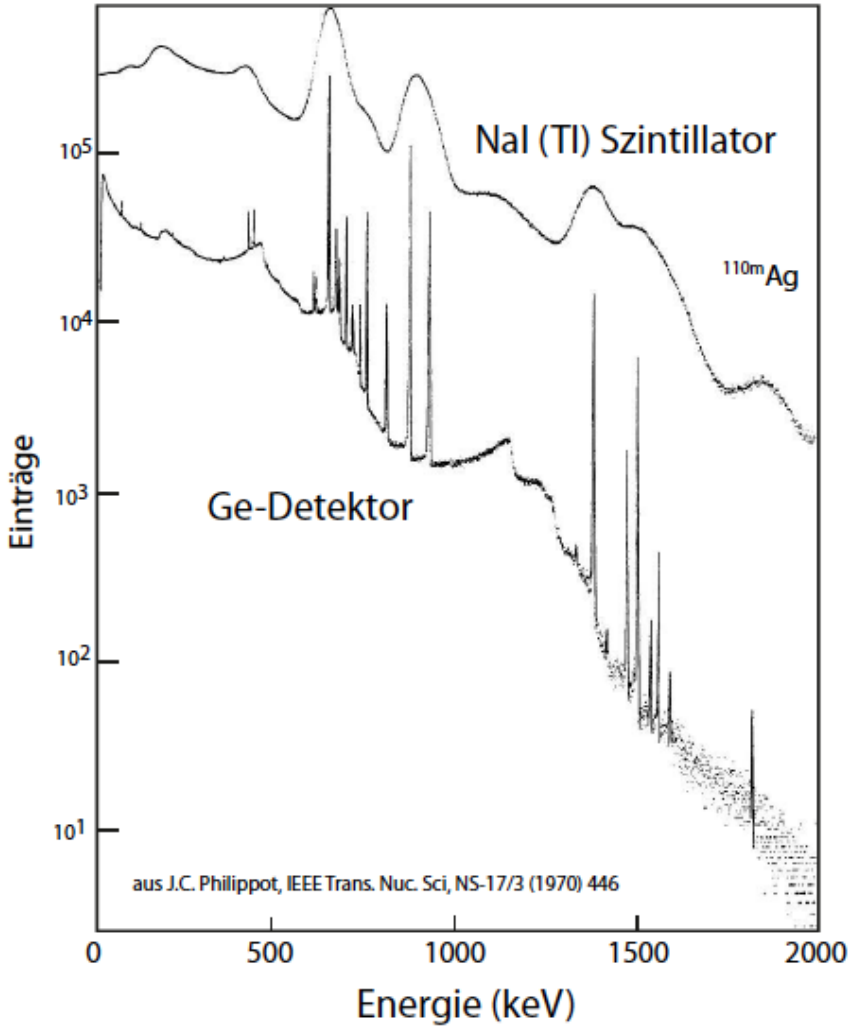
$$\sigma^2 = \lim_{T\to\infty} \frac{1}{T}\int_0^T \left(I(t) - I_0\right)^2 dt$$

$$dP_n/df = \frac{1}{R}\, d\langle u^2\rangle/df = R\, d\langle i^2\rangle/df$$

When to care about noise …

- always …
- but particularly, when situation is like this





- even if you are not interested in an energy measurement, remember … thresholds

Noise

shot noise

white noise

current noise

resistor noise

switching noise

series noise

flicker noise

popcorn noise

Nyquist Noise

Johnson Noise

parallel noise

kT/C noise

1/f noise

RTS noise

Thermal noise

Noise in a pixel/strip detector (ionisation detector)

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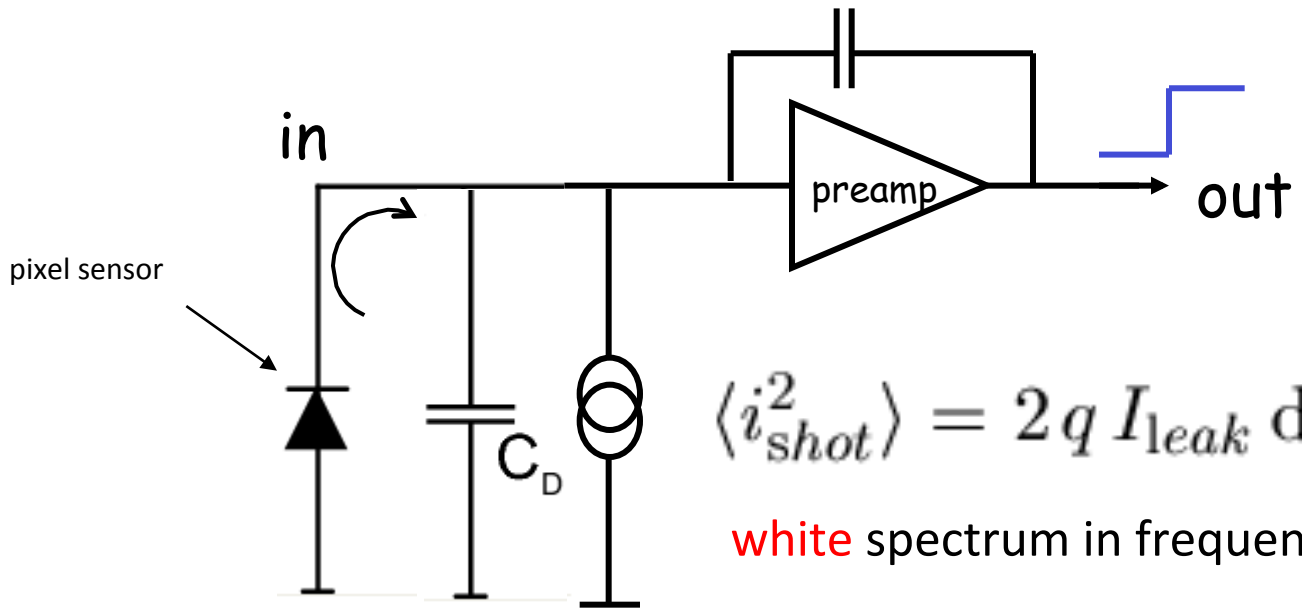
three physical noise sources:

number fluctuations of quanta	→	1. shot noise	$\langle i^2 \rangle = 2q \langle i \rangle df$
		2. 1/f noise	$\langle i^2 \rangle$ = const. 1/f df
velocity fluctuations of quanta	→	3. thermal noise	$\langle i^2 \rangle = 4kT / R\ df$

where do they appear in a typical pixel detector readout chain ?



$$\langle i^2_{shot} \rangle = 2\,q\,I_{leak}\,\mathrm{d}f$$

white spectrum in frequency f

Noise in a pixel/strip detector (ionisation detector)

universitätbonn

three physical noise sources:

number fluctuations of quanta	→	1. shot noise	$\langle i^2 \rangle = 2q \langle i \rangle df$
		2. 1/f noise	$\langle i^2 \rangle = \text{const.}\ 1/f\, df$
velocity fluctuations of quanta	→	3. thermal noise	$\langle i^2 \rangle = 4kT / R\, df$

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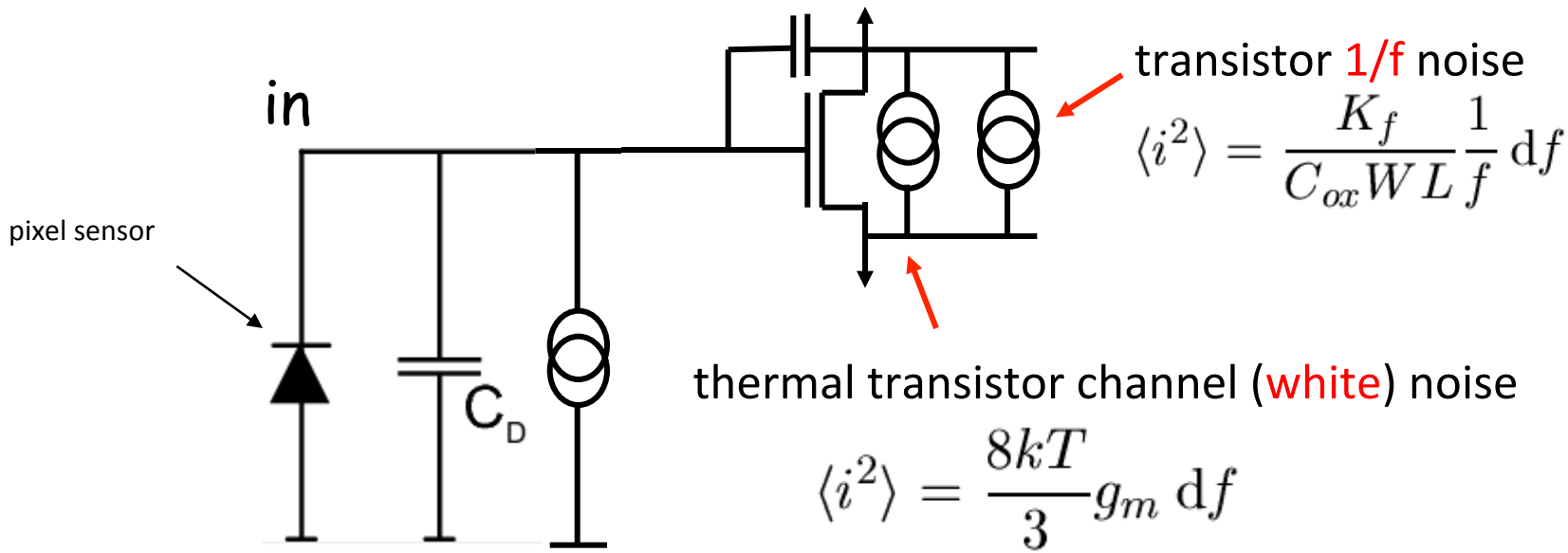

Noise in a pixel/strip detector (ionisation detector)

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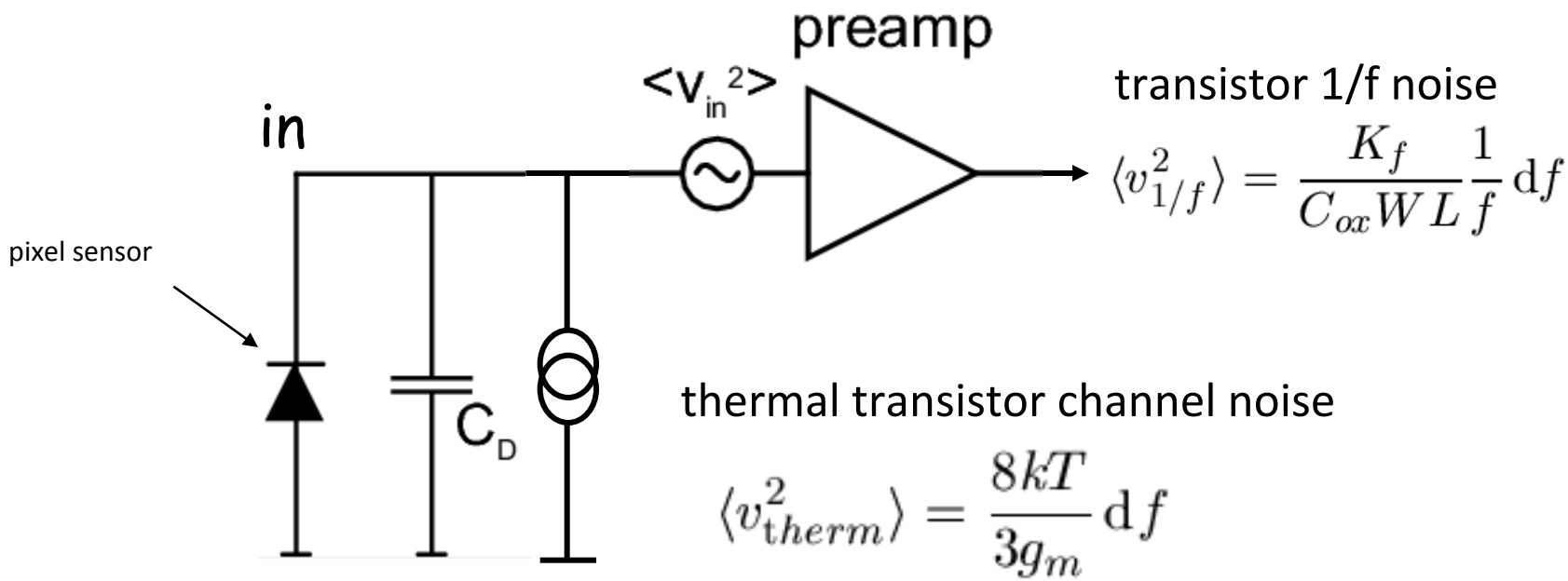

Noise in a pixel/strip detector (ionisation detector)

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equivalent noise charge $\mathrm{ENC} = \dfrac{\text{noise output voltage (rms)}}{\text{signal output voltage for the input charge of } 1e^-}$

$$ENC_{tot}^2 = ENC_{shot}^2 + ENC_{therm}^2 + ENC_{1/f}^2$$

charge sensitive preamplifier only

$$ENC_{\text{shot}} = \sqrt{\frac{I_{leak}}{2q}\tau_f} = 56e^- \times \sqrt{\frac{I_{leak}}{\text{n}A}\frac{\tau_f}{\mu s}}$$

$$ENC_{\text{therm}} = \frac{C_f}{q}\sqrt{\langle v_{\text{therm}}^2\rangle} = \sqrt{\frac{kT}{q}\frac{2C_D}{3q}\frac{C_f}{C_{load}}} = 104e^- \times \sqrt{\frac{C_D}{100\,\text{fF}}\frac{C_f}{C_{load}}}$$

$$ENC_{1/\text{f}} \approx \frac{C_D}{q}\sqrt{\frac{K_f}{C_{ox}WL}}\sqrt{\ln\left(\tau_f\frac{g_m}{C_{load}}\frac{C_f}{C_D}\right)} = 9e^- \times \frac{C_D}{100\,\text{fF}}(\text{for NMOS trans.})$$

W, L = width and length of trans. gate
K_f = 1/f noise coefficient
C_{ox} = gate oxide capacitance

C_f = feedback capacitance
C_{load} = load capacitance
C_D = detector capacitance
τ_f = feedback time constant

reference
Rossi, Fischer, Rohe, Wermes
Pixel Detectors. Springer 2006

Noise in a pixel/strip detector (ionisation detector)

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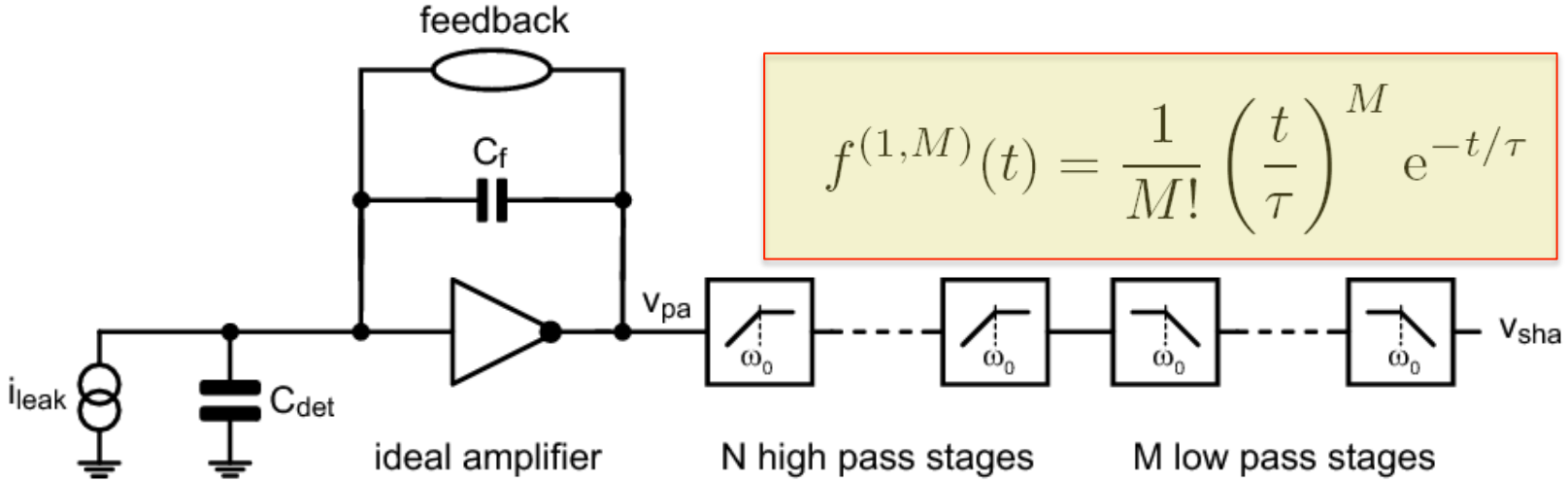
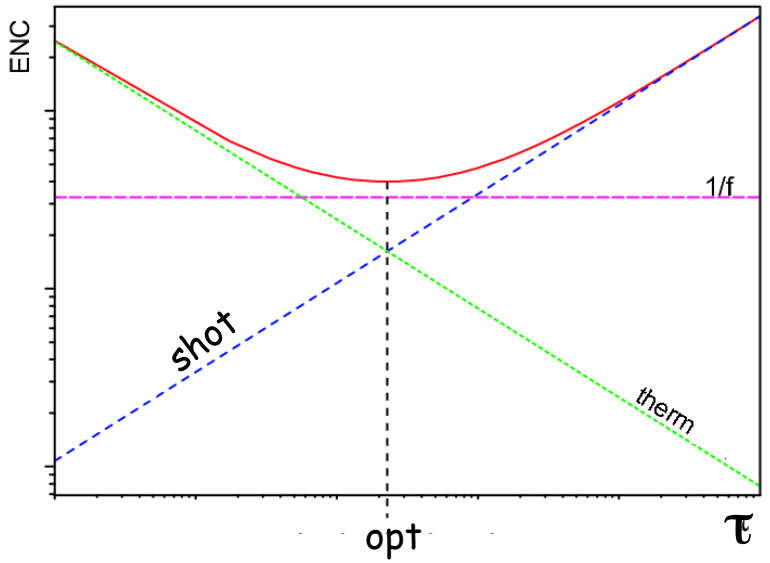
… with an additional filter amplifier (shaper) being the band width limiter



$$f^{(1,M)}(t) = \frac{1}{M!}\left(\frac{t}{\tau}\right)^{M} e^{-t/\tau}$$

$$\mathrm{ENC}^2(e^2) = 11\, I_0(\mathrm{nA})\,\tau(\mathrm{ns}) + 740\,\frac{1}{WL(\mu\mathrm{m}^2)}\,C_D^2(100\,\mathrm{fF}) + 4000\,\frac{1}{g_m(\mathrm{mS})}\,\frac{C_D^2(100\,\mathrm{fF})}{\tau(\mathrm{ns})}$$



Noise in a pixel/strip detector (ionisation detector)

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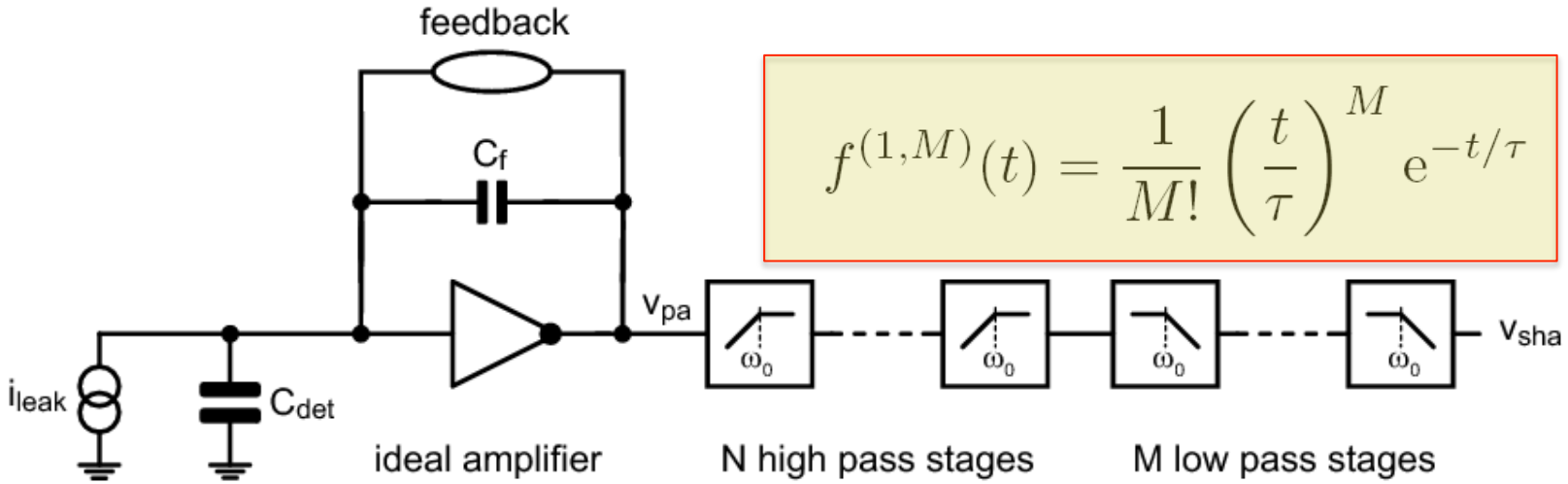
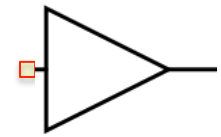
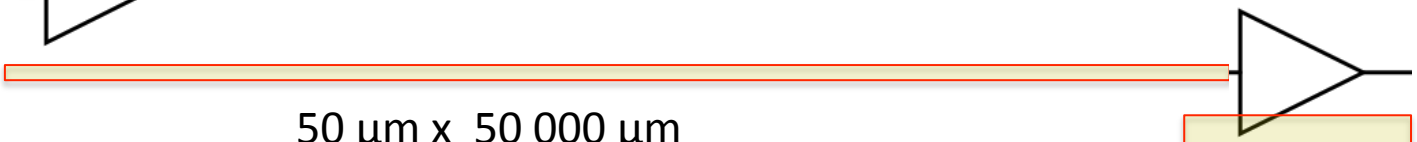


$$f^{(1,M)}(t) = \frac{1}{M!}\left(\frac{t}{\tau}\right)^{M} e^{-t/\tau}$$

comparing pixels and strips



50 x 250 µm² or 100 x 150 µm²



50 µm x 50 000 µm

	C_D	I_0	τ	W	L	g_m	ENC therm	ENC 1/f	ENC shot	ENC tot
pixel	200 fF	1 nA	50 ns	20 µm	0.5 µm	0.5 mS	25 e^-	17 e^-	24 e^-	**40 e^-**
strip	20 pF	1 µA	50 ns	2000 µm	0.4 µm	5 mS	800 e^-	200 e^-	750 e^-	**1100 e^-**

Signal/Noise in a pixel detector

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- typical figures for an LHC pixel detector

- Noise = 150 e^- initially
  200 e^- after 10 years @ LHC
- Signal = 20000 e^- total charge in 250 µm Si
  13000 e^- including charge sharing
  6000 – 8000 e^- after 10 yrs @ LHC

- S/N > 30

The typical S/N situation (... here ATLAS)

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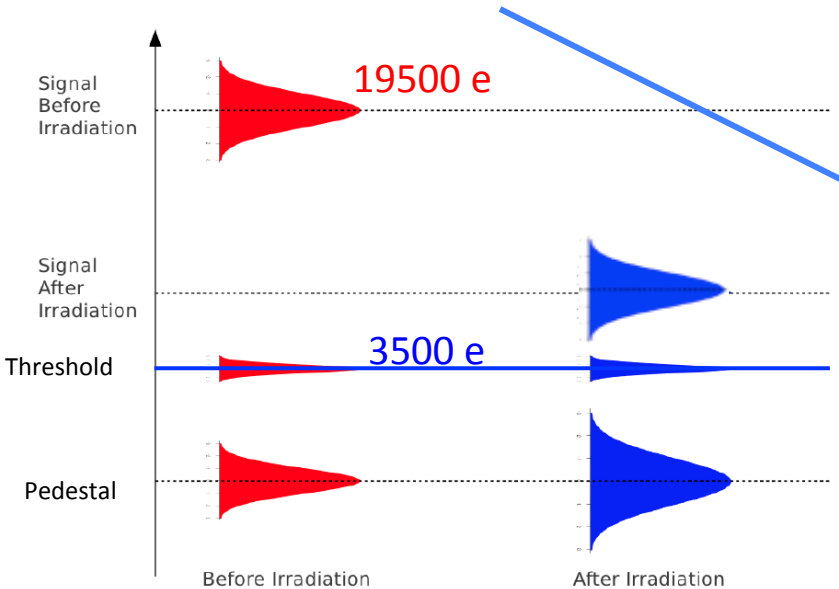
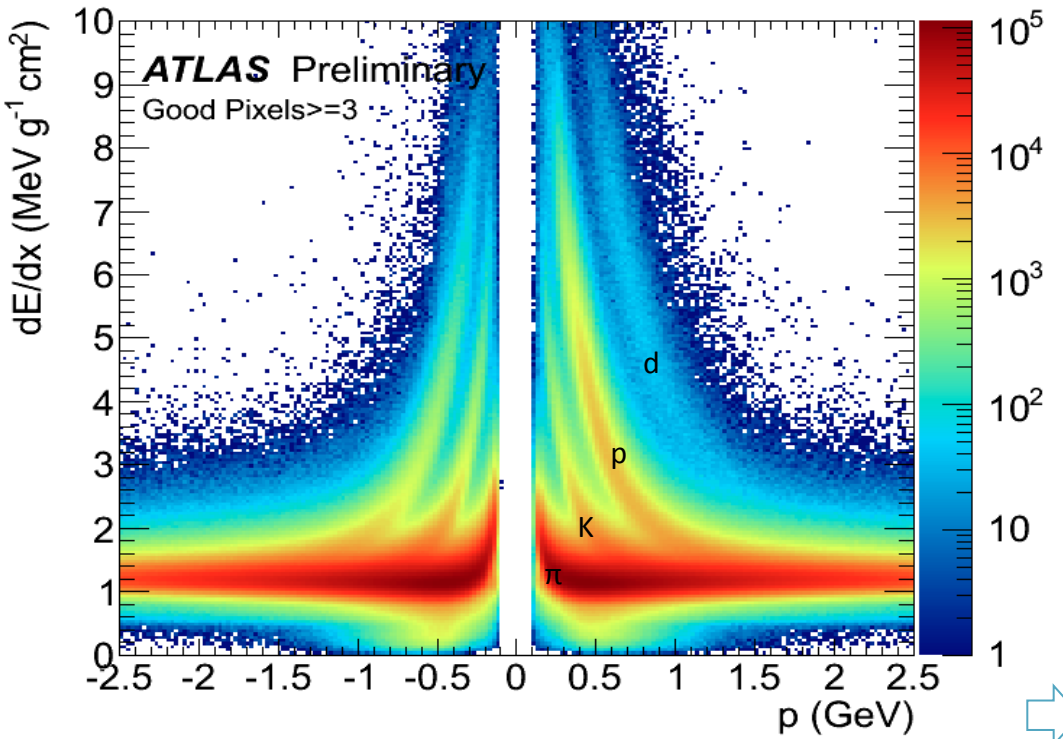
Signal of a high energy particle ≙ 19500 e^- → <10000 e^- after irradiation

Charge on more than 1 pixel => S/N > 30 → S/N ~ 10

- Discriminator thresholds = 3500 e, ~40 e spread, ~170 e noise
- 99.8% data taking efficiency
- 95.9% of detector operational
- ca. 10 µm x 100 µm resolution (track angle dependent)
- 12% dE/dx resolution

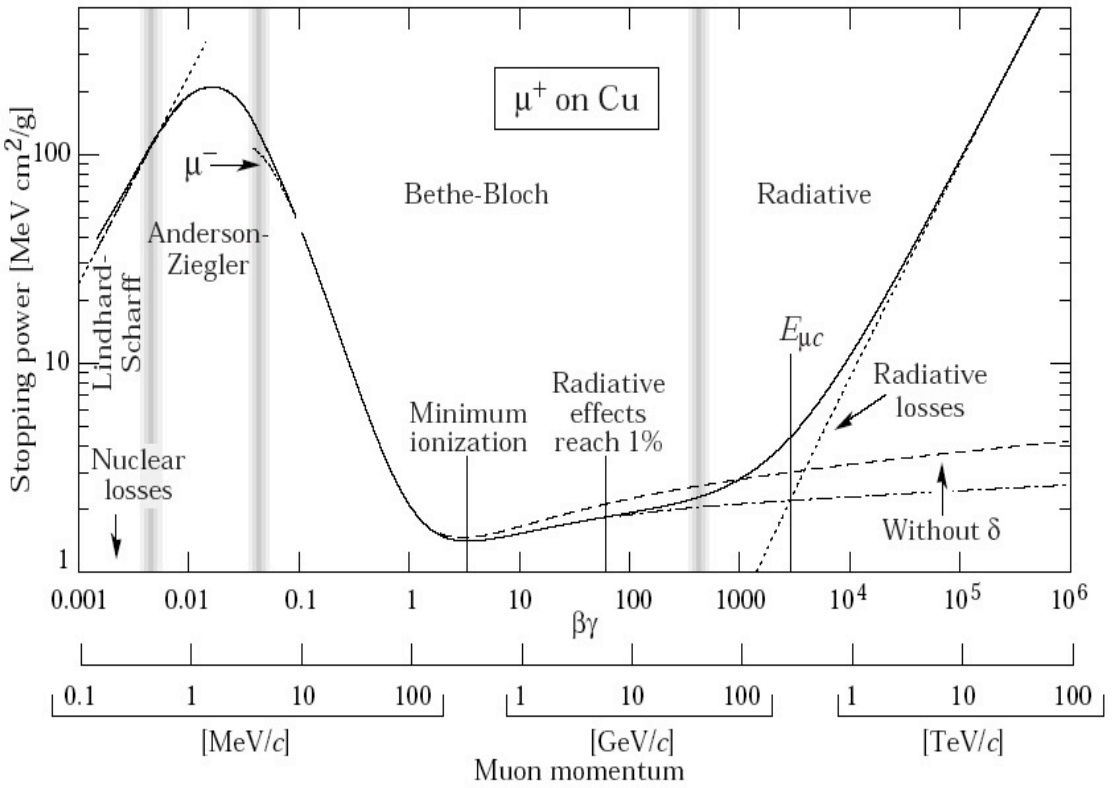




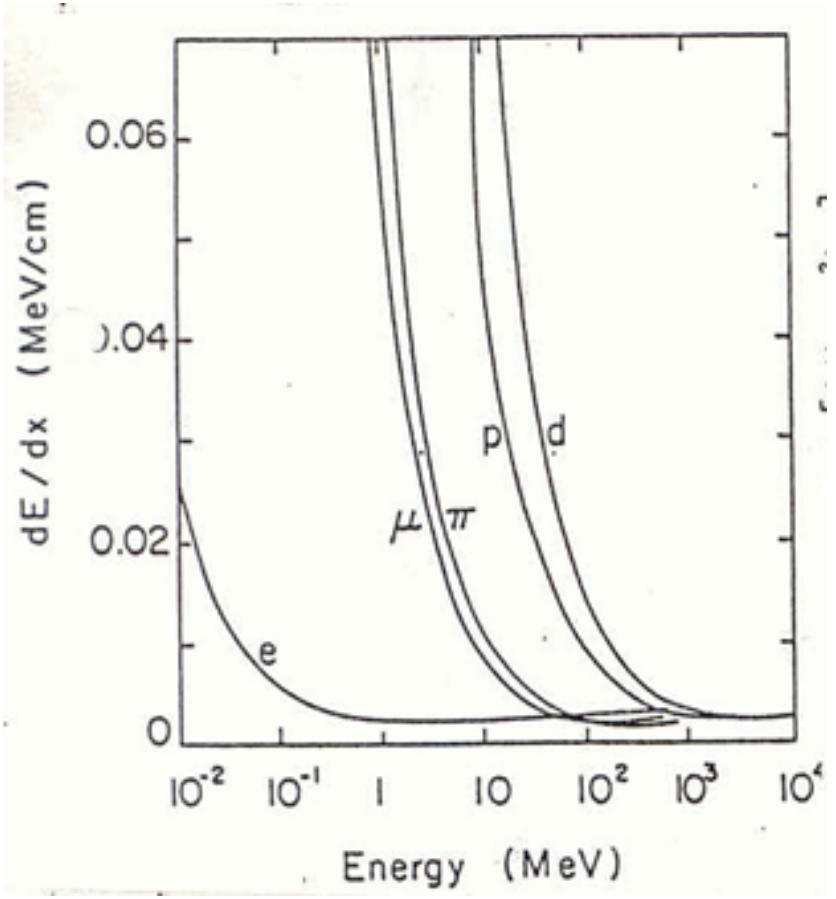
C. Gemme et al., ATLAS-CONF-2011-016

move to noise
skip dE/dx

Particle Identification by dE/dx



$$\beta\gamma = \frac{p}{E}\frac{E}{m} = \frac{p}{m}$$



possibility to identify different particles when E or p is known

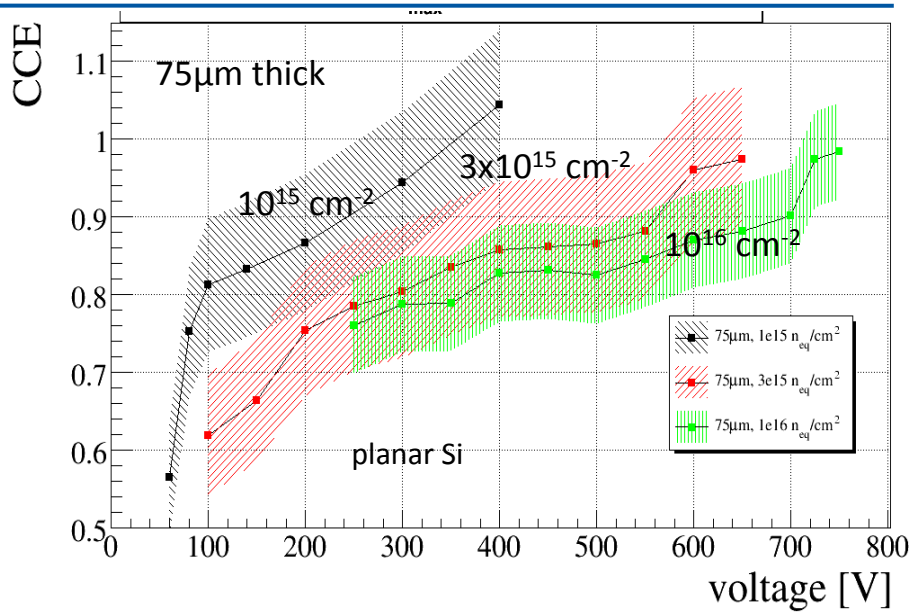
→ particle identification by dE/dx

How to make things better?

How to make sensors more radiation hard

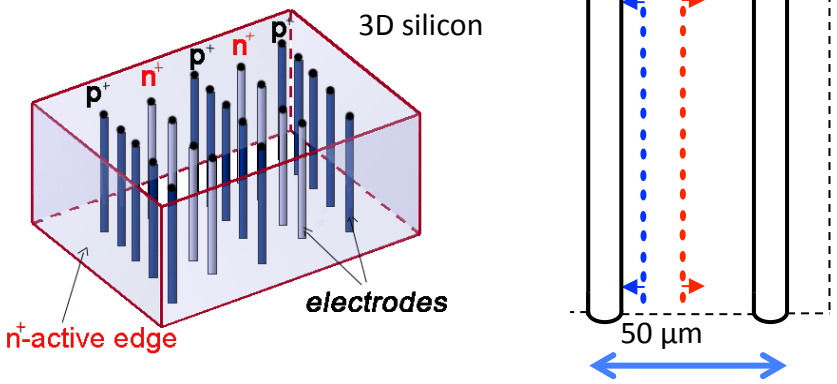
Planar sensors: (PPS collab.)

- work at 2x10^{16} n_{eq}/cm^2
- but need high bias voltage
- n in n (inner), n in p (outer layers)
- slim edges (guard ring optimization)



3D-Si sensors: (3D-Si collab.) → special geometry

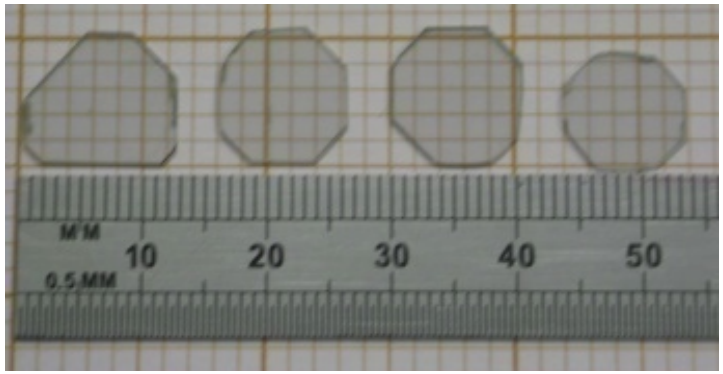
- 50 µm electrode spacing → V_{bias} ~200 V only
- option for inner layers



Diamond sensors: (RD42 & DBM collab)

- ~2000e at 2x10^{16} n_{eq} cm^2 → need low thresh.
- but S/N potentially better than Si at high fluence
- option for inner layers

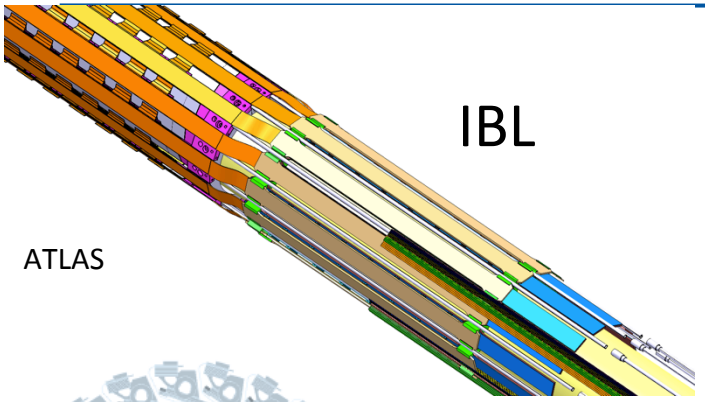
mono-crystalline CVD diamond



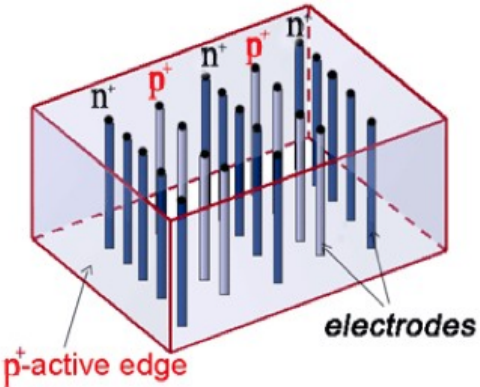
current focus on poly-crystalline pixel modules (ATLAS DBM)

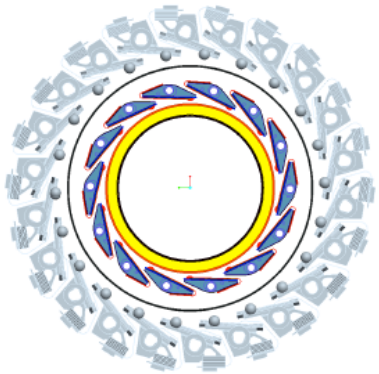
skip 3D and CVD?

LHC upgrades .... ATLAS IBL (installed 5/2014)



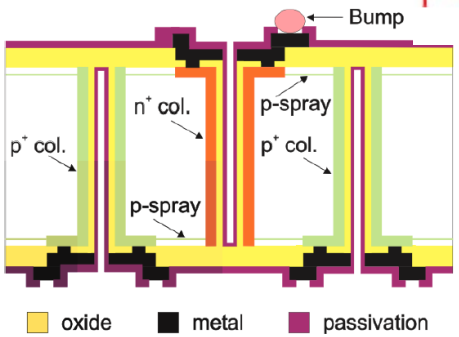
25% 3D Si sensors
75% planar Si

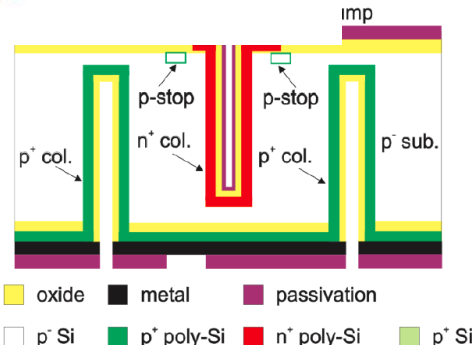


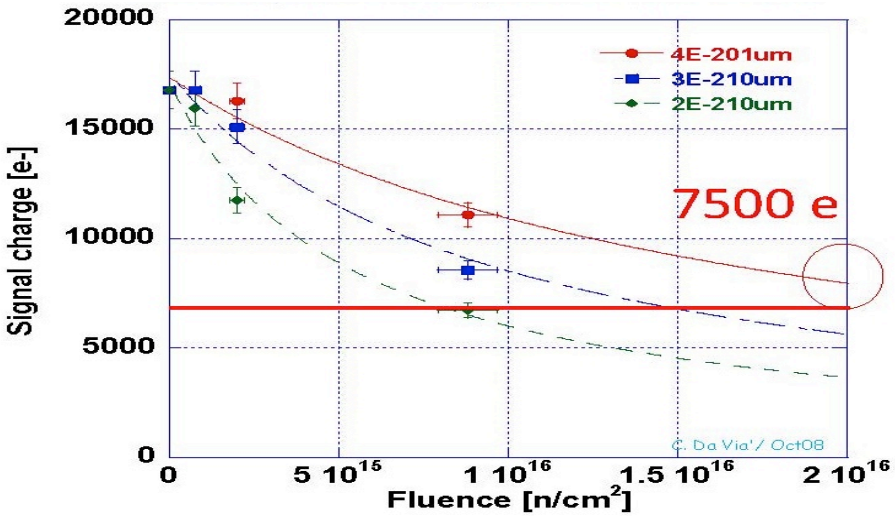


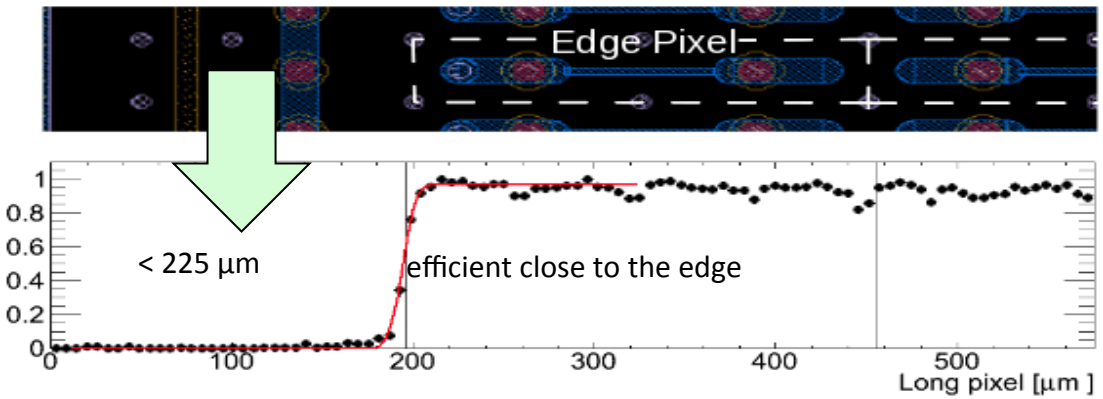
- low bias voltage
- small drift distance

=> radiation harder









CVD diamond as a sensor material

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property	diamond	Si
band gap [eV]	5.47	1.12
breakdown field [V/cm]	10^7	3×10^5
resistivity [Ω cm]	$>10^{15}$	2.3×10^5
intrinsic carrier density [cm^{-3}]	$<10^3$	1.5×10^{10}
mass density [g cm^{-3}]	3.52	2.33
atomic charge	6	14
dielectric constant	5.7	11.9
displacement energy [eV/atom]	43	13–20
energy to create e–h pair [eV]	13	3.6
radiation length [cm]	12.2	9.4
avg. signal created/µm [e]	36	89
avg. signal created/0.1% rad. length X_0 [e]	4400	8400

Diamond is

- "newer" … pCVD … scCVD not in large quantities …
- has no leakage current, smaller C_{det}
  … has nice thermal features
- has lower minmium displacement energy => radiation harder
- to be traded off against a ~2.5x smaller signal (unirr. 36e/µm)

DBM – Diamond Beam Monitor

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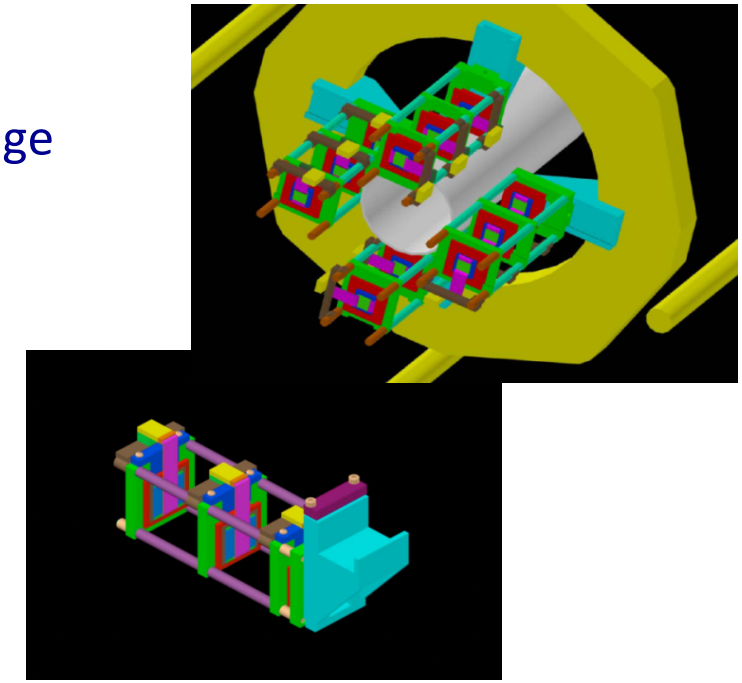
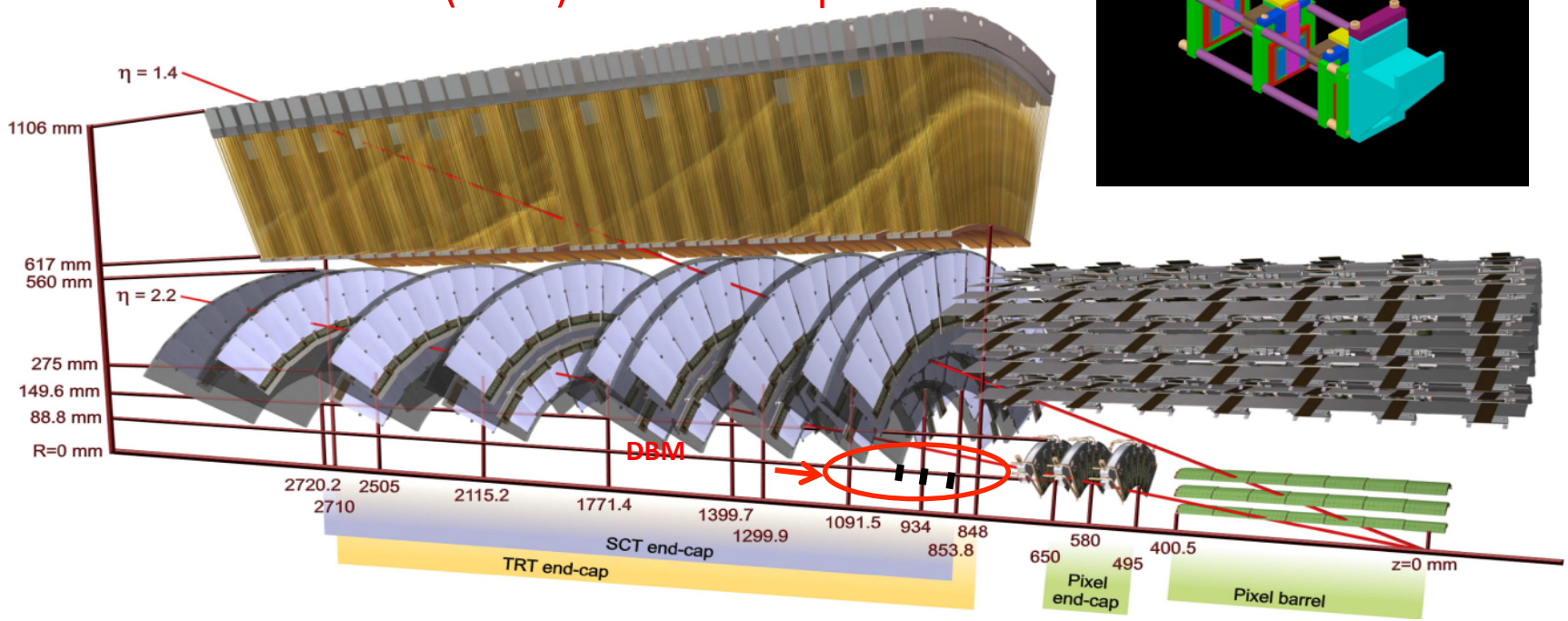
- radiation hard due to
  - 5x larger band gap than Si ⇒ no leakage current
  - strong lattice (x2 stronger than Si) ⇒ less NIEL damage
- low Z
- first pixel use in ATLAS:
  Diamond Beam Monitor (DBM) – 24 telescopes





Hybrid Pixel Detectors @ LHC: PROs and CONs

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- complex signal processing already in pixel cells possible
  - zero suppression
  - temporary storage of hits during L1 latency
- radiation hardness to 10^{15} n_{eq}/cm^2
- spatial resolution ~ 10 – 15 µm

PRO

… but also

- relatively large material budget: ~ 3% X_0 per layer (1% X_0 @ ALICE)
  - cooling, services
- complex and laborious module production
  - bump-bonding / flip-chip → expensive
  - many production steps
  - expensive

CON

Rate and radiation challenges at the innermost pixel layers

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Hybrid Pixels

	BX time	Particle Rate	Fluence	Ion. Dose
	ns	kHz/mm^2	n_{eq}/cm^2 per lifetime*	Mrad per lifetime*
LHC (10^{34} cm^{-2}s^{-1})	25	1000	2×10^{15}	79
HL-LHC (10^{35} cm^{-2}s^{-1})	25	10000	2×10^{16}	> 500
LHC Heavy Ions (6×10^{27} cm^{-2} s^{-1})	20.000	10	$>10^{13}$	0.7
RHIC (8×10^{27} cm^{-2}s^{-1})	110	3,8	few 10^{12}	0.2
SuperKEKB (10^{35} cm^{-2}s^{-1})	2	400	~3 x 10^{12}	10
ILC (10^{34} cm^{-2}s^{-1})	350	250	10^{12}	0.4

Monolithic Pixels

lower rates
lower radiation
smaller pixels
less material
better resolution

DEPFET: Belle II
MAPS: STAR@RHIC
and future
ALICE ITS

assumed lifetimes:
LHC, HL-LHC: 7 years
ILC: 10 years
others: 5 years

NEW developments

DEPFET Pixels -> Belle II

Monolithic Pixels -> STAR@RHIC, ALICE

(Mixed) monolithic/hybrid -> LHC Upgrade?

(Semi)-Monolithic Pixel Detector Projects

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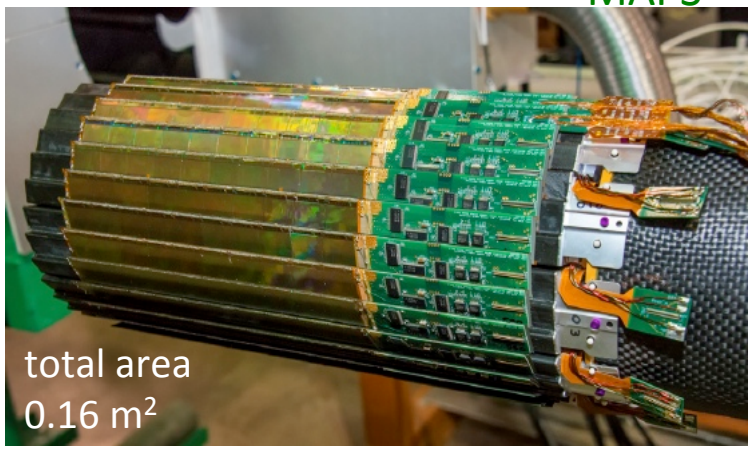
STAR / RHIC

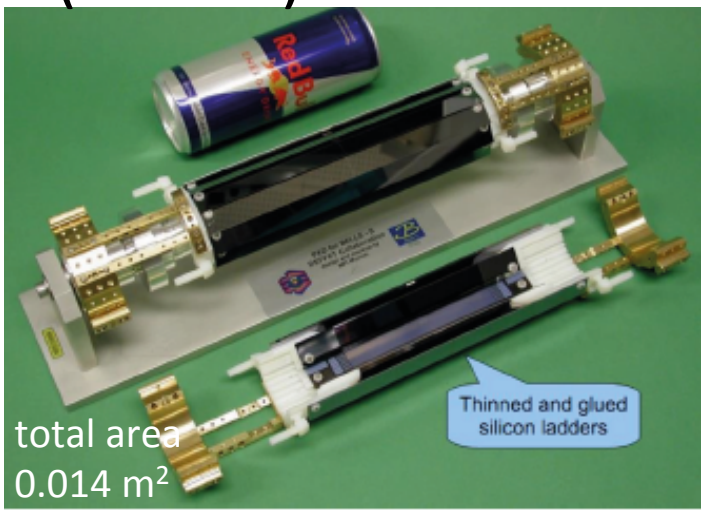
MAPS



in operation since 2014

(Belle II)

DEPFET

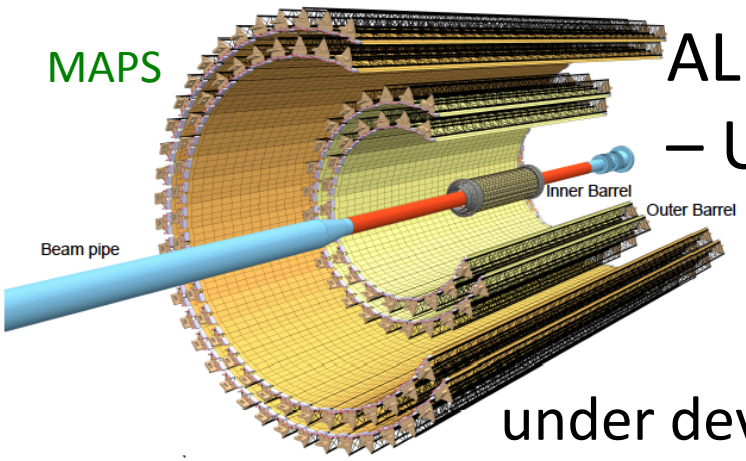


in production for 2017

(talk by C. Marinas on Wednesday)

ALICE – Upgrade

MAPS

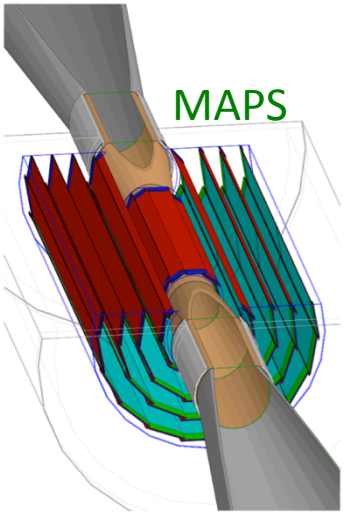


total area
~10 m²

under development
target: 2018

ILC

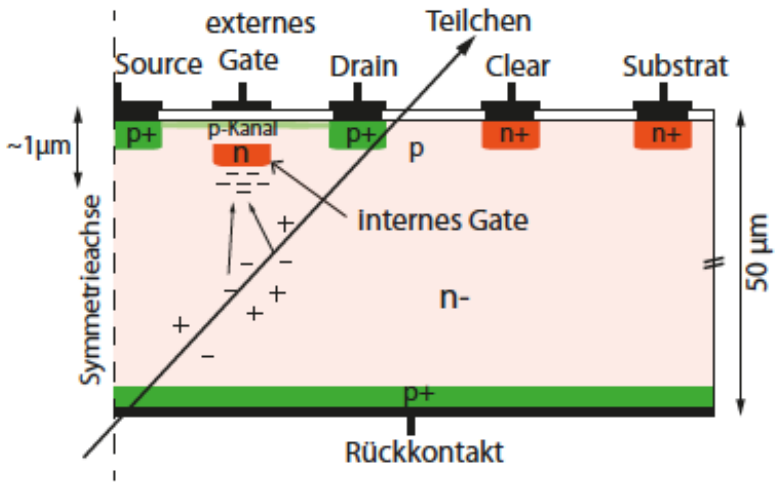
MAPS

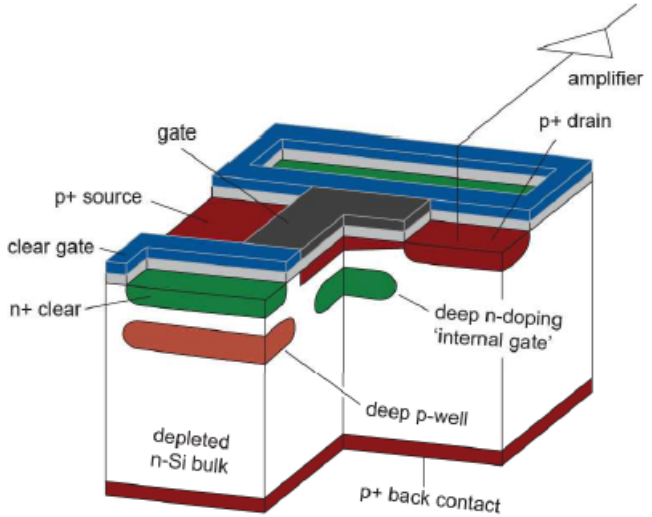


total area
? m²

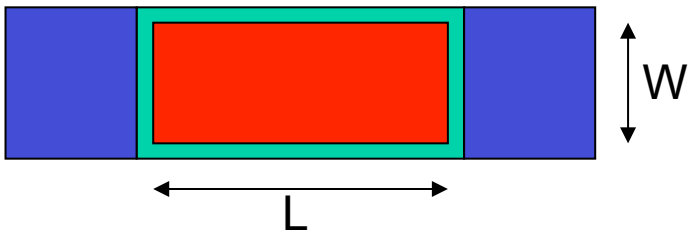
current baseline

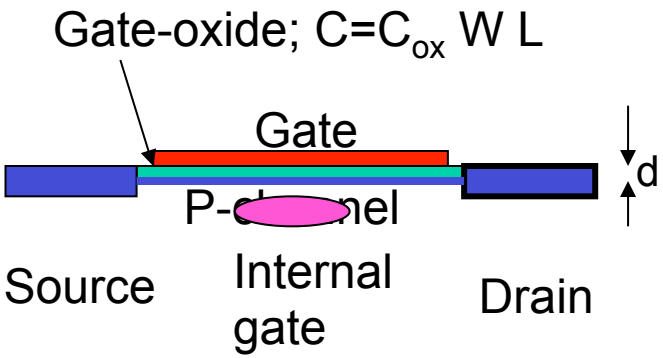
DEPFET Pixels





How does a DEPFET work?





A charge q in the internal gate induces a mirror charge αq in the channel (α <1 due to stray capacitance). This mirror charge is compensated by a change of the gate voltage: $\Delta V = \alpha\, q / C = \alpha\, q / (C_{ox}\, W\, L)$ which in turn changes the transistor current I_d .

q

FET in saturation:

$$I_d = \frac{W}{2L}\mu C_{ox}\left(V_G + \frac{\alpha q_s}{C_{ox}WL} - V_{th}\right)^2$$

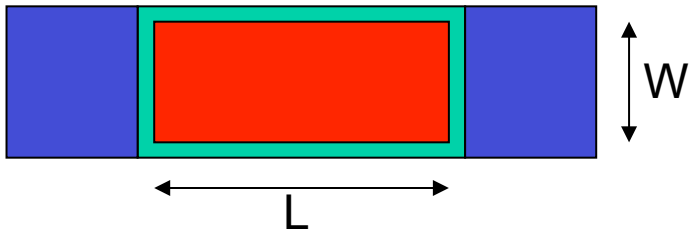
I_d: source-drain current
C_{ox}: sheet capacitance of gate oxide
W,L: Gate width and length
μ: mobility (p-channel: holes)
V_g: gate voltage
V_{th}: threshold voltage

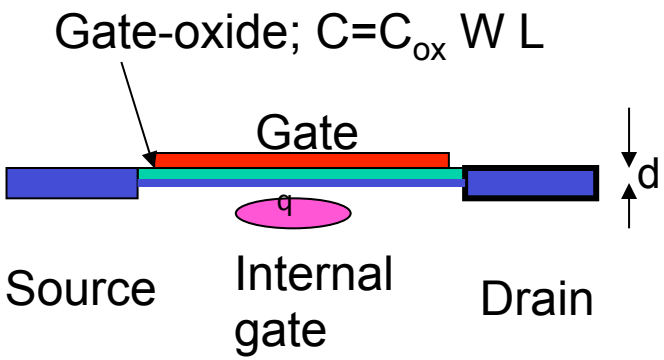
Conversion factor:

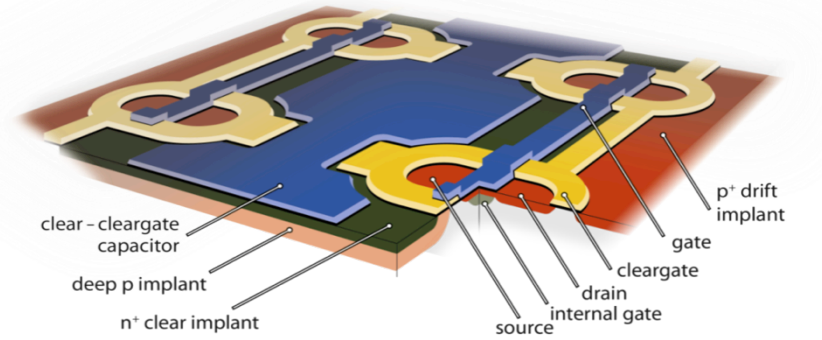
$$g_q = \frac{dI_d}{dq_s} = \frac{\alpha\mu}{L^2}\left(V_G + \frac{\alpha q_s}{C_{ox}WL} - V_{th}\right) = \alpha\sqrt{2\frac{I_d\mu}{L^3 W C_{ox}}}$$

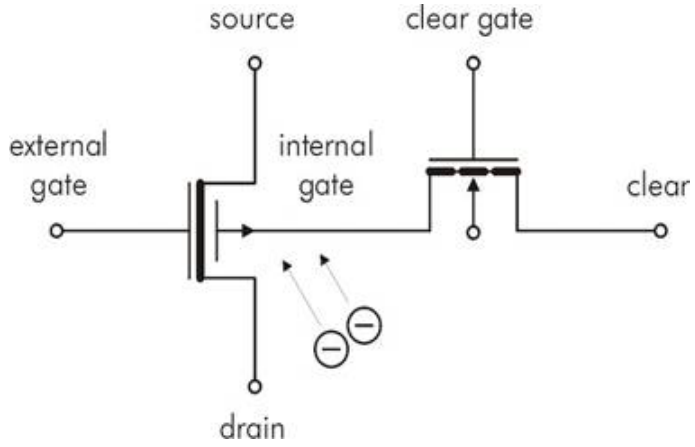
$$g_m : g_q = \alpha\frac{g_m}{WLC_{ox}} = \alpha\frac{g_m}{C}$$

How does a DEPFET work?









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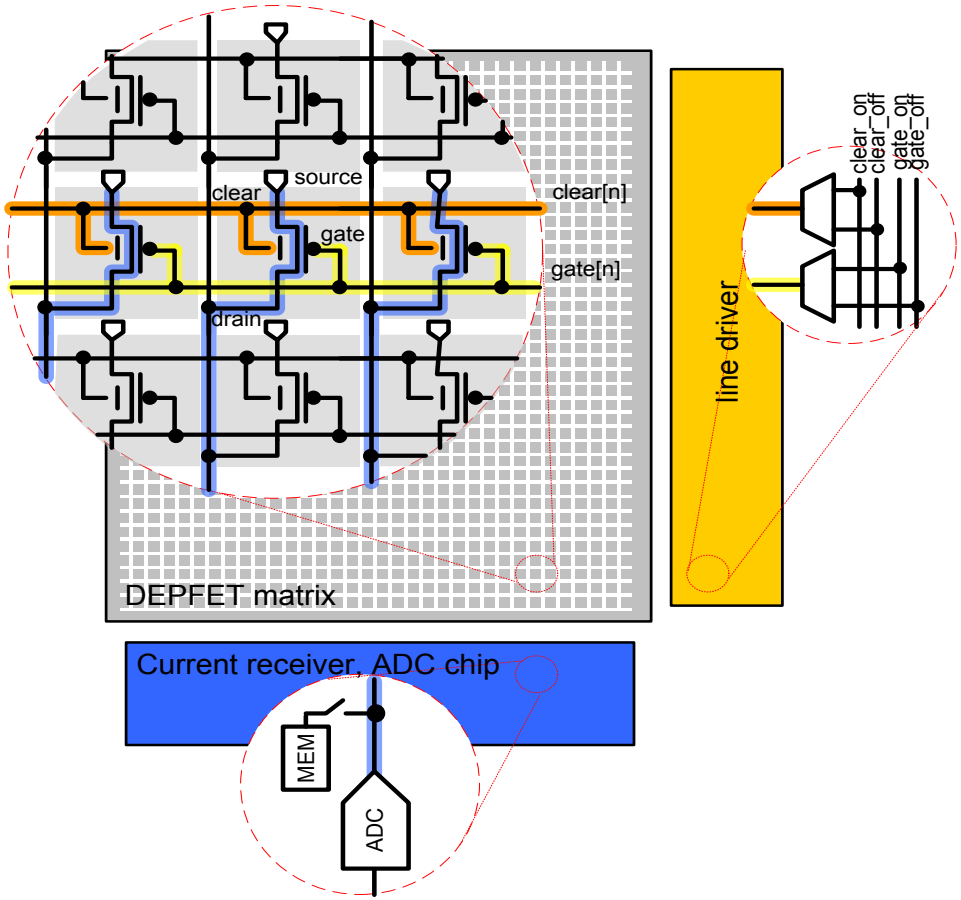
- Internal amplification g_q~ 500 pA/e$^-$
- Small intrinsic noise
- Sensitive off-state, no power consumption

DEPFET pixel array



- DEPFET pixel transistors arranged in a matrix
- row wise select -> column wise readout of transistor (drain) currents
- Gate and clear lines need a steering chip
- Long drain readout lines to keep material out of the acceptance region
- 100 ns per row
  20 µs per frame

DEPFET PXD ... very different from LHC pixels

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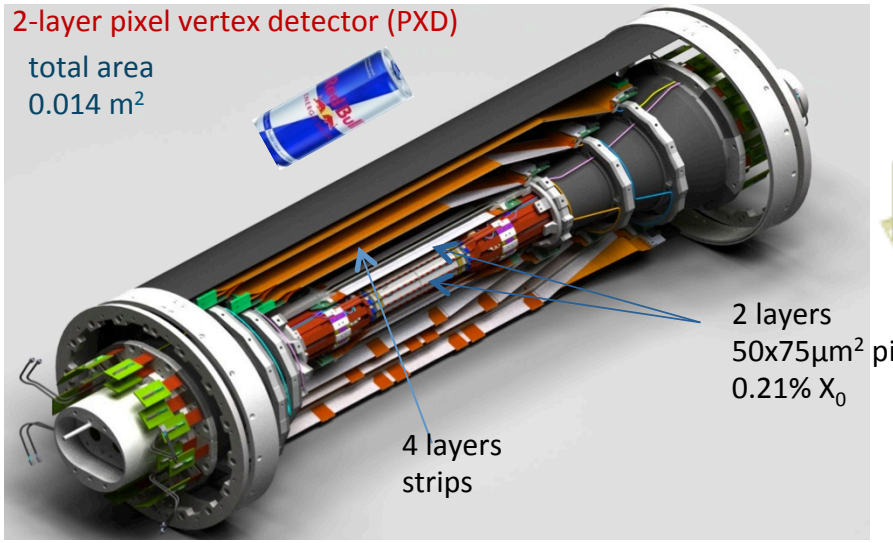
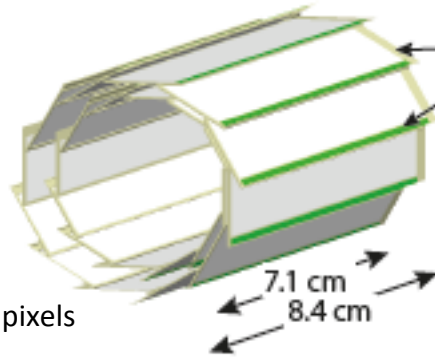
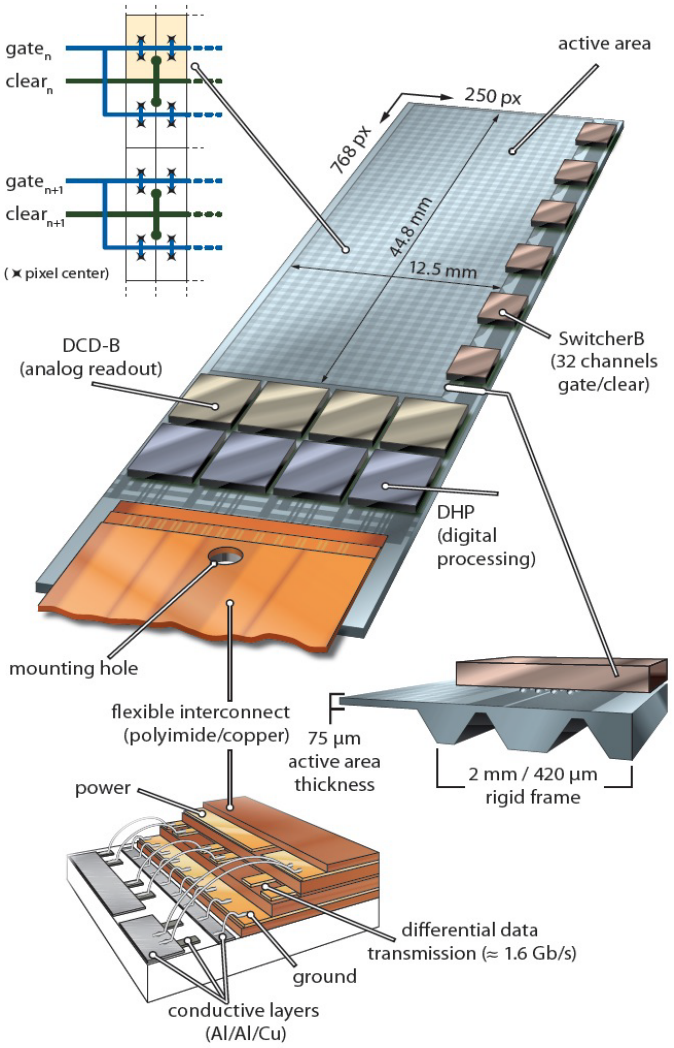


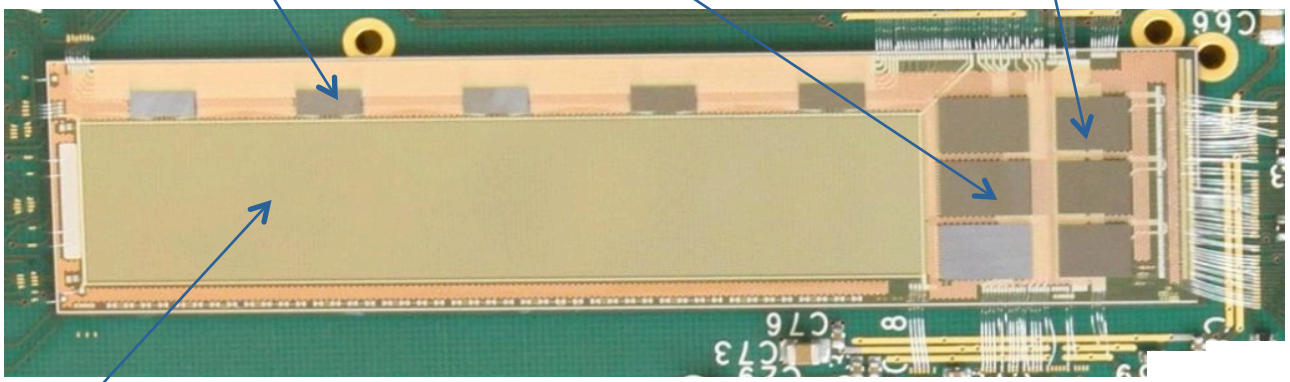




switcher chips

current digitizer chips

data processing chips

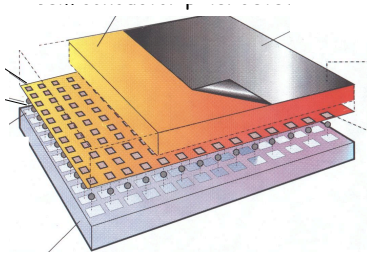


DEPFET sensor

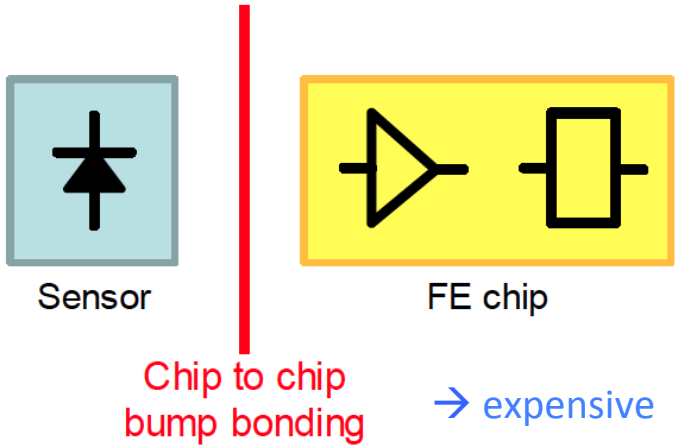
CMOS Pixels (sometimes called MAPS)

skip ?

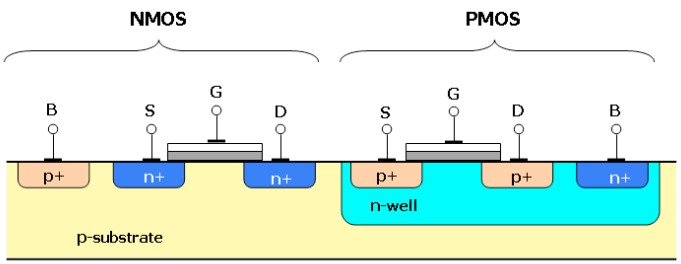
From HYBRID to (more) monolithic …

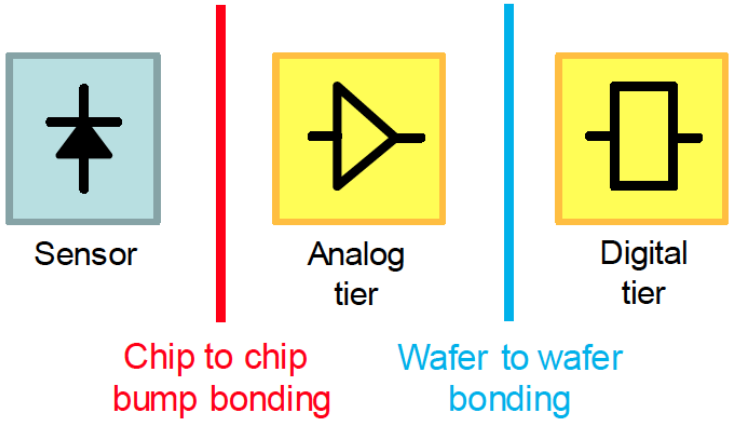


- standard HYBRID pixels
  - various sensors: planar-Si, 3D-Si, diamond
  - mixed signal R/O chip (FE-I3, FE-I4, ROC …)



- 3D integration of CMOS Tiers
  - separate analog / digital / opto
  - FE-TC4 (Tezzaron/Chartered)





A classification ... from HYBRID to new challenges

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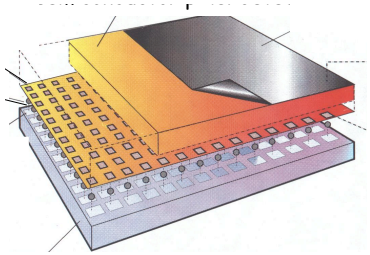
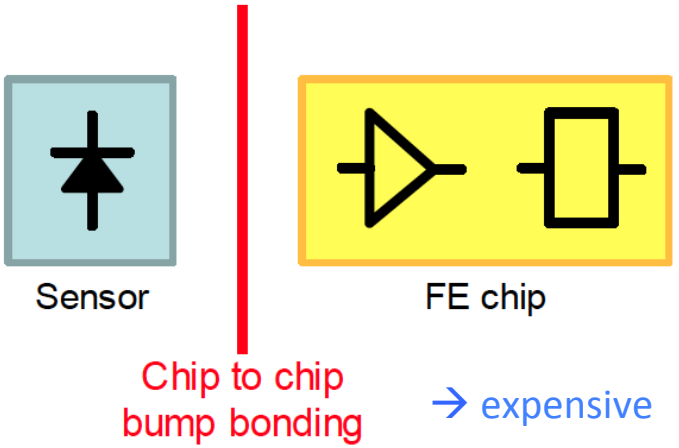
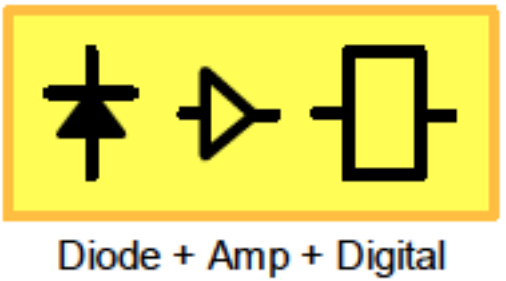


- standard HYBRID pixels
  - various sensors: planar-Si, 3D-Si, diamond
  - mixed signal R/O chip (FE-I3, FE-I4, ROC ...)



- Monolithic Active Pixel Sensors
  - MAPS using CMOS with Q-collection in epi-layer (usually by diffusion → recent advances)
  - depleted DMAPS using HR substrate or HV process to create depletion region: $d \sim \sqrt{\rho \cdot V}$
  - CMOS on SOI



A classification ... from HYBRID to new challenges

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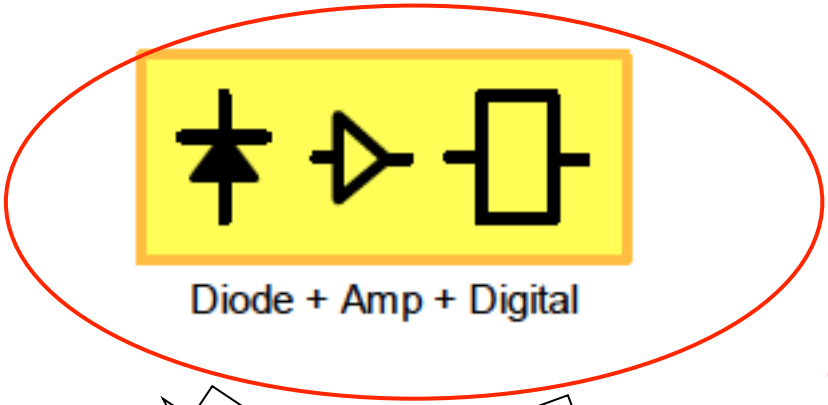
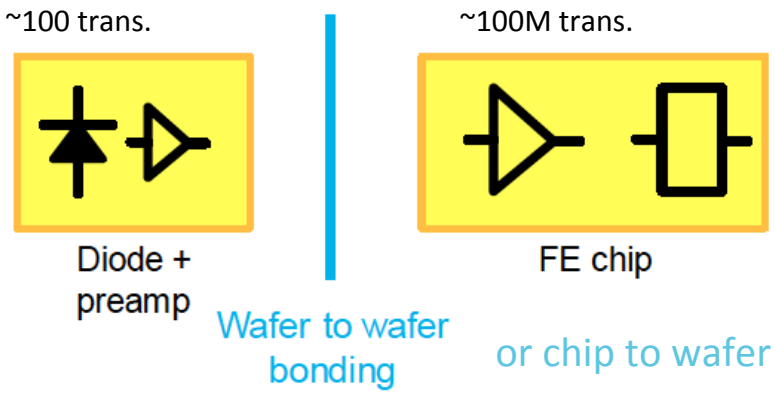
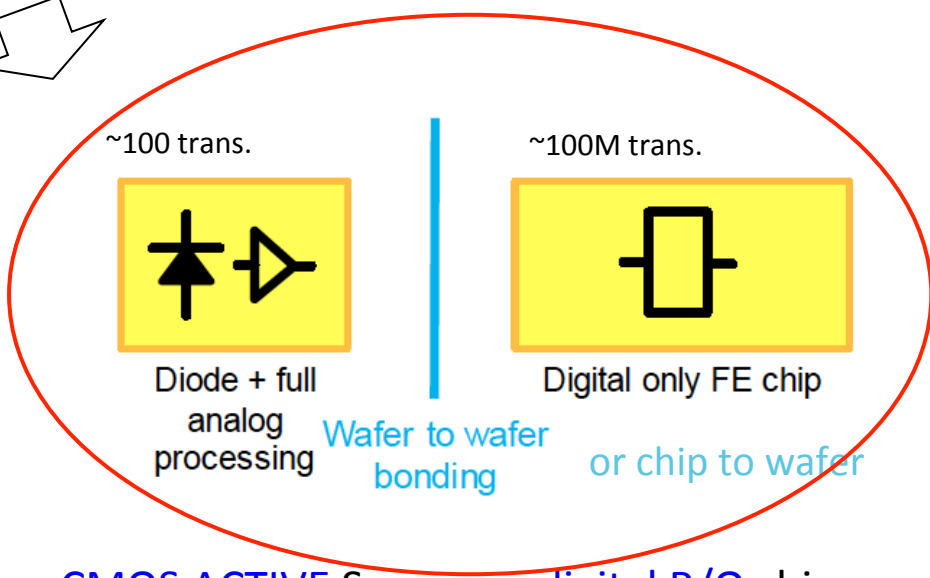
- (D)MAPS



attractive for
low momenta (thin),
imaging applications
also, but challenging, for
LHC

attractive for LHC



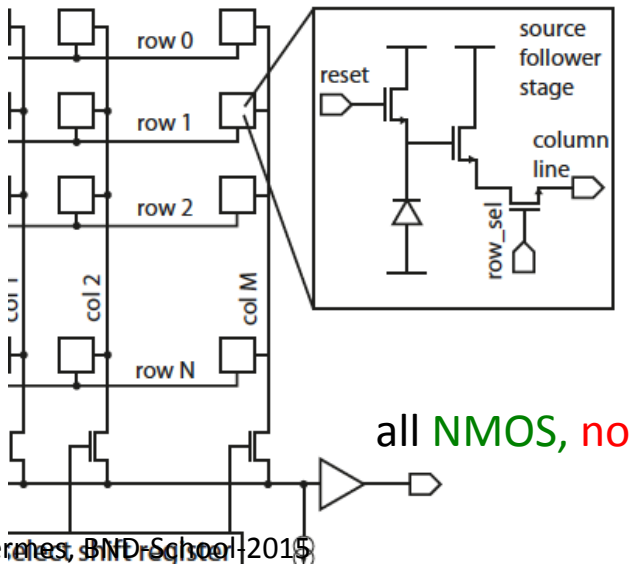


- HYBRID pixels using "active" sensors
  - 8" HV or HR sensor w/ few transistors
  - (voltage) signal coupled to R/O-chip
- DEPFET pixels (one in-pixel transistor)

- CMOS ACTIVE Sensors + digital R/O chip
  - HR or HV CMOS sensor with CSA+disc
  - dedicated digital R/O chip

MAPS - epi

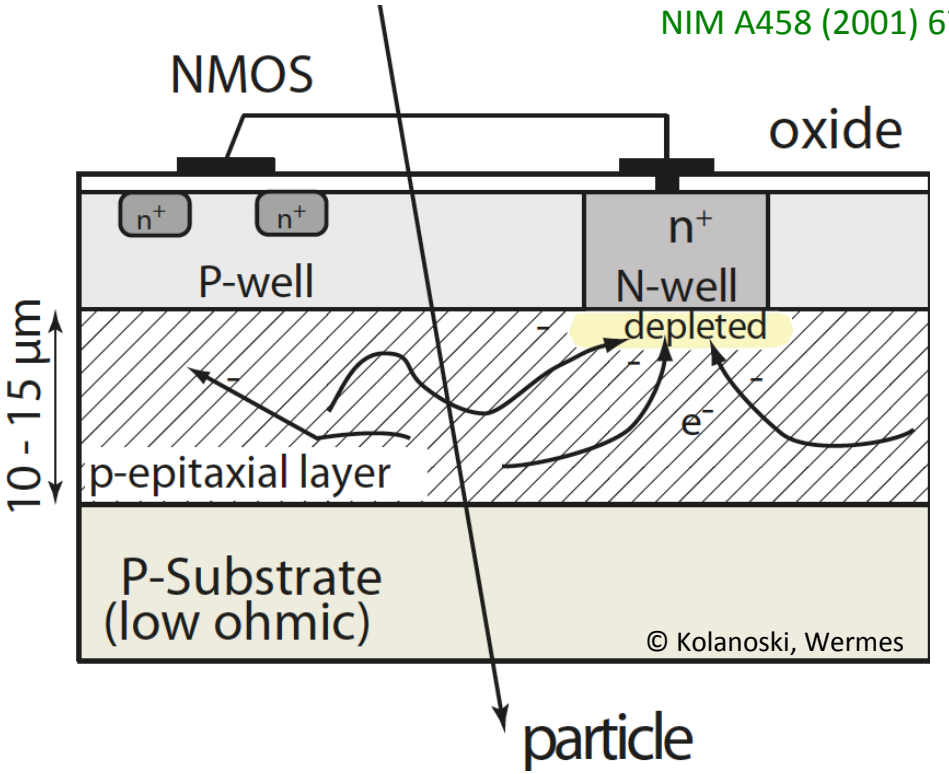
+ ‘standard CMOS’ process
+ fewer interconnections
+ very thin ... low mass
+ low power
+ small pixel size
+ CMOS circuitry, but limited to NMOS
− small signal
− slow charge collection
− frame readout, rolling shutter
− area limited by chip size
− radiation tolerance



all NMOS, no PMOS

CMOS with epi-layer as active layer

R. Turchetta et al
NIM A458 (2001) 677-689



- realized 2014
  in STAR experiment
- target for ALICE upgrade

MAPS – epi: PROBLEM

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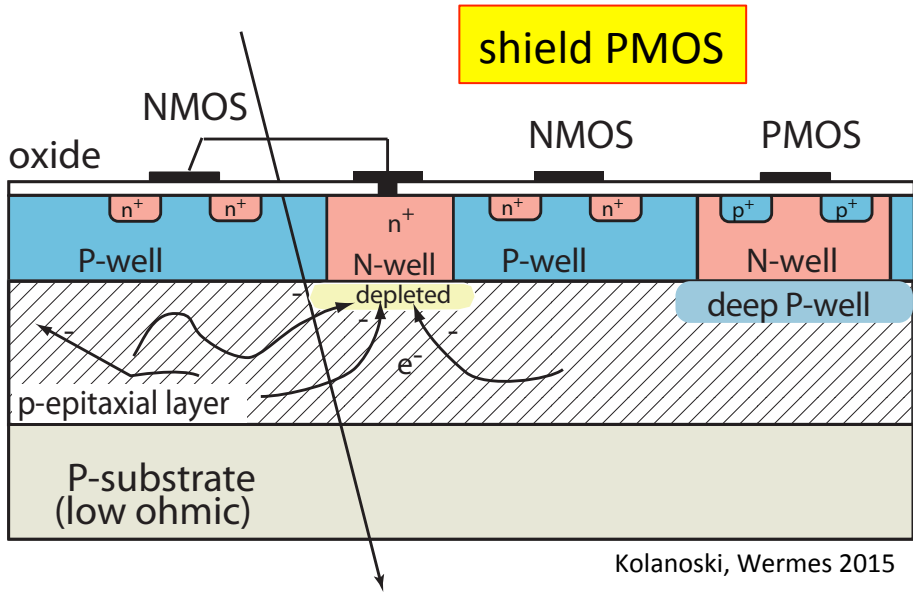
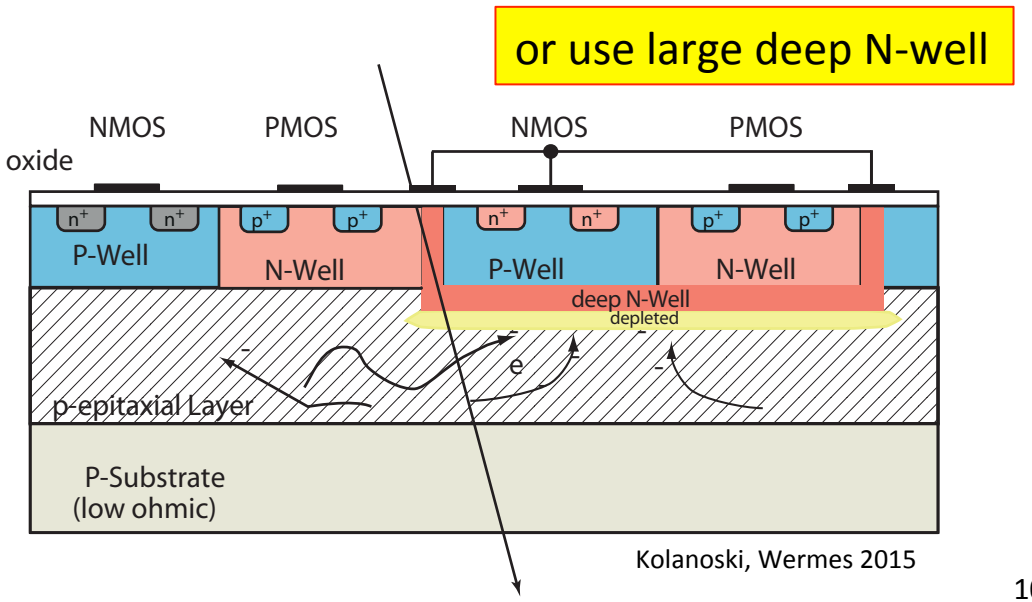
+ ‘standard CMOS’ process
+ fewer interconnections
+ very thin ... low mass
+ low power
+ small pixel size
+ CMOS circuitry, but limited to NMOS
– small signal
– slow charge collection
– frame readout, rolling shutter
– area limited by chip size
– radiation tolerance

skip HV/HR?



Kolanoski, Wermes 2015



Kolanoski, Wermes 2015

MAPS for ALICE (2018) and for the ILC (20xx?)

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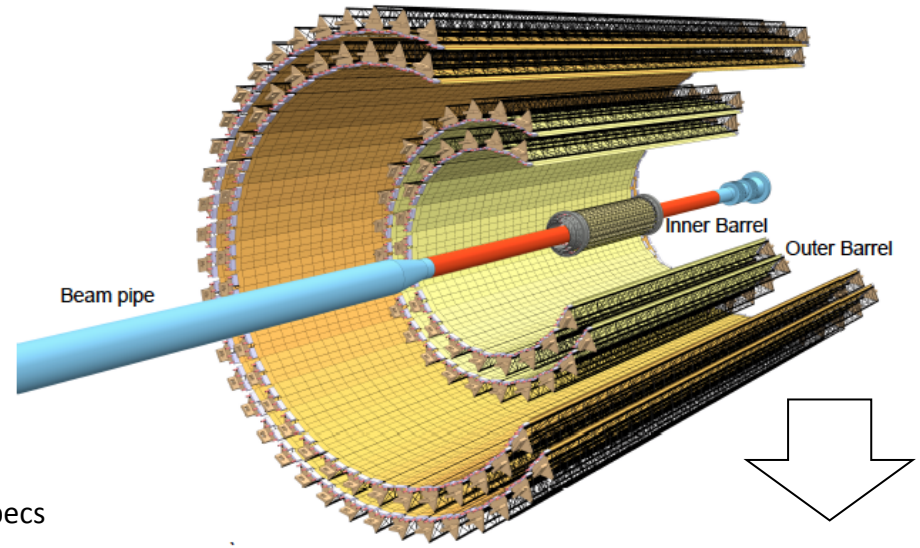
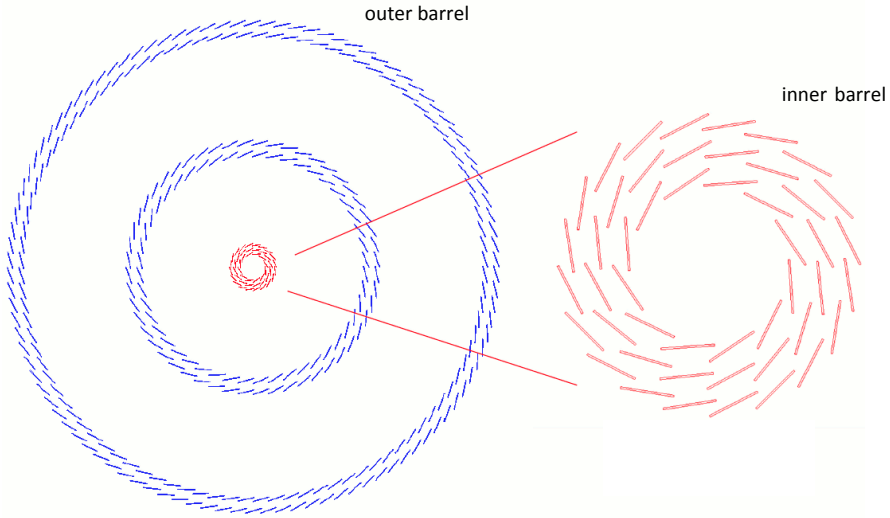
ALICE

10.7m²

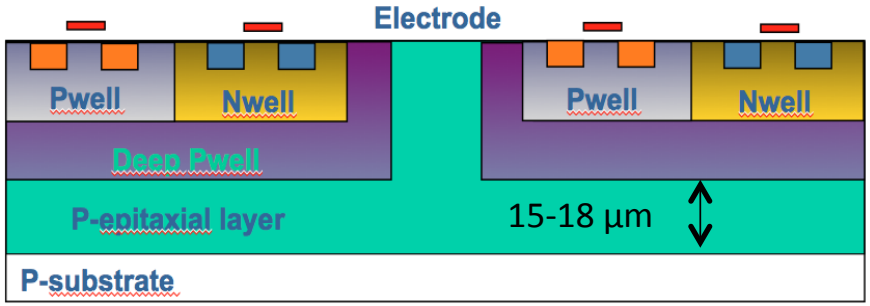




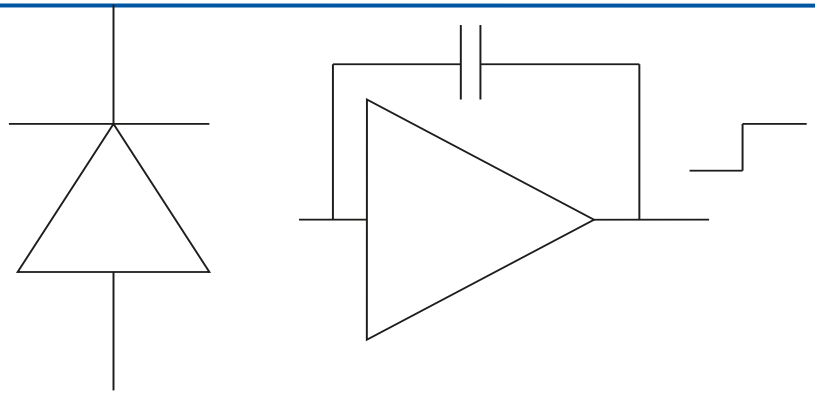
specs

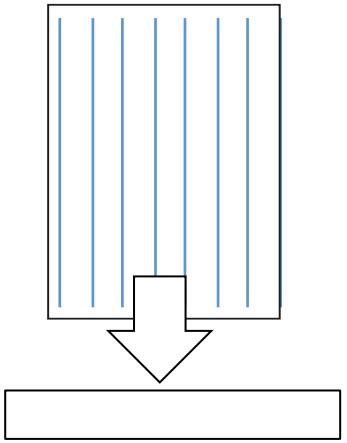
Parameter	Inner barrel	Outer barrel
Max. silicon thickness	50 µm	
Intrinsic spatial resolution	5 µm	30 µm
Chip size	15 mm × 30 mm ($r\phi \times z$)	
Max. dead area on chip	2 mm ($r\phi$), 25 µm (z)	
Max. power density	300 mW/cm²	100 mW/cm²
Max. integration time	30 µs	
Max. dead time	10 % at 50 kHz Pb–Pb	
Min. detection efficiency	99 %	
Max. fake hit rate	10^{-5}	
TID radiation hardness[a]	700 krad	10 krad
NIEL radiation hardness[a]	10^{13} 1 MeV n_{eq}/cm²	3×10^{10} 1 MeV n_{eq}/cm²

[a] This includes a safety factor of ten



And for LHC – upgrade? ...





pixel-
sensor

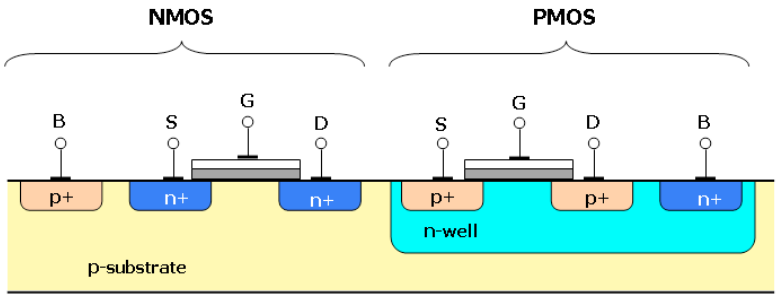
chip: pixel cell: amplifier,
discriminator ...
o(100) transistors

chip: column/region architecture
buffers, periphery ...
o(>100M) transistors ...
requires full CMOS
i.e. pMOS and nMOS in circuit

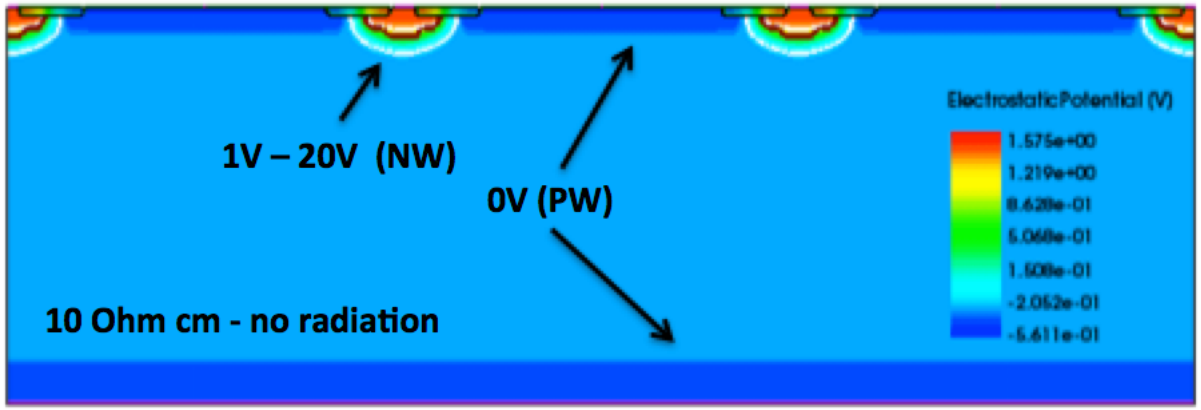
signal ∝ depletion depth

$$d \sim \sqrt{\rho \cdot V}$$

skip HV/HR?



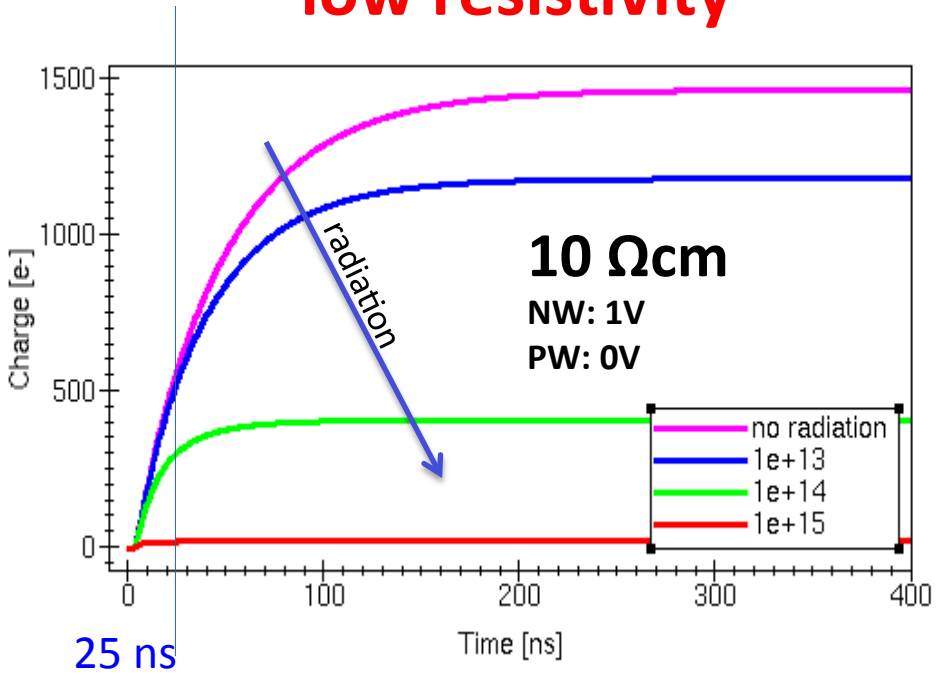
TCAD simulations: resistivity – voltage – fill factor



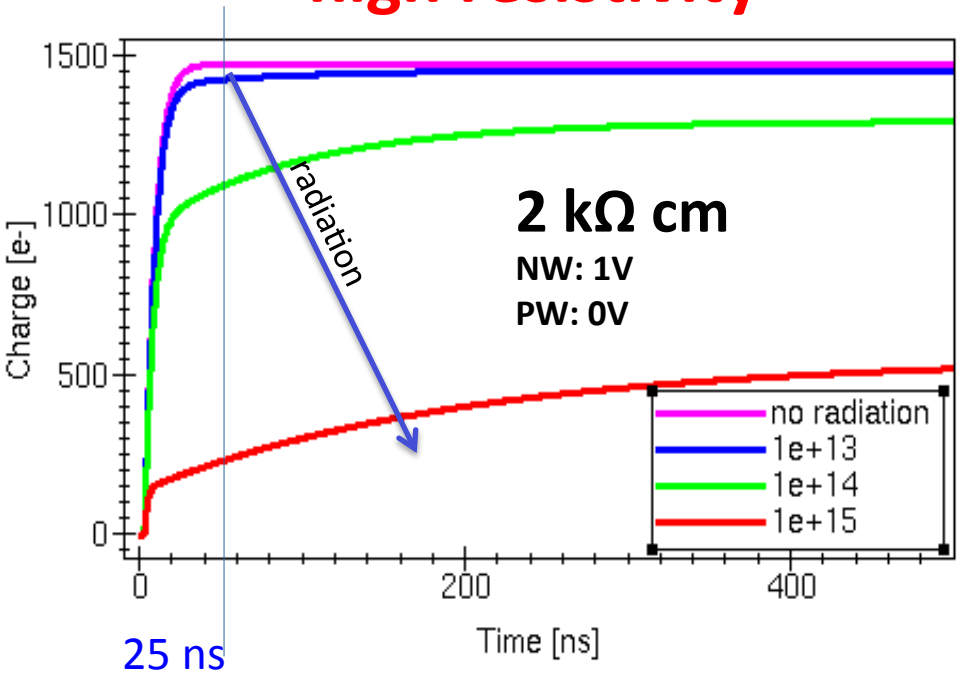
Substrate: 10 Ωcm – 2kΩ cm
Nwell: 1V – 20 V
Pwell: 0V

from Tomasz Hemperek

low resistivity



high resistivity



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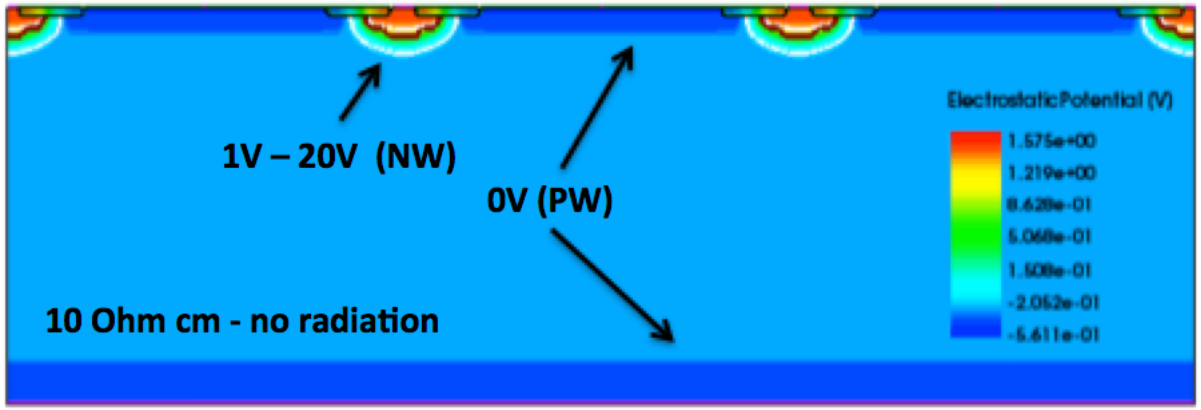

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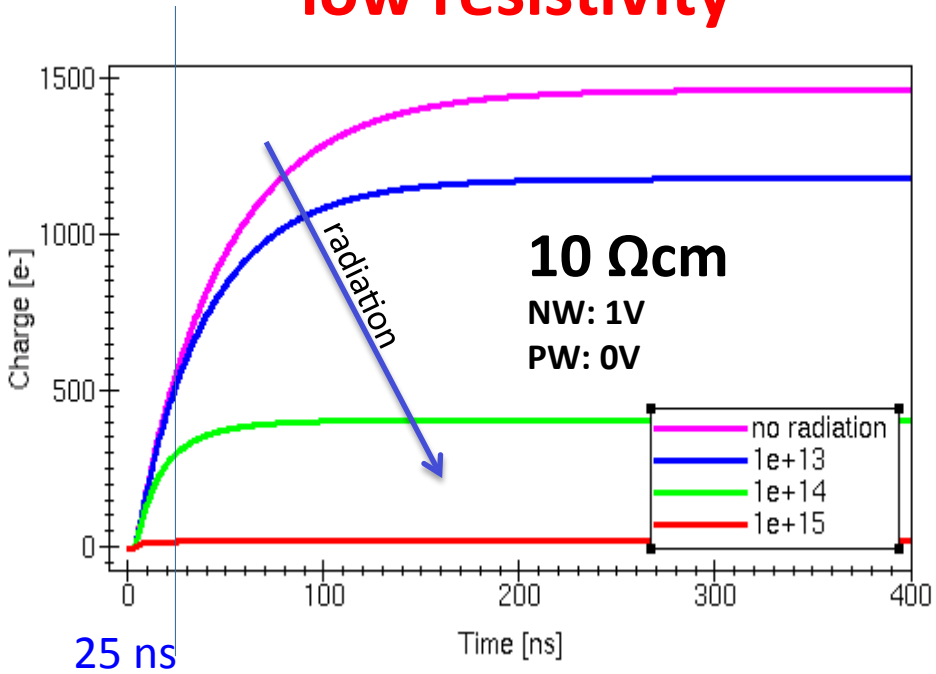
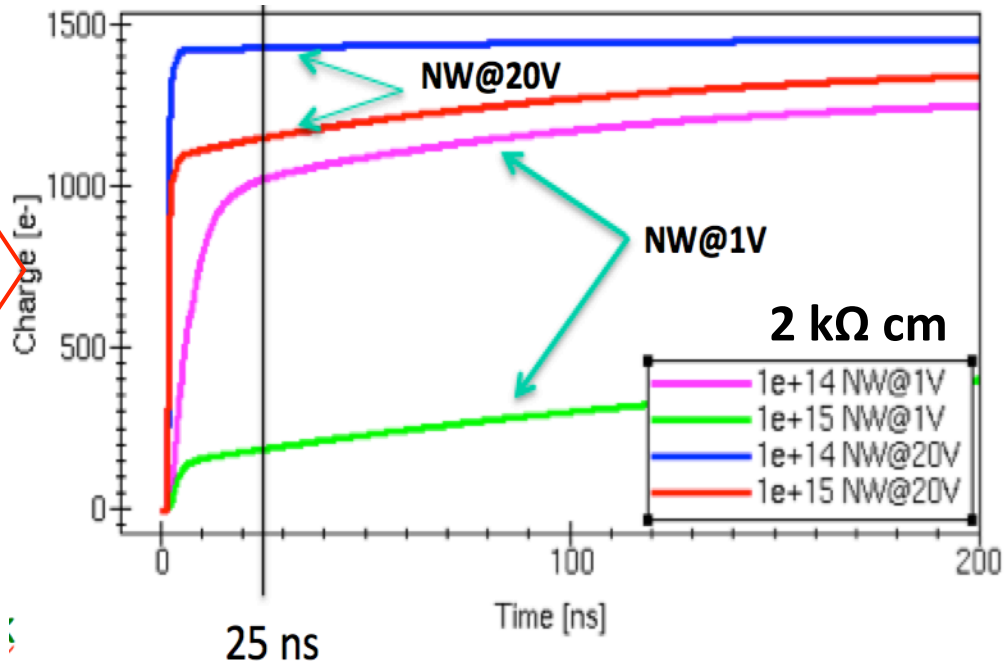


HR plus (high) voltage



Fill Factor influence: here at 10^{15} n_{eq}/cm^2

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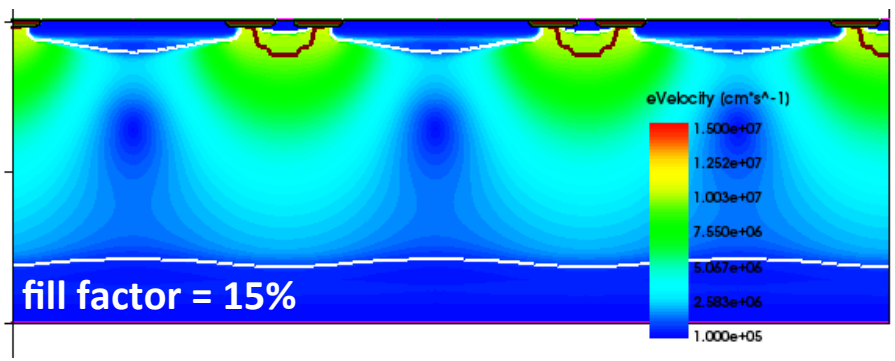
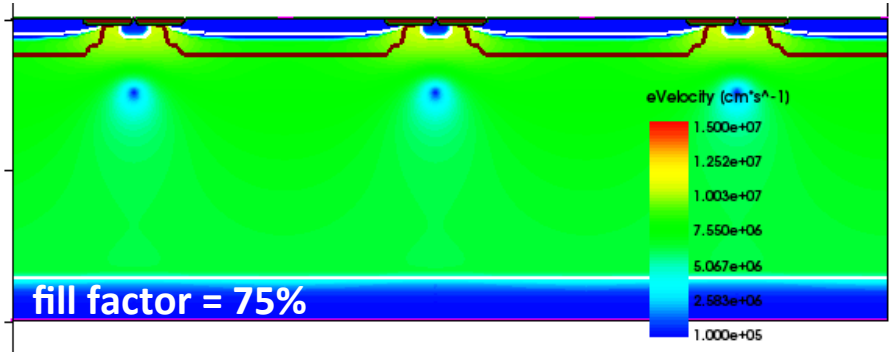
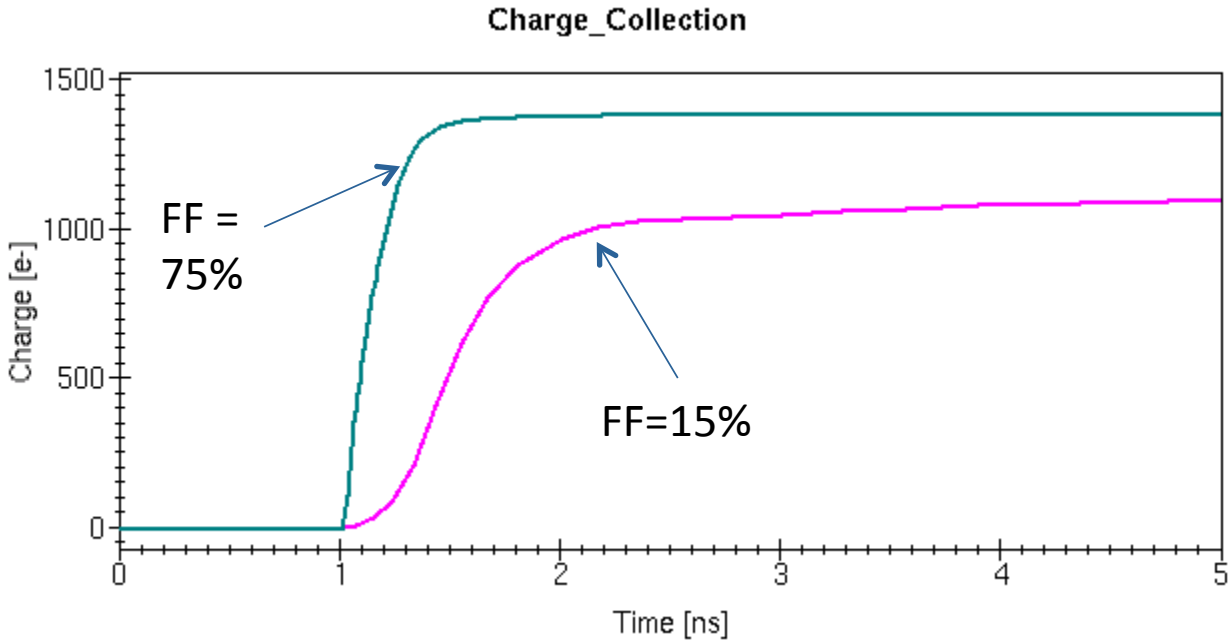
Electron Velocity







NW: 20V
PW: 0V
Substrate:2kΩ cm
Dose: 10^{15} n_{eq}/cm^2

Tomasz Hemperek

Summary: Resistivity, Voltage, Fill-Factor

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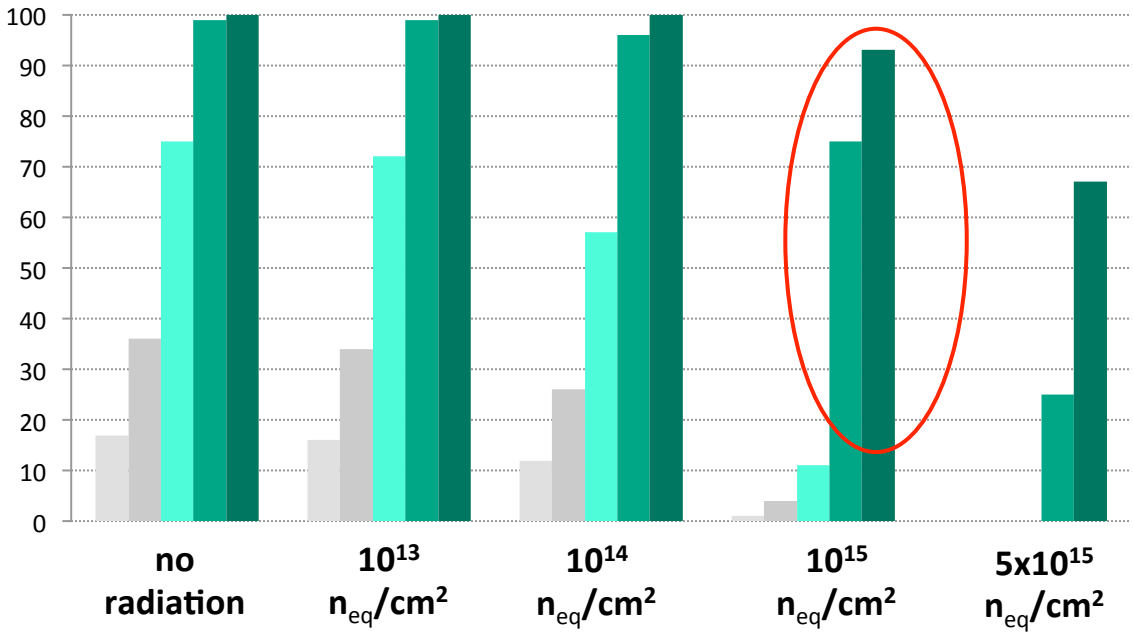
fraction of collected charge in first 10ns



	substrate resistivity [Ωcm]	Bias [V]	Fill Factor [%]
	10	1	15
	10	20	15
	2k	1	15
	2k	20	15
	2k	20	75

from Tomasz Hemperek

Enabling technologies

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"High" Voltage add-ons

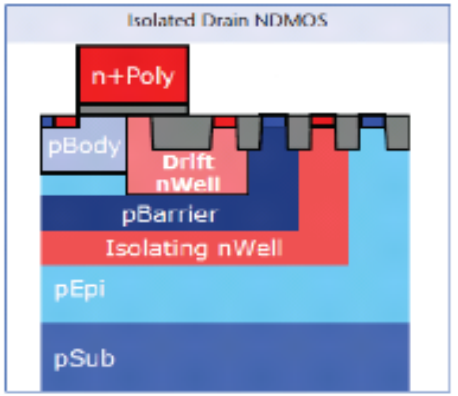
Special processing add-ons (from automotive and power management applications) **increase the voltage handling capability** and create a depletion layer in a well's pn-junction of o(10-15 µm).

"High" Resistive Wafers

8" hi/mid **resistivity** silicon wafers **accepted/qualified by the foundry**. Create depletion layer due the high resistivity.

Technology features (130-180 nm)

Radiation hard processes with **multiple nested wells**. Foundry must accept some process/DRC changes in order to optimize the design for HEP.



from: www.xfab.com

Backside Processing

Wafer thinning from backside and backside implant to fabricate a **backside contact** after CMOS processing.

Current approaches (a classification)

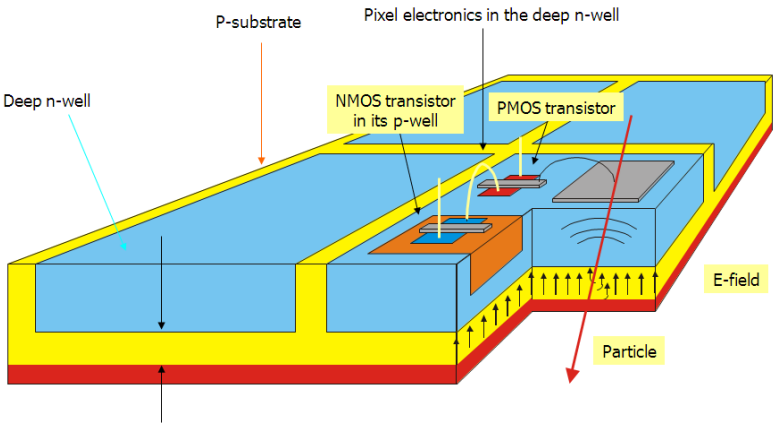
HV - CMOS

$$d \sim \sqrt{\rho \cdot V}$$

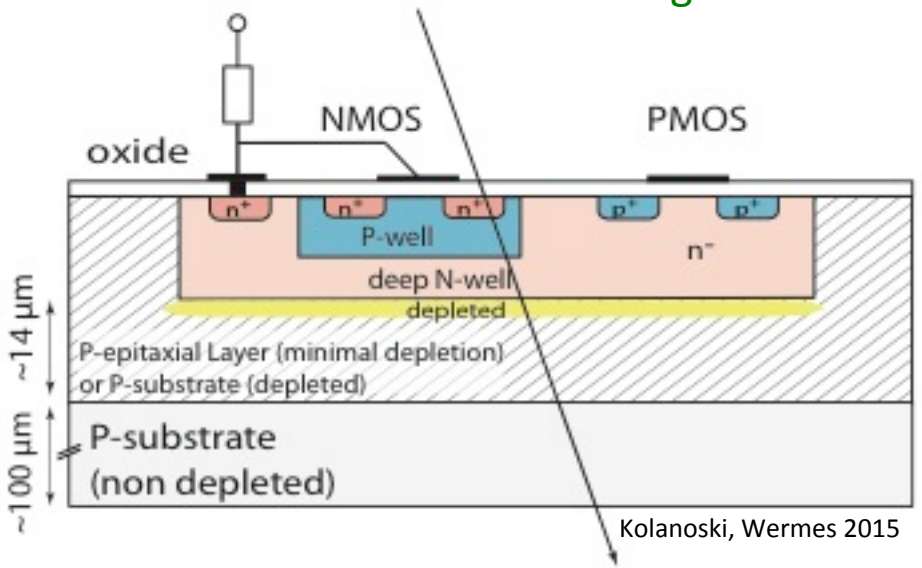
I. Peric et al.

Nucl.Instrum.Meth. A582 (2007) 876-885

Nucl.Instrum.Meth. A765 (2014) 172-176



e.g. AMS technology



- AMS 350 nm and 180 nm HV process (p-bulk) ... 60-100 V
- deep n-well to put nMOS (in extra p-well) and pMOS (limitation)
- ~10 - 15 µm depletion depth → 1-2 ke signal
- various pixel sizes (~20 x 20 to 50 x 125 µm^2)
- can also replace „sensor“ (amplified signal) in a „hybrid pixel“ bonding (bump, **glue**, other...) to FE-chip => **CCPD**

Current approaches (a classification)

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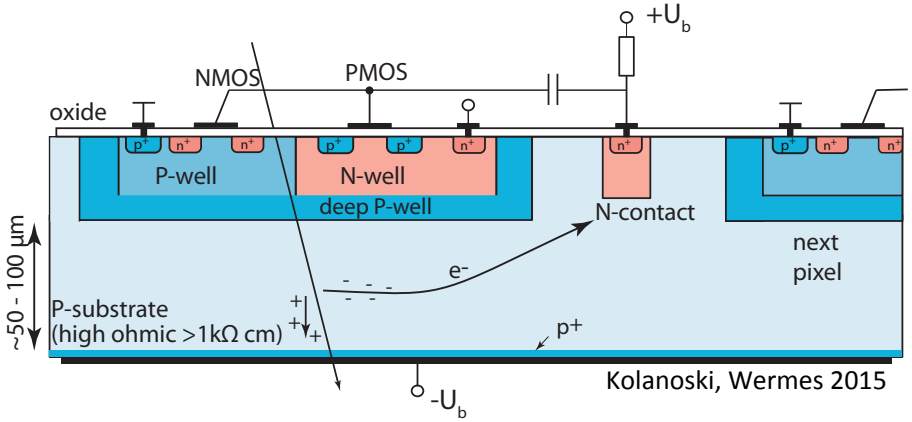
HR - CMOS

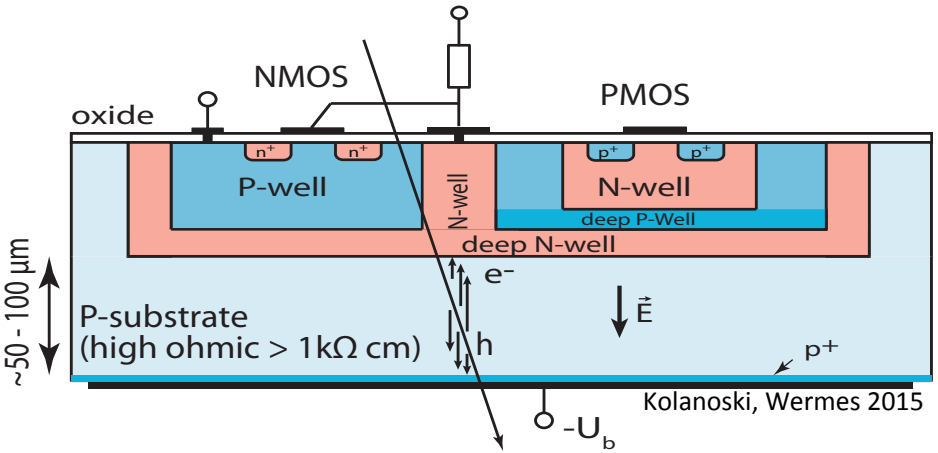
$$d \sim \sqrt{\rho \cdot V}$$

Mattiazzo, S,. W. Snoeys et al.
NIM A718 (2013) 288-291
Havranek, Hemperek, Krüger, NW et al.
JINST 10 (2015) 02, P02013



- (D)MAPS like configuration but w/ depleted bulk
- small collection node
- long drift path

=> **smaller C, more trapping**



- deep n and deep p wells
- large collection node
- short drift path

=> **larger C, less trapping**

skip to end ?

Current approaches (a classification)

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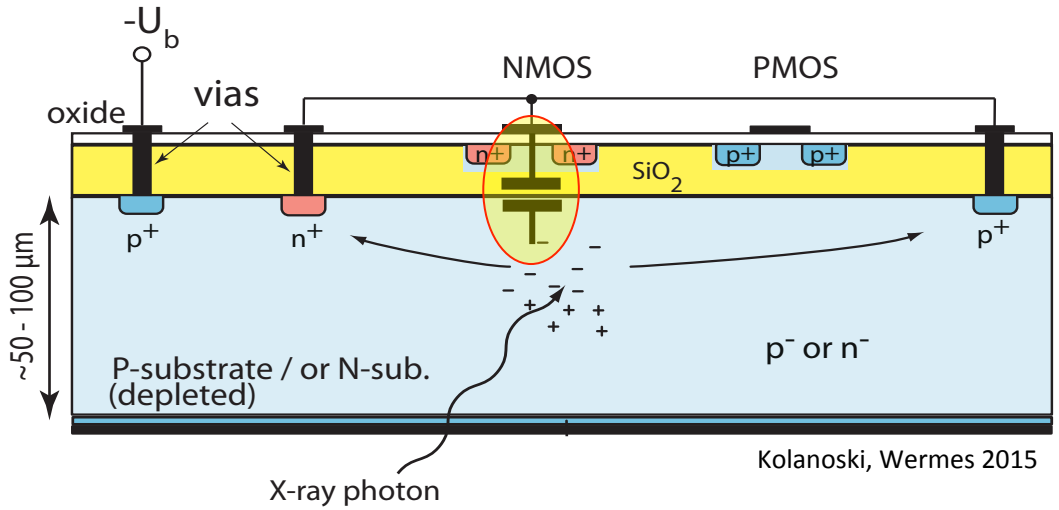
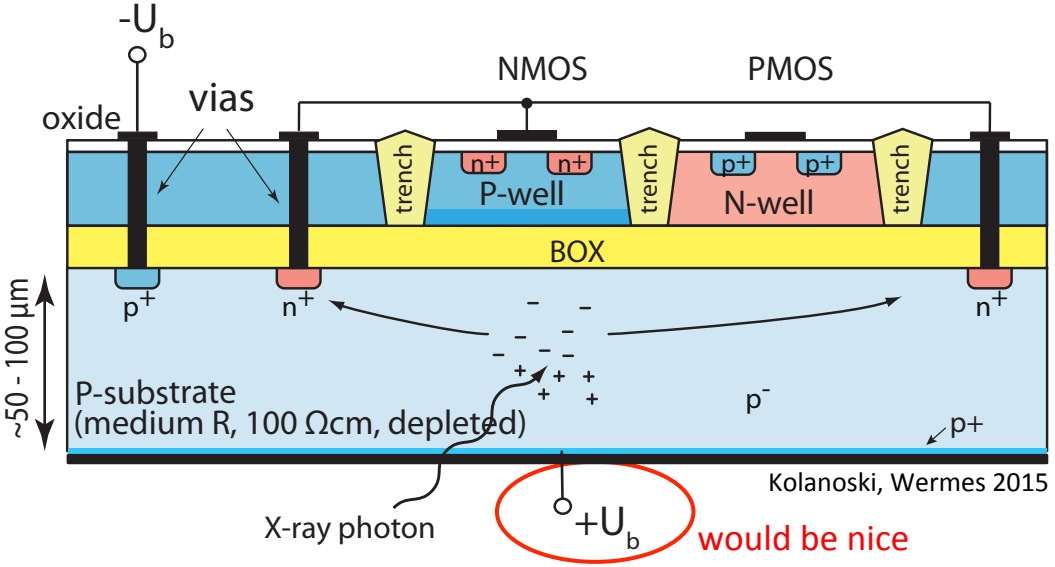
CMOS on SOI

$$d \sim \sqrt{\rho \cdot V}$$

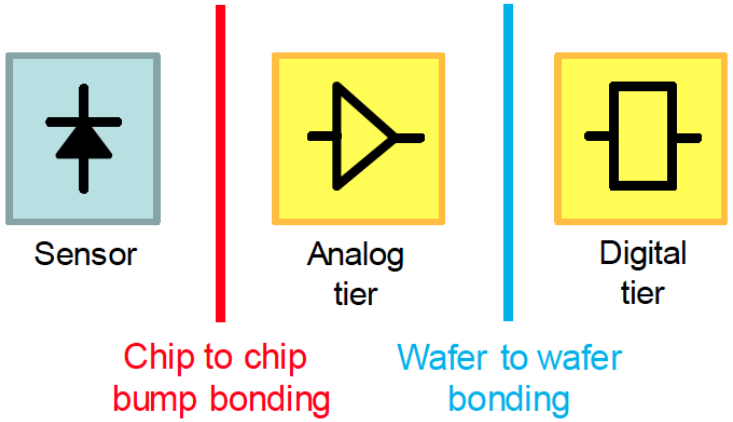


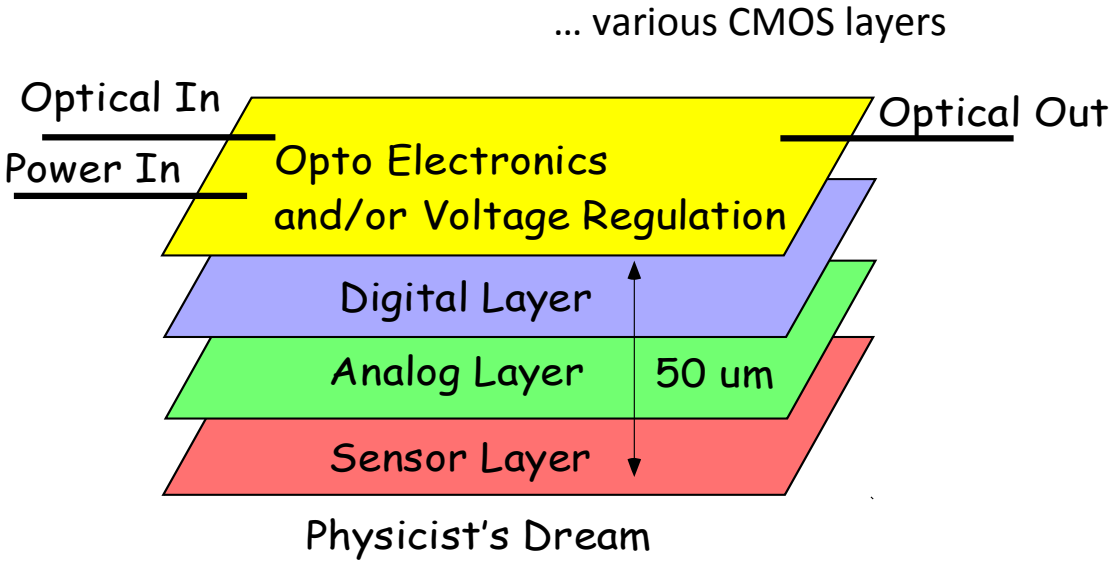
- **FD-SOI**
- OKI/LAPIS/KEK
  Y. Arai et al.
- issues
  - back gate effect
  - radiation issues due to BOX
- cures invented in recent years
- but not suited for LHC - pp



- **HV-SOI (thick film)**
- Hemperek, Kishishita, Krüger, NW
  doi:10.1016/j.nima.2015.02.052
- a promising alternative
- doped, non-depleted P- and N-wells prevent back gate effect and increase the radiation tolerance

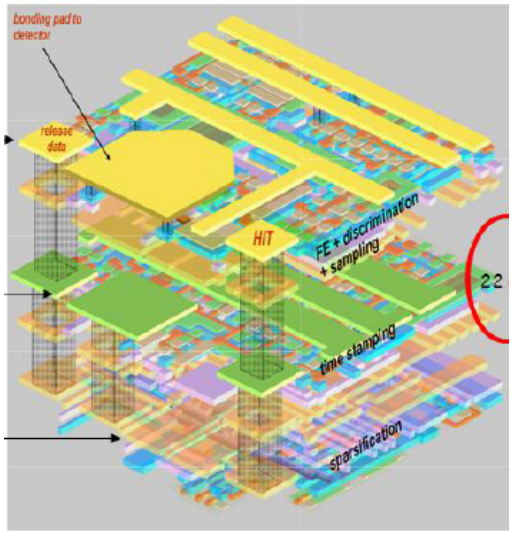
3D integration …





3D integration promises

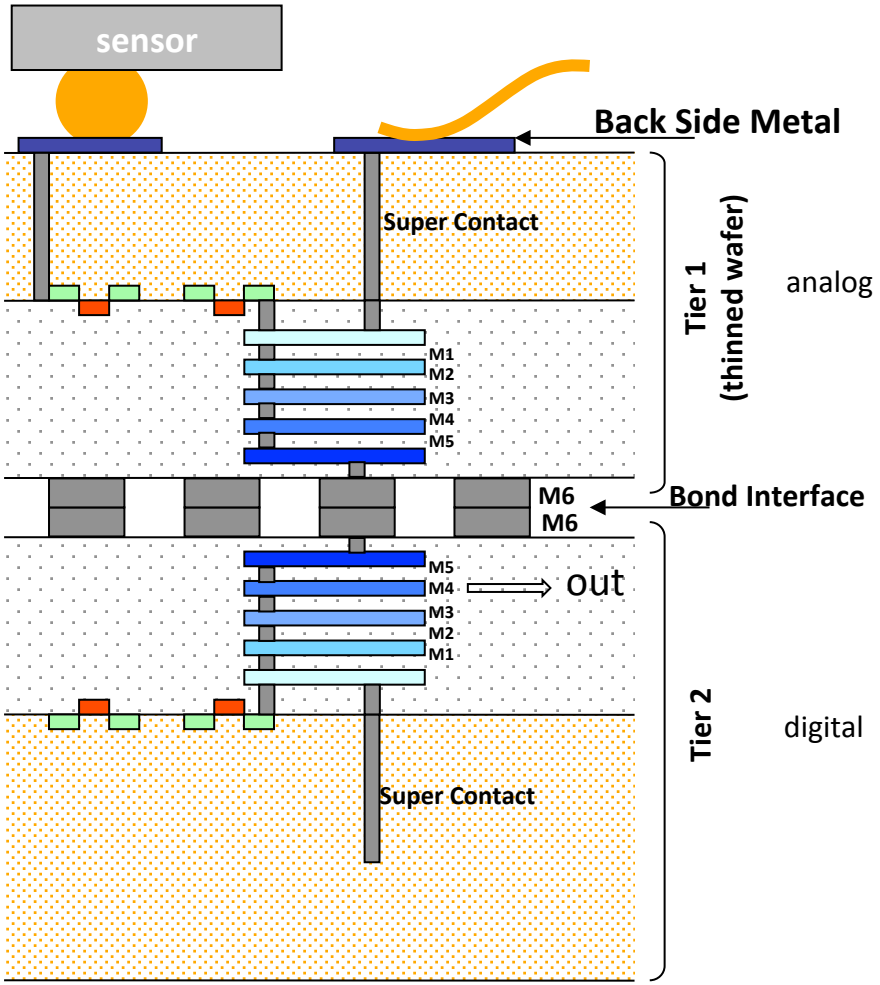
- higher granularity (smaller pixel size)
- lower power
- large active over total area ratio
- dedicated technology for each functional layer
- but: complex fabrication → yield is an issue



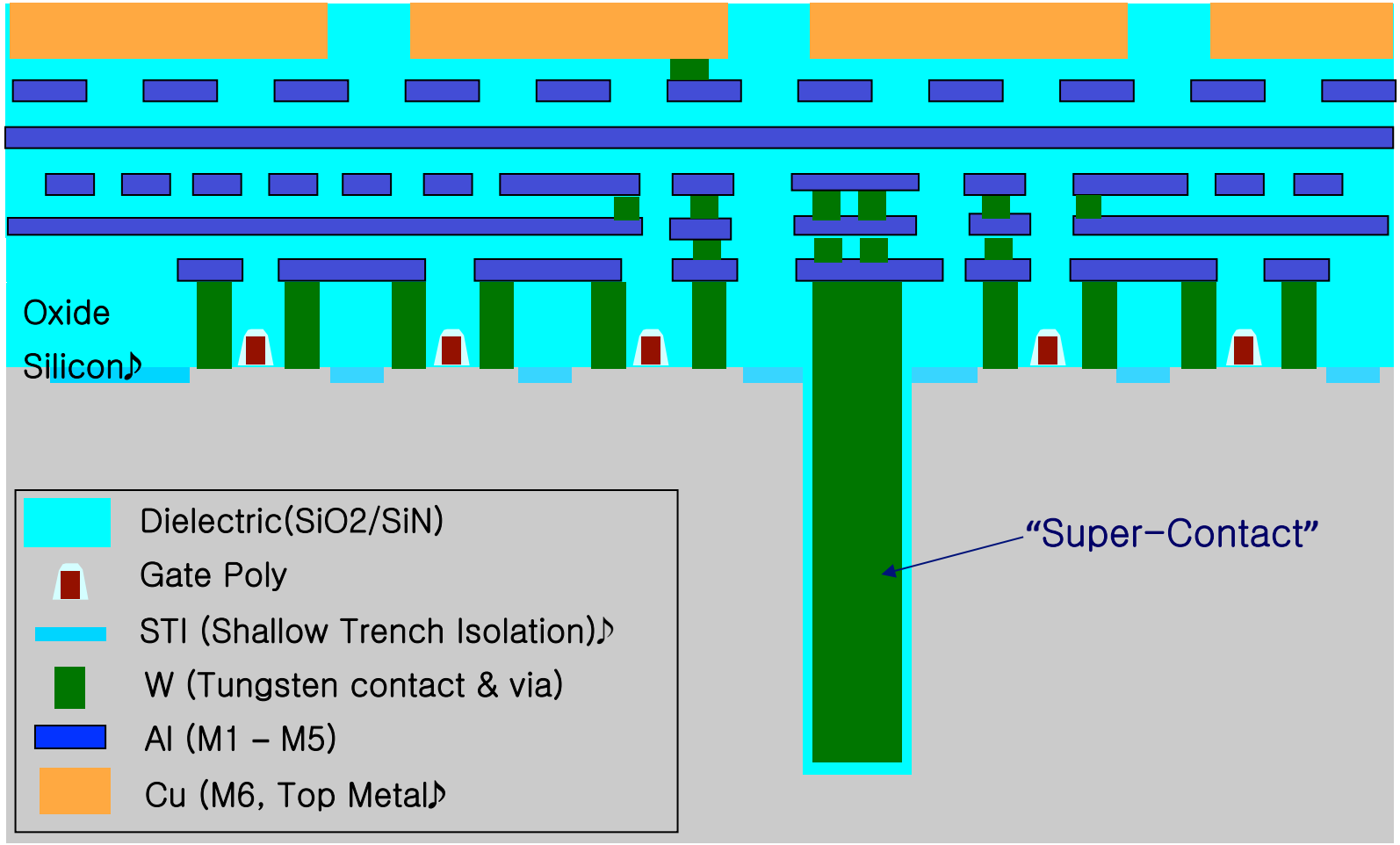
CMOS vias first …

Tezzaron/Chartered 0.13 um Process
Large reticule (25.76 mm x 30.26 mm)
12 inch wafers

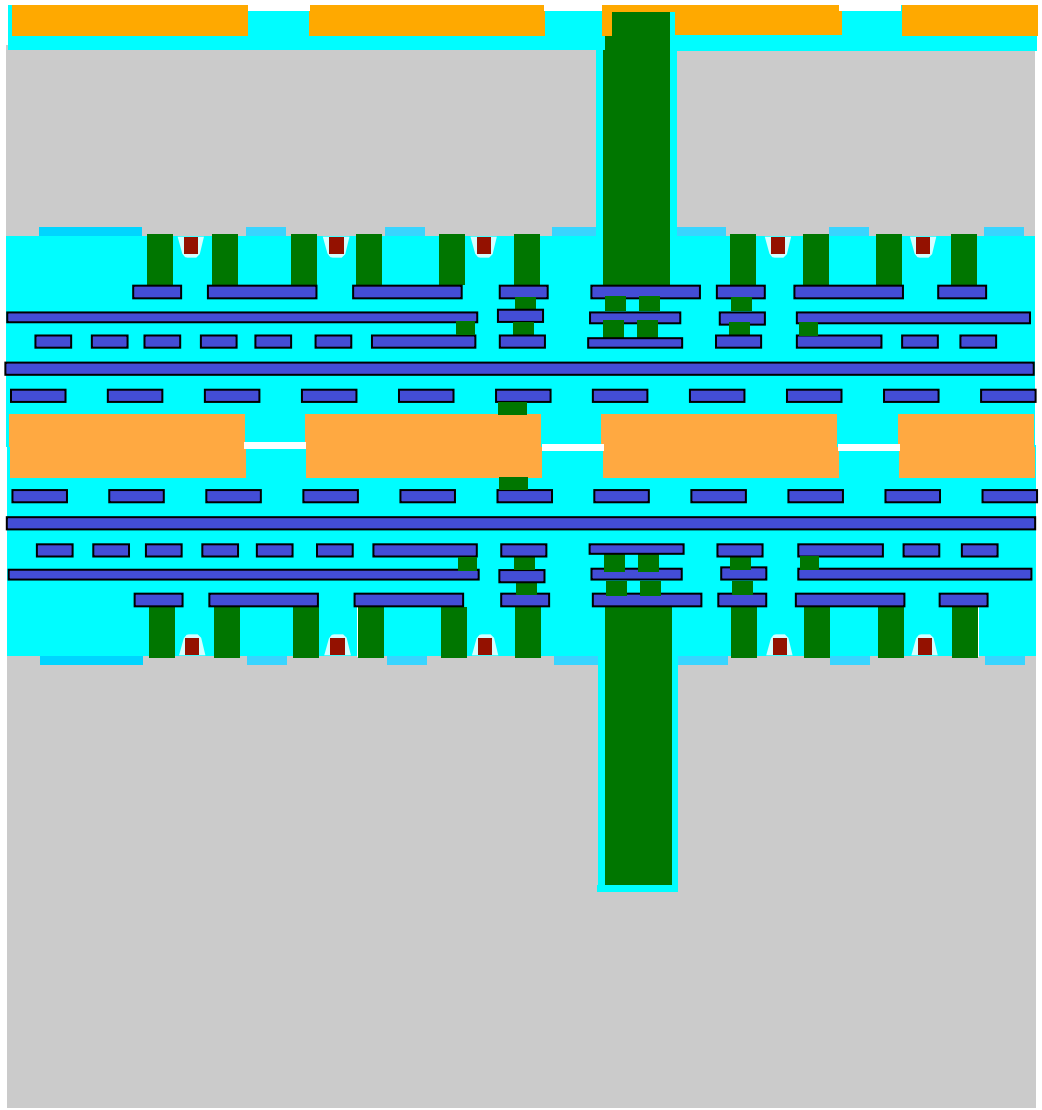
vias: 1.6 x 1.6 x 10 µm^3, 3.2 µm pitch
missing bonds: < 0.1 ppm



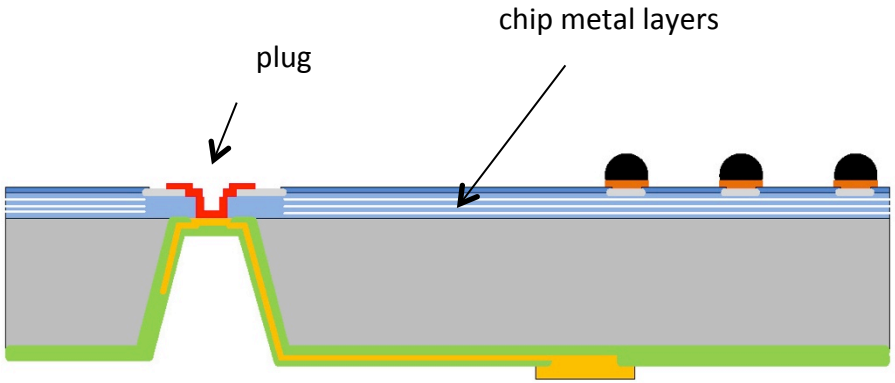
Wafer-Level Stacking

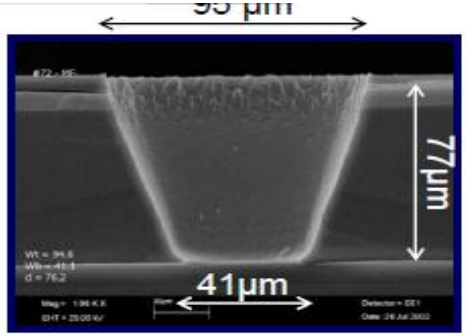


Next, Stack a Second Wafer (thin)



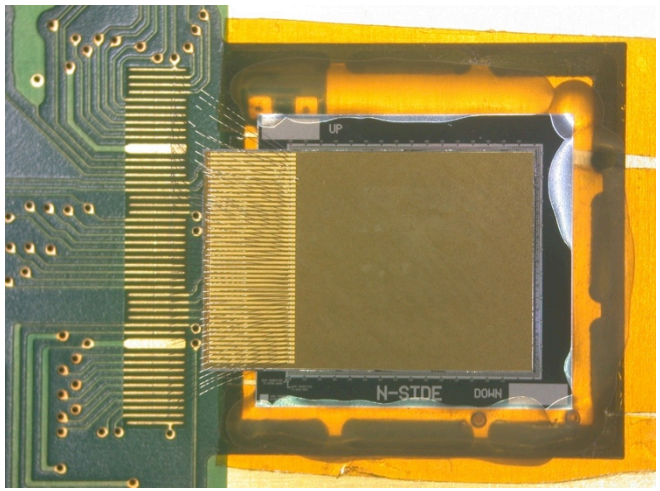
3D integration … vias last

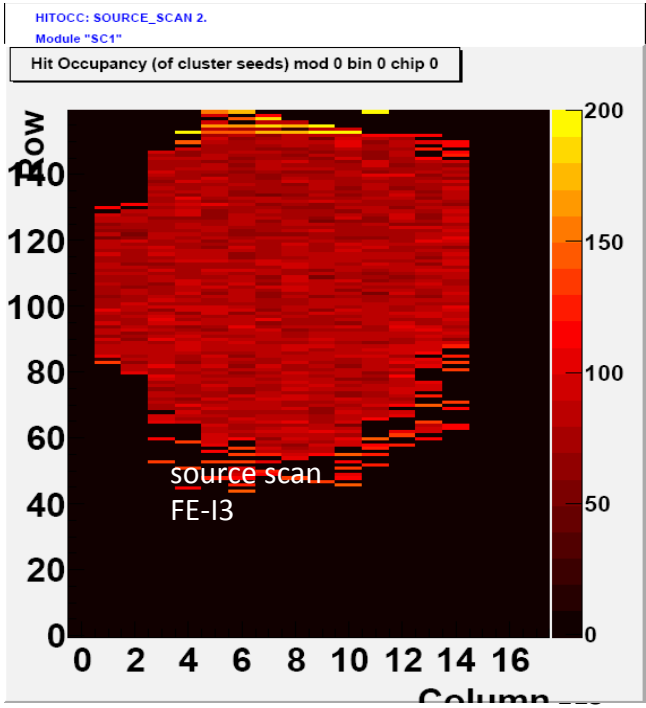




- aims to get through the chip silicon
- can connect to other tier
- can use backside as distribution layer

FE-I3 operated through TSVs (^{241}Am)





M. Barbero, T. Fritzsch, L. Gonella, F. Hügging et al., JINST 7 (2012) P08008

Conclusions

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Semiconductor micro pattern detector development is at the forefront of technological advances

- They are the working horse choice for present and future tracking detectors
- There is a large momentum in R&D and building of new detectors for the LHC upgrade
- R&D profits from modern micro technologies and their rapid progress
- Pixels/strips have applications in HEP and X-ray imaging (synchrotron light, medical ... not discussed

Further Reading

- G. Lutz, “Semiconductor Radiation Detectors”, Springer Berlin-Heidelberg-New York, 1999.

- Rossi, Fischer, Rohe, Wermes, “Pixel Detectors: From Fundamentals to Applications”, Springer Berlin-Heidelberg-New York, 2006, (ISBN 3-540-283324)

- ATLAS Pixel Detector, Technical Design Report, CERN/LHCC/98-13 (1998)
  CMS Tracker Technical Design Report, CERN/LHCC/98-6 (1998)
  ALICE Inner Tracker System, Technical Design Report, CERN/LHCC/99-12 (1999)

- N. Wermes, “Pixel Detectors for Charged Particles”
  Published in Nucl.Instrum.Meth. A604 (2009) 370-379,
  e-Print Archive: physics/0811.4577

- Kolanoski, H. and Wermes, N.
  Teilchendetektoren – Grundlagen und Anwendungen, Spektrum-Verlag, (2016) in print