FPGA tutorial

Lecture 4

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XILINX®

Putting all together ...

- Final Exercise
  - 8-bit decimal counter (0 – 255)
  - 7 segment display
  - Enable
  - Up / Down
  - driven by ~ 10 Hz

What do we need?

- all the things we programmed before
  - 7segment lookup ✅
  - address decoder (1 cold) ✅
  - several counter ✅
  - BCD encoder ✅

How to generate a slow clock?

- It is always nice to have a clock with
  - dutycycle of 50% (50% low, 50% high)
  - defined phase with respect to the master clock
- use a counter
  - count up and down → this ensures 50% duty cycle

Clock divider

- divider is set via maxCNT

Clock divider I provide!

always running up down counter
no enable, no reset
you might use your counter with
by setting .RST(0) .EN(1)

```
counter mycnt(  .dir(CLKout),
                .CLK(CLKin),
                .cnt(cnt_reg) );
```

On every clock change

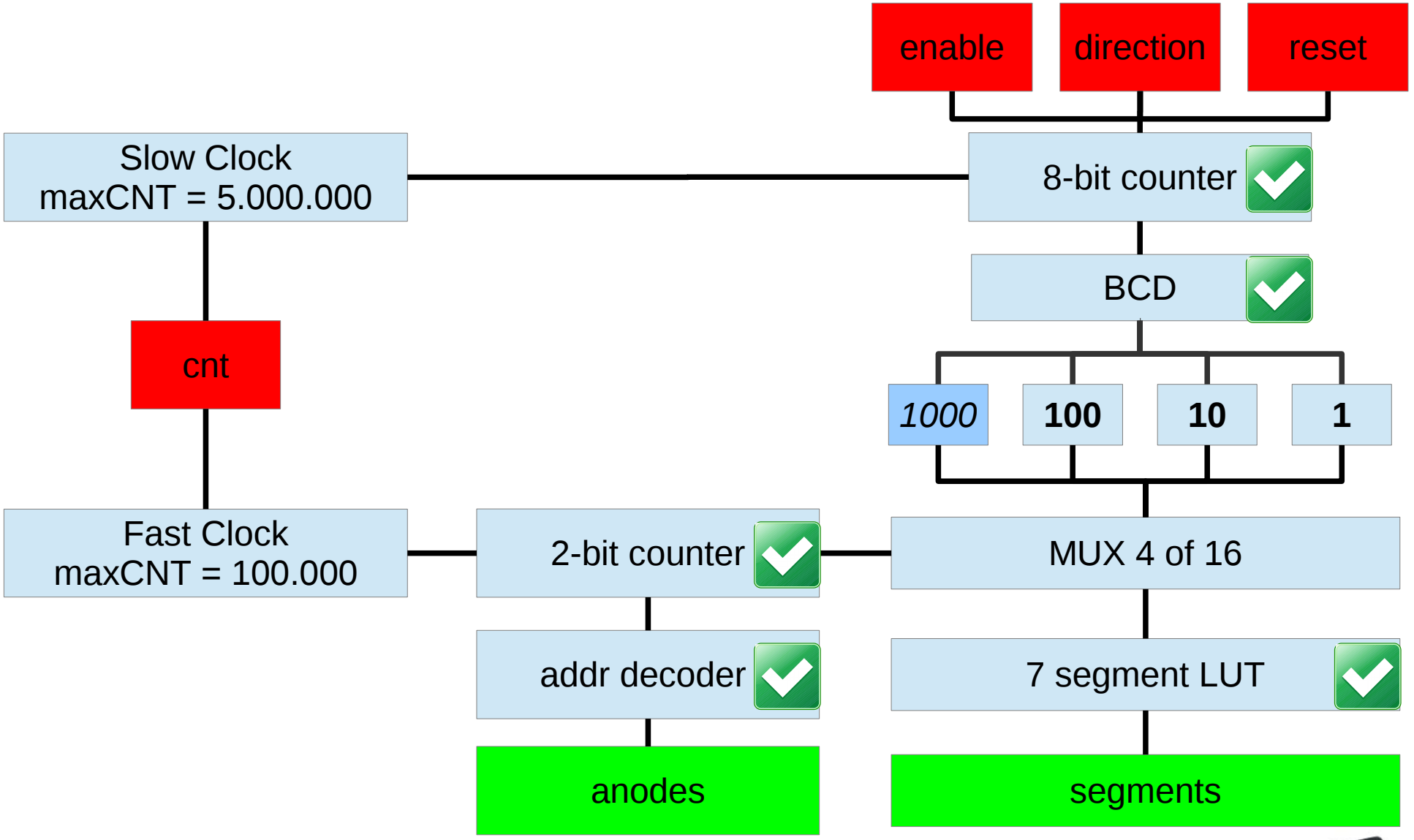
```
always @( cnt_reg ) begin
    if( (cnt_reg == maxCNT) ) begin
        CLKout = 1; // count down
    end
    if( (cnt_reg == 0 ) ) begin
        CLKout = 0; // count up
    end
end
```

we use CLKout as the direction!

7^{th} - Project

- I provide you all the modules needed.
- Use them!
- Just connect them in the right way.
- You just have to write the top module
  - in BND_07skel part of the top module is already filled.
  - If you like to, you can delete this and start from scratch
  - If you are not that familiar with FPGAs, just connect the modules with each other

7th – Project


enable
direction
reset
Slow Clock
maxCNT = 5.000.000
8-bit counter
BCD
cnt
1000
100
10
1
Fast Clock
maxCNT = 100.000
2-bit counter
MUX 4 of 16
addr decoder
7 segment LUT
anodes
segments

If there is time...

- Try to modify the working solution
  - add a real stop watch behaviour
  - one button for start / stop

At the end of the lecture ...

- Please return the Laptops to the right box
  - they have a number written on top
  - each box has a number, please match them