Addressing Future HPC Demand with Multi-core Processors

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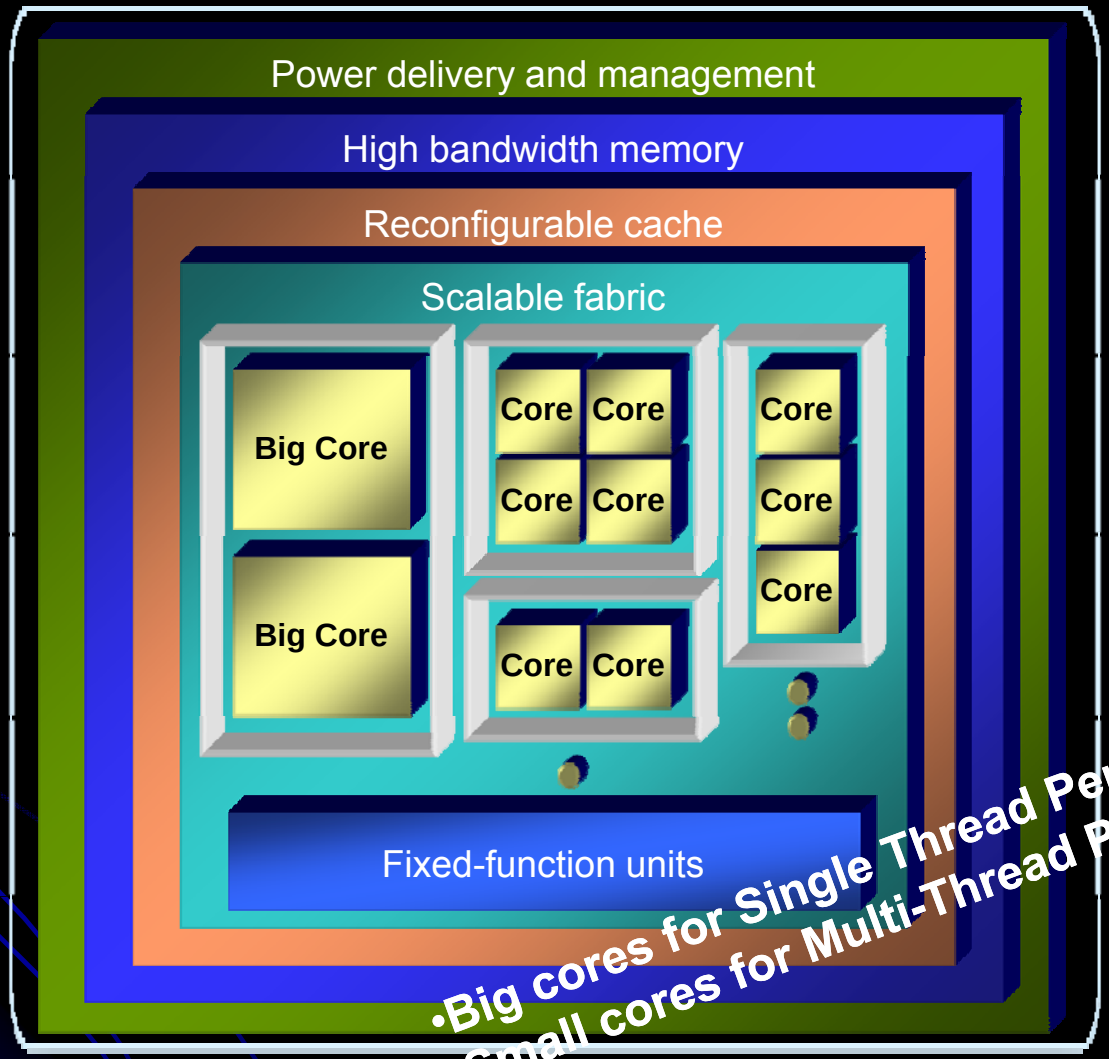
Intel Is Listening…

With multi-core processors, however, we finally get to a scheme where the HEP execution profile shines. Thanks to the fact that our jobs are embarrassingly parallel (each physics event is independent of the others) we can launch as many processes (or jobs) as there are cores on a die. However, this requires that the memory size is increased to accommodate the extra processes (making the computers more expensive). As long as the memory traffic does not become a bottleneck, we see a practically linear increase in the throughput on such a system. A ROOT/PROOF analysis demo elegantly demonstrated this during the launch of the quad-core chip at CERN.

Source: "Processors size up for physics at the LHC"
Sverre Jarp, CERN Courier, March 28, 2007

HEP – High Energy Physics
LHC - Large Hadron Collider

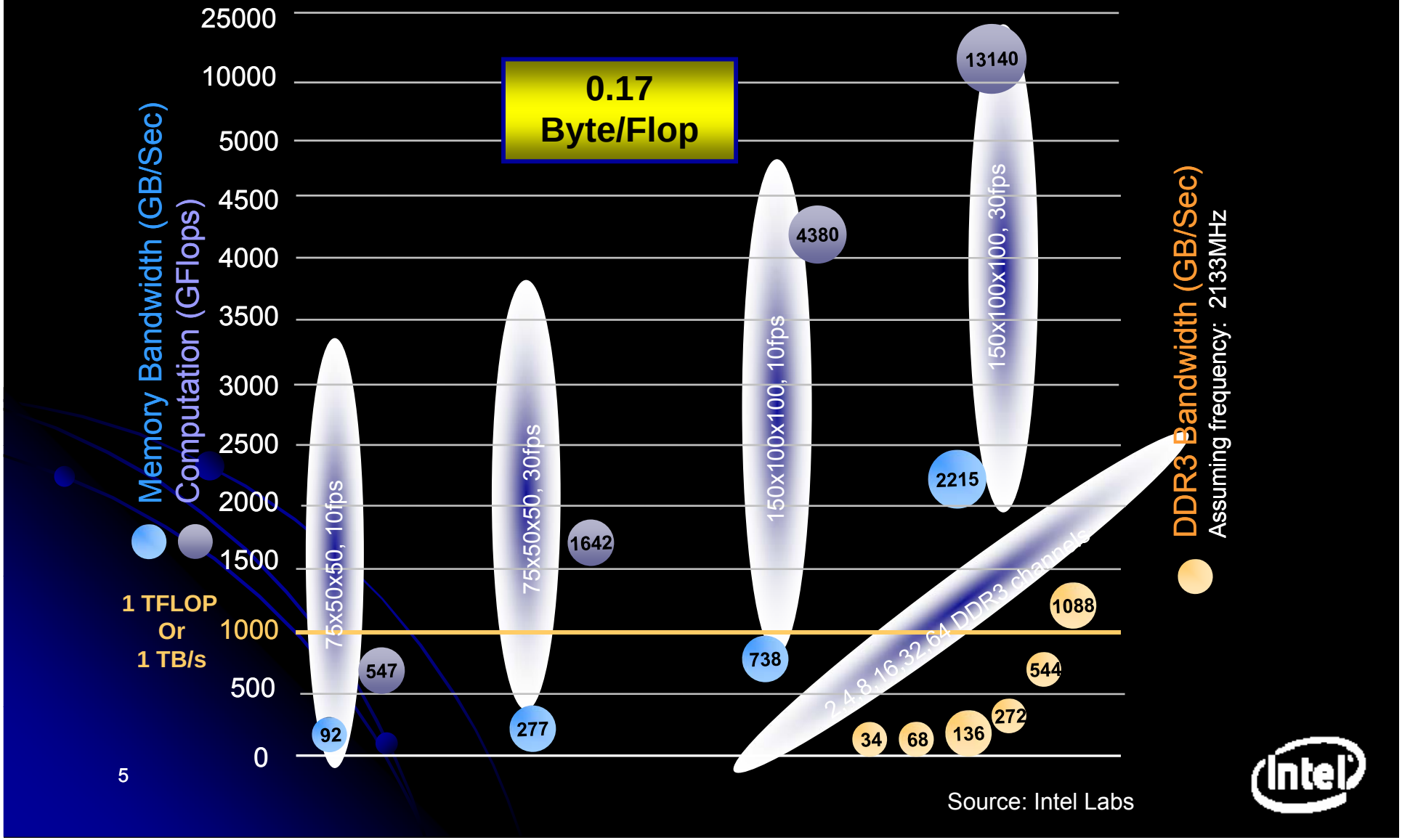
Accelerating Multi- and Many-core



Performance Through Parallelism

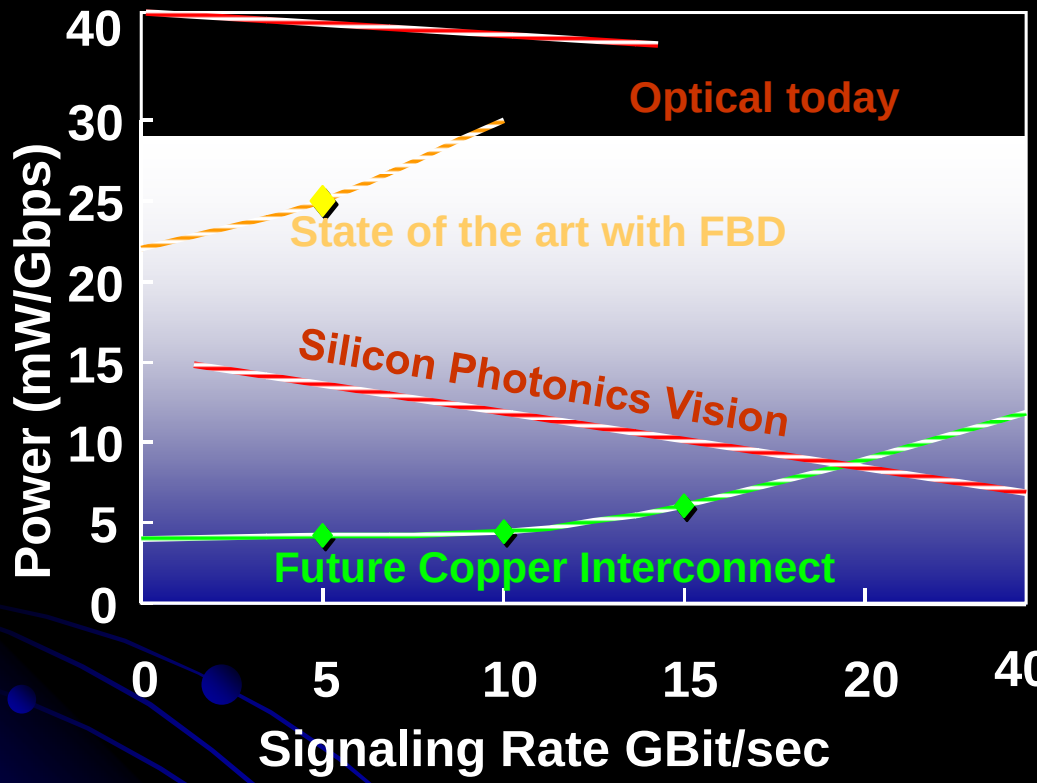
Memory Bandwidth Demand

Computational Fluid Dynamic (CFD) - Splash

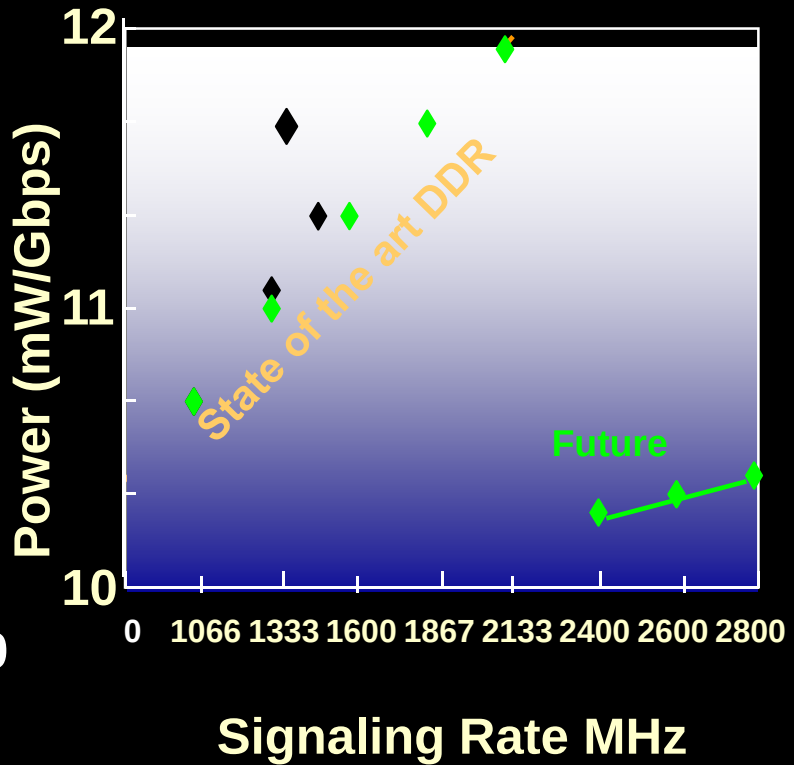


Increasing Signaling Rate

More Bandwidth & Less Power



Differential Copper Interconnect & Silicon Photonics

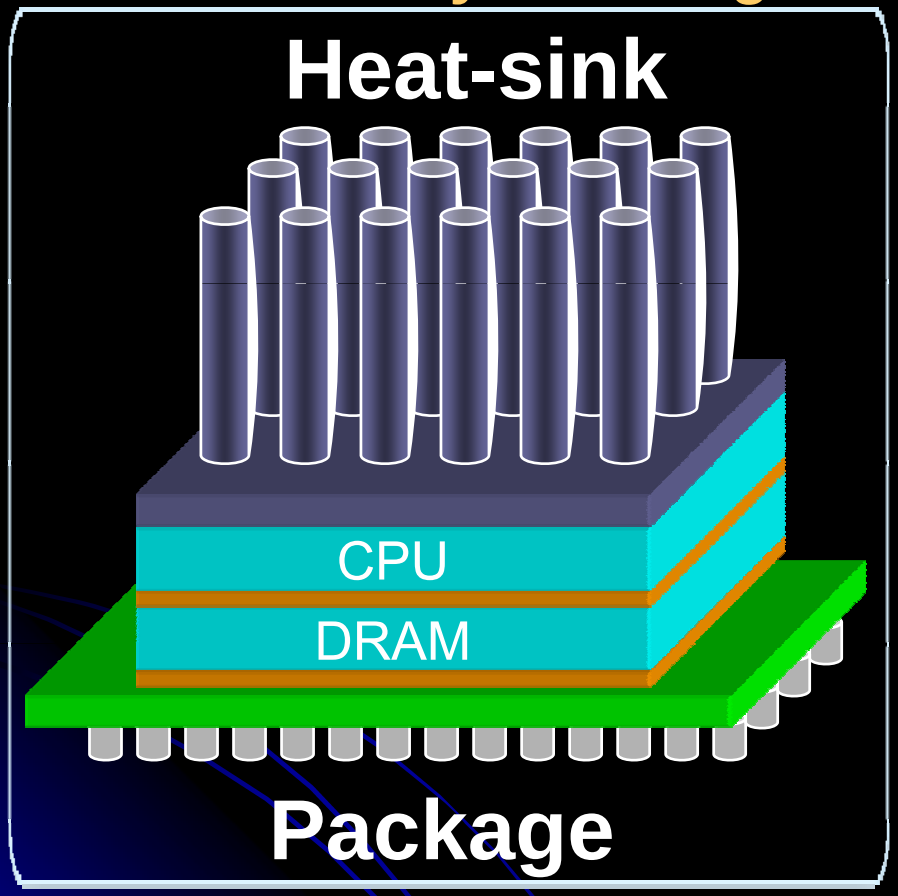


Single-ended Interconnect

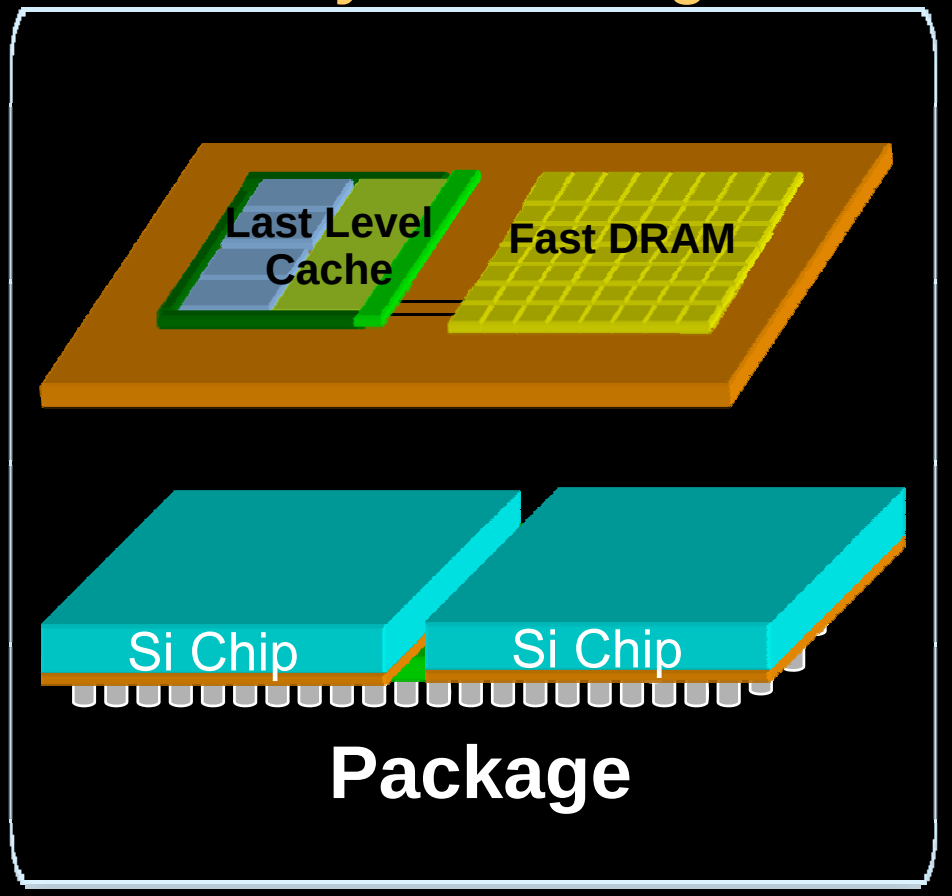
State of the Art with FBD (@25mW/Gbps & 5Gb/s):
100 GB/sec ~ 1 Tb/sec = 1,000 Gb/sec ✕ 25mw/Gb/sec = **25 Watts**
Bus-width = 1,000 Gb/sec / 5 = 200, about **400 pins** (differential)

Addressing Memory Bandwidth

3D Memory Stacking



Memory on Package

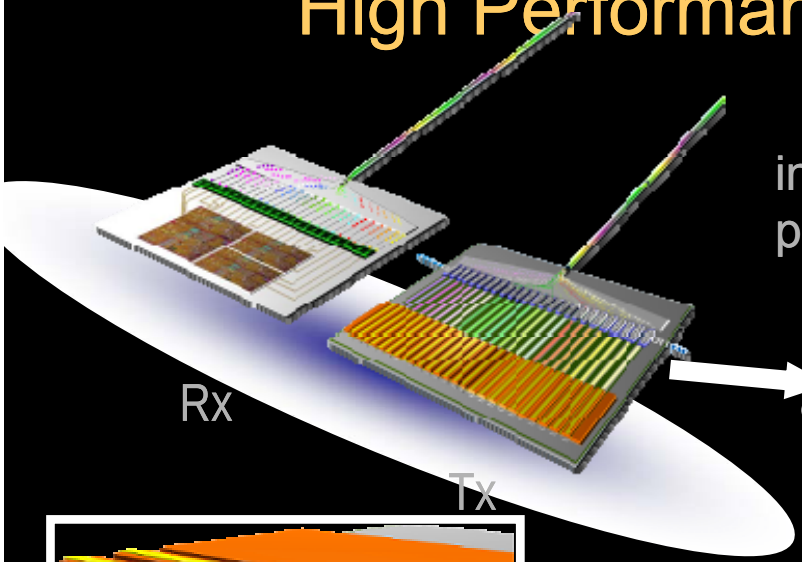


*Future Vision, does not represent real Intel product

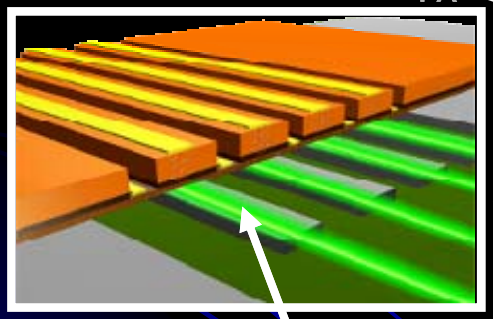
Bringing Memory Closer to the Cores

Photonics For Memory BW and Capacity

High Performance with Remote Memory

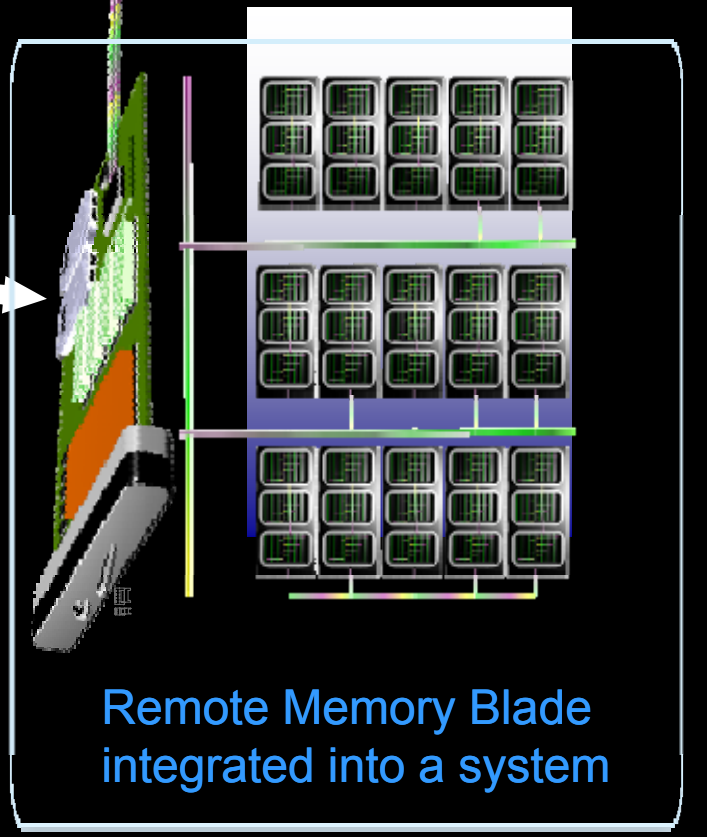


integrated silicon photonic chip



The silicon acts as laser cavity - Light bounces back and forth and get amplified by InP based material

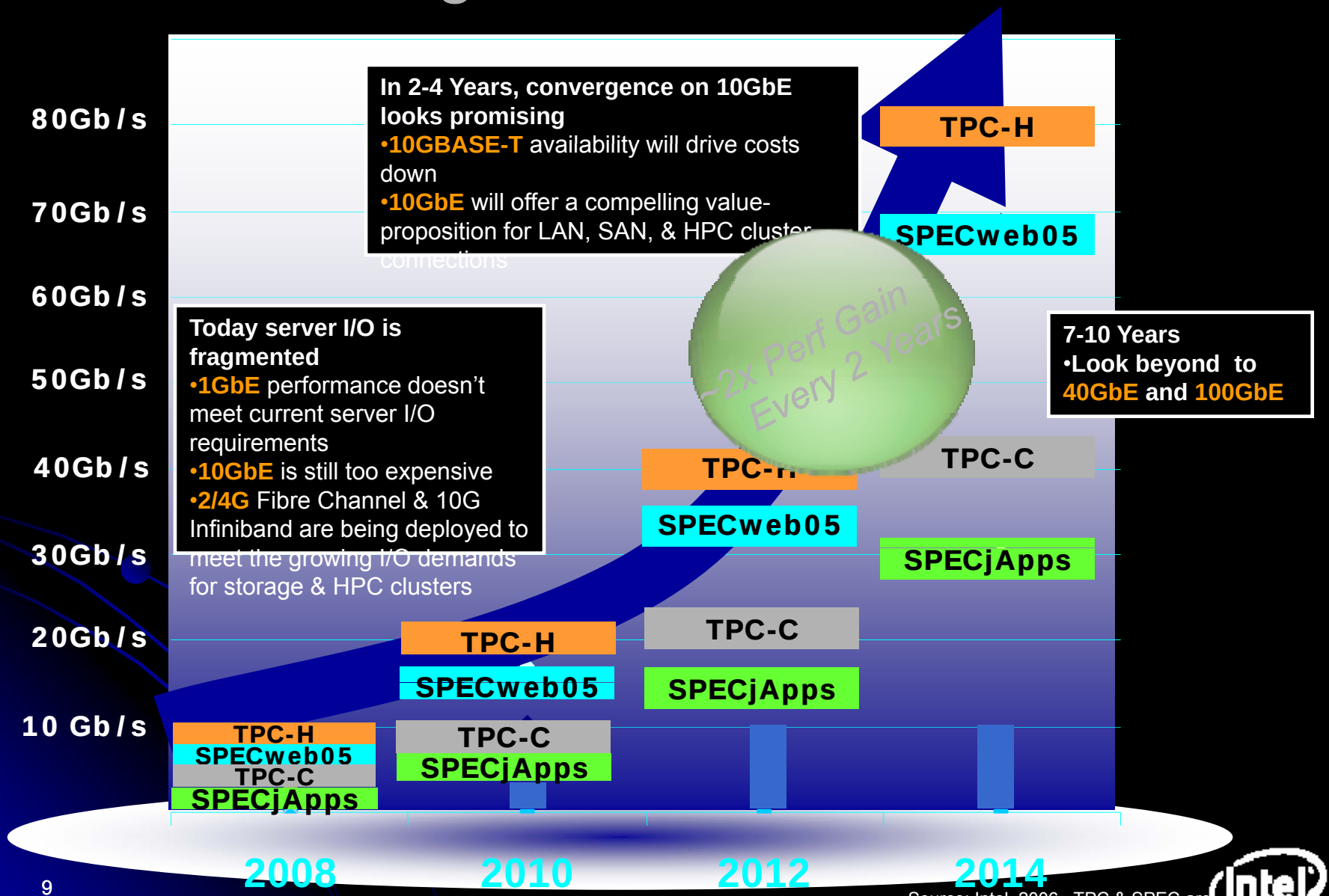
The Indium Phosphide emits the light into the silicon waveguide



Remote Memory Blade integrated into a system

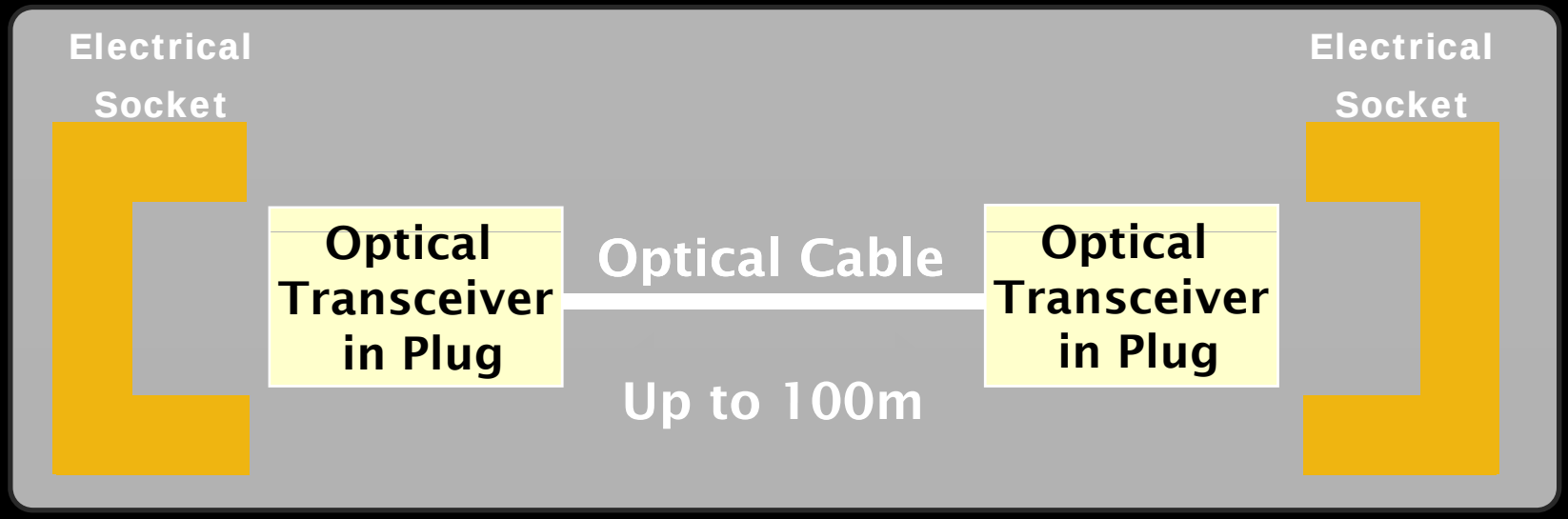
Integrated Tb/s Optical Link on a Single Chip

Increasing Ethernet Bandwidth



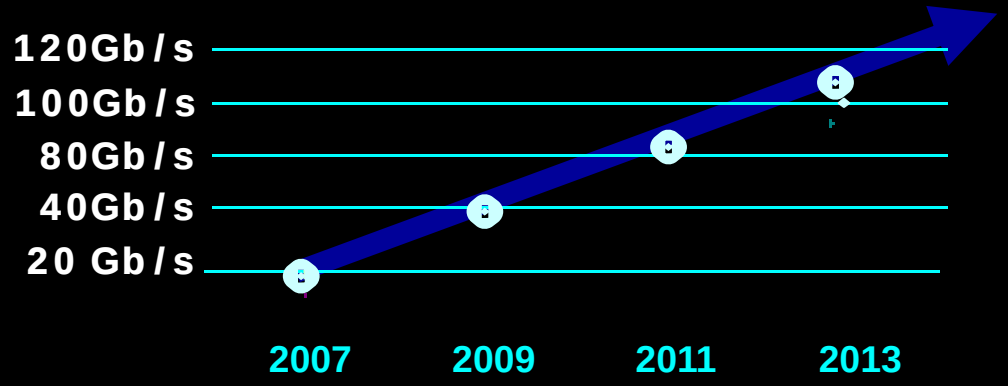
Source: Intel, 2006. TPC & SPEC are standard server application benchmarks

Outside the Box:
HPC Networking with Optical Cables



Benefit Over Copper:

- Scalable, BW, throughput
- Longer distance – today up to 100m
- Higher reliability: 10^{-15} Bit Error Rate (BER) or lower
- Smaller & lighter form factor



Doubling the Data Rate Every 2 Years

Power Aware Everywhere

Silicon:

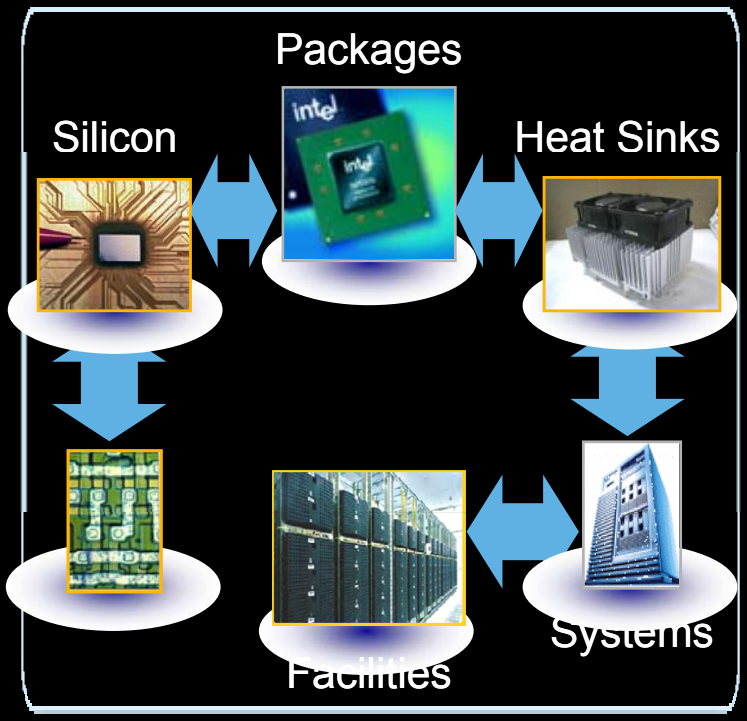
Moore's law, Strained silicon, Transistor leakage control techniques, Hi-K Dielectric, Clock gating, etc.

Processor and System Power:

Multi-core, Integrated Voltage Regulators (IVR), Fine grain power management, etc.

Facilities:

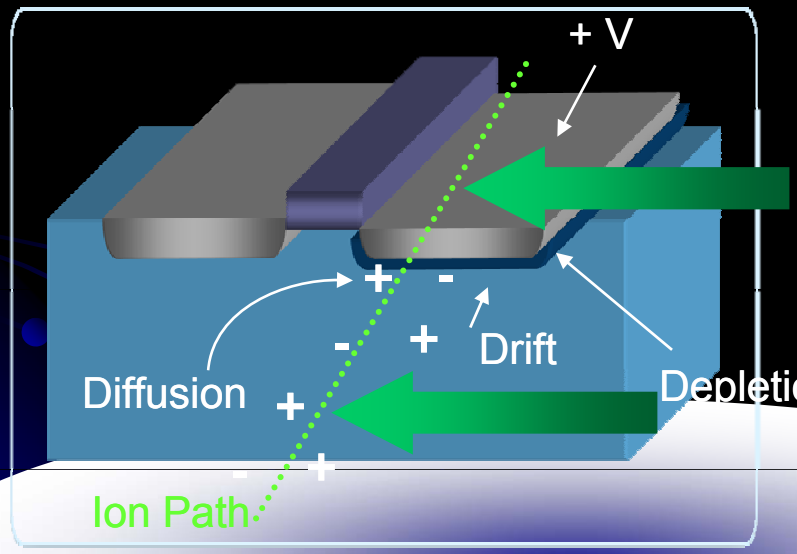
Efficient Power Conversion and Cooling



Reliability Challenges & Vision

An exponential growth in FIT/chip

- *FIT/bit of memory cell*: expected to be roughly constant, but,
- *Moore's law*: increasing the bit count exponentially: 2x every 2 years



Architectural Techniques

Micro Solutions

Parity
SECDED ECC
π bit

Macro Solutions

Lockstepping
Redundant multithreading (RMT)
Redundant multi-core CPU

Circuit Techniques

Device Param Tuning

Rad-hard Cell Creation

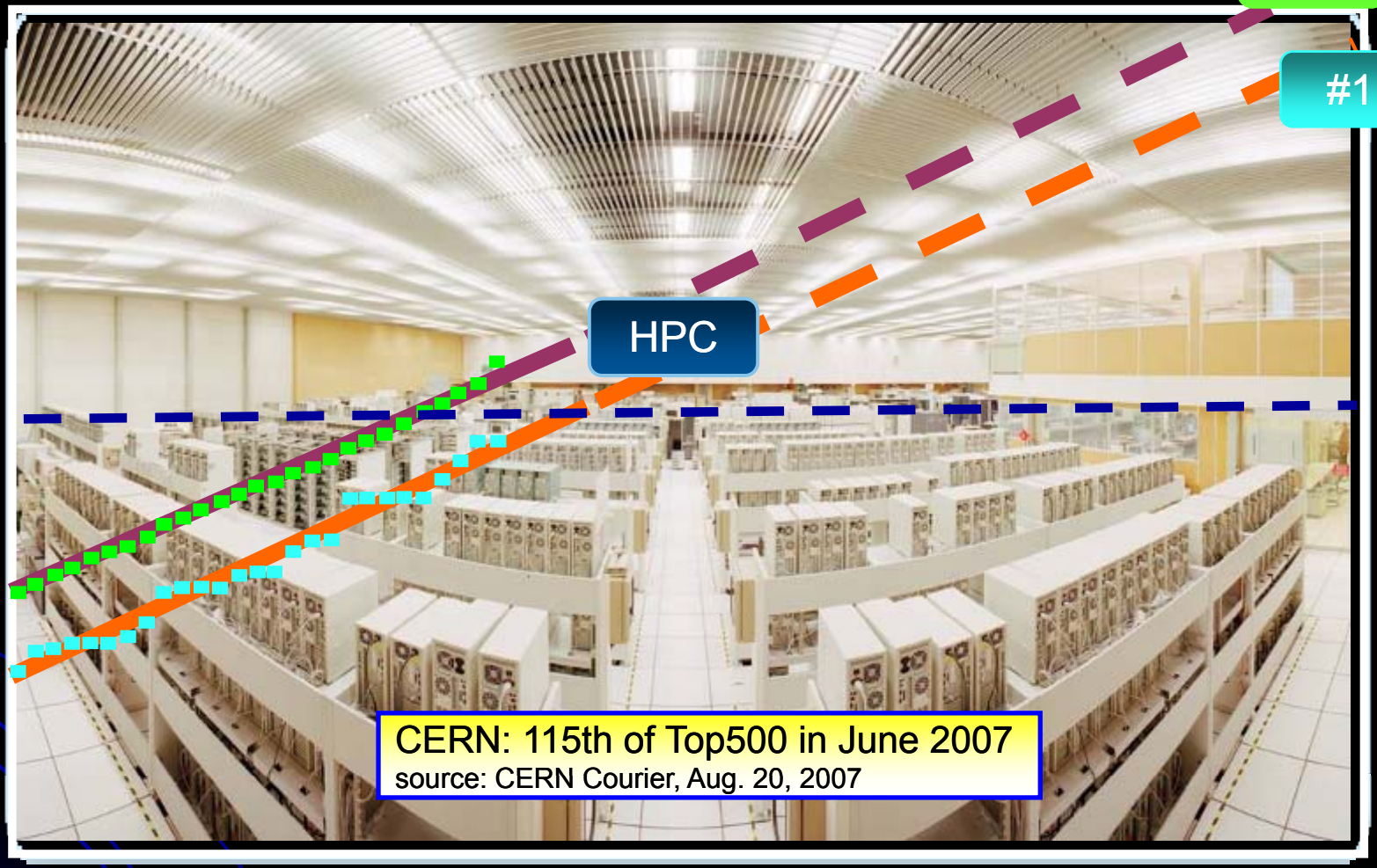
Process Techniques

State-of-Art Processes

Soft Error: one of many reliability challenges

Source: Intel

What Can We Expect?!



Beyond Petascale

Background picture from CERN OpenLab, Intel HPC Roundtable '06

What can Intel do for you?