MONOLITHIC PIXEL DETECTORS

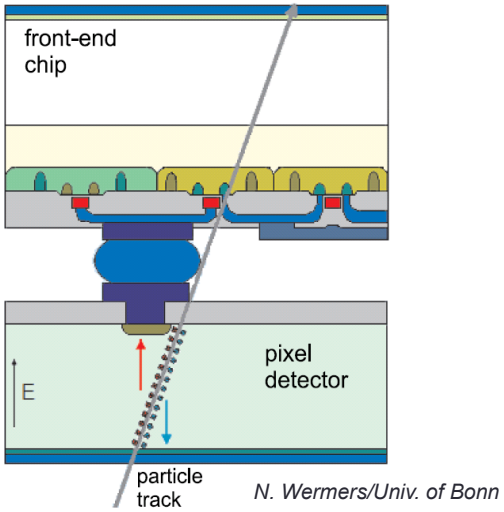
P. Riedler, CERN

Workshop on requirements for future detector technologies in view of FCC-hh
February 3 and 4, 2015, CERN

Monolithic Pixel Detectors

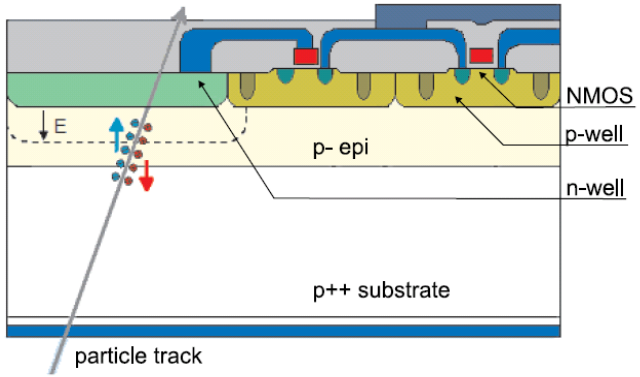
Compared to hybrid pixel detectors, the **sensitive volume and part or the full readout circuitry is combined in one piece of silicon**. The generated charge is collected on a dedicated collection electrode.

Hybrid Pixel Detector



N. Wermers/Univ. of Bonn

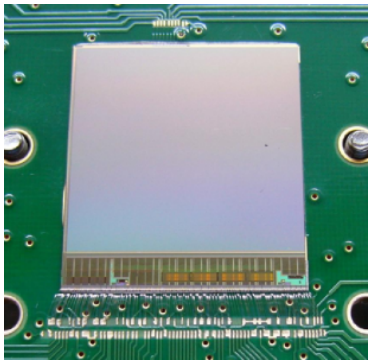
Monolithic Pixel Detector (example)



Monolithic Pixel Detectors

Monolithic pixel detectors for HEP exist in many different flavours and offer significant advantages:

- Commercial CMOS processing (many foundries, larger wafer diameter, potentially low cost per area, stitching, ..)
- Thin detectors (O(50 µm Si))
- High granularity (small cell sizes, O(20 µm x 20 µm))
- No need for cost intensive fine pitch bump bonding



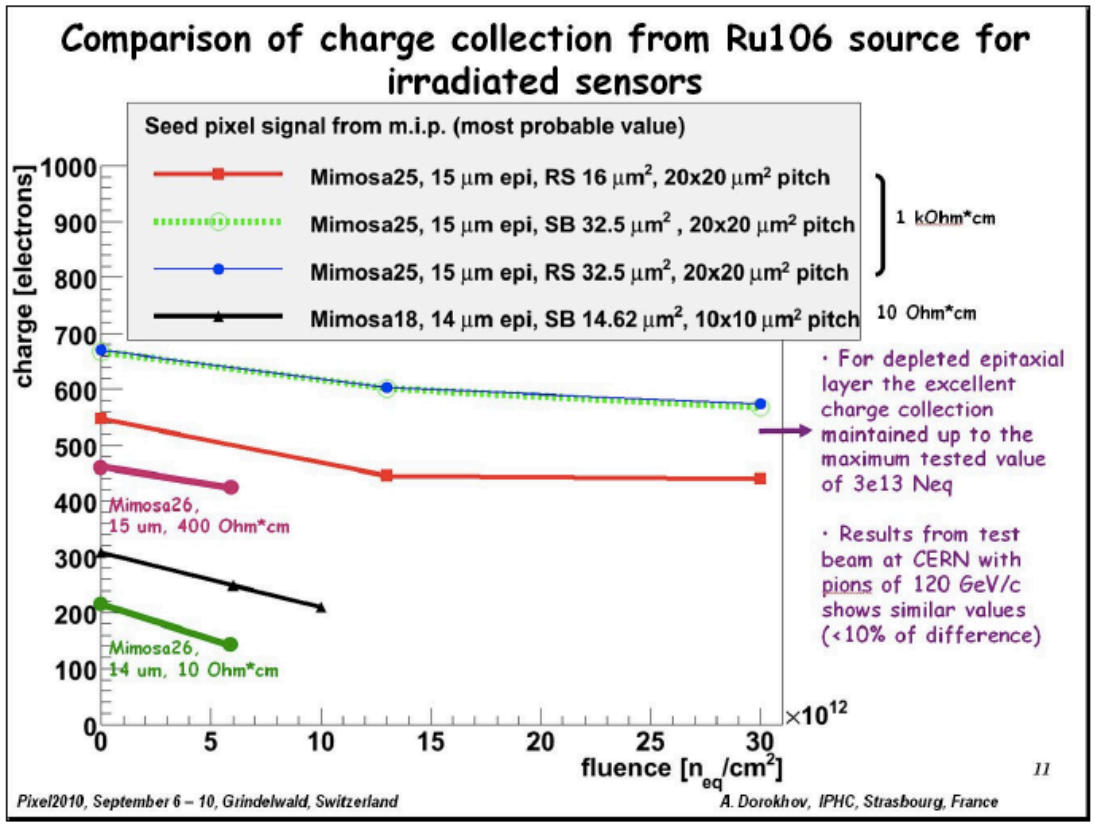
MAPS: ULTIMATE chip for STAR upgrade
Data taking since 2014

- Twin well 0.35 µm CMOS
- Readout time 190 µs
- TID 150 krad, NIEL few 1012 neq

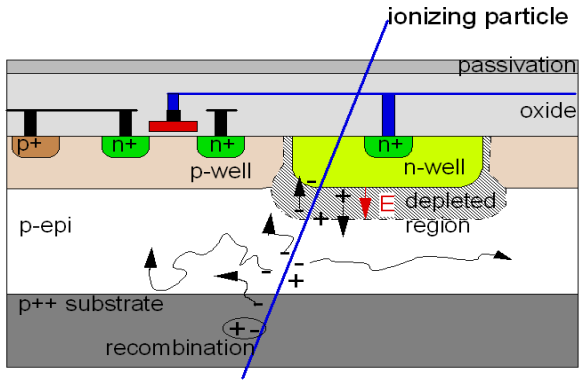
In traditional MAPS (Monolithic Active Pixel Sensors):

- No reverse substrate bias
  → signal collected mainly by diffusion, sensitive to displacement damage
- Only one type of transistor in pixel (twin well)
  → simple in pixel circuit
- Rolling shutter readout

Radiation Tolerance of Traditional MAPS



A. Dorokhov et al., Pixel 2010



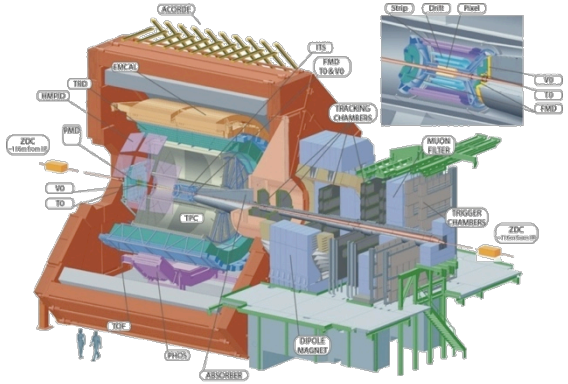
M. Winter

Charge is mainly collected by diffusion (not fully depleted)

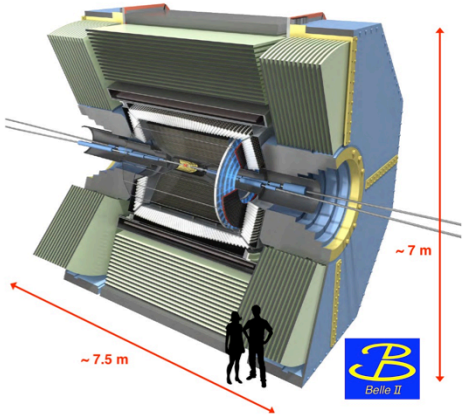
Monolithic Pixel Detectors in HEP Experiments

Several experiments have selected monolithic pixel detectors for their tracker upgrades:

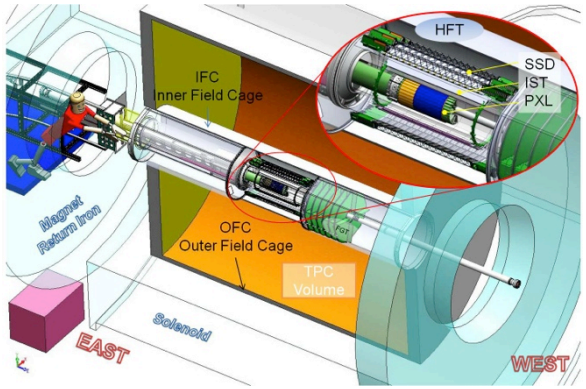
ALICE



BELLE II



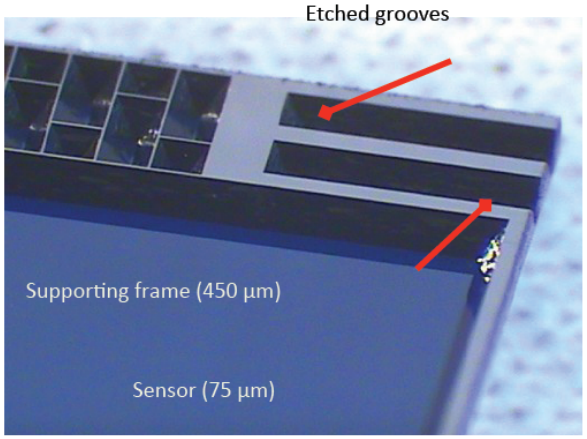
STAR



Belle II Pixel Detector at SuperKEKB: DEPFET

Pixel detector based on **DEPFET** sensors to be installed in 2015 (physics in 2016)

- 2 barrel layers (r=1.4 cm and 2.2 cm)
- Pixel size 50 µm x 75 µm
- Row-wise read-out (rolling shutter), 20 µs/frame
- Special thinning of the matrix area to reduce material budget (75 µm thick)



C. Lacasta, VERTEX 2013

S. Tanaka, HSTD9, 2013

Radiation environment:
~ 1.9 Mrad / year
~ 1.2 10^{13} 1MeV n_{eq}/cm^2 per year

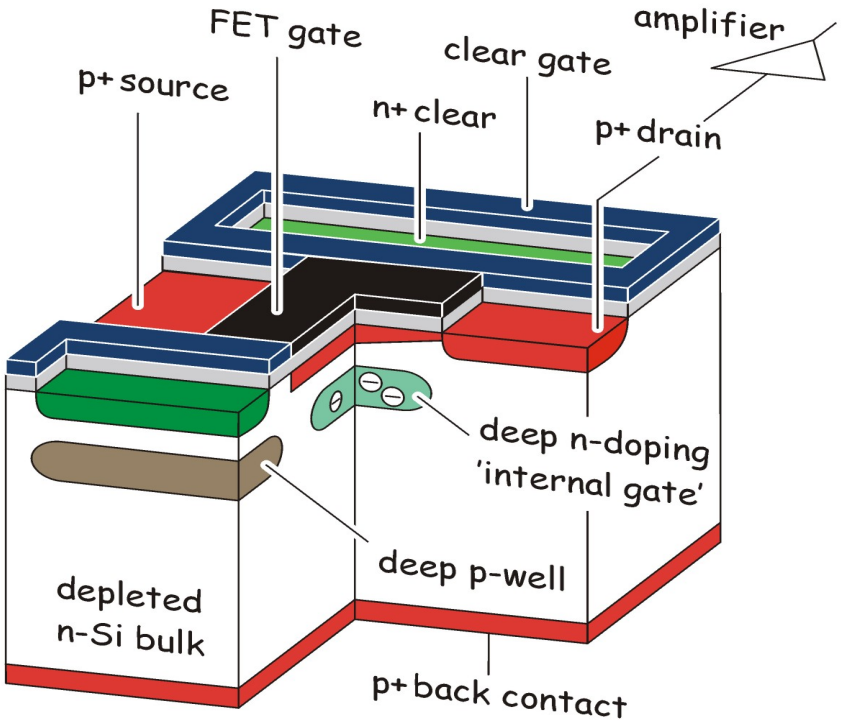
Material budget:
0.21 % X_0 per layer

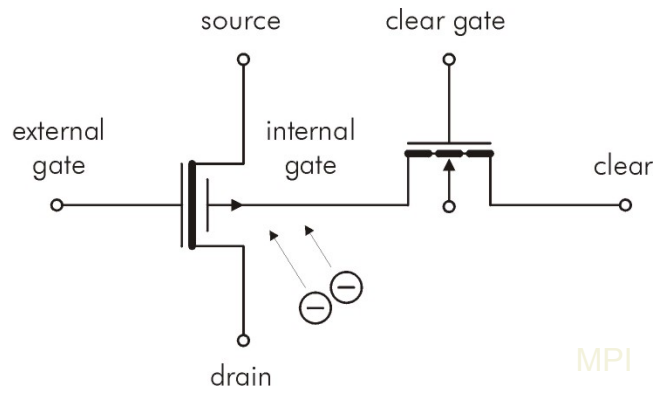
DEPFET

Depleted p-channel FET on high resistivity substrate (Kemmer & Lutz, 1987)

- First stage amplification in pixel
- Fully depleted bulk
- Charge is stored underneath an internal gate causing a modulation in the transistor current
- Charge needs to be cleared after readout
- Requires off-chip read-out circuitry

Used in the BELLE II pixel detector upgrade

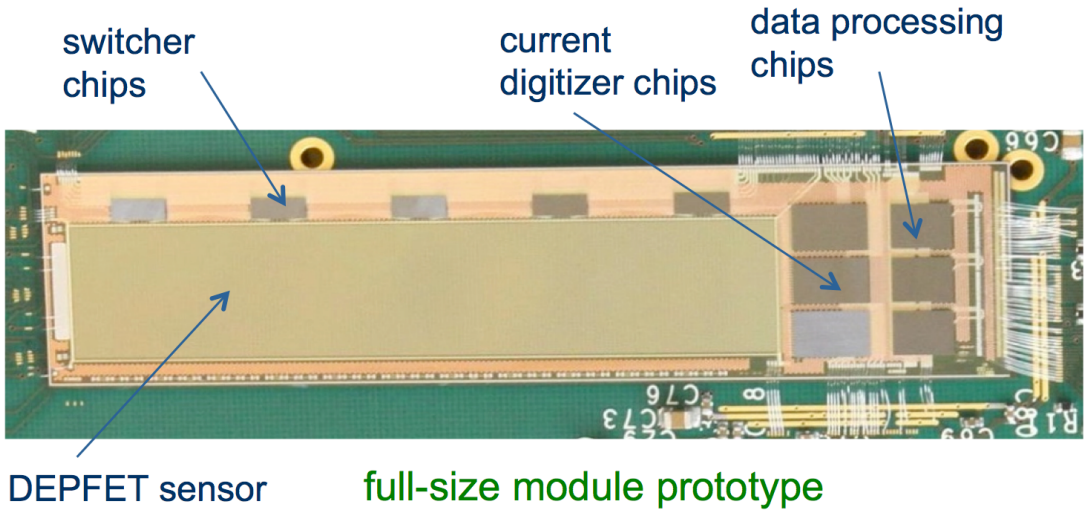


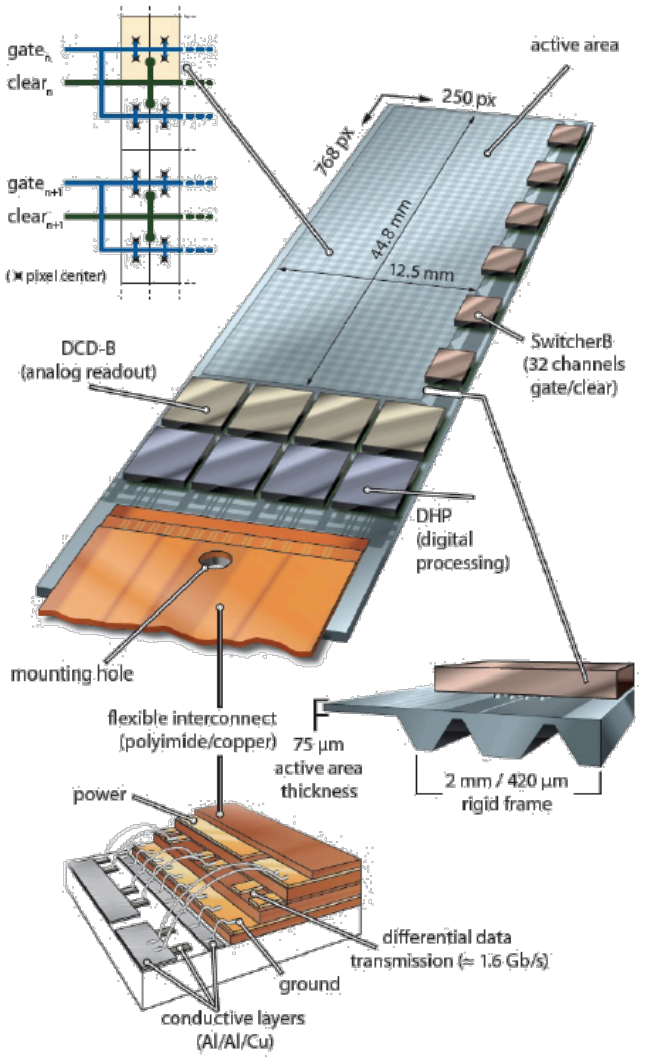


Belle II Pixel Detector at SuperKEKB

Ladder contains 2 half-modules with DEPFET sensor and auxiliary ASICS:

- First stage amplification in the pixel cell
- Three auxiliary ASICS bump bonded to the DEPFET sensor frame:
  - SWITCHER: row selection and clear
  - DCD-B: amplification and digitisation
  - DHP: pedestal subtraction and zero suppression, timing and trigger control



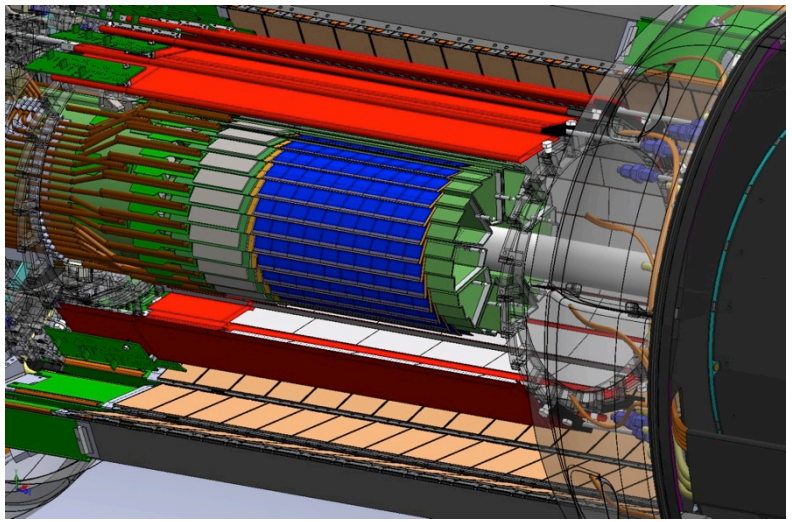


N. Wermes, CERN Seminar, 29/11/2013

STAR Heavy Flavour Tracker (HFT) at RHIC

Monolithic Active Pixel Sensors – **MAPS**

- **2 barrel layers**
- **ULTIMATE chip** developed by IPHC Strasbourg (2 cm x 2 cm)
- 0.35 µm CMOS process
- Pixel size 20.7 µm x 20.7 µm (hit res. 6 µm)
- Rolling shutter readout with discriminators at the end of column
- Integration time 185.6 µs, in-pixel CDS
- Power dissipation ~170 mW/cm² @ 3.3V
- Chips thinned to 50 µm



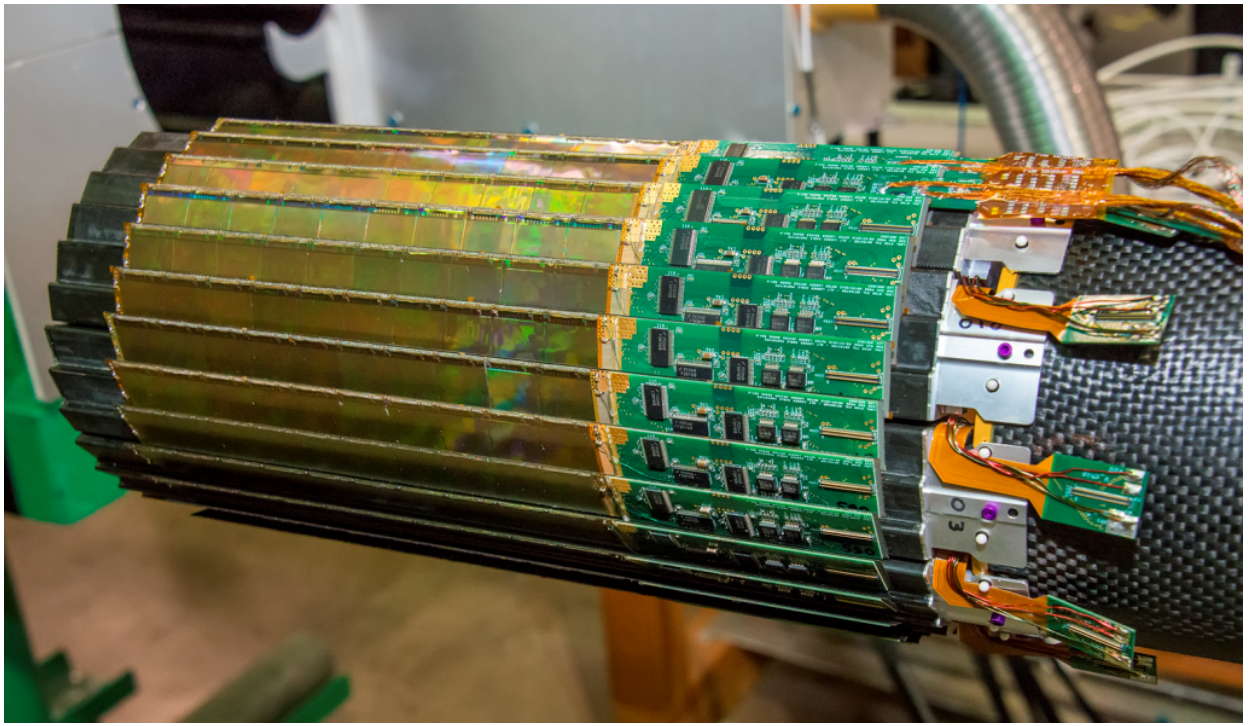
L. Greiner, FEE 2014

Radiation environment:
20 to 90 krad / year
$2*10^{11}$ to 10^{12} 1MeV n_{eq}/cm^2

Material budget:
0.37 % X_0 per layer

356 M pixels
~0.16 m^2

STAR Heavy Flavour Tracker (HFT) at RHIC



L. Greiner, FEE 2014

- **Detector installed end 2013, started data taking in Au-Au run 2014**
- Spare detector will be ready in about one month – will be used in the next run (1 day installation time)
- First operation experience shows resolution performance as expected

ALICE Inner Tracking System Upgrade at LHC

Based on high resistivity epi layer MAPS

3 Inner Barrel layers (IB)
4 Outer Barrel layers (OB)

Radial coverage: 21-400 mm

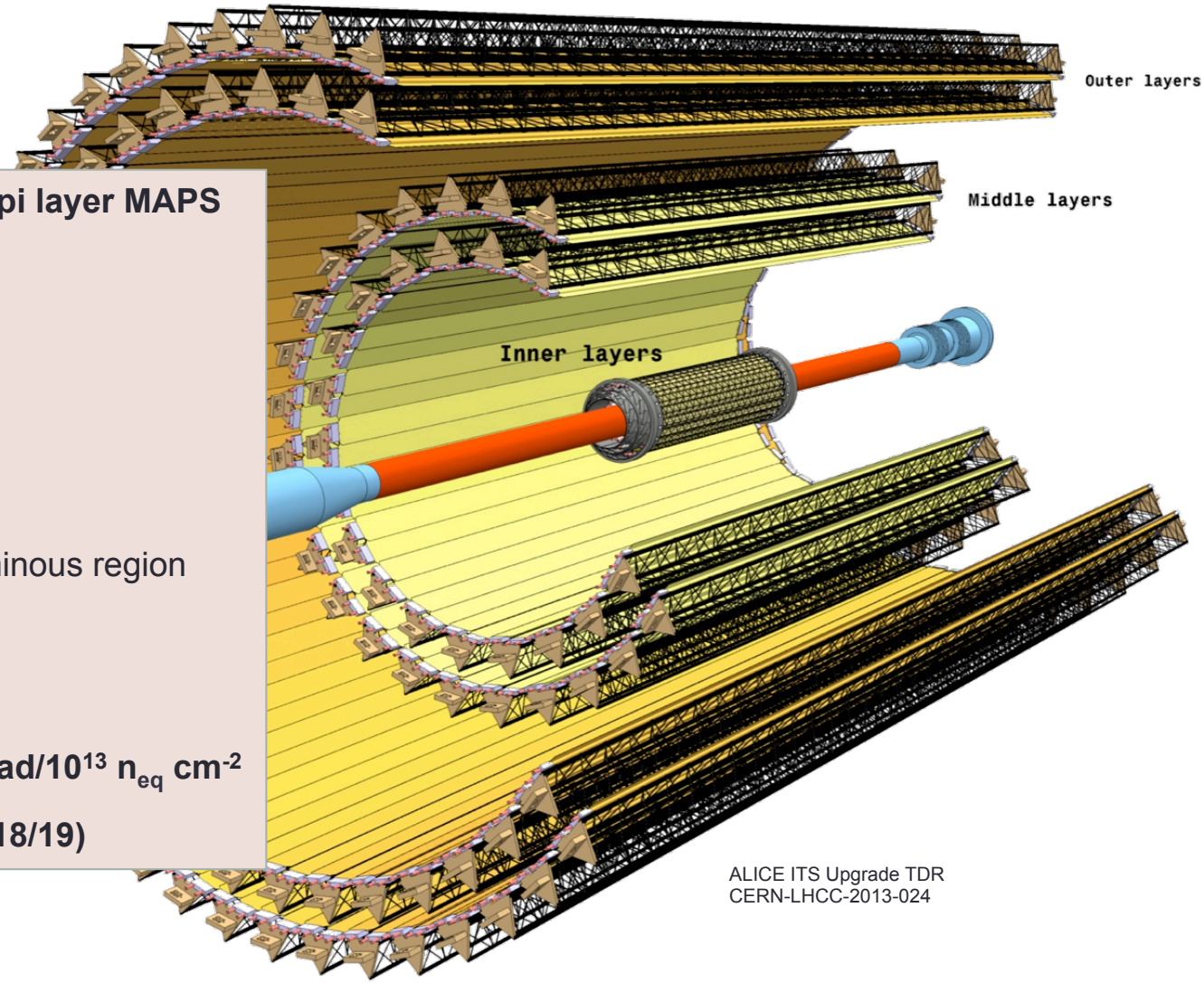
~ 10 m^2

$|\eta|<1.22$ over 90% of the luminous region

0.3% X_0/layer (IB)
0.8 % X_0/layer (OB)

Radiation level (L0): 700 krad/10^{13} n_{eq} cm^{-2}

Installation during LS2 (2018/19)



ALICE ITS Upgrade TDR
CERN-LHCC-2013-024

ALICE ITS Upgrade: High res epi layer MAPS

General Requirements*:

- Chip size: 15 mm × 30 mm
- Sensor thickness: 50 µm
- Spatial resolution: 5 µm / 10 µm
- Detection efficiency: > 99 %
- Fake hit rate: $< 10^{-5}$ evt^{-1}pixel^{-1}
- Integration time: < 30 µs
- Power density (mW/cm^2): < 300 / < 100
- Temperature: 20 °C to 30 °C
- TID rad. hardness (krad): 700 / 10
- NIEL rad. hardness (1 MeV n_{eq}/cm^2): 1×10^{13} / 3×10^{10}

* Colour code: Inner Barrel / Outer Barrel, if not equal

F. Reidt, Vertex 2014

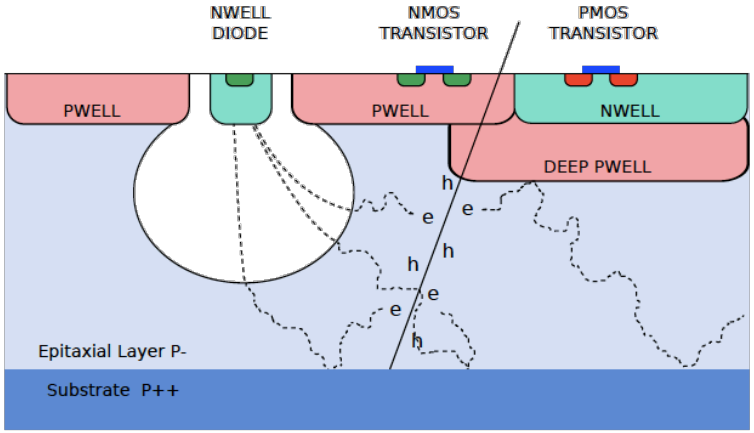
- Very **thin sensors**
- Very **high granularity**
- **Large area** to cover
- **Modest radiation levels**

Monolithic silicon pixel sensors

ALICE ITS Upgrade: High res epi layer MAPS

N-well collection electrode in high resistivity epitaxial layer (>1kohmcm)
TowerJazz 0.18 um CMOS Imaging Process

- Special deep p-well for full CMOS within matrix (based on experience of RAL)
- 6 metal layers -> suited for high density, low power circuitry
- Small n-well diode (2-3 µm diameter), ~ 100 times smaller than pixel → low capacitance
- 3 nm gate oxide -> TID tolerant
- Epi thicknesses 20-40 µm tested → higher cluster signal
- Partial depletion of the epi layer (limited by circuitry)



Schematic cross-section of CMOS pixel sensor
(*ALICE ITS Upgrade TDR*)

NWELL diode output signal:

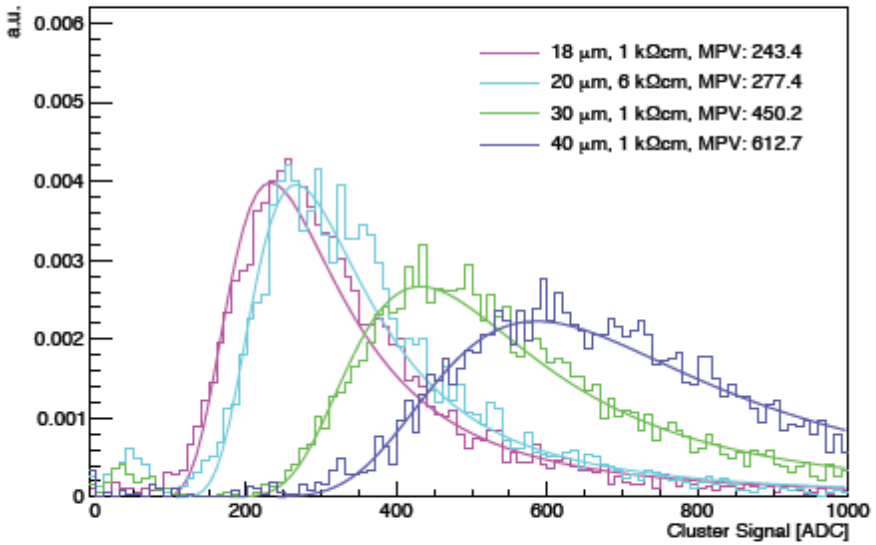
$$V \sim Q/C$$

- Increase charge collected by the central pixel
- Minimize capacitance:
  - diode surface
  - depletion volume

→ (reverse substrate) bias

ALICE ITS Upgrade: High res epi layer MAPS

Analogue prototype chip (Explorer1) with variable integration and readout time, two different pixel pitches (20 µm, 30 µm) → study of charge collection, reverse bias, noise



Epitaxial Layer		
Type	Thickness [µm]	Resistivity [kΩ cm]
HR-18	18	> 1
HR-20	20	6.2
HR-30	30	≈ 1
HR-40A	40	≈ 1
HR-40B	40	7.2

Cluster signal for different epi thicknesses at $V_{bb} = -6\,V$ measured at test beam at DESY with 3.2 GeV/c electron beam (pixel size 20× 20 µm²)

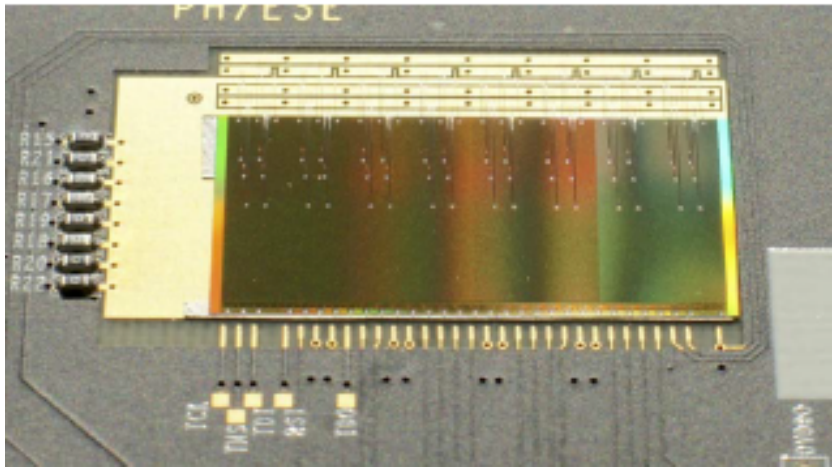
J. Van Hoorne, TIPP2014

Pixel Chip Full-Scale Prototypes in 2014

ALPIDE Full Scale prototype

- Dimensions: 30mm x 15 mm
- About 0.5 M pixels 28μm x 28μm
- 40 nW front-end (4.7mW / cm^2)
- ~40mW/cm^2 total
- Pulse width ~5 μs

Chips characterized at PS, SPS

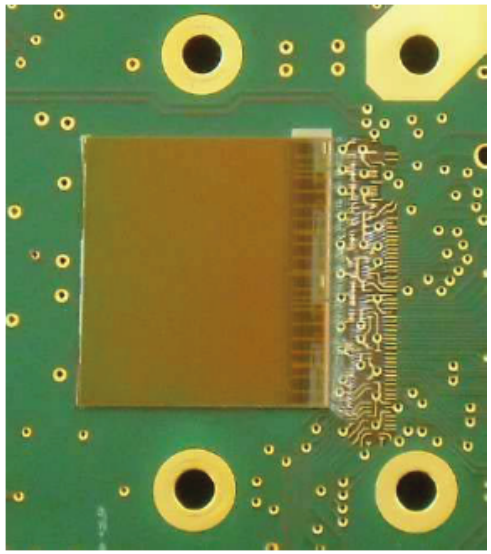


pALPIDEfs

MISTRAL FSBB-M0 (Full Scale Building Block Mistral 0)

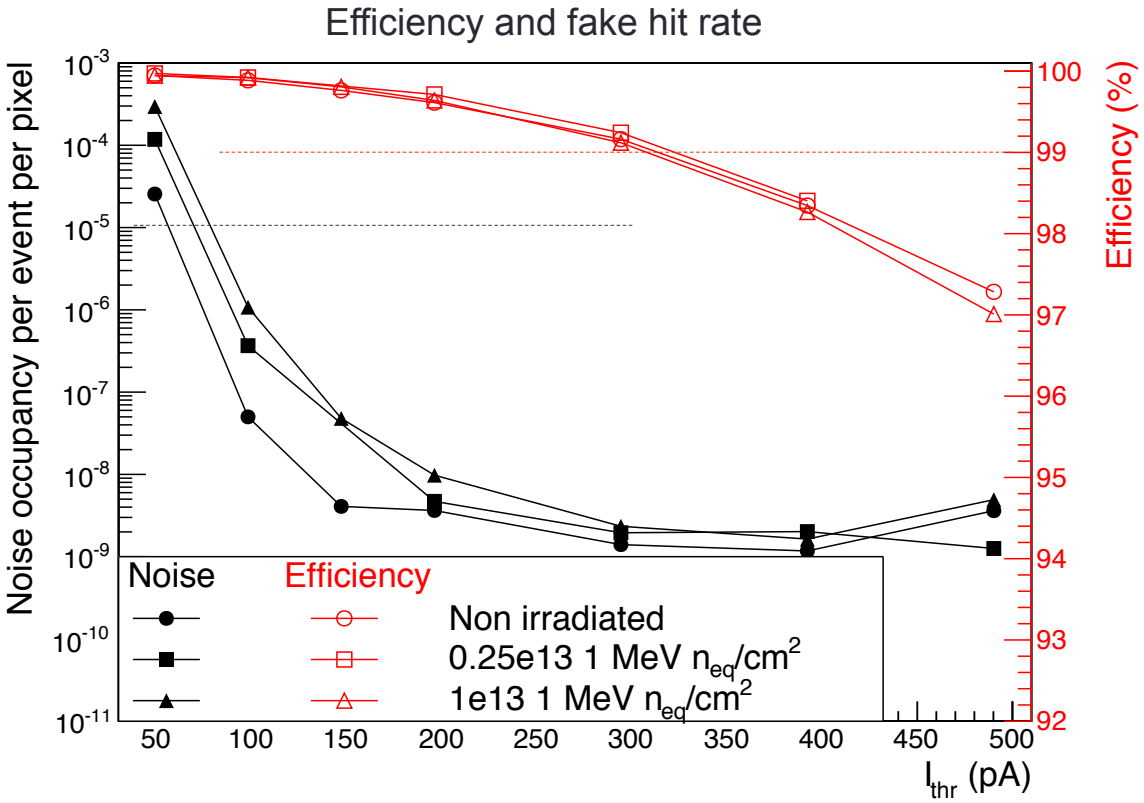
- About 1/3 of a complete sensor (approx. 9mm x 17mm)
- 416 x 416 pixels of 22μm x 33μm (final chip 36μm x 62μm)
- 40μs integration time (final chip ~ 20μs)
- Full chain working (front-end, discr., zero suppression)

Chips non-irradiated characterized at SPS



FSBB M0

pALPIDE-1 – Measurements at PS Test Beam

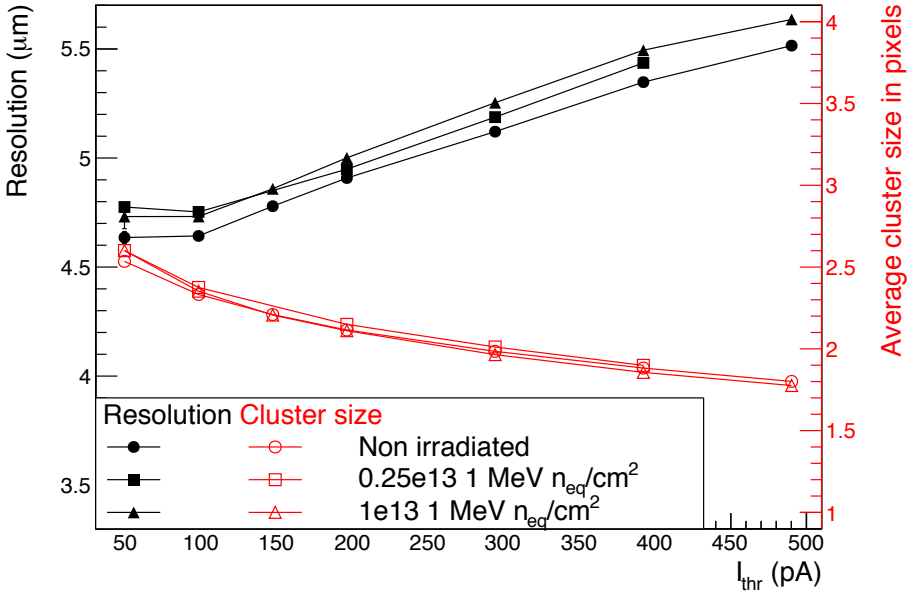


$\lambda_{fake} << 10^{-5}$ / event/pixel @ $\varepsilon_{det} > 99\%$ ➡ very large margin over design requirements

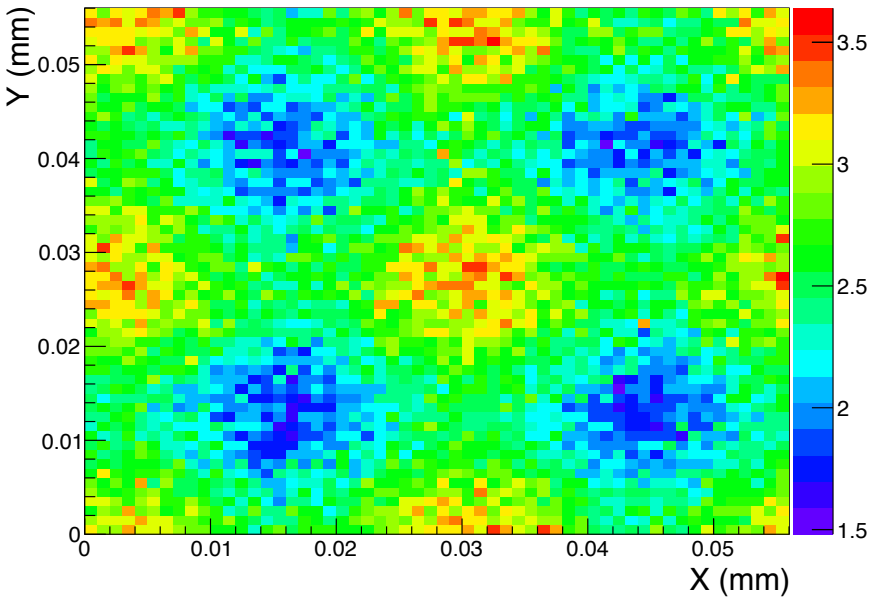
- Measurements at PS: 5 – 7 GeV π^-
- Results refer to 50 μm thick chips: non irradiated and irradiated with neutrons 0.25 x 10^{13} and 10^{13} 1MeV n_{eq} / cm^2 (10 x load expected in 6 years)

pALPIDE-1 – Measurements at PS Test Beam

Spatial resolution



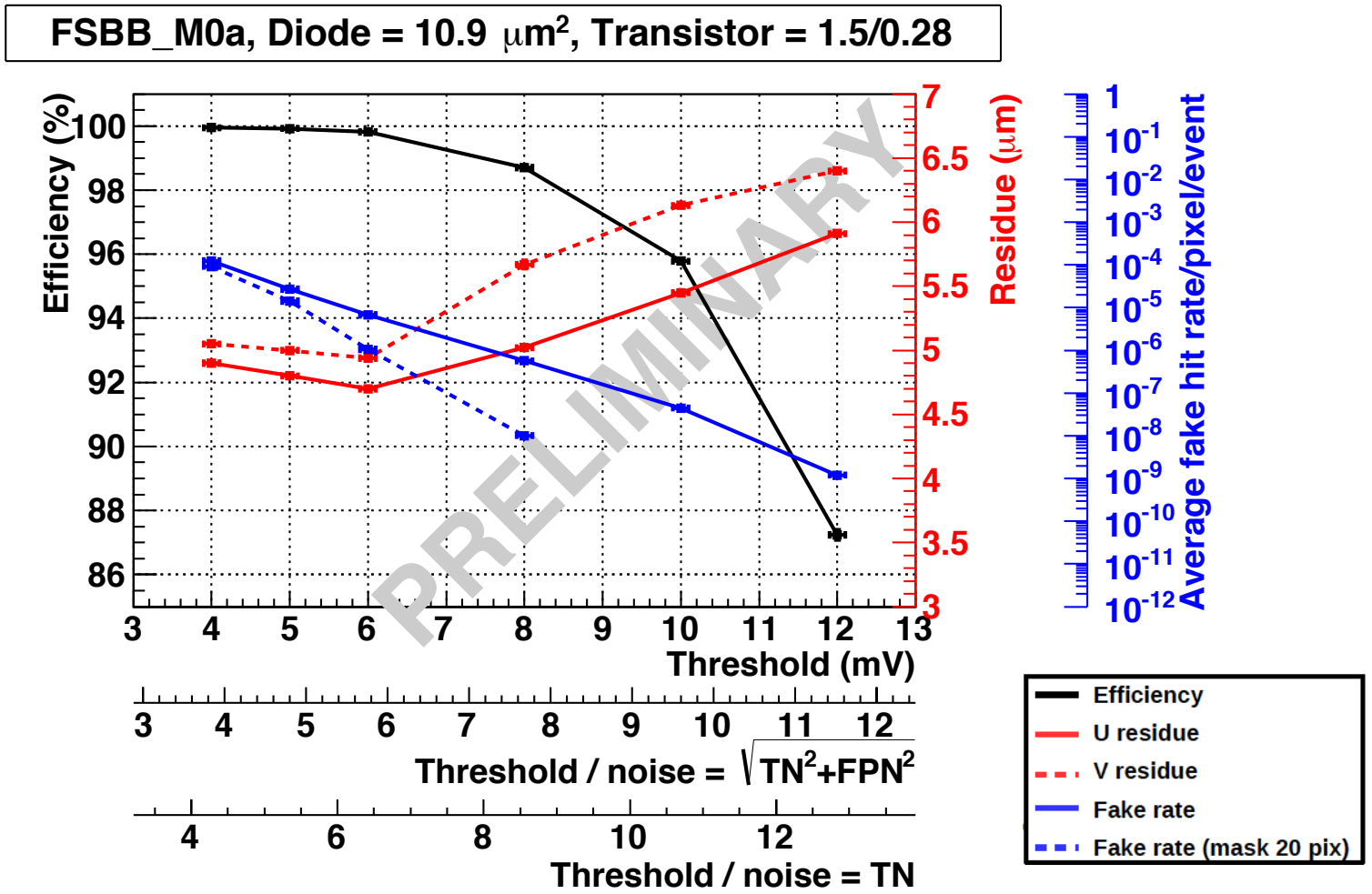
Cluster size vs. position within pixel



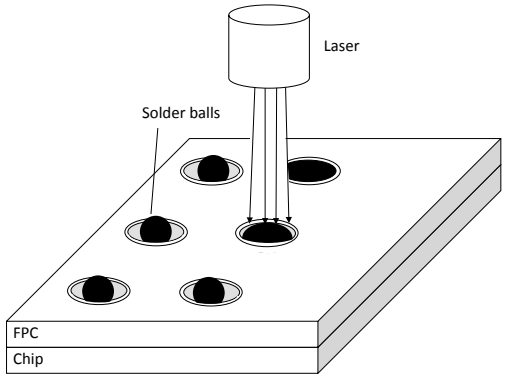
$\sigma_{det} < 5\ \mu m$ is achieved with sufficient margin of operation

- Measurements at PS: 5 – 7 GeV π^-
- Results refer to 50 μm thick chips: non irradiated and irradiated with neutrons 0.25 x 10^{13} and 10^{13} 1MeV n_{eq} / cm^2 (10 x load expected in 6 years)

MISTRAL-FSBB – Measurements at SPS Test Beam

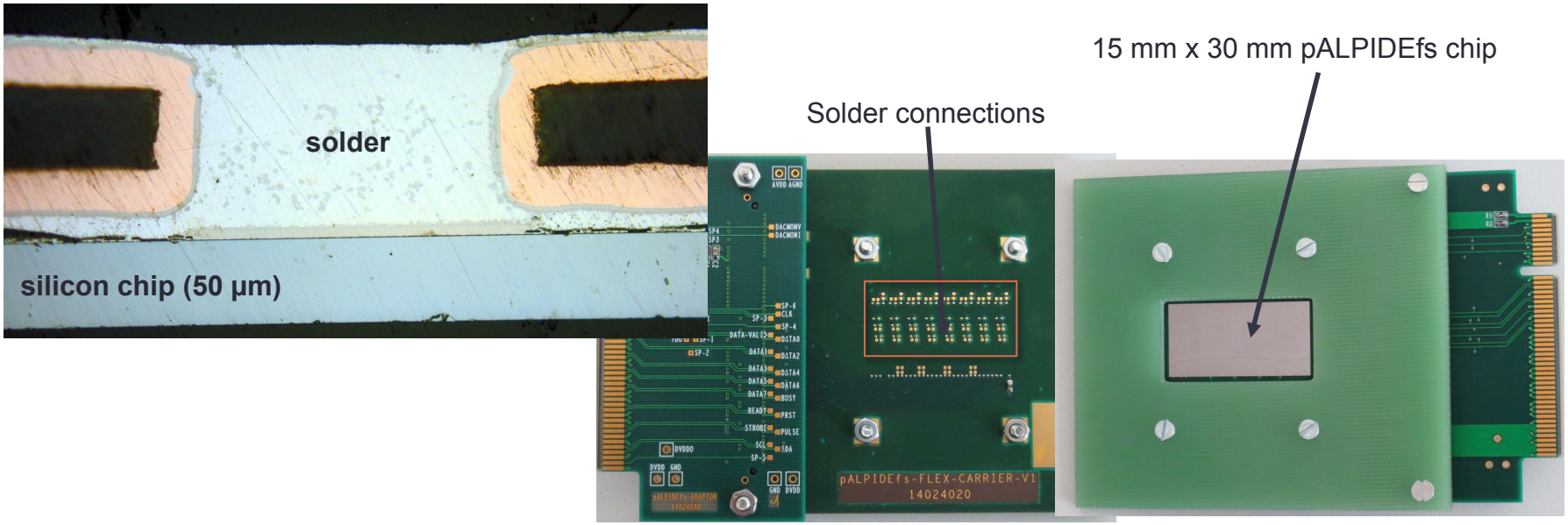


ALICE Inner Tracking System Upgrade



Laser soldering developed for module assembly:

- Solder balls (200 µm diam.) placed in metallized flex vias
- Soldered directly onto the chip pad using IR laser
- Solder points distributed across the full pixel chip surface → provide electrical and mechanical connection to the flex (no glue!)



Radiation Load - Inner Tracking Regions

	Fluence [n_{eq}/cm^2 per lifetime]	Ion. Dose [Mrad per lifetime]
LHC (10^{34} $cm^{-2}s^{-1}$)	2 x 10^{15}	79
HL-LHC (10^{35} $cm^{-2}s^{-1}$)	2 x 10^{16}	>500
LHC HI (6 x 10^{27} $cm^{-2}s^{-1}$)	10^{13}	0.7
RHIC (8 x 10^{27} $cm^{-2}s^{-1}$)	few 10^{12}	0.2
SuperKEKB (10^{35} $cm^{-2}s^{-1}$)	~3 x 10^{12}	10
ILC (10^{34} $cm^{-2}s^{-1}$)	10^{12}	0.4

N. Wermes, CERN Seminar, 29/11/2013
Lifetime: LHC, HL-LHC: 7 years; ILC: 10 years; others: 5 years

FCC phase I: 2.8 10^{16} n_{eq} cm^{-2} , 9 MGy
FCC phase II: 2.8 10^{17} n_{eq} cm^{-2}, 90 Mgy

(W. Riegler, FCC-hh workshop, Feb. 3, 2015)

Towards More Radiation Tolerance and Speed

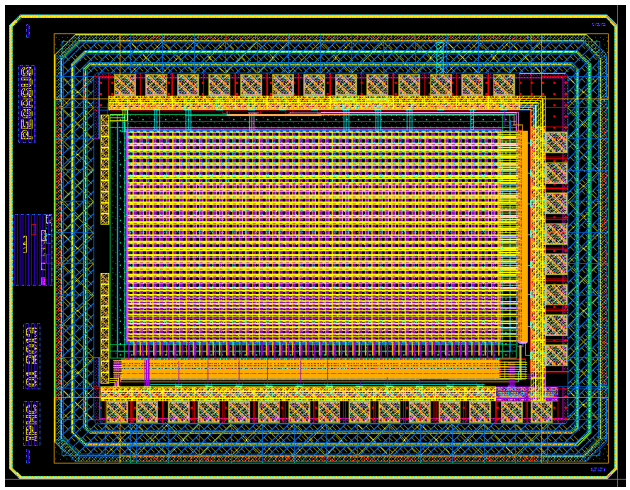
Moving towards smaller CMOS nodes: reduce sensitivity to TID due to smaller gate oxide thickness (traditional MAPS produced 0.35 µm CMOS → 0.18 µm CMOS or lower)

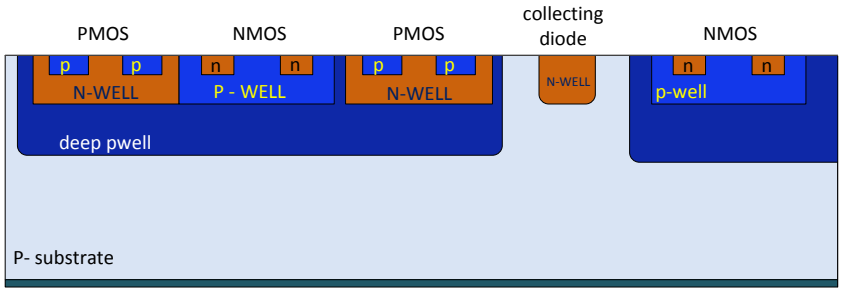
Collection of the charge (mainly) by drift → need to deplete collection layer: less sensitive to NIEL damage, faster signal collection

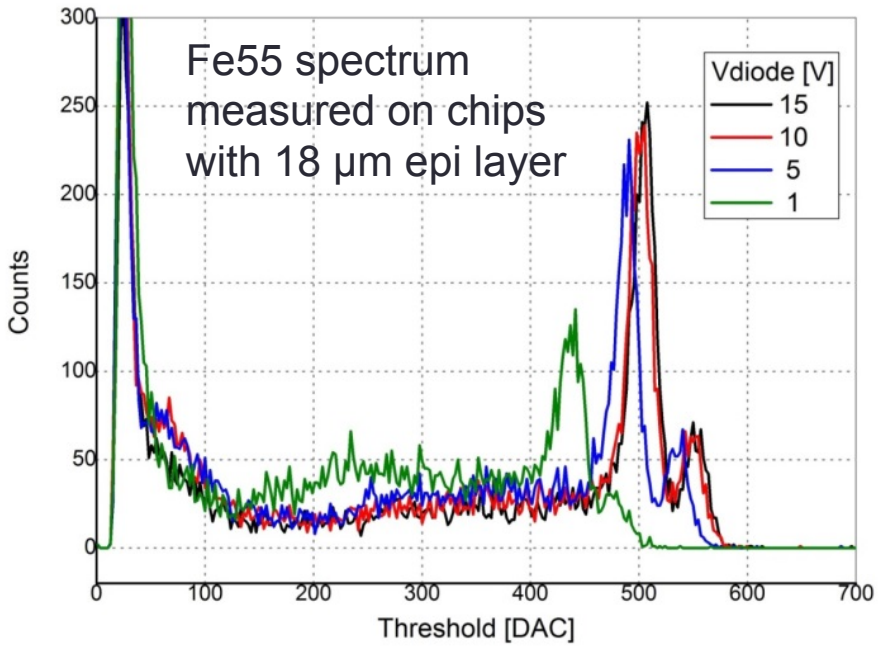
- **Junction on the front with circuit in a well**: possible, but requires high circuit well voltage and ac coupling, easier with simple circuit (e.g. Dulinski et al, Pegasus, CPIX14)
- **Circuit in collection electrode:** HV/HR CMOS, radiation tolerance demonstrated, but needs simple circuit to maintain reasonable capacitance (e.g. I. Peric, CPIX14)
- **Junction on the back:** works, but not in part of standard foundries processes, alternatives under study (e.g. Lauxtermann, CPIX14)
- **Silicon on Oxide:** significant progress, addressing challenges: charging of oxide, circuit-sensor-interaction (e.g. Arai et al, CPIX14)

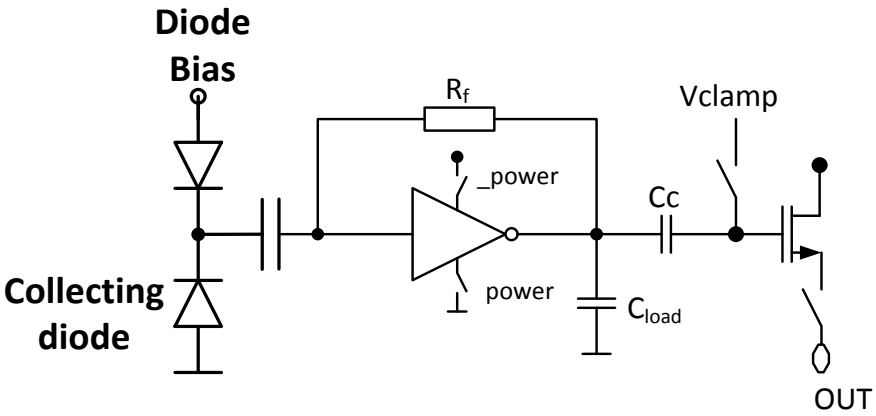
Example: Pegasus

- 180nm CMOS (Tower)
- Various types of epi in submission
- 25 x 25µm^2 pixels
- Matrix - 56x32 with 4 versions of pixels
  - Two source followers
  - Two amplifiers





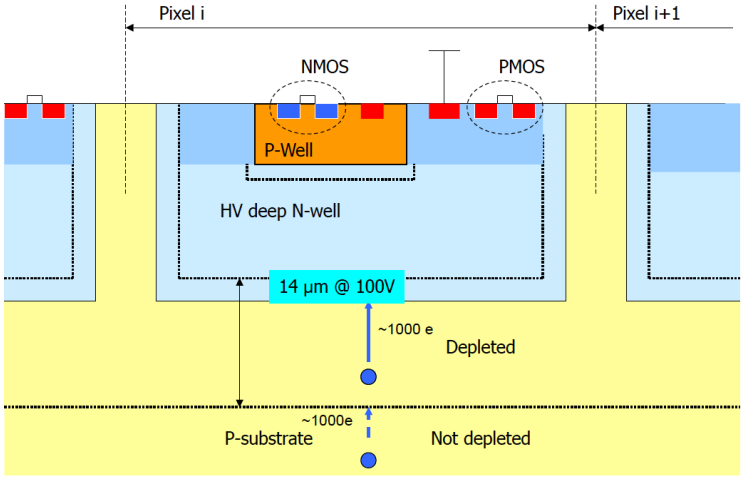




Example: HV CMOS

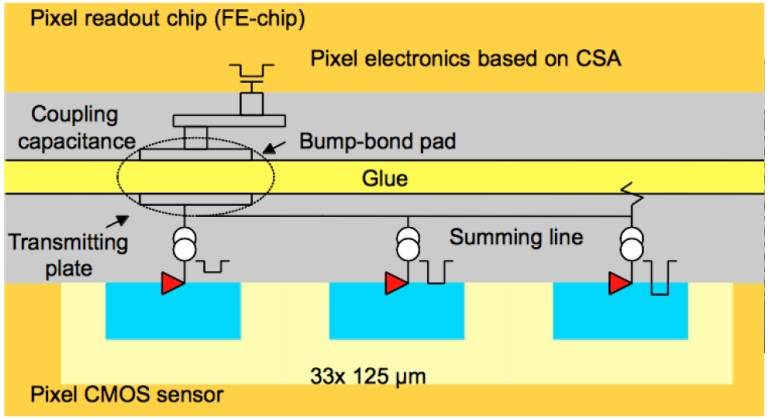
CMOS process with deep n-well collection electrode

- Structures realized in 0.18 and 0.35 µm CMOS
- Substrate resistivity ~ 10 Ohmcm
- **Biasing of the substrate up to ~100V →** homogeneous depletion layer (~ 14 µm deep)
- First stage amplification in pixel and additional electronics (e.g. discriminator etc.) possible
- Radiation tests with FEI-4 glue bonded indicate radiation hardness up to 10^{16} $n_{eq}cm^{-2}$



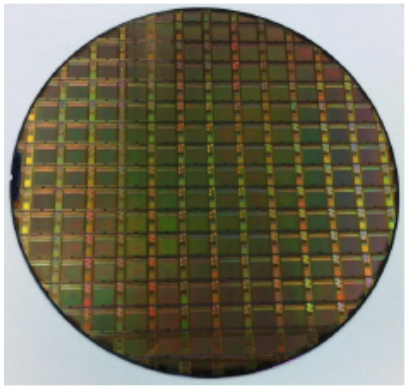
CMOS electronics placed inside the diode (inside the n-well)

D. Münstermann, VERTEX 2013

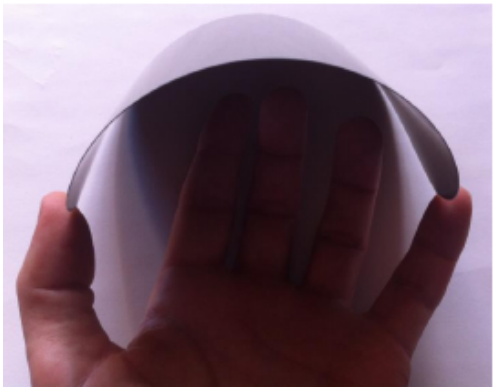


D. Münstermann, VERTEX 2013

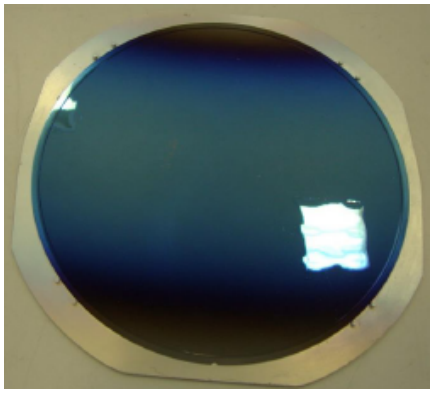
Example: Junction on the Back



Finished CMOS wafer on high resistivity



Wafer thinned to 50 um



Thinned wafer with anti-reflective coating

Chip mounted in camera

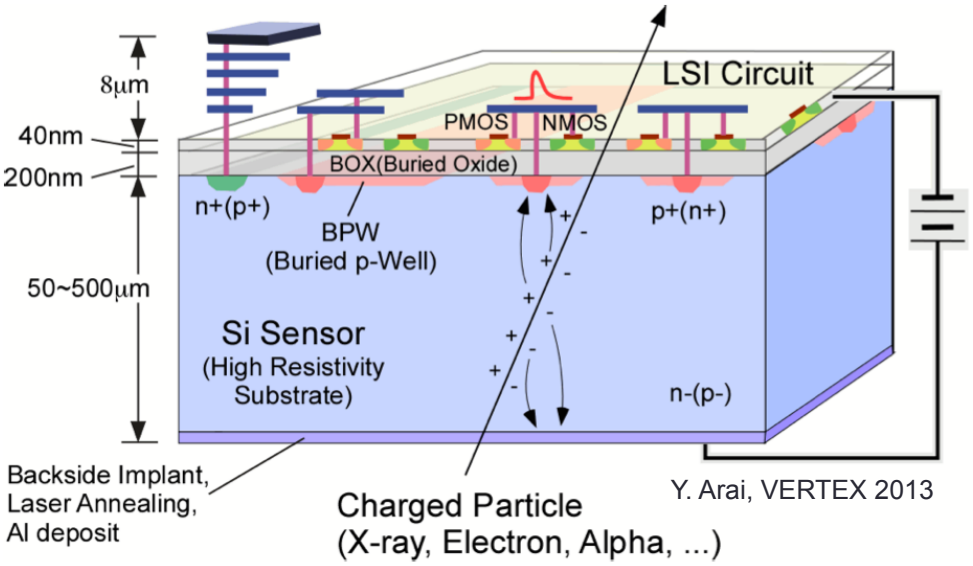
Example: post CMOS wafer thinning & back-side processing

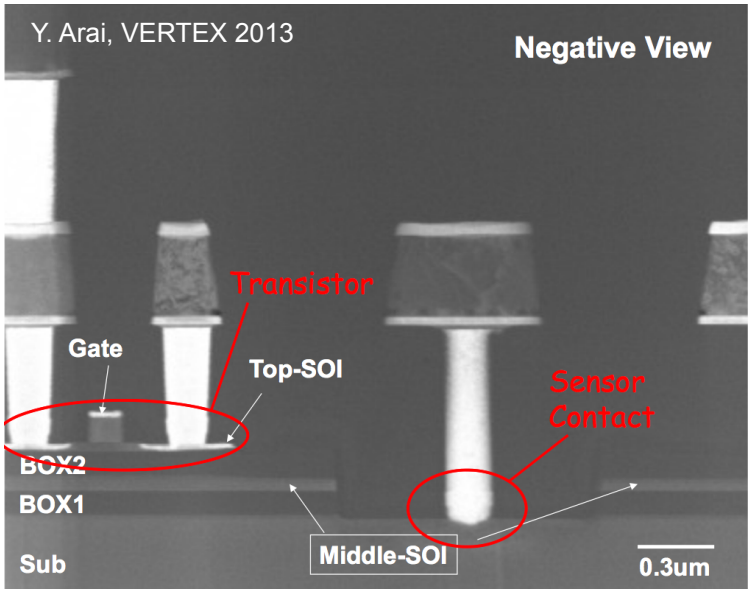
S. Lauxterman CPIX14

- several similar developments
- other possibility epi of opposite type as substrate
- In general:
  - Watch die edge/junction termination
  - Radiation tolerance to be investigated/confirmed

Example: SOI – Silicon On Insulator

- SOI wafer with high resistivity sensor part and thin CMOS chip connected via oxide
- Fully depleted thick sensing region with low C, offers good Q/C
- BOX causes reduced radiation tolerance, double BOX improves this, further development in progress.
- Is one of the ways to integrate large amount of in-pixel circuitry





TIPP2014: A. Takeda, H. Matsumura,T. Miyoshi, S. Honda

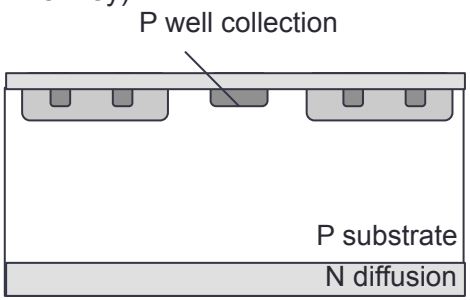
Ideally one would like to achieve:

- Low capacitance → low power
- Good S/N
- ~ns time resolution
- High rate capability (>10 MHz/mm^2)
- Full depletion → radiation tolerance
- Single sided processing → low cost mass production

No unique solution for all yet, but some aspects addressed

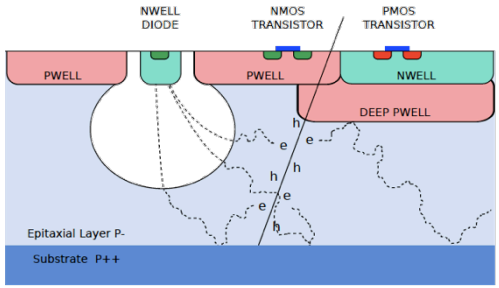
High resistivity substrate with back side processing and simple amplification stage in pixel, e.g:

- DEPFET (see next slides)
- Junction on the back (W. Snoeys, S. Parker, J. Plummer, C. Kenney)

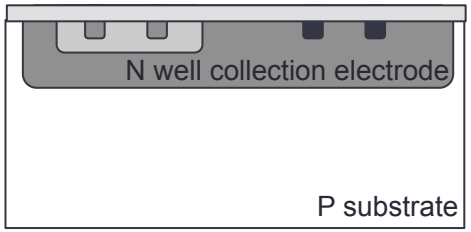


High resistivity epi layer with full CMOS circuitry in pixel:

- ALICE ITS upgrade (see next slides)



Schematic cross-section of CMOS pixel sensor (*ALICE ITS Upgrade TDR*)

All circuit inside deep n-well collection electrode, e.g:

- LePIX
- HV CMOS (see next slides)