IMB-CNM R&D Activities for Future Linear Colliders

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Out Line

- **R&D Basic Lines**
  - ✓ R&D Projects
  - ✓ Scientific Objectives
  - ✓ Technological Targets

- **Future Works**
  - ✓ N on P LGAD
  - ✓ P on P LGAD
  - ✓ Pad Diodes LGAD & microStrips
  - ✓ Resistive Electrodes
  - ✓ Thin Detectors
  - ✓ 6 inch Fabrication Process

R&D Basic Lines

- **R&D** Projects:
  - ✓ **Det4Hep** (FPA2010-22163-C02-01/02)
  - ✓ **PhysDetLc** (FPA2013-48387-C6-2-P)

- **Aim**:
  - ✓ R&D on Innovative **Tracking Technologies** for Future Experiments (LC, HL-LHC),
  - ✓ Play a **Leading Role** in the production of Silicon Detectors to be integrated in the **FTD** of the Future Linear Colliders.

Det4Hep Project. FPA2010-22163-C02-01/02

- **R&D** Lines:
  - ✓ **MicroStrip Detectors** for ILD Silicon Tracker
    - ➢ **Resistive** Sensors
    - ➢ **Thin** Sensors
    - ➢ **Semitransparent** Sensors
  - ✓ Low Gain Avalanche Pad Detectors (**LGAD**)

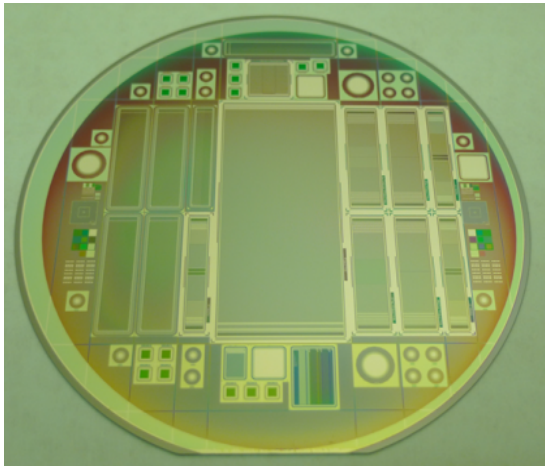


Figure 1. General view of a wafer with the new **resistive microstrip** detectors fabricated at IMB-CNM clean room

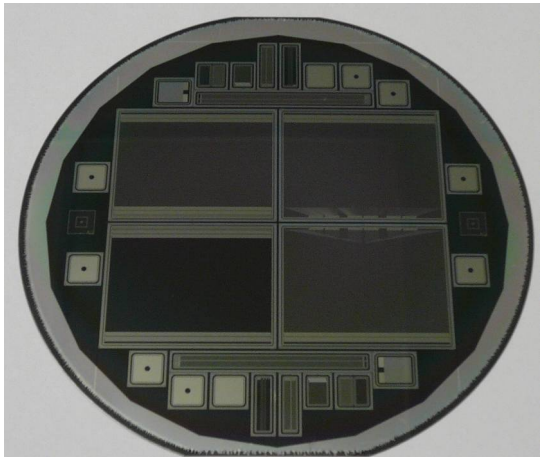


Figure 2. General view of a wafer with **thin substrate microstrips** detectors fabricated at IMB-CNM clean room

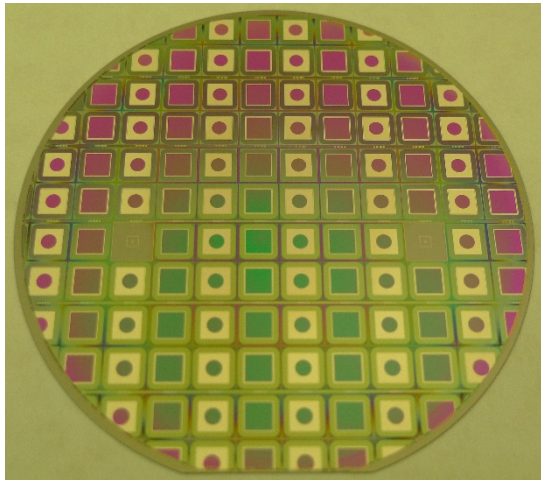


Figure 3. General view of a wafer with **LGAD** detectors (APD evolution) fabricated at IMB-CNM clean room

PhysDetLc Project. FPA2013-48387-C6-2-P

- Play a **Leading Role** in the production of Silicon Detectors to be integrated in the **FTD** of the Future Linear Colliders
  - ✓ **AC-coupled**, **200 µm** thick, microStrip sensors fabricated on **6 inch** wafers

- Development of **Low Gain Thin Resistive microStrip Detectors** on **6 inch** wafers
  - ✓ **Resistive** microStrips Detectors
  - ✓ **Thin** Detectors
  - ✓ Integrated **Gain** Concept
    - ➢ **New** microStrip Detectors with Integrated Gain
    - ➢ **Faster & Larger Area** Detectors
    - ➢ **More** Detectors per Wafer
    - ➢ **Lower** Material Budget

- Numerical Simulation Models Development
  - ✓ **New TCAD Libraries** definition to facilitate the detectors design and optimization

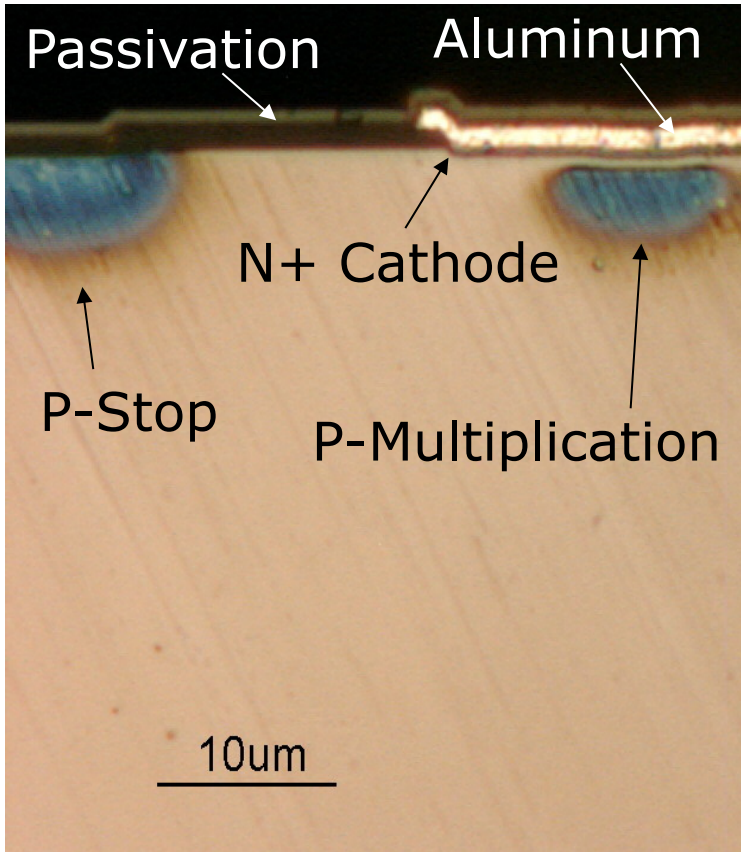
PhysDetLc Project. Technical Objectives

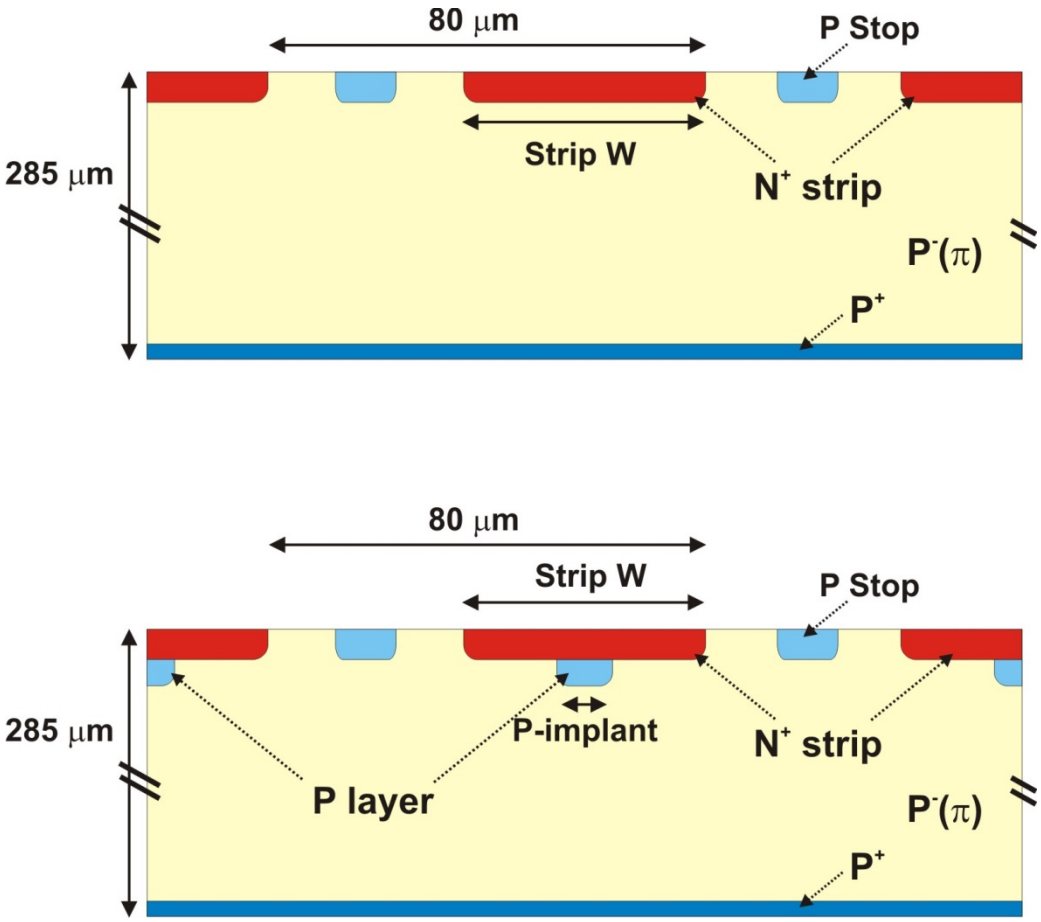
- **CNM Clean Room** adaptation to **produce** silicon detectors to be integrated in the **FTD** of the Future Linear Colliders
  - **Definition** of the Fabrication Processes on **6 inch** wafers
  - Fabrication Processes **Optimization**
  - Fabrication Technology **Stabilization**

- Development of **Low Gain Thin Resistive microStrip Detectors 6 inch** Fabrication Process

PhysDetLc Project. P on P MicroStrips with Low Gain

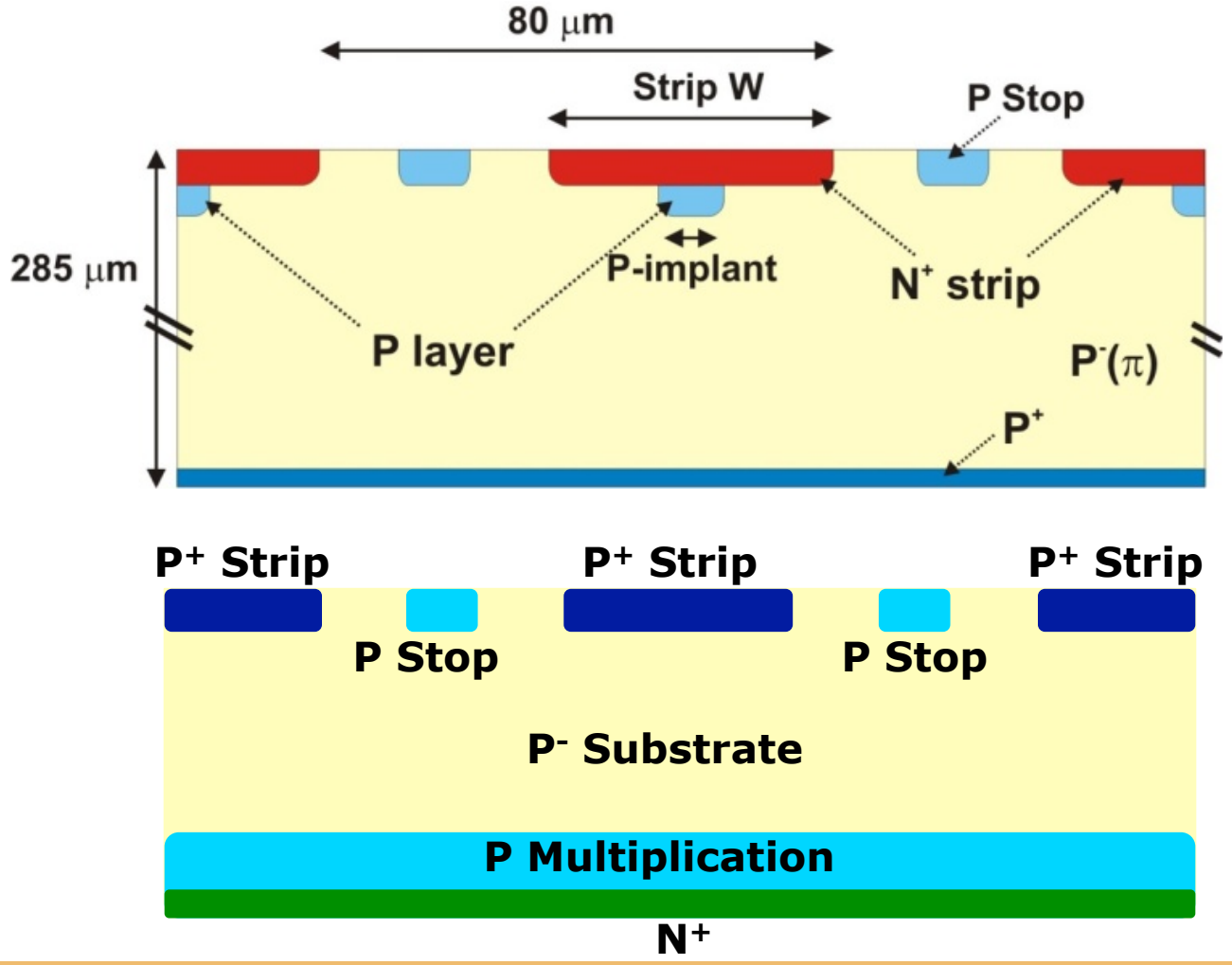
- **N on P** microStrips. **PiN** vs **LGAD**





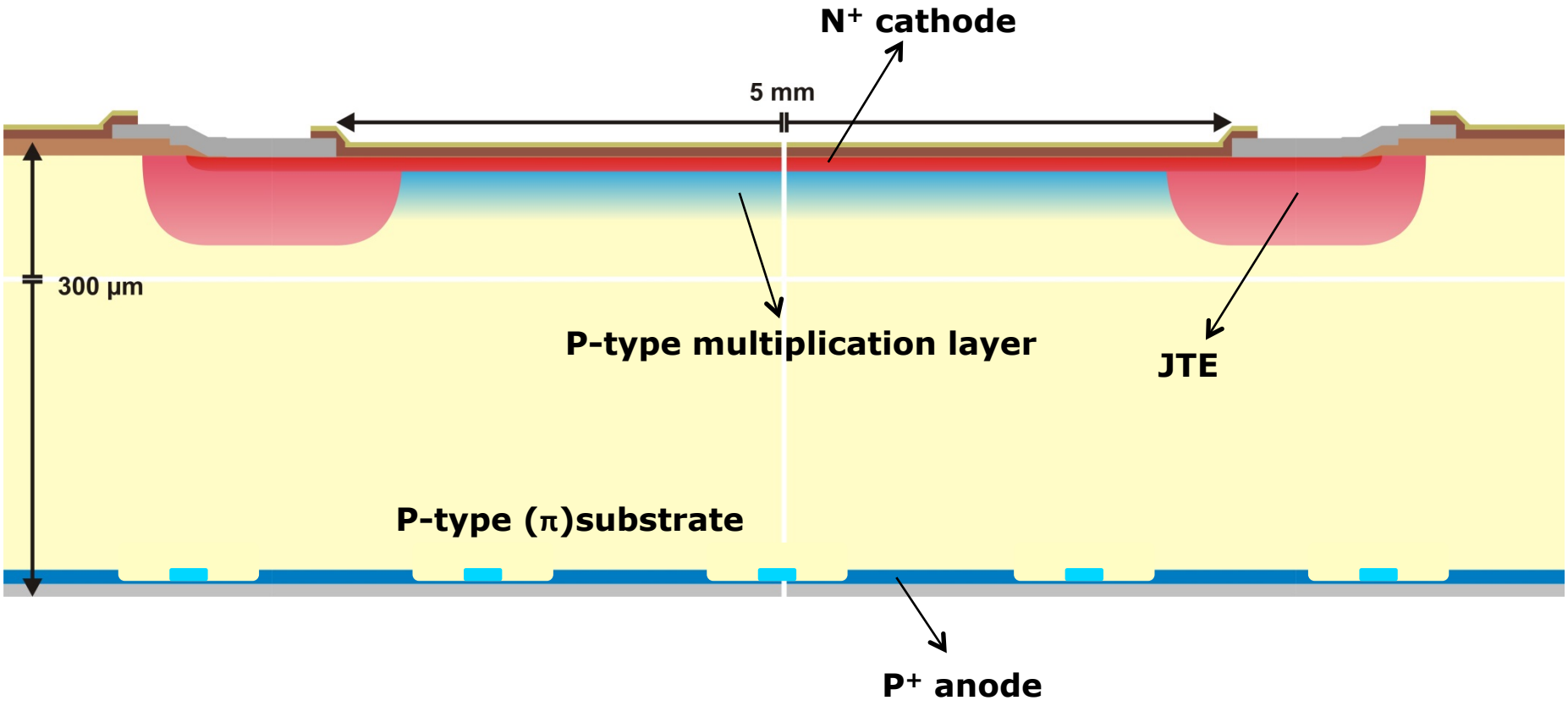
PhysDetLc Project. P on P MicroStrips with Low Gain

- **N on P** vs **P on P LGAD** microStrips Comparison



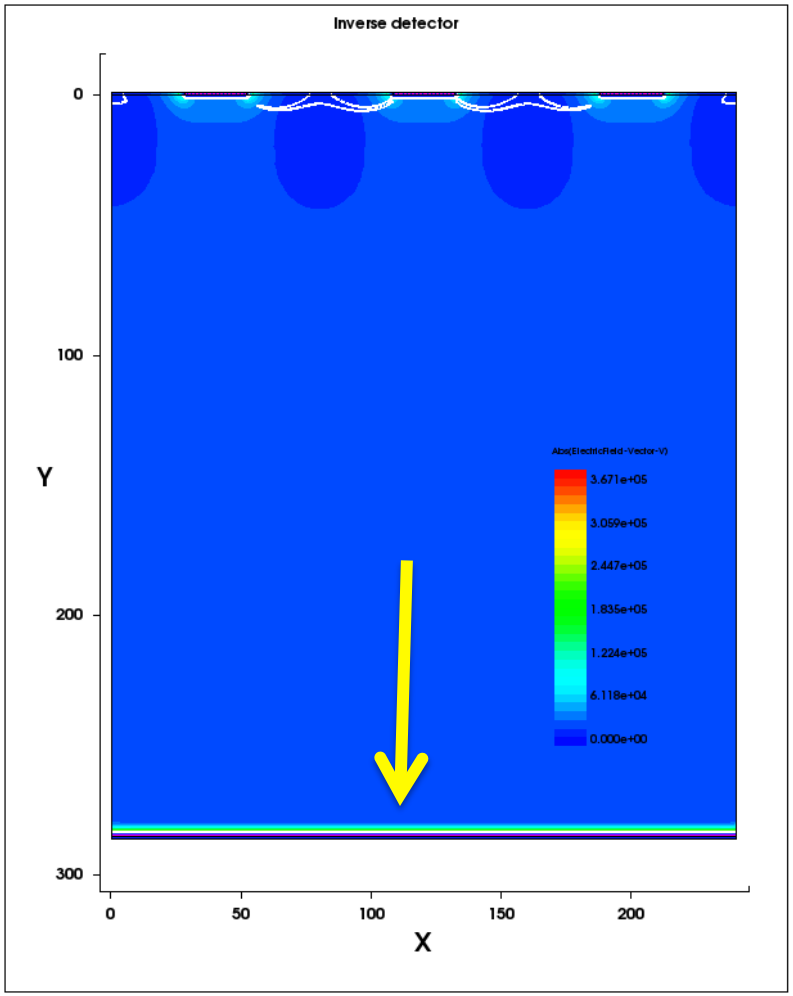
PhysDetLc Project. P on P MicroStrips with Low Gain

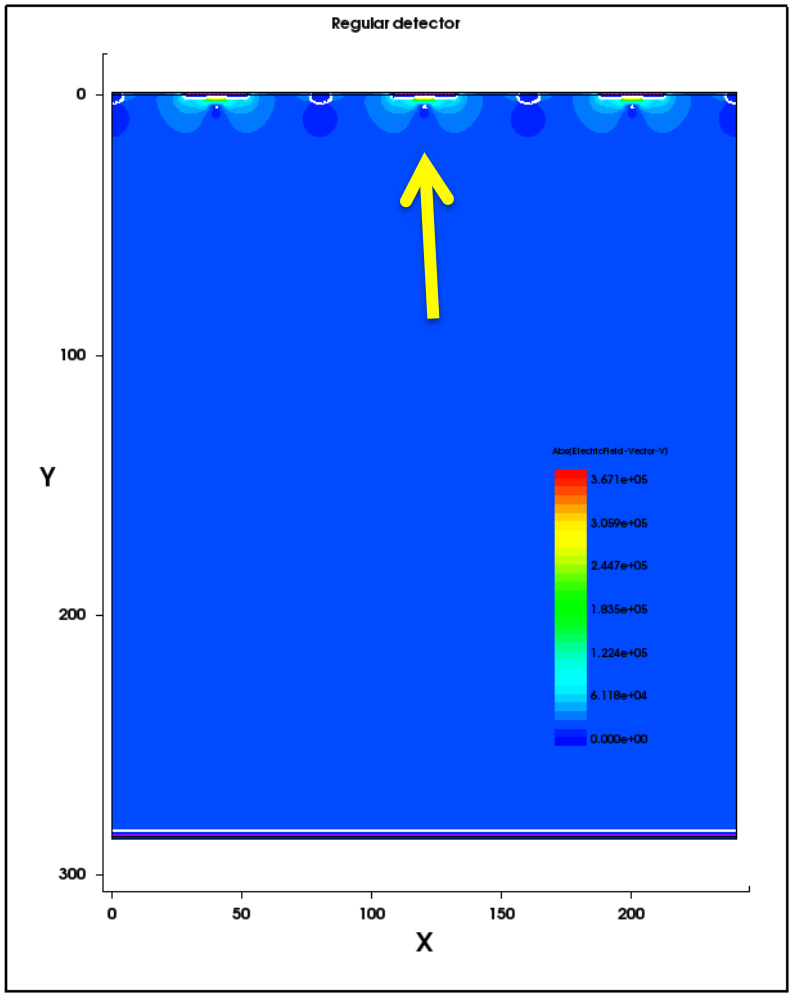
- **Pad Diodes LGAD** with P microStrips at Back Plane



PhysDetLc Project. P on P MicroStrips with Low Gain

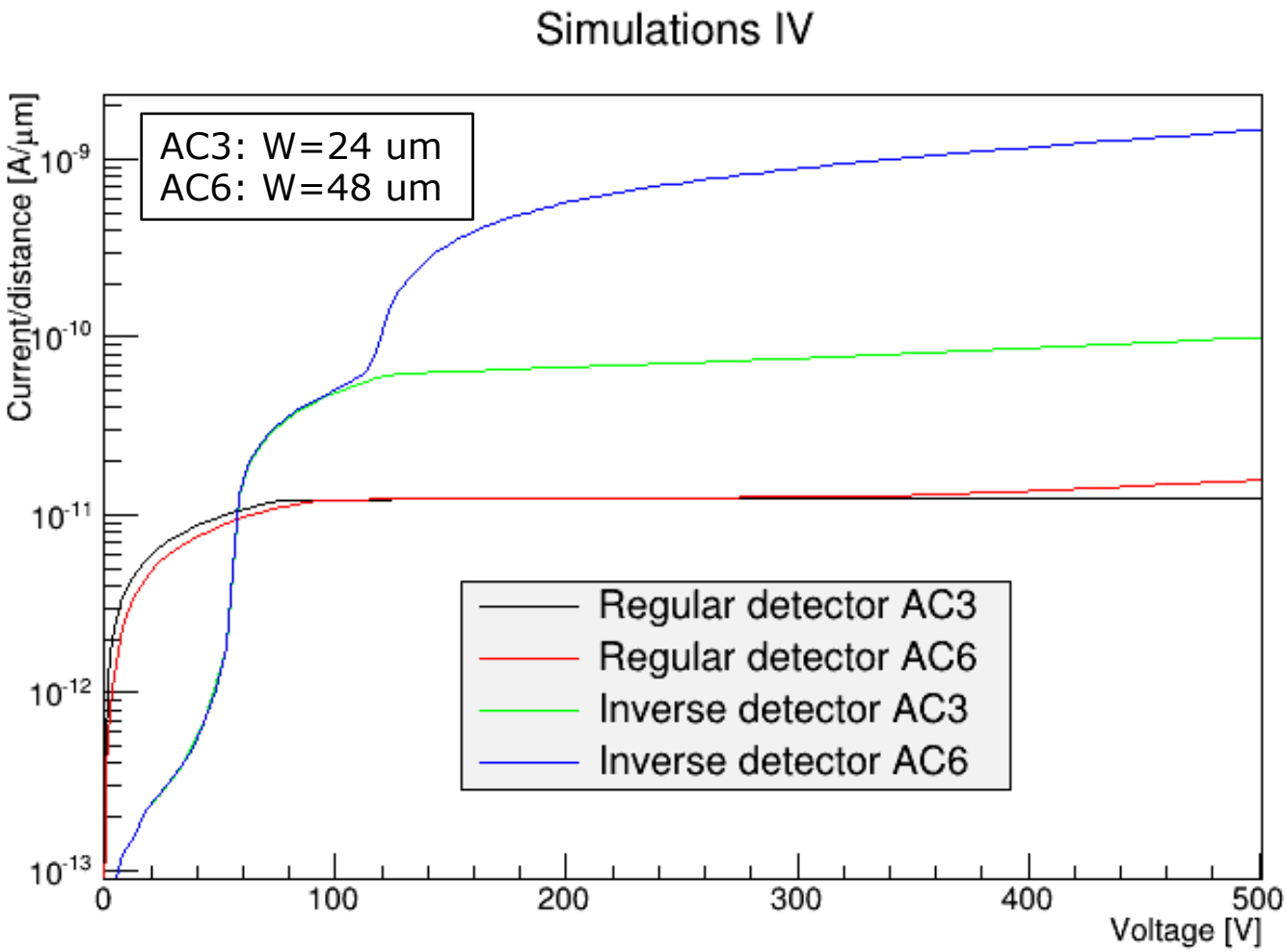
- **Three** microStrips Simulation. **Electric Field** 2D Distribution. **Maxim @ Junctions**





PhysDetLc Project. P on P MicroStrips with Low Gain

- **Three** microStrips Simulation. **I(V)**



PhysDetLc Project. P on P MicroStrips with Low Gain

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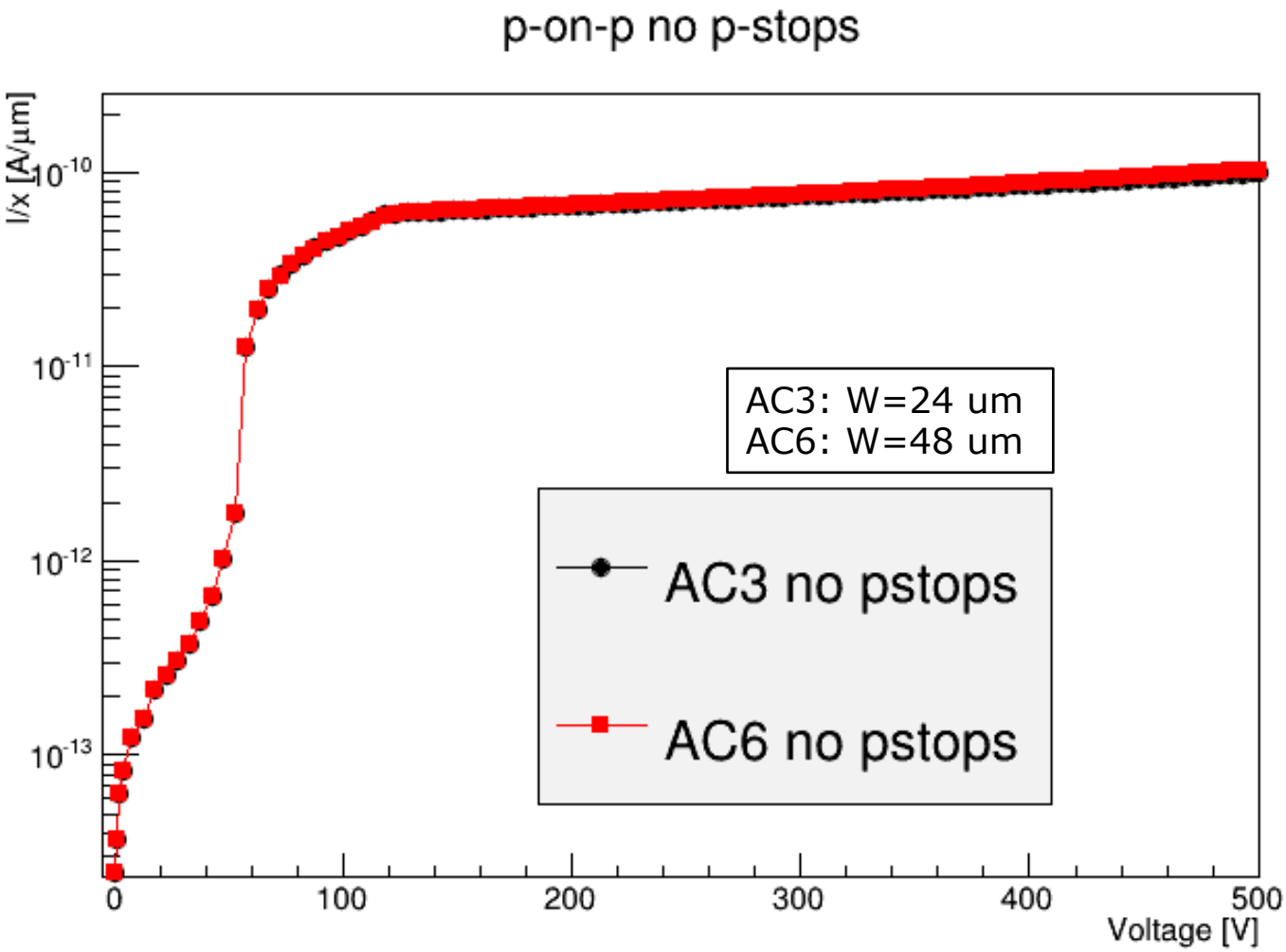
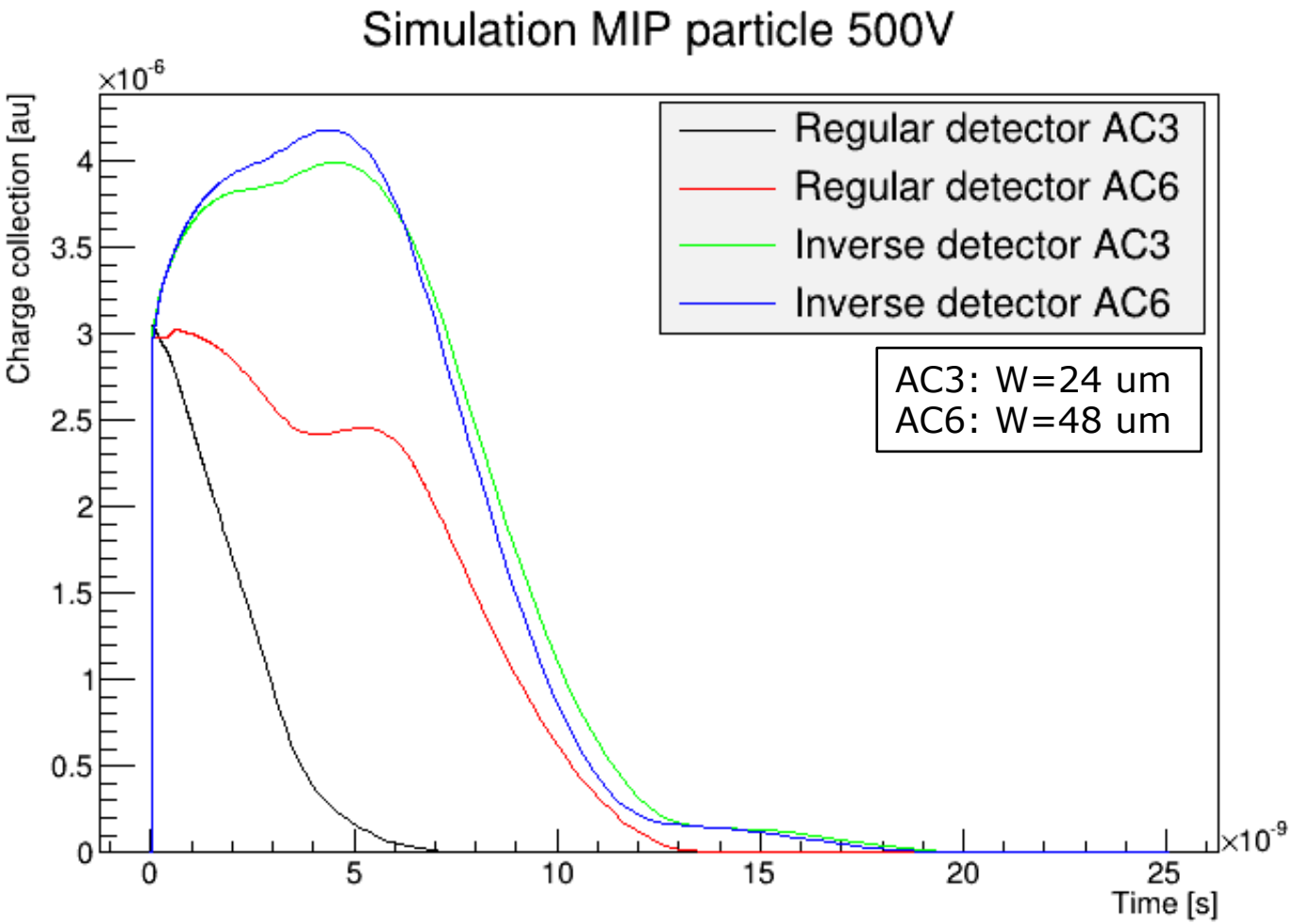


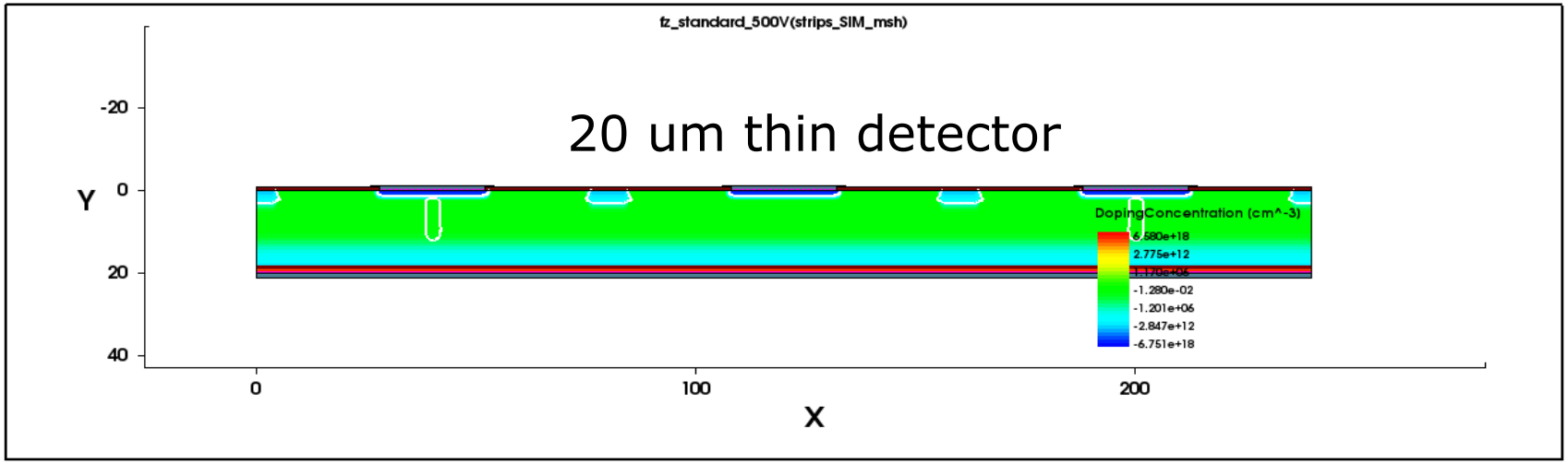
PhysDetLc Project. P on P MicroStrips with Low Gain

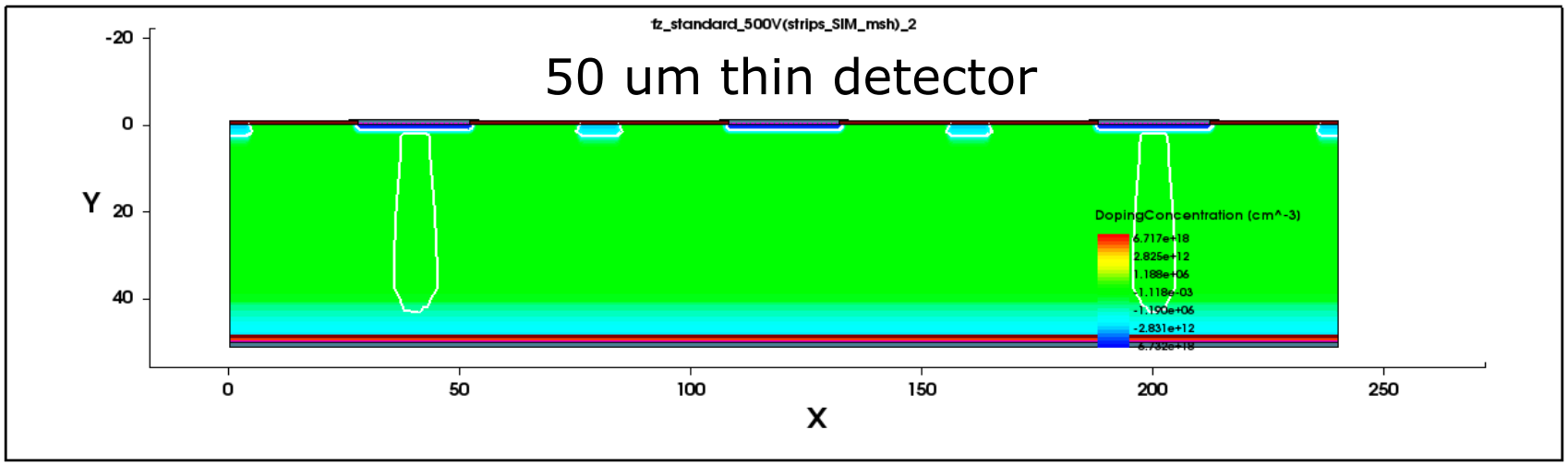
- **MIP** through the middle of the sensors (the central strip) **@ 500 V**



PhysDetLc Project. P on P LGAD MicroStrips. Thin Detectors

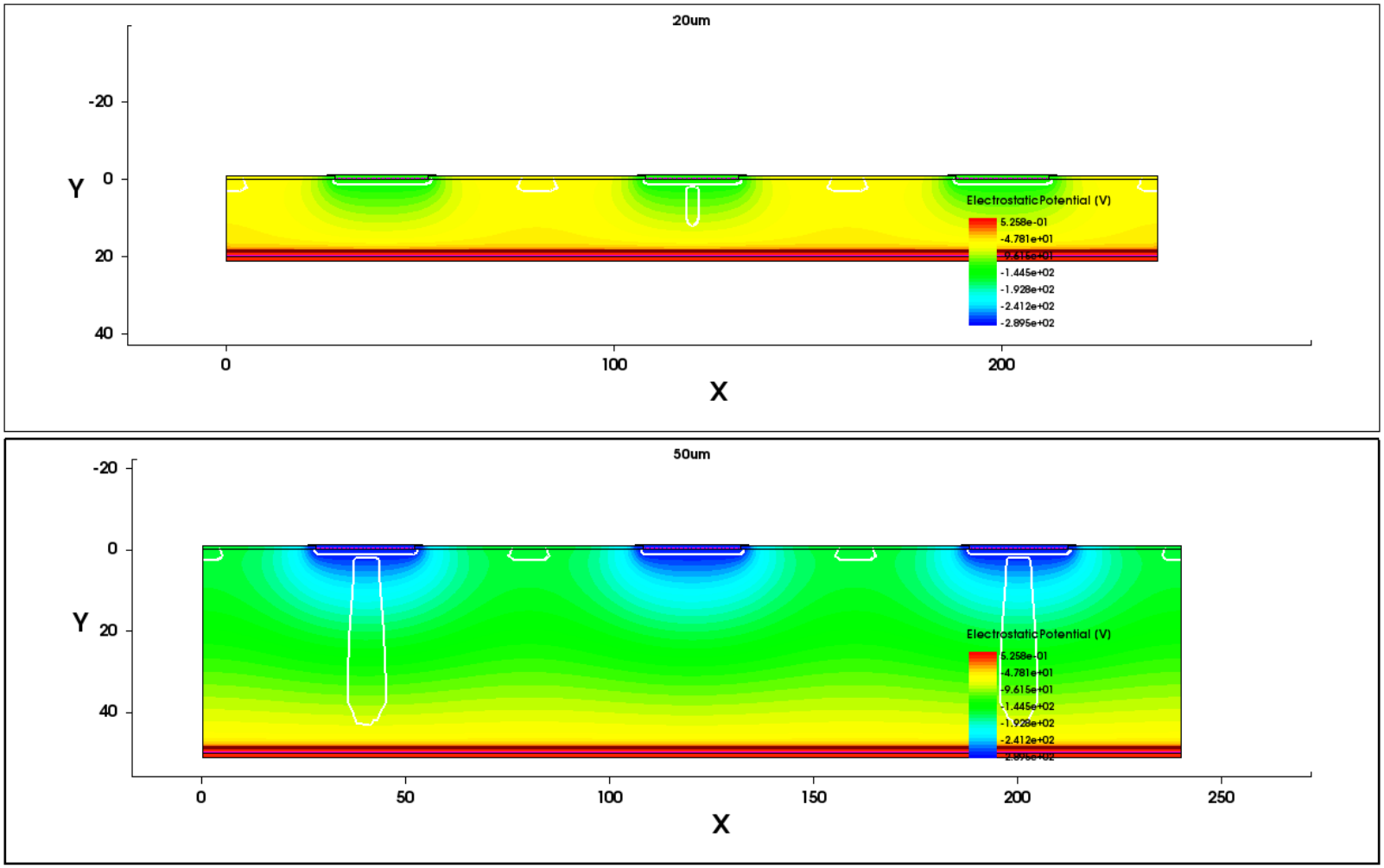
- **Three** microStrips Simulation. **Doping Concentration** 2D Distribution





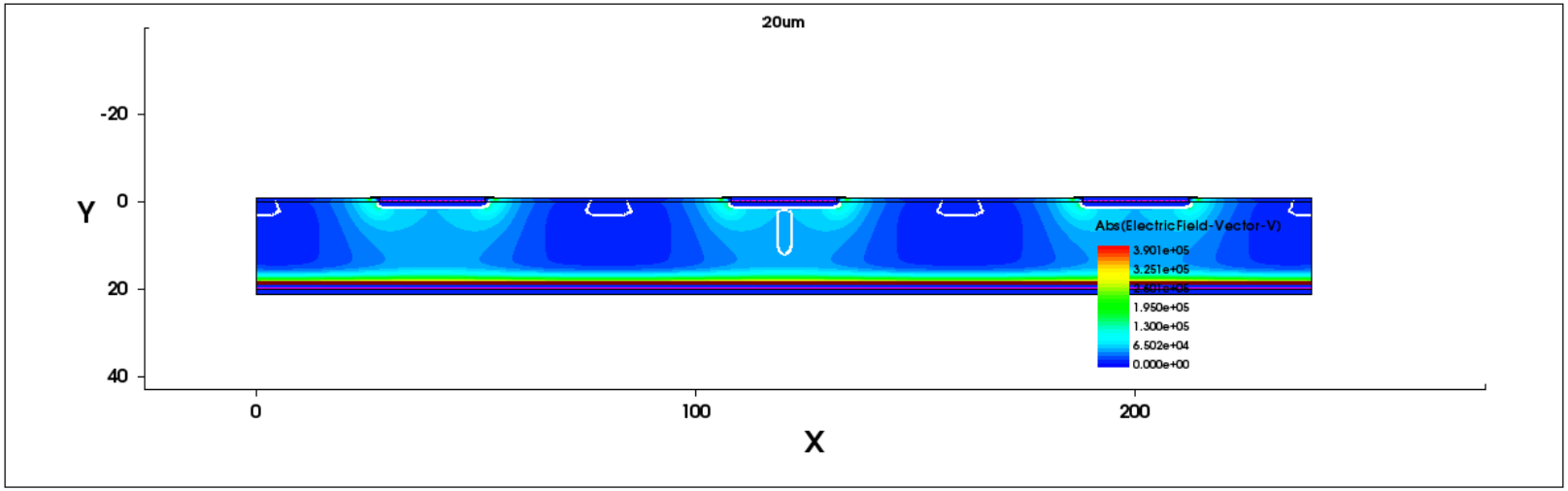
PhysDetLc Project. P on P LGAD MicroStrips. Thin Detectors

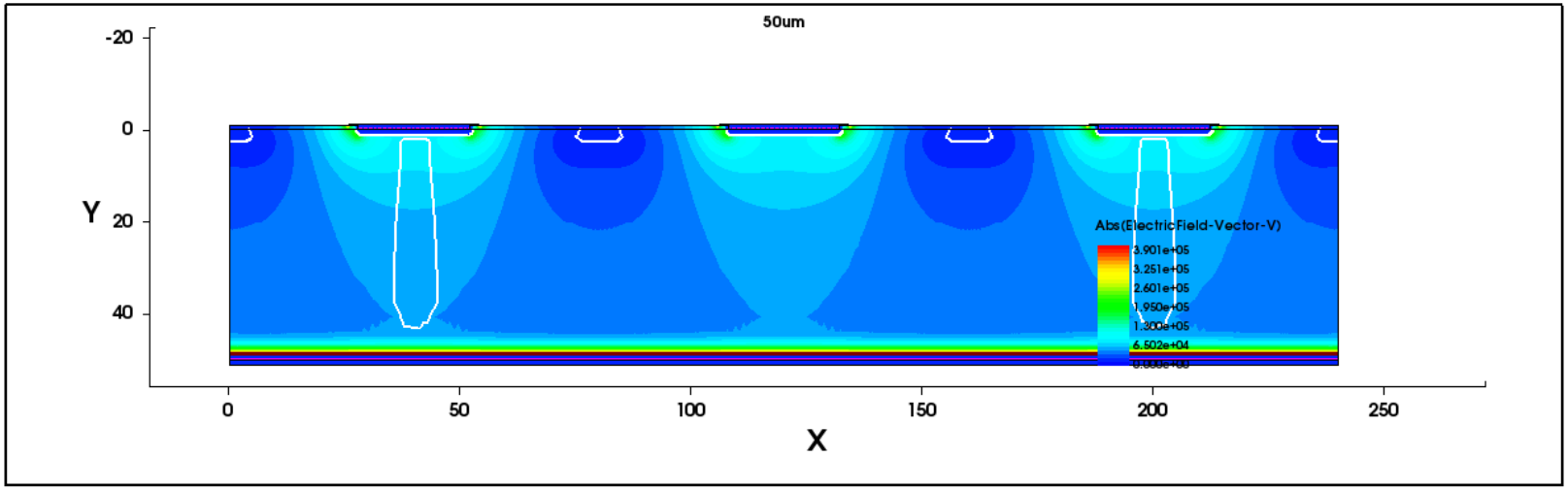
- **Three** microStrips Simulation. **Electrostatic Potential** 2D Distribution **@ V_{BR}**



PhysDetLc Project. P on P LGAD MicroStrips. Thin Detectors

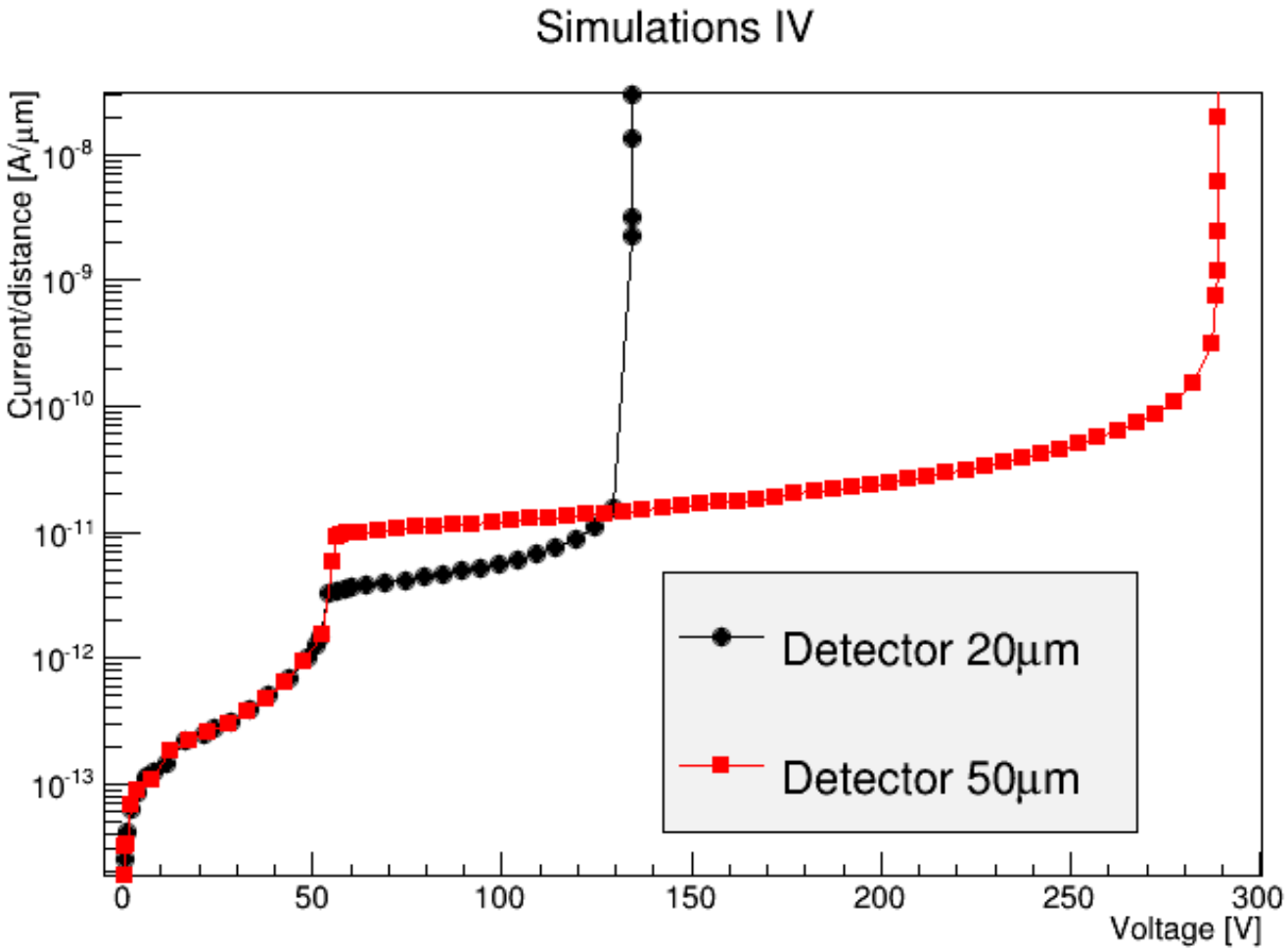
- **Three** microStrips Simulation. **Electric Field** 2D Distribution **@ V_{BR}**





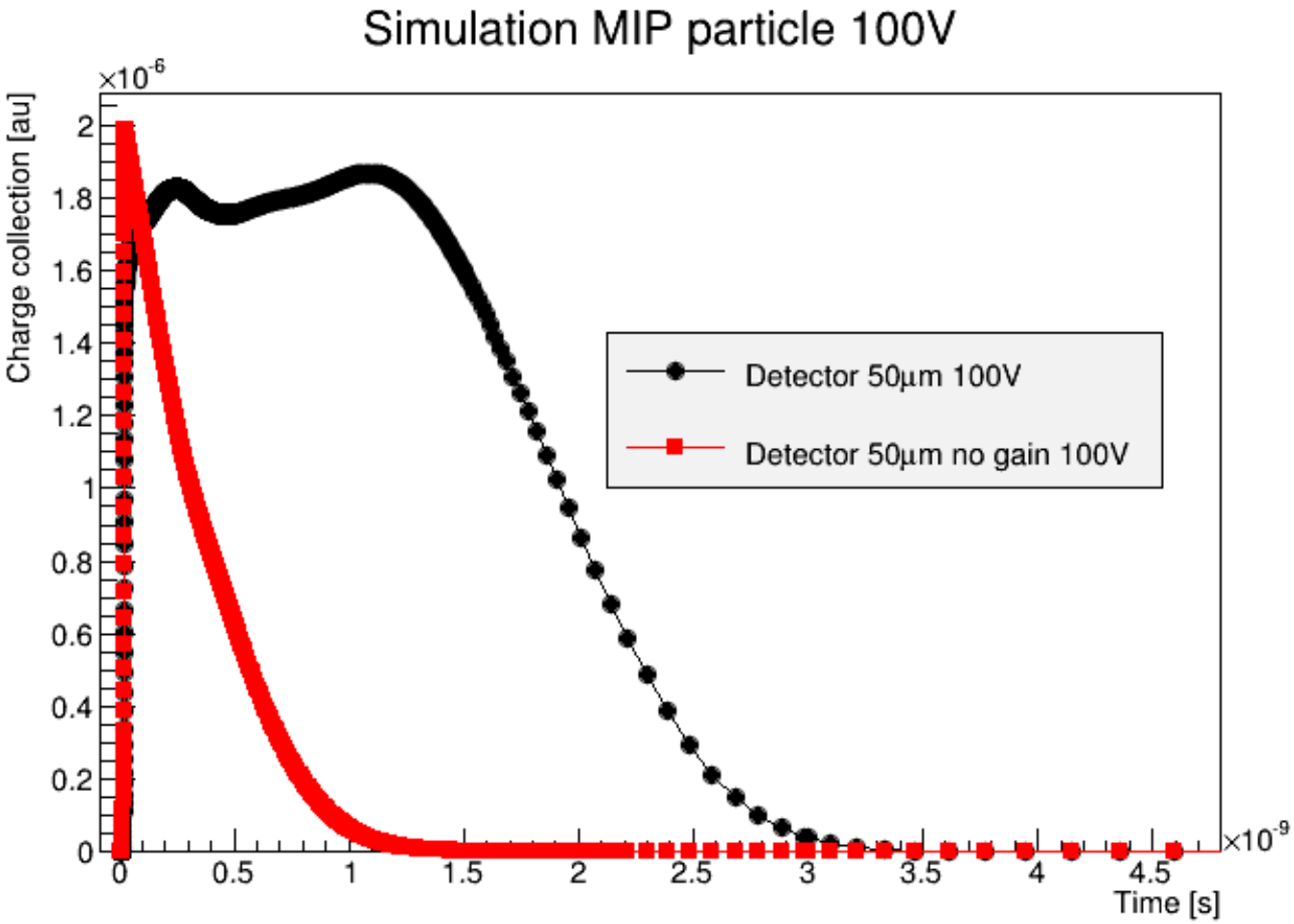
PhysDetLc Project. P on P LGAD MicroStrips. Thin Detectors

- **Three** microStrips Simulation. **I(V)**

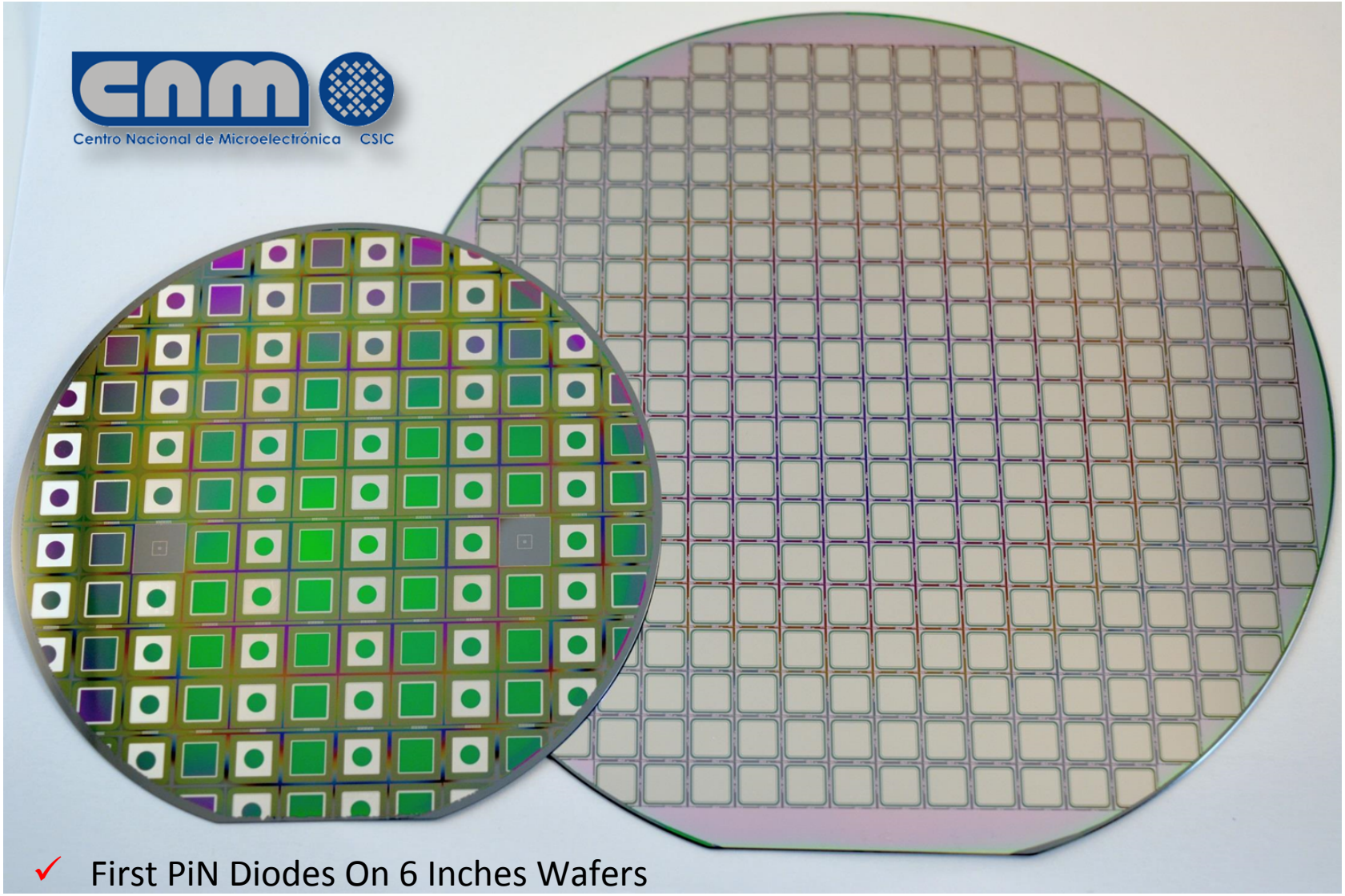


PhysDetLc Project. P on P LGAD MicroStrips. Thin Detectors

- **MIP** through the middle of the sensors (the central strip) **@ 100 V**



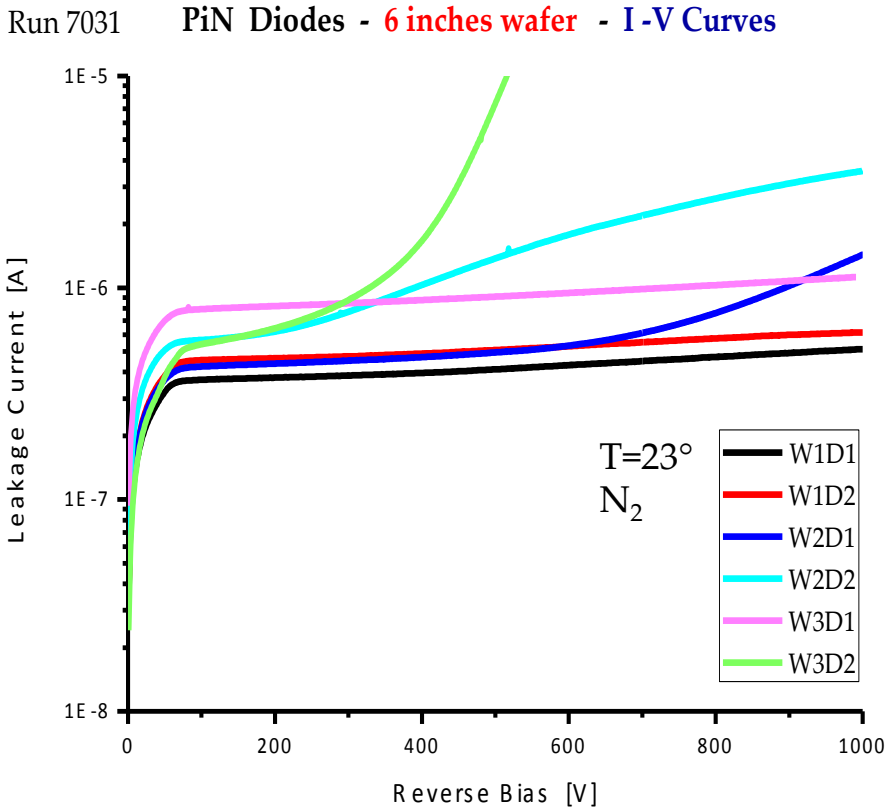
6 inch Technological Process

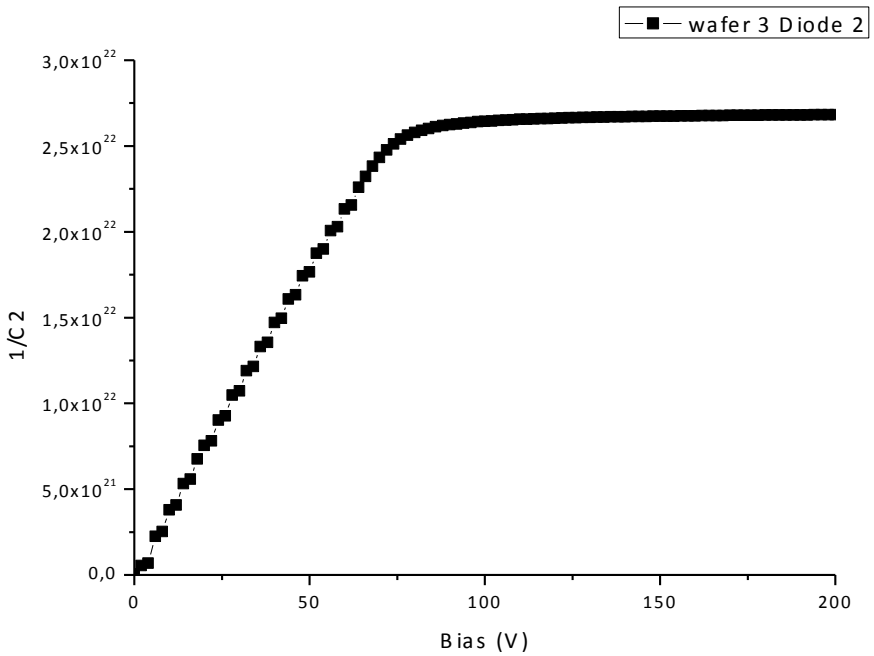


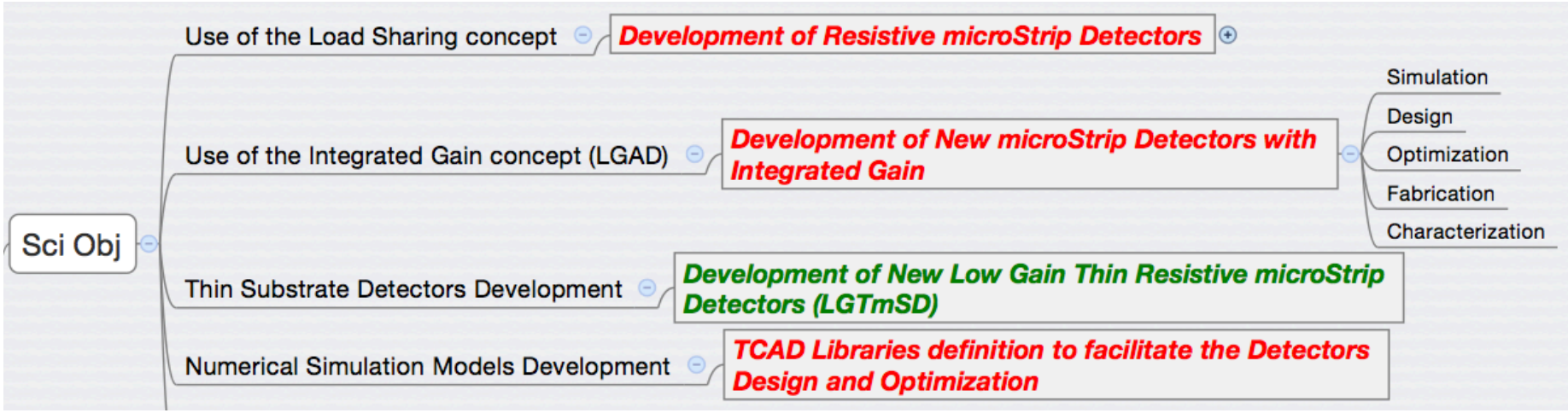
✓ First PiN Diodes On 6 Inches Wafers

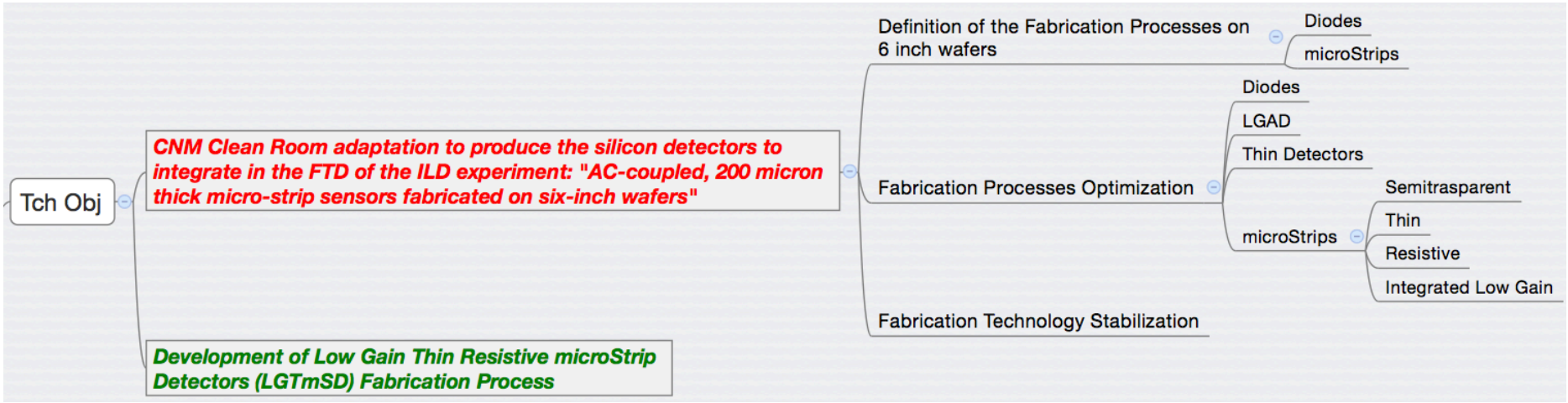
6 inch Technological Process

- First Results:
  - ✓ **Good** electrical performances
  - ✓ **Comparable** to **4 inch** technology PiN diodes






Sci Obj
Use of the Load Sharing concept
Development of Resistive microStrip Detectors
Use of the Integrated Gain concept (LGAD)
Development of New microStrip Detectors with Integrated Gain
Simulation
Design
Optimization
Fabrication
Characterization
Thin Substrate Detectors Development
Development of New Low Gain Thin Resistive microStrip Detectors (LGTmSD)
Numerical Simulation Models Development
TCAD Libraries definition to facilitate the Detectors Design and Optimization


Tch Obj
CNM Clean Room adaptation to produce the silicon detectors to integrate in the FTD of the ILD experiment: "AC-coupled, 200 micron thick micro-strip sensors fabricated on six-inch wafers"
Development of Low Gain Thin Resistive microStrip Detectors (LGTmSD) Fabrication Process
Definition of the Fabrication Processes on 6 inch wafers
Diodes
microStrips
Fabrication Processes Optimization
Diodes
LGAD
Thin Detectors
microStrips
Semitrasparent
Thin
Resistive
Integrated Low Gain
Fabrication Technology Stabilization

Objetivos Científicos

S DEVELOPMENT OF MICRO-STRIP DETECTORS

Conveners: M. Fernández (IFCA), S. Hidalgo (IMB-CNM)

Involved institutes: CERN, IMB-CNM, IFCA, ITA, UB, US

External institutes: HEPHY Viena

The aim of the microstrip detector R&D line is twofold: (1) we aim to develop a set of innovative technologies (new sensor concepts, ultralight and smart mechanics, low dissipation powering systems and low noise read out ASIC) to cope with the unprecedented tracking precision requirements of the future high-energy lepton linear collider; and (2) we enable the participating research and technological groups to provide a complete and realistic silicon-based tracking solution. The PhysDetLC microstrip R&D line is organized along five working packages each of them addressing a specific technical issue needed to produce a ready-to-build engineering design of a forward tracking detector.

OS1: Enable IMB-CNM as a qualified silicon sensor supplier for ILD for the Forward Tracker Disk of the ILD experiment by extending its technological capabilities to fabricate big area microstrip silicon sensors on 6-inch wafers.
OS2: Development of advanced tracking sensors: 2D position sensitive microstrips with resistive electrodes based on the resistive charge division concept; microstrips sensors with integrated proportional signal amplification
OS3: Characterization of sensors and manufacturing of a integrated microstrip system prototype. The goals are to complete the full characterization of the sensors manufactured in OS1 and OS2; develop new techniques for the silicon sensors characterization; and the experimental evaluation of an integrated prototype including sensors, front-end electronics and powering system.
OS4: Design development and assessment of a power pulsing system. One of the main requirements for the ILC experiments is that the FEE will be synchronized with the small duty cycle of the beam (0.5%). The PS system should be able to deliver this power remotely and generate the required high currents locally to minimize transient effects.

OS5: To provide a multichannel read-out ASIC for reading silicon micro-strips with the ILC structure (timing sequence). A low number of channels are envisaged to prove that the design is effective and integrable into ILC or other detectors with similar readout structure.

Objetivos Científicos

S DEVELOPMENT OF MICRO-STRIP DETECTORS

In this R&D line we develop all aspects of micro-strip detector technology (CERN, IFCA, IMB-CNM, ITA, UB, US), in collaboration with INTA.

S1 - MICROSTRIP SENSORS FOR THE FTD BASELINE DESIGN

S1.1 Fabrication of 6-inch diodes

Most of the equipment in the IMB-CNM clean-room have the capability to process six-inch wafers, but process optimization is required and will be performed via fabrication of standard p-on-n diodes in order to check uniformity (within wafer, WIW, and wafer-to-wafer, WTW) of the process parameters.

S1.2 Fabrication of 6-inch microstrip sensors

After the completion of the S1.1 task, standard “small” area micro-strip sensors will be produced. Each wafer will contain several microstrip sensors with standard design already used in four-inch technology; in this way, uniformity (WIW and WTW) of the microstrip sensor technology and performances will be checked. Dummy sensors will also be processed with the FTD layout and shapes in order to perform mechanical and thermal testing in dedicated mock-ups. All these sensors will be characterized and tested in the work package S3.

Objetivos Científicos

S2- DEVELOPMENT OF ADVANCED TRACKING SENSORS

This workpackage is structured in two tasks at the end of which two novel microstrip technologies of interest for a ILC silicon-based tracker will be delivered.

S2.1. Resistive microstrip detectors: Simulation, design, optimization and fabrication

This task is a follow up of the activity started in the preceding project DET4HEP (FPA2010-222163) where we probed for the first time the feasibility of the charge-division concept on silicon microstrip detectors to obtain a two-dimensional information of the passing point of the ionizing radiation. In this new proposal we aim to close the R&D phase of this development by developing a full-fledged microstrip sensor with resistive electrodes suitable for ILC tracking requirements.

S2.2. Low gain microstrip detectors: Simulation, design, optimization and fabrication

In this task we will adjust the technological manufacturing processes at IMB-CNM for fabricating microstrip sensors with signal multiplication; this work is based on the LGAD devices (Low Gain Avalanche Diodes) developed at previous DET4HEP project (FPA2010-222163). The critical technological issues to tackle are: the large number of photolithographic steps, the adjustment of the critical dopant diffusions to implement, the optimization of the oxides, the etching of metal layers and the development of specific technological steps at the periphery of the microstrip.