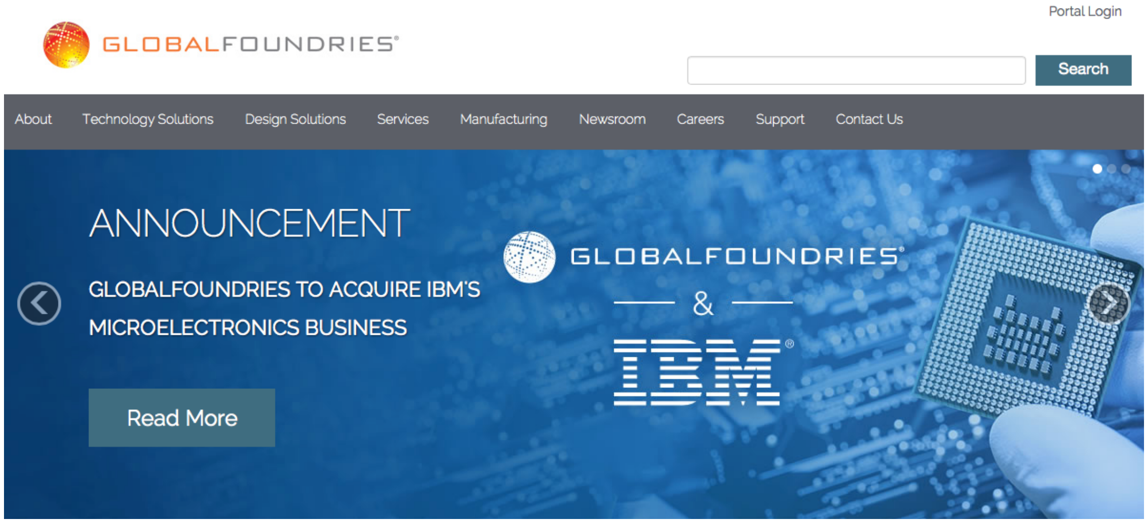
TID results of a new 0.13um technology for future HEP ASIC design

S. Michelis, F.Faccio, D.Cornale

Last year news

http://globalfoundries.com/newsroom/press-releases/2014/10/20/globalfoundries-to-acquire-ibm's-microelectronics-business?utm_source=homepage&utm_medium=brief&utm_campaign=IBM



ANNOUNCEMENT

GLOBALFOUNDRIES TO ACQUIRE IBM'S MICROELECTRONICS BUSINESS

The future of our legacy 130nm technology is uncertain, therefore it is necessary to find a suitable alternative technology

A new technology has been found and it needs to be tested for radiation tolerance.

This seminar is focused on Total Ionizing Dose (TID) tests done on the new 130nm technology

The new 130nm technology has different fabs

Fab 14
12 inches
(6 sub/year)

Fab 6
8 inches
(2 sub/year)

Fab 12
12 inches
(4 sub/year)

Fab: semiconductor fabrication plant

The new 130nm technology has different fabs

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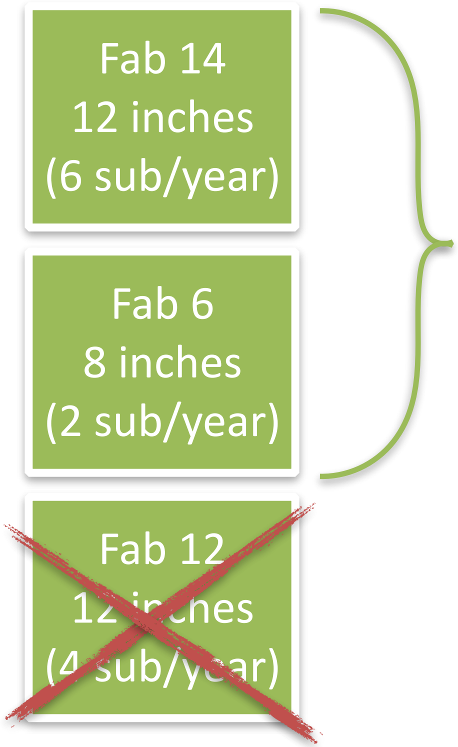


Fab 14
12 inches
(6 sub/year)

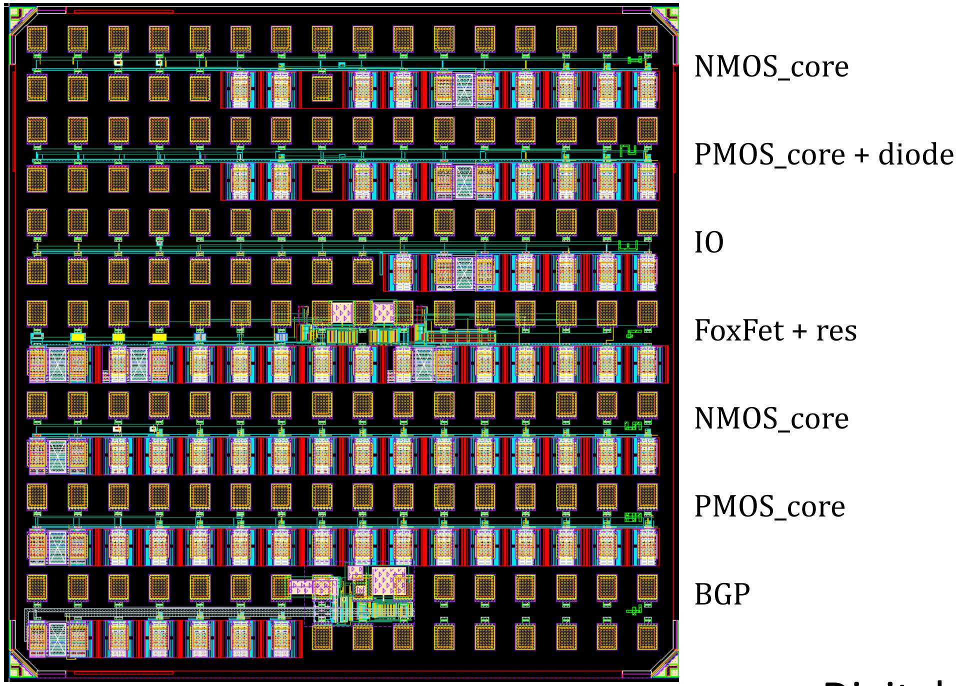
Fab 6
8 inches
(2 sub/year)

~~Fab 12~~
~~12 inches~~
~~(4 sub/year)~~

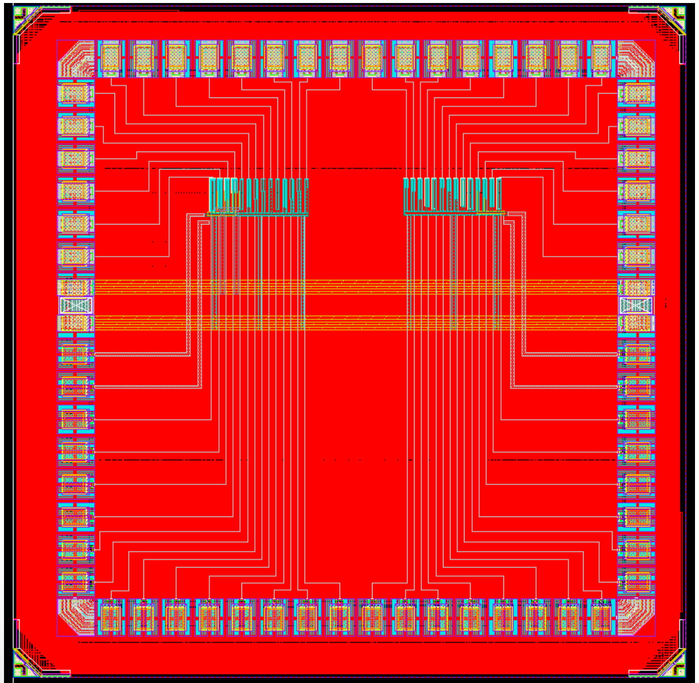
Xray tested for TID.
Results are the
topic of this talk

Fab: semiconductor fabrication plant

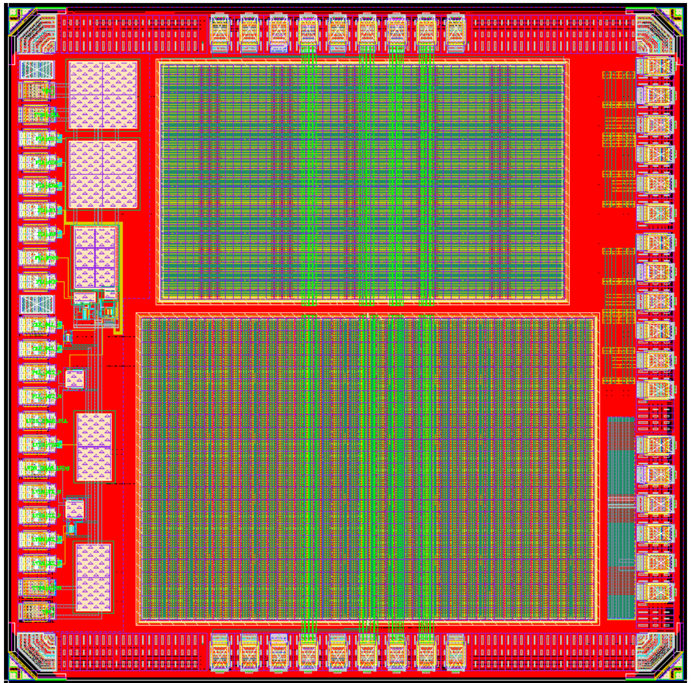
TID_CHIP



Noise_CHIP



Digital_CHIP



Thanks to Xavi and the colleagues in Cracow for their help (Marek, Mirek and Tomek)

Several devices are included in the TID_chip

Core transistors (NMOS and PMOS) rated for 1.2V with different flavors
(high Vth, low Vth and regular)

IO transistors (NMOS and PMOS) rated for 2.5V

Diodes: p in Nwell, DTNMOS and DTPMOS

Foxfet

Additionally a first version of a Bandgap based on DTNMOS has been included

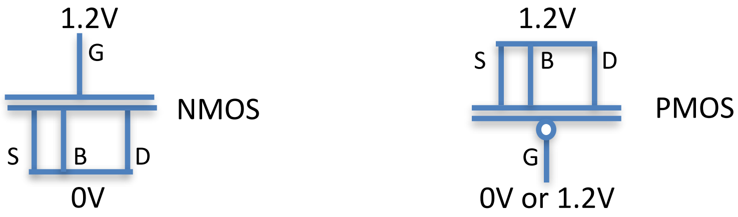
TID: Total Ionizing Dose

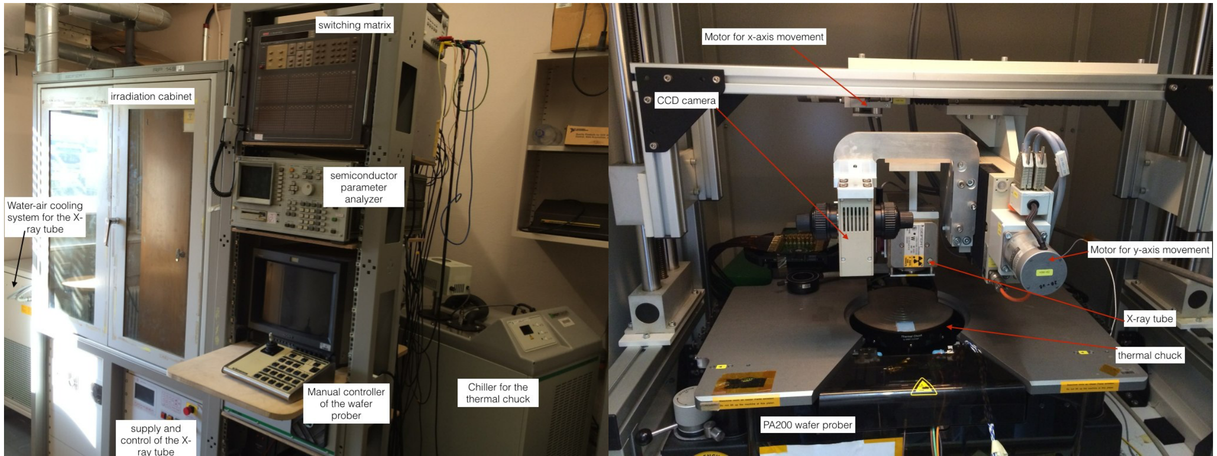
Legacy technology has been tested up to TID=100Mrad with a dose rate ~ 1.5Mrad/h, at 25C.

The new technology has been tested up to TID=400Mrad at 25C and -30C

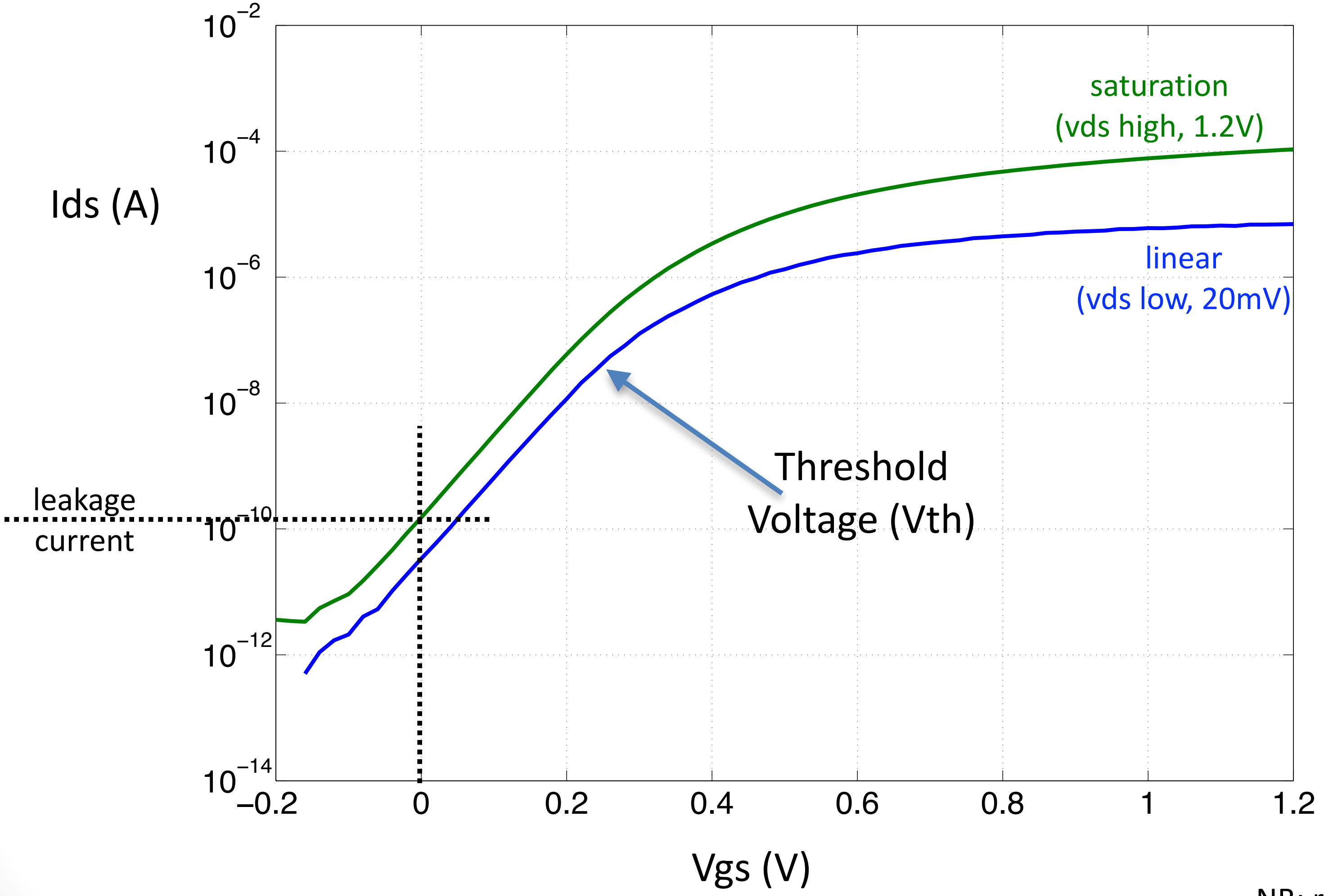
2 dose rates used: high dose rate (HDR) ~ 9Mrad/h (200Mrad/day)
low dose rate (LDR) ~ 90Krad/h (2Mrad/day)
dose rate for LHCb Velopix application: 0.2Mrad/day (400Mrad over 10years, assuming 200 beam days/year)

Irradiation condition:



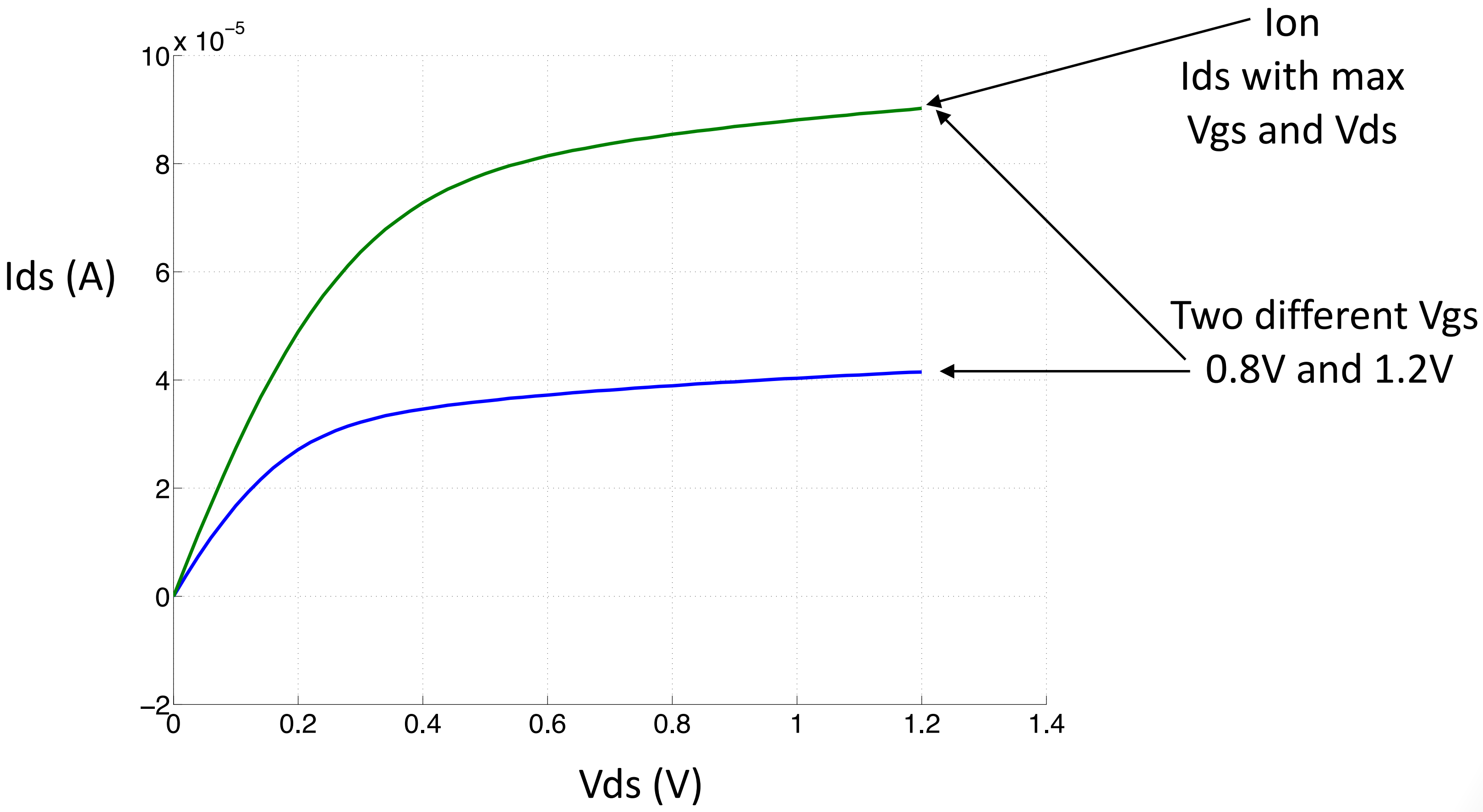


A small reminder… IdVg



NB: real measurement

A small reminder… IdVd



Ion
Ids with max
Vgs and Vds

Two different Vgs
0.8V and 1.2V

NB: real measurement

Outcome of the test

Outcome of the test

GOOD NEWS!

Outcome of the test

GOOD NEWS!

The new 130nm technology from Fab6 is performing better than legacy 130nm technology in term of intrinsic TID tolerance.

It can be therefore considered as a valid alternative.

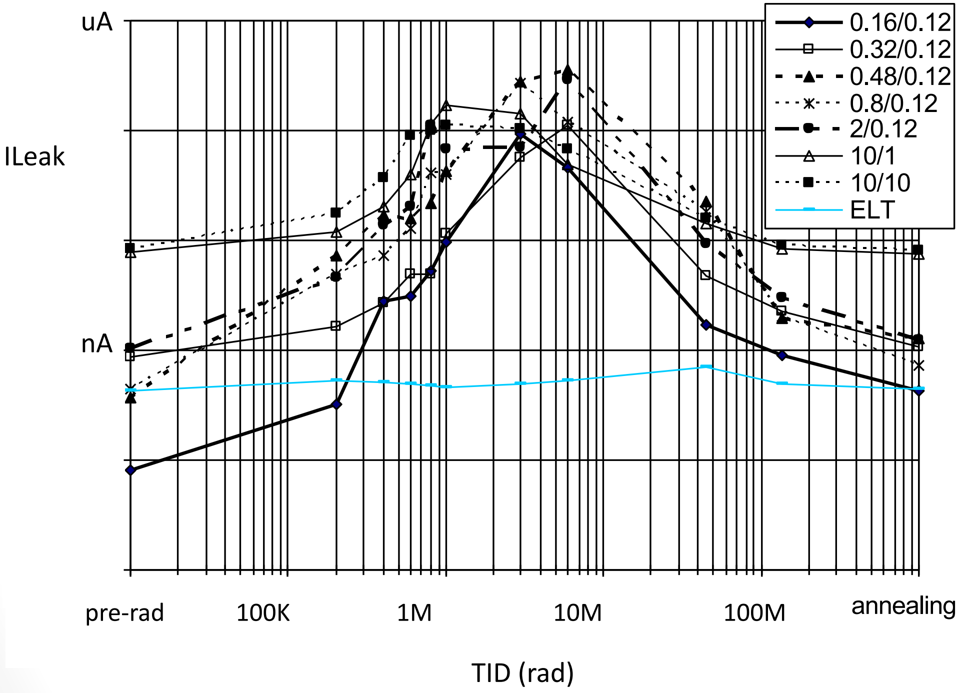
For Fab14 there are differences for the NMOS.

NMOS Core, 1.2V

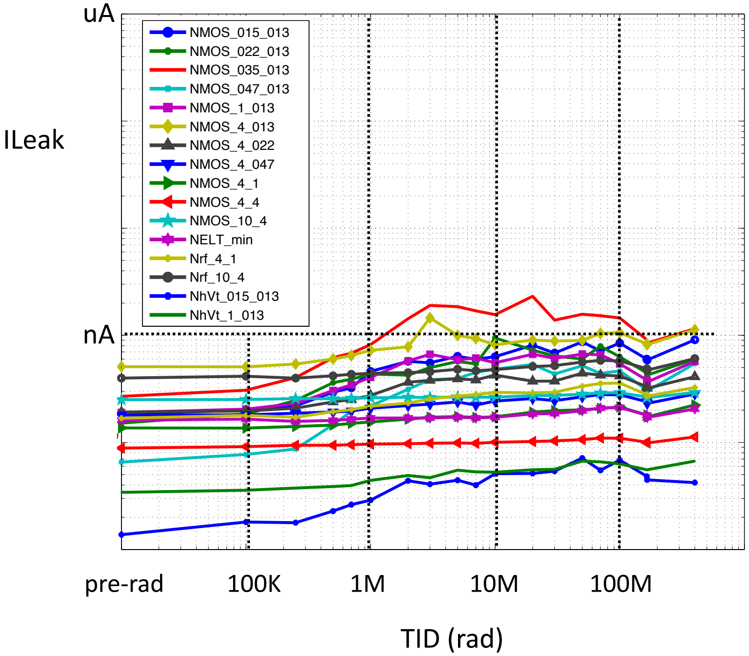
NB: Fab6

NMOS leakage current increase is limited

Legacy 130nm

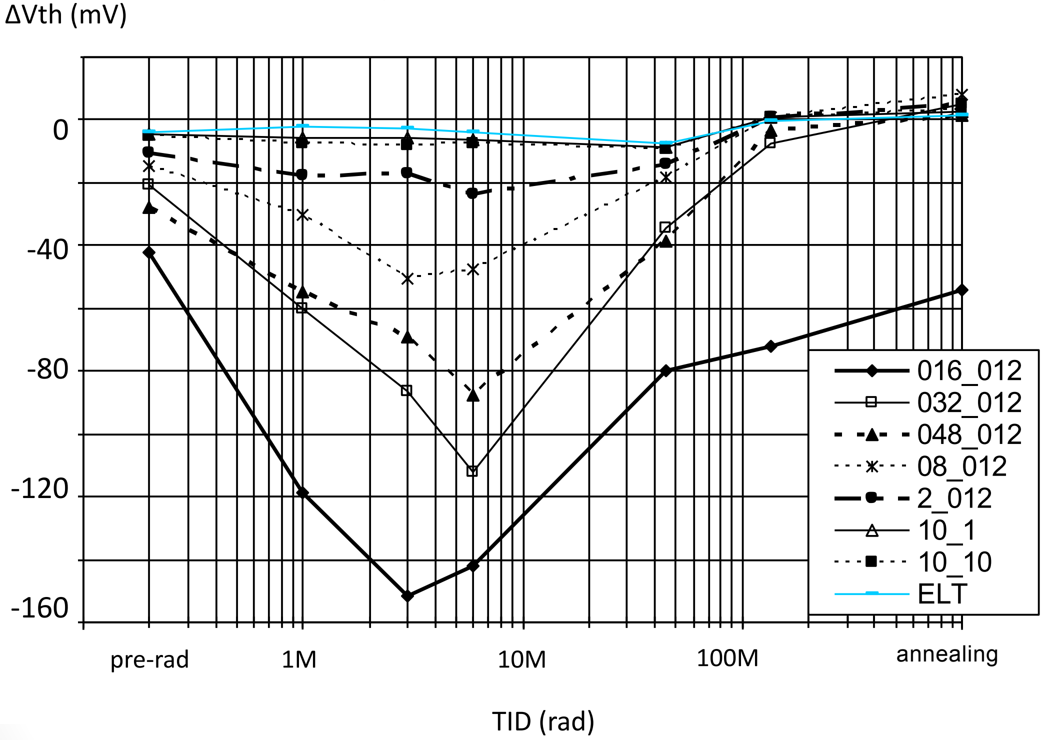


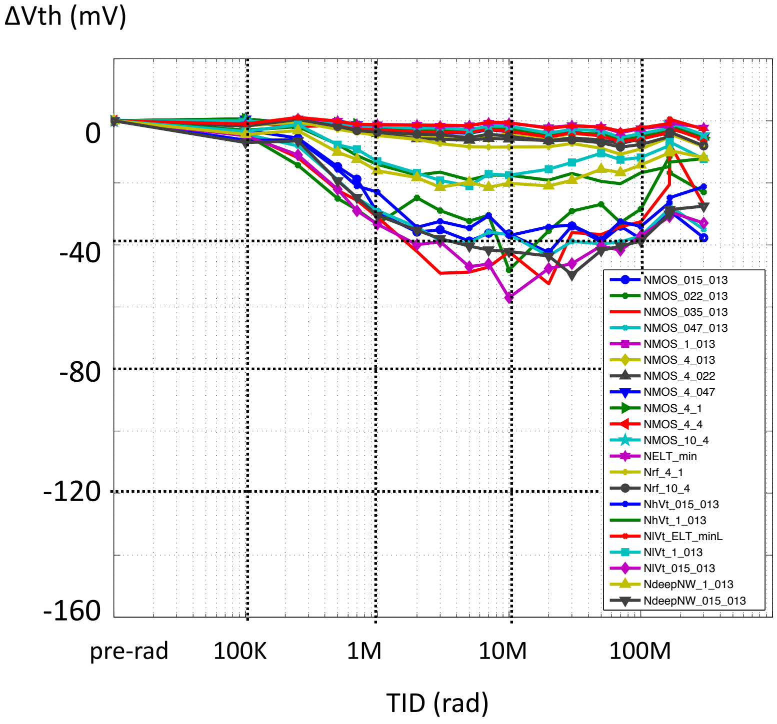
New 130nm



NB: Fab6

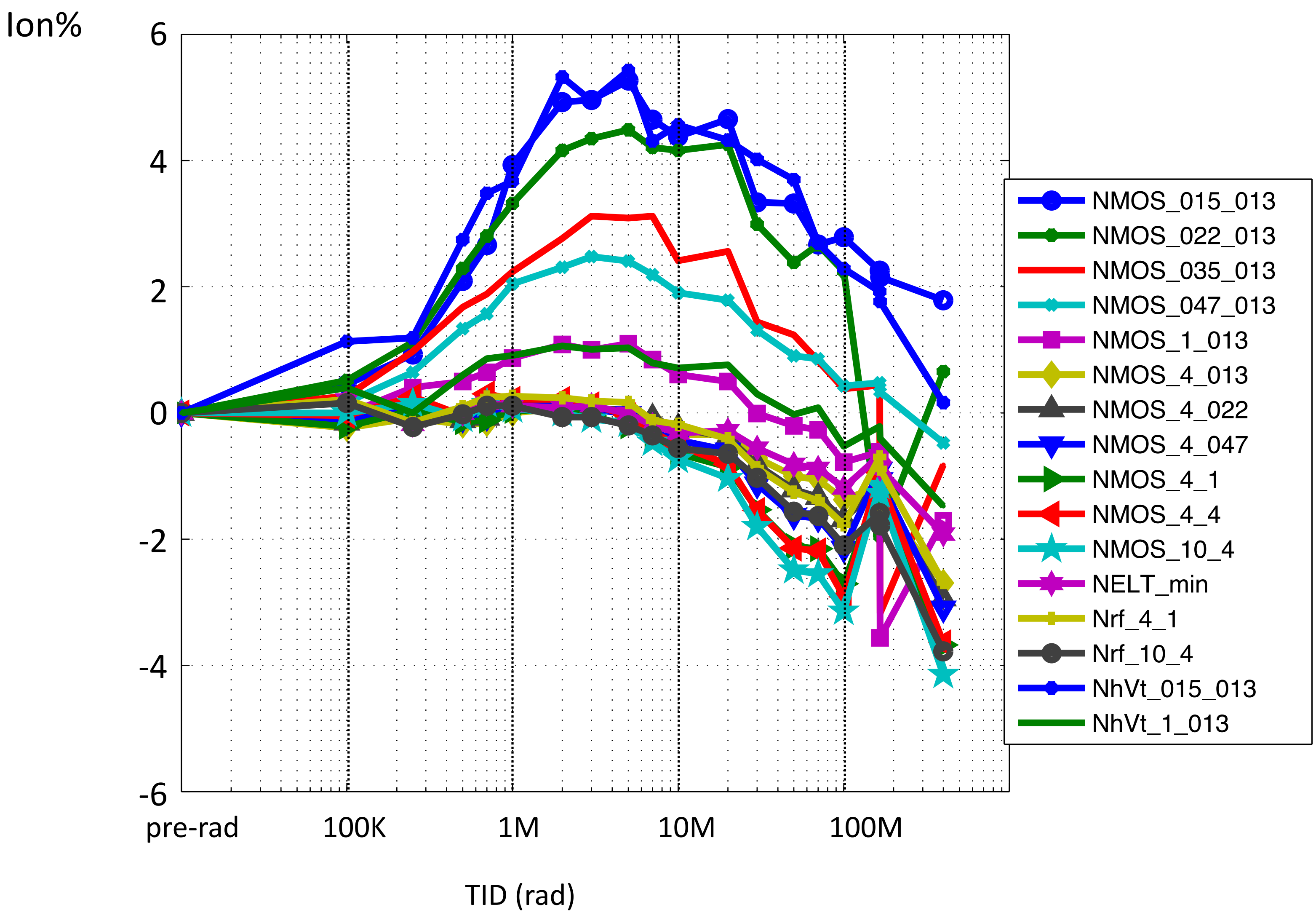
NMOS Vth shift is below 50mV


Legacy 130nm


New 130nm

NB: Fab6

NMOS Ion degradation is limited

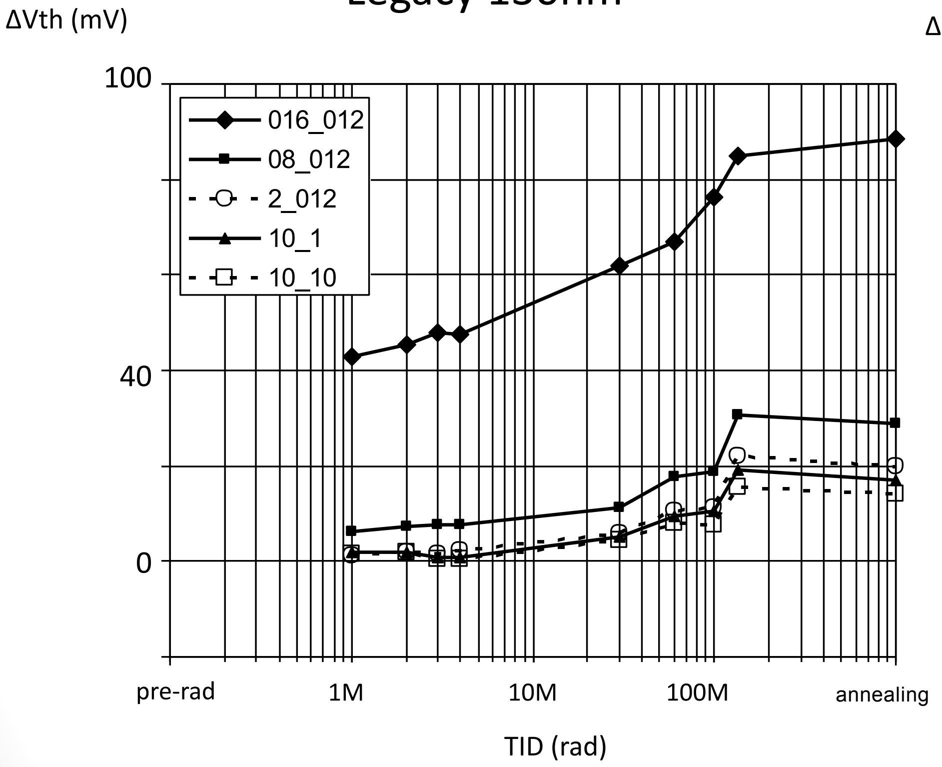


PMOS Core, 1.2V

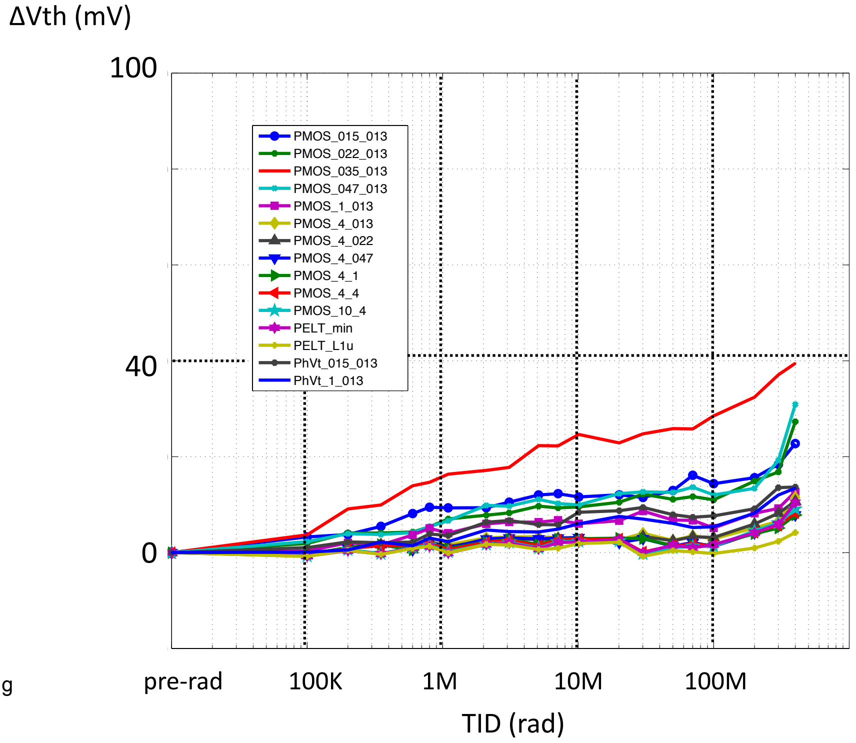
NB: Fab6 & Fab14

PMOS Vth shift is below 40mV

Legacy 130nm

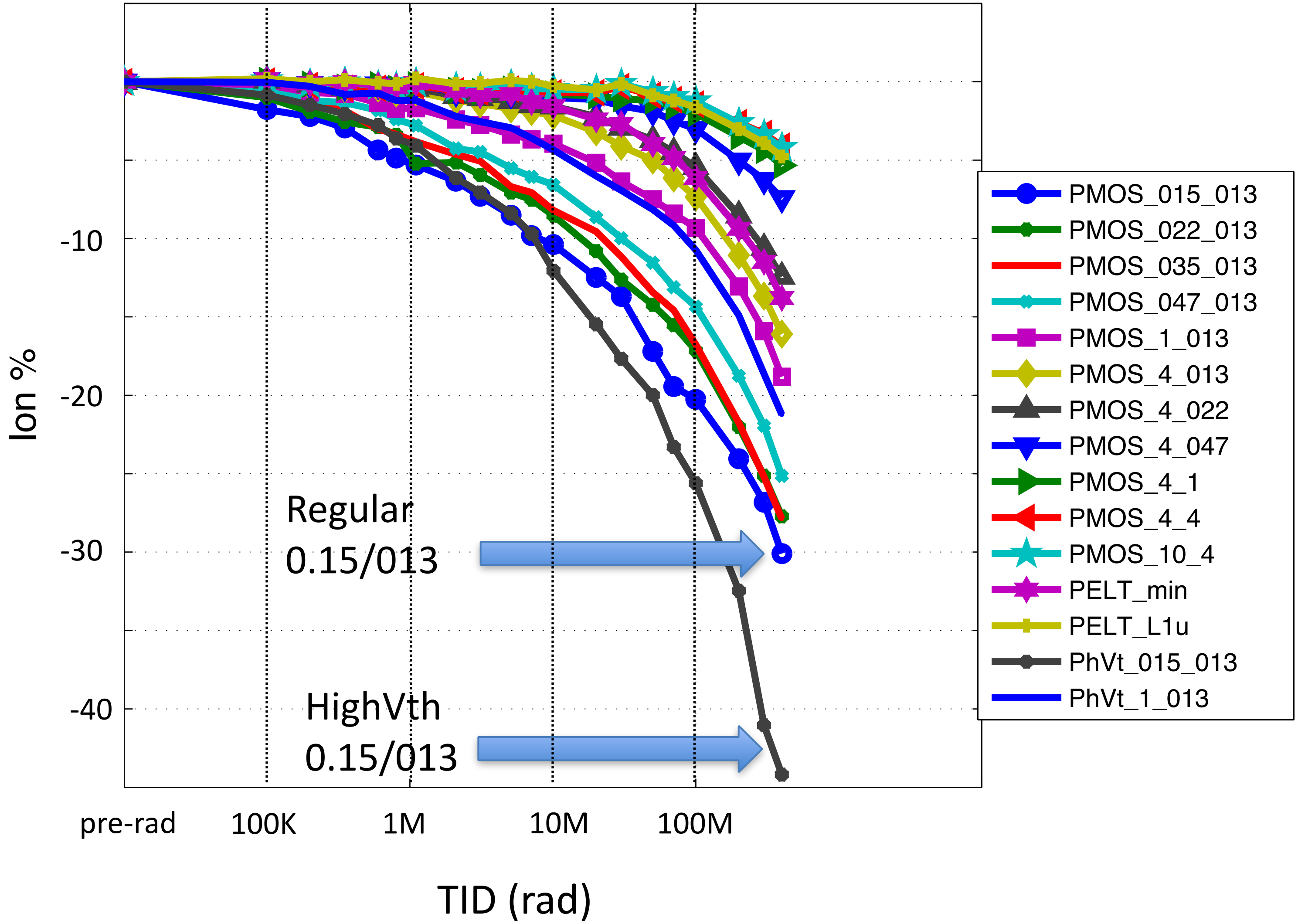


New 130nm



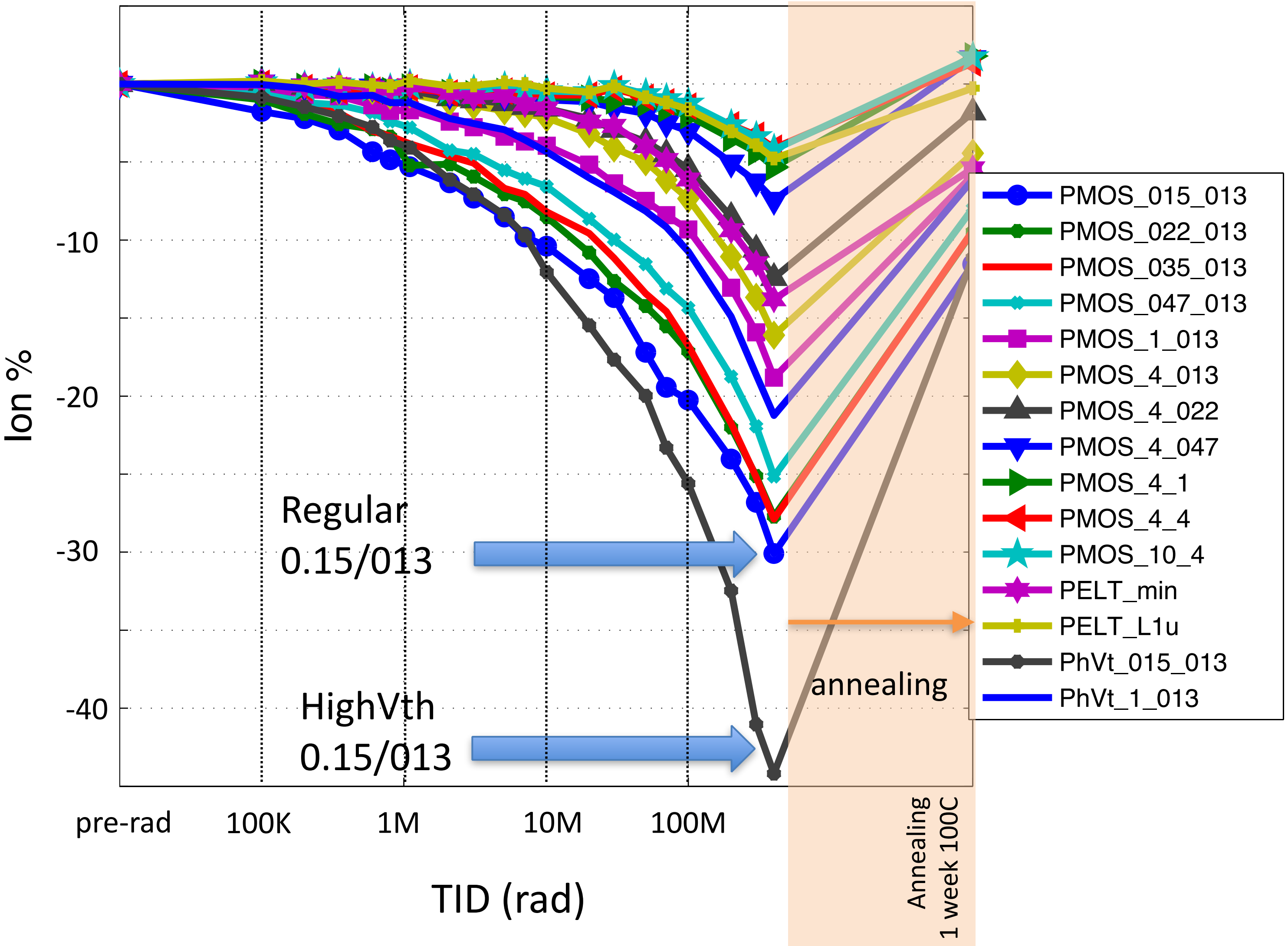
NB: Fab6 & Fab14

The PMOS Ion degradation is large starting from 100Mrad



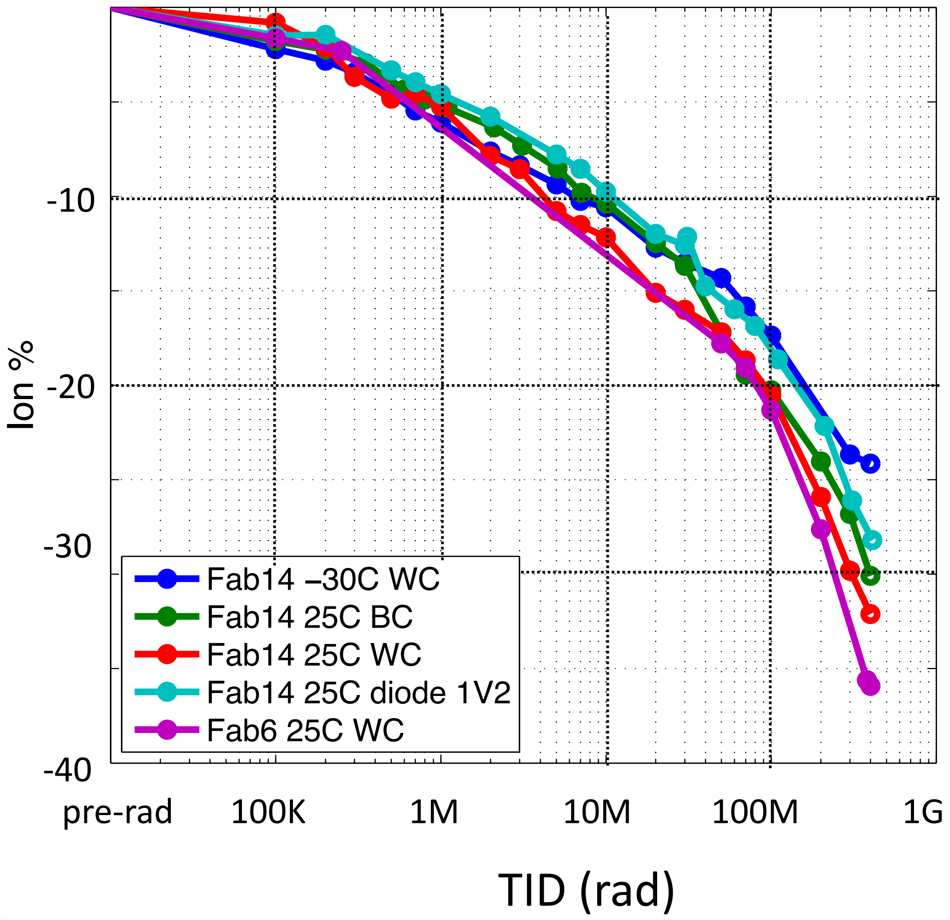
NB: Fab6 & Fab14

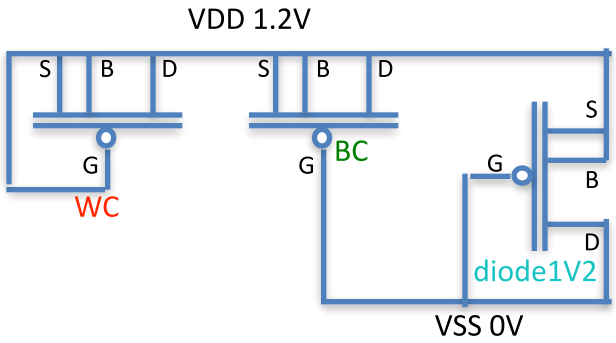
The PMOS Ion degradation is large starting from 100Mrad



NB: Fab6 & Fab14

The Ion degradation is similar in all fabs.
A little better at -30C

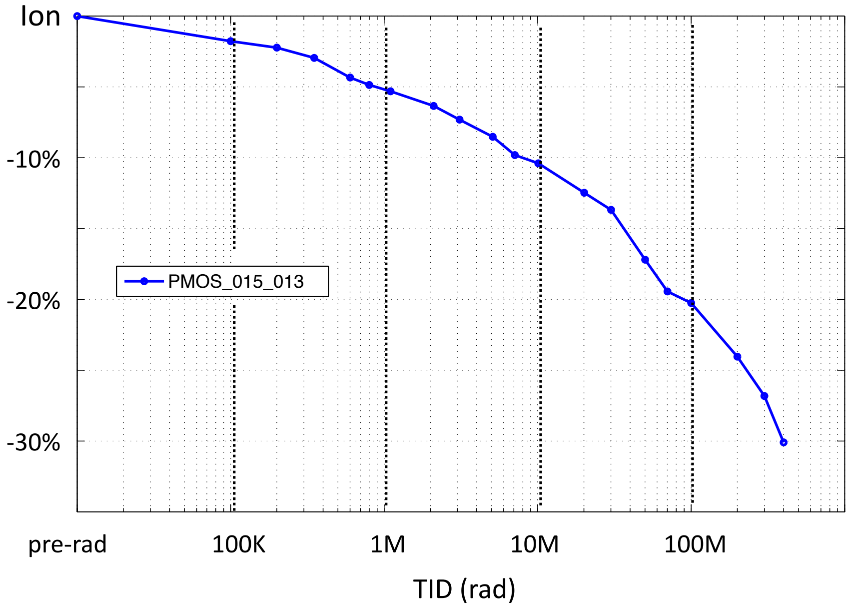


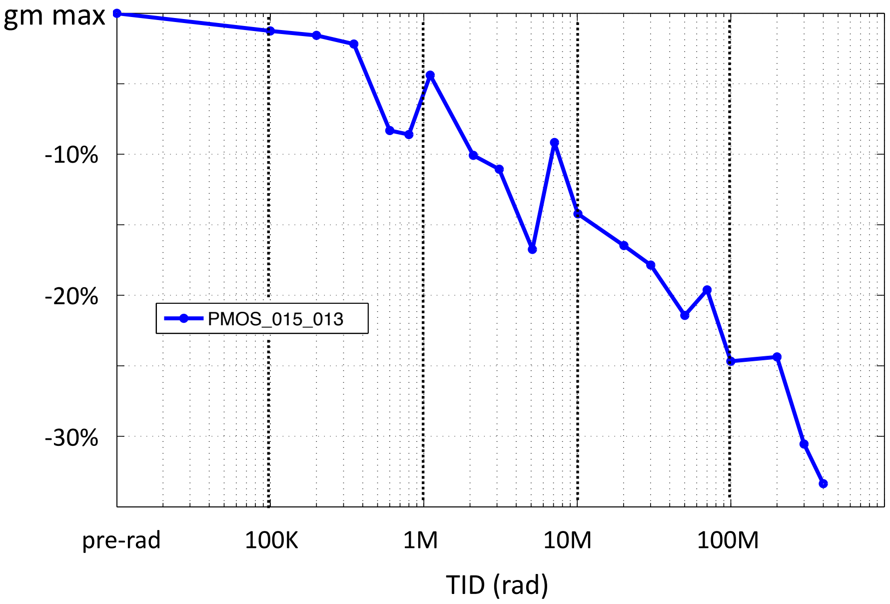


PMOS min size
0.15/0.13

NB: Fab6 & Fab14

The Ion degradation is mainly related to gm degradation

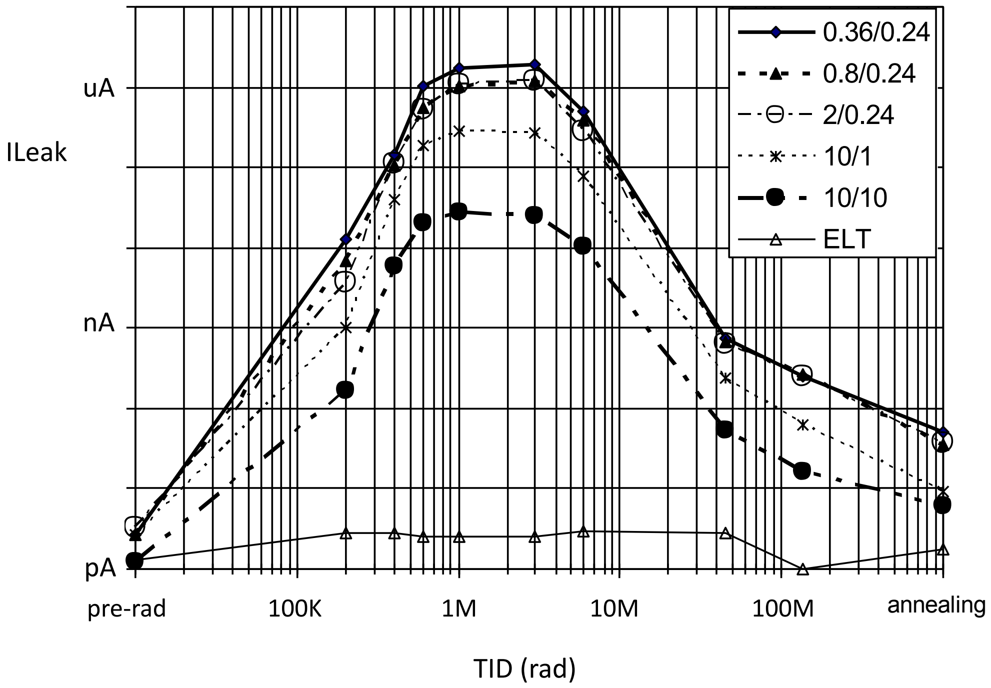




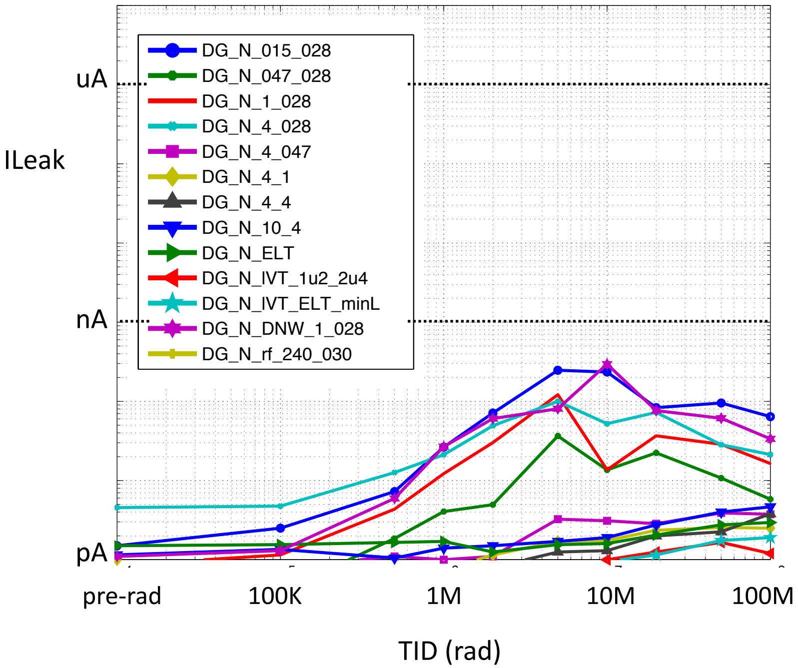
NMOS I/O, 2.5V

NB: Fab6

I/O NMOS Leakage current is below nA



Legacy 130nm

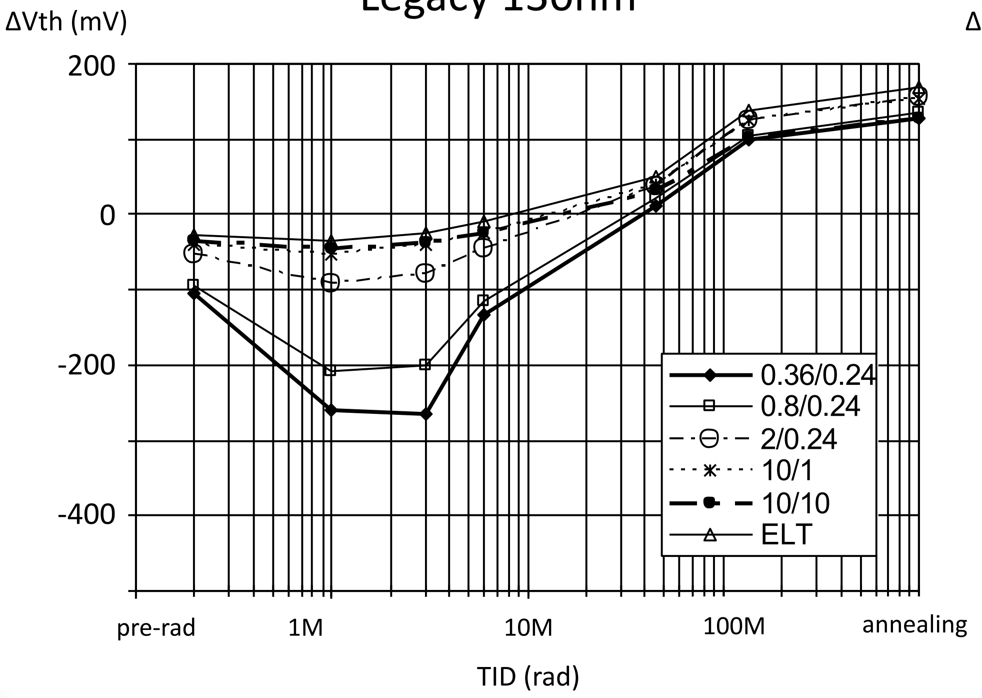


New 130nm

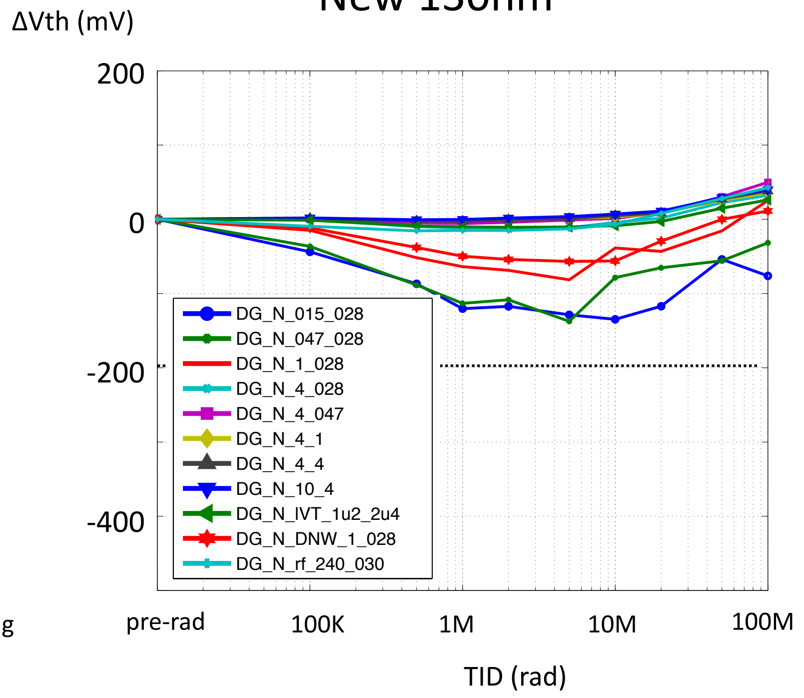
NB: Fab6

I/O NMOS Vth shift is below 200mV

Legacy 130nm



New 130nm

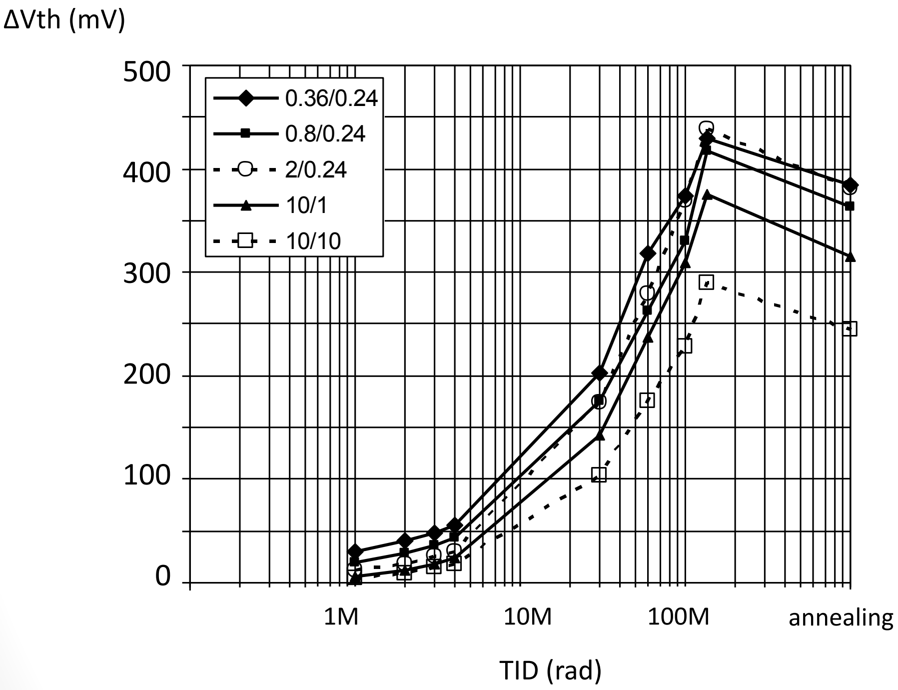


PMOS I/O, 2.5V

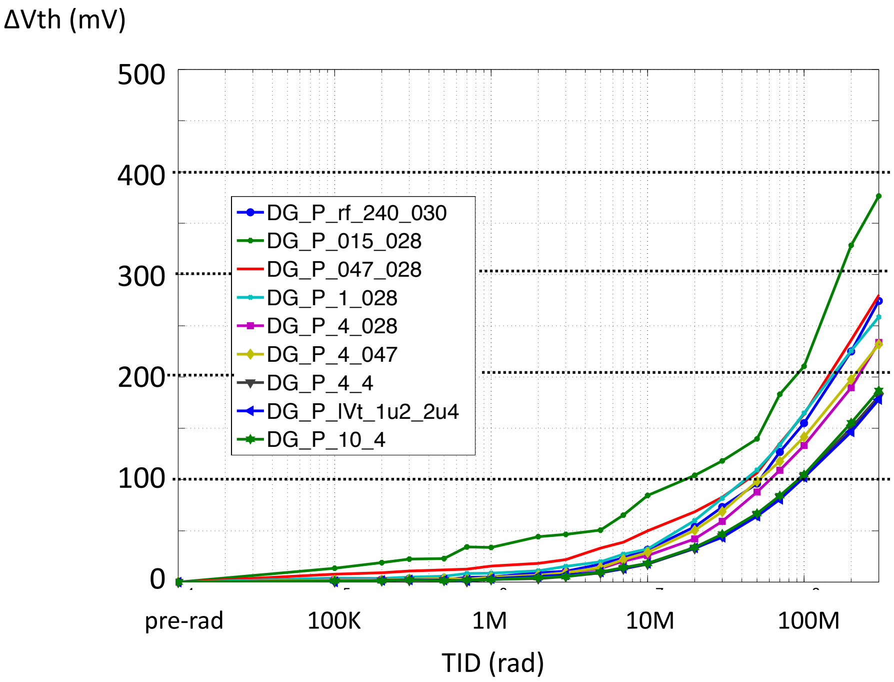
NB: Fab6 & Fab14

I/O PMOS Vth shift

Legacy 130nm



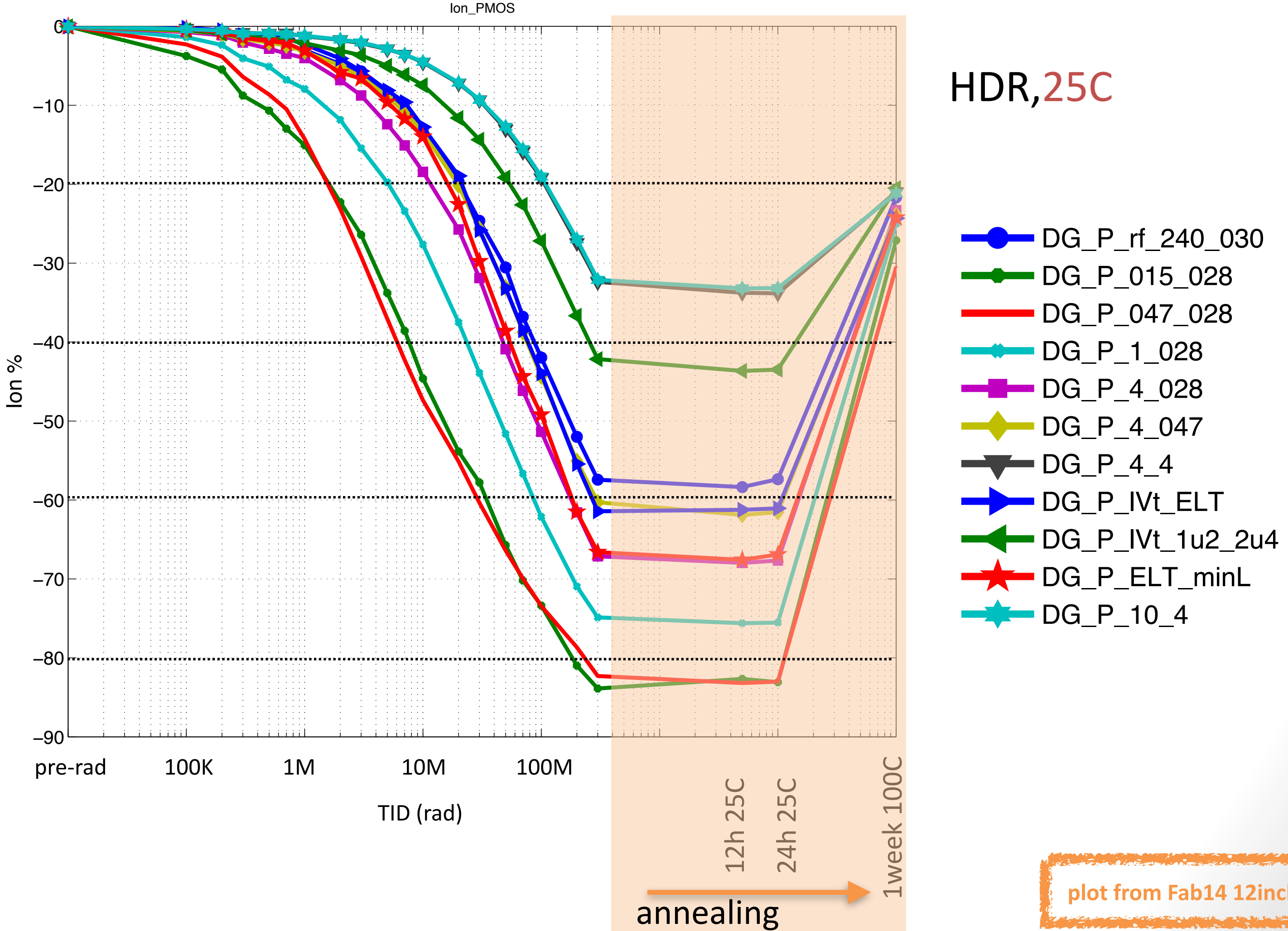
New 130nm



NB: Fab6 & Fab14

I/O PMOS Ion degradation is severe

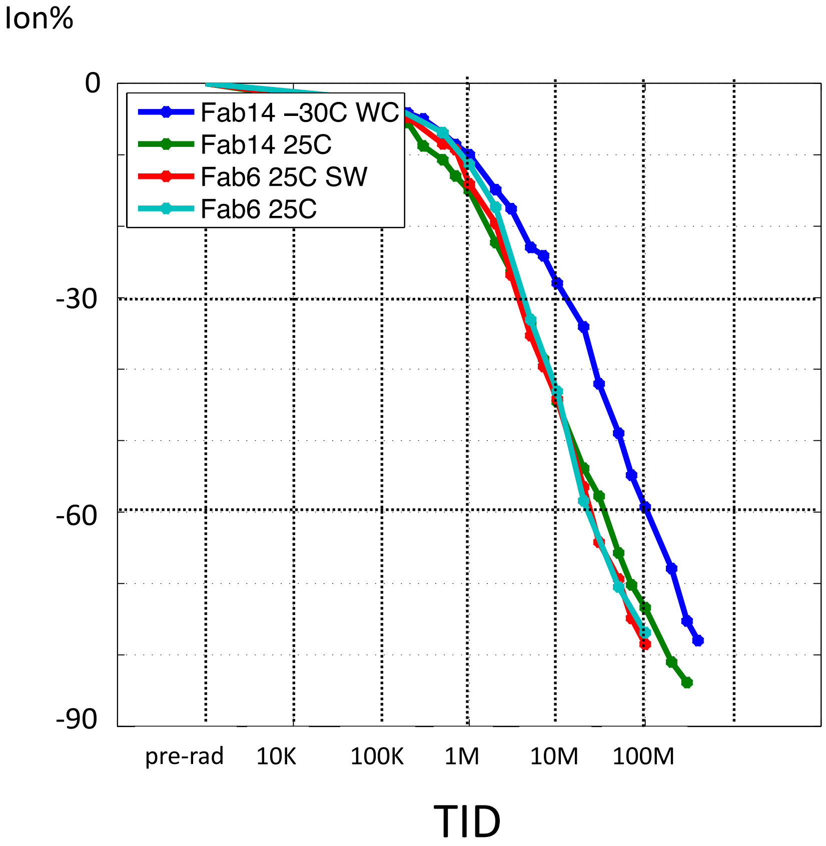
At 400 Mrad it reaches -80% for small size transistors. Also ELT PMOS shows an important degradation (-68%). Only after an annealing of 1week at 100C there is a recovery of the Ion. There are no big differences at -30C.

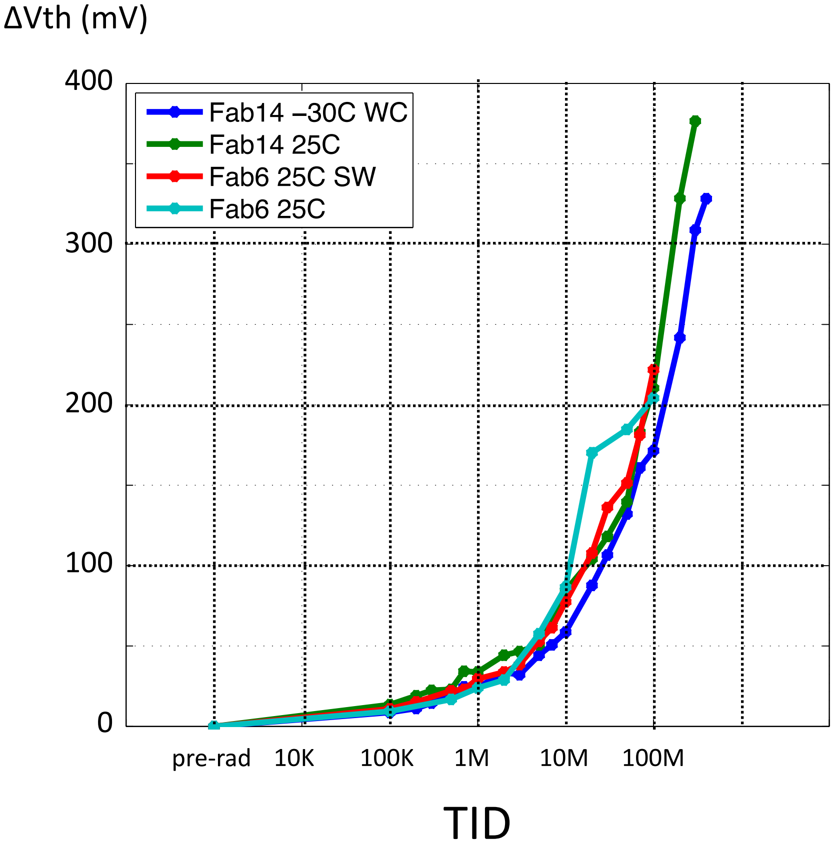


plot from Fab14 12inches

NB: Fab6 & Fab14

Difference between Fabs, temperature and bias condition



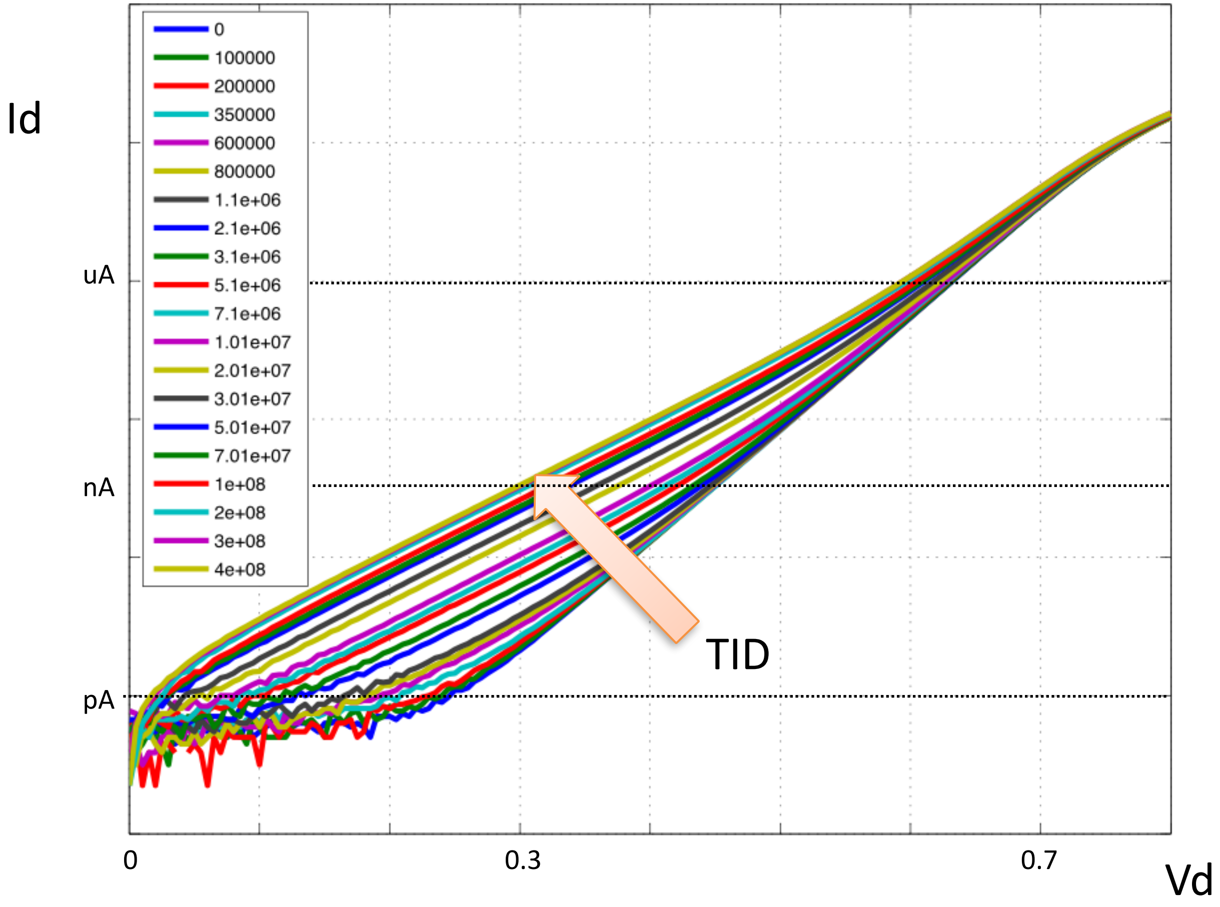


I/O PMOS min size
0.15/0.28

Diodes

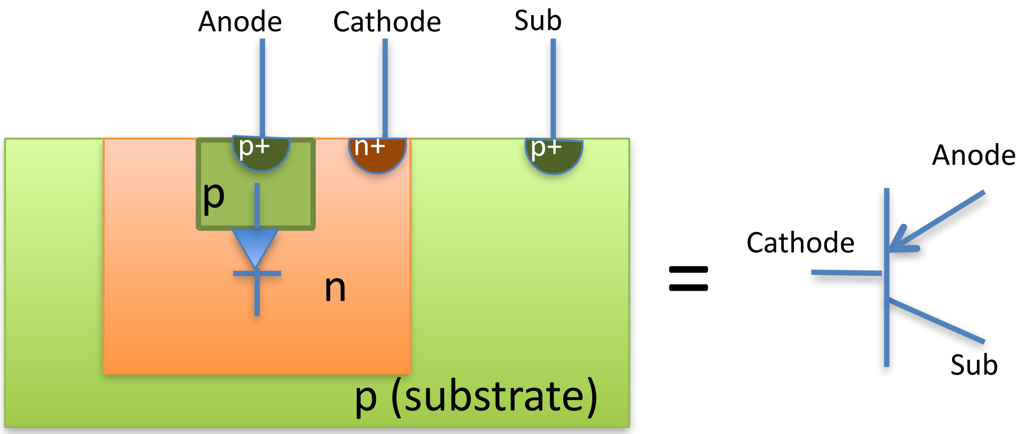
IdVd degradation

NB: Fab6 & Fab14



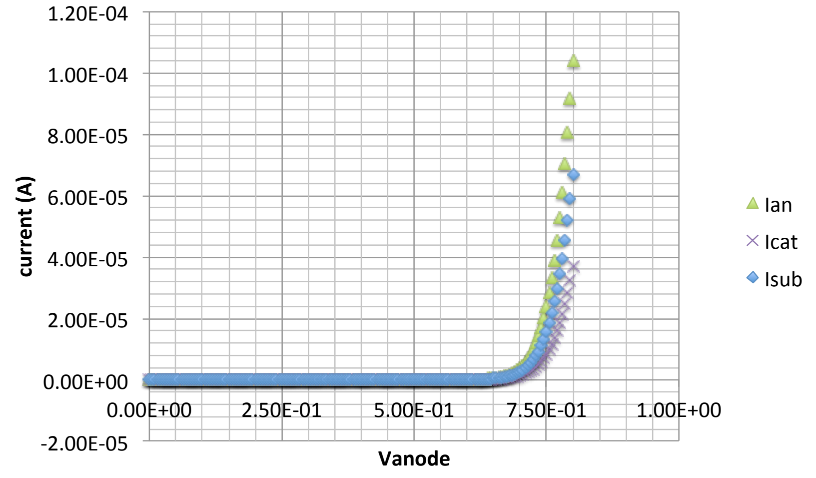
All the p in NW diodes suffer of a large leakage current which makes them difficult to be used for Bandgap application.

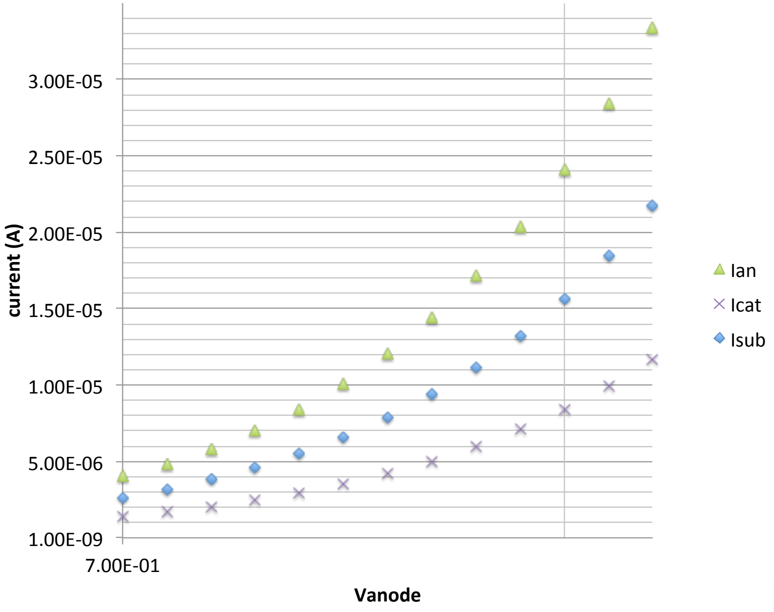
Not really diodes, but pnp!



P-in-NW diodes are in reality part of a bipolar parasitic structure (pnp) with a certain gain.

Plotting the I vs Vanode for the three terminals it appears that $I_{cathode} << I_{anode}$ and even more important $I_{sub} > I_{cathode}$.





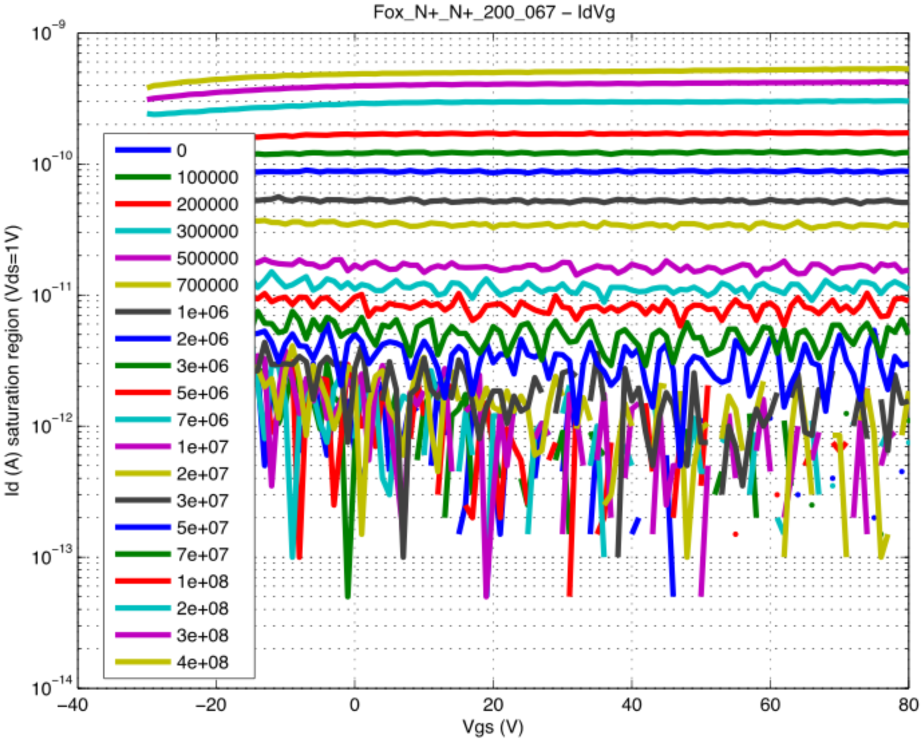
FOXFET

FOXFET

5 FOXFETs (filed oxide transistors) have been tested to see the leakage current between devices.

The FOXFETs are:

- N+ N+ (W/L=200/0.67)
- N+ Nwell (W/L=200/0.32)
- N+ Nwell (W/L=200/0.6)
- Nwell Nwell (W/L=200/1)
- Nwell Nwell (W/L=200/1.48)



The increase of leakage current is negligible therefore there is no indication of need of guard rings.

Summary of the results

GOOD NEWS!

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It can be therefore considered as a valid alternative.

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BUT… For Fab14 (12 inches) there are differences for the NMOS.

Differences between Fabs

PMOS (core and I/O) and diodes from Fab6 and Fab14 show the same degradation

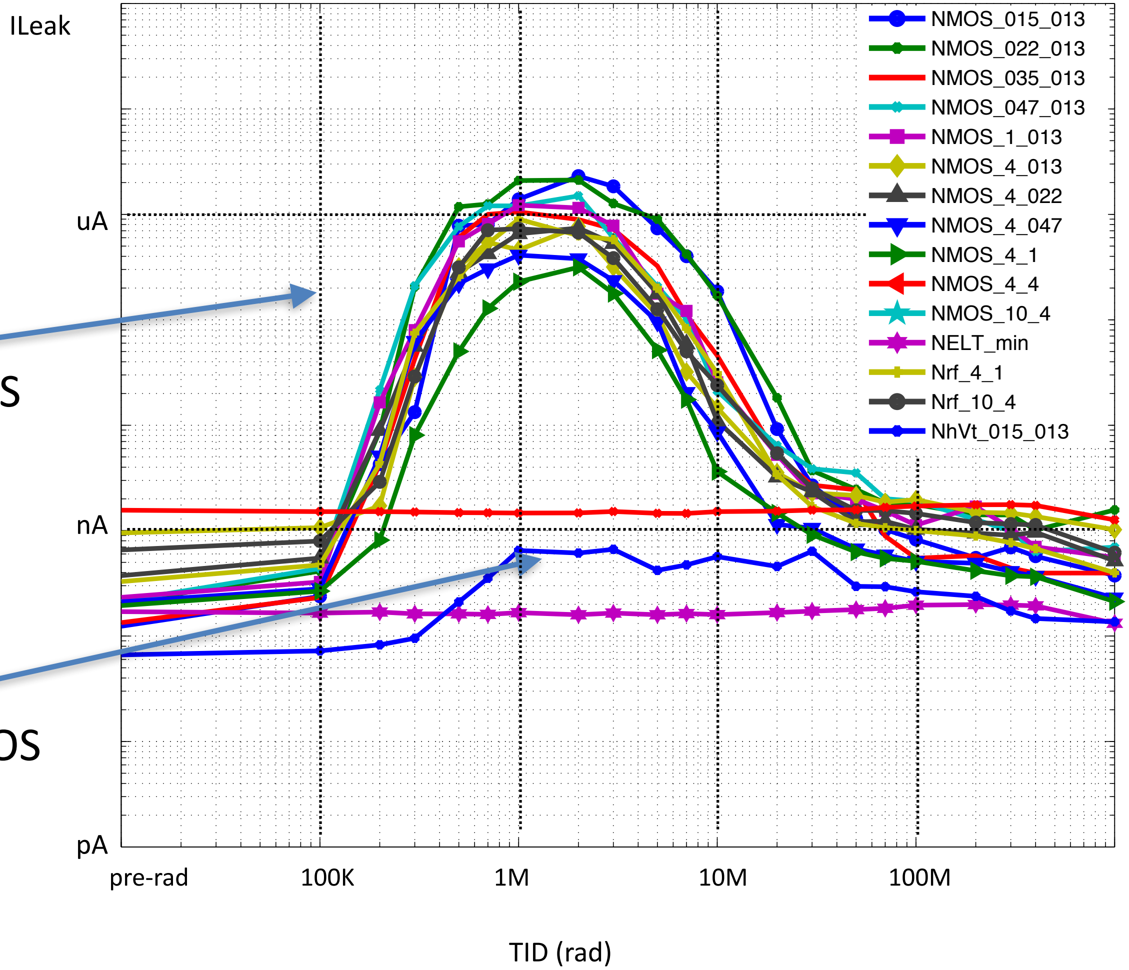
NMOS (core and I/O) from the two Fabs show very different behavior:

- Fab6 do not show increase of leakage current
- Fab14 have large increase of the leakage current, but the annealing time is fast

NMOS Core and I/O

NB: Fab14

NMOS Leakage current for Fab14



Regular NMOS

ELT or hVth NMOS

Measurements at 25C

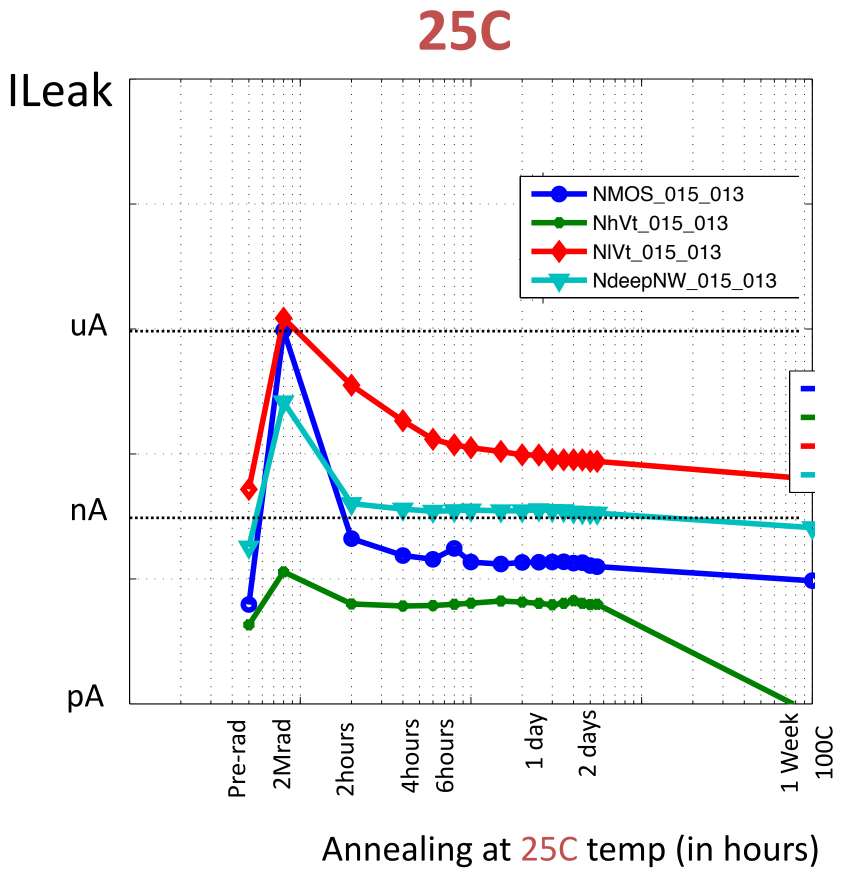
At -30C the peak is ~4 times higher

NB: Fab14

NMOS Leakage current with annealing

The aim is the understanding of the annealing behavior at 25C and -30C

Procedure: irradiation up to 2 Mrad (highest peak)
annealing for 48 hours with 2-5h delay between measurements



Annealing time:
at 25C is ~hours
at -30C is ~days

plot from Fab14 12inches

NB: Fab14

NMOS Leakage current with annealing

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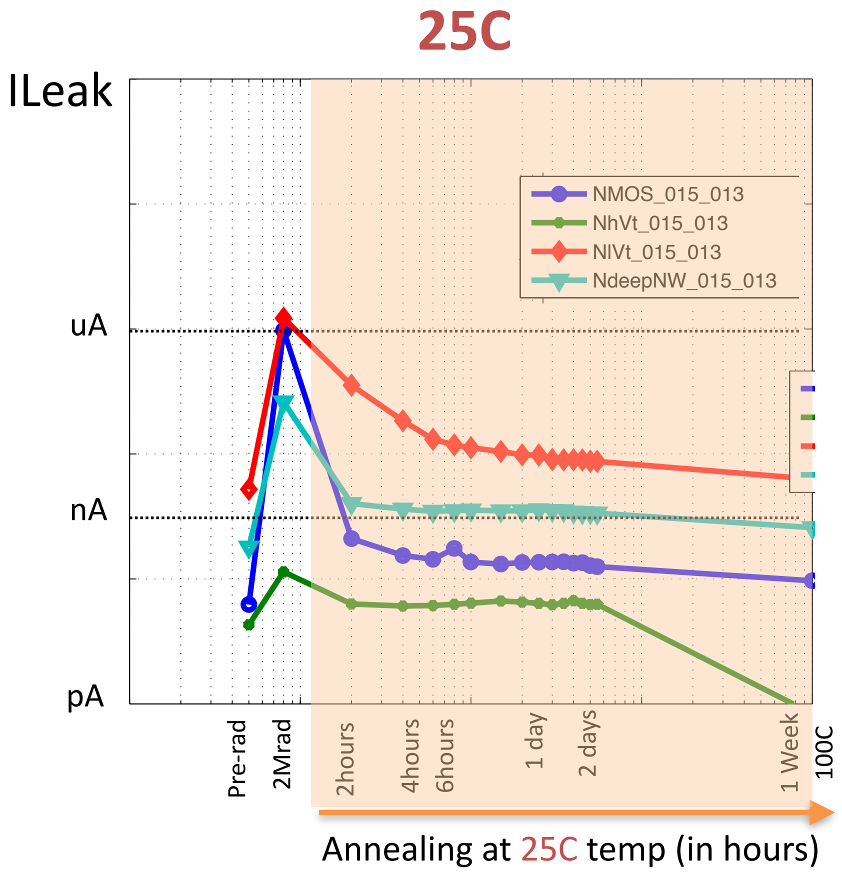
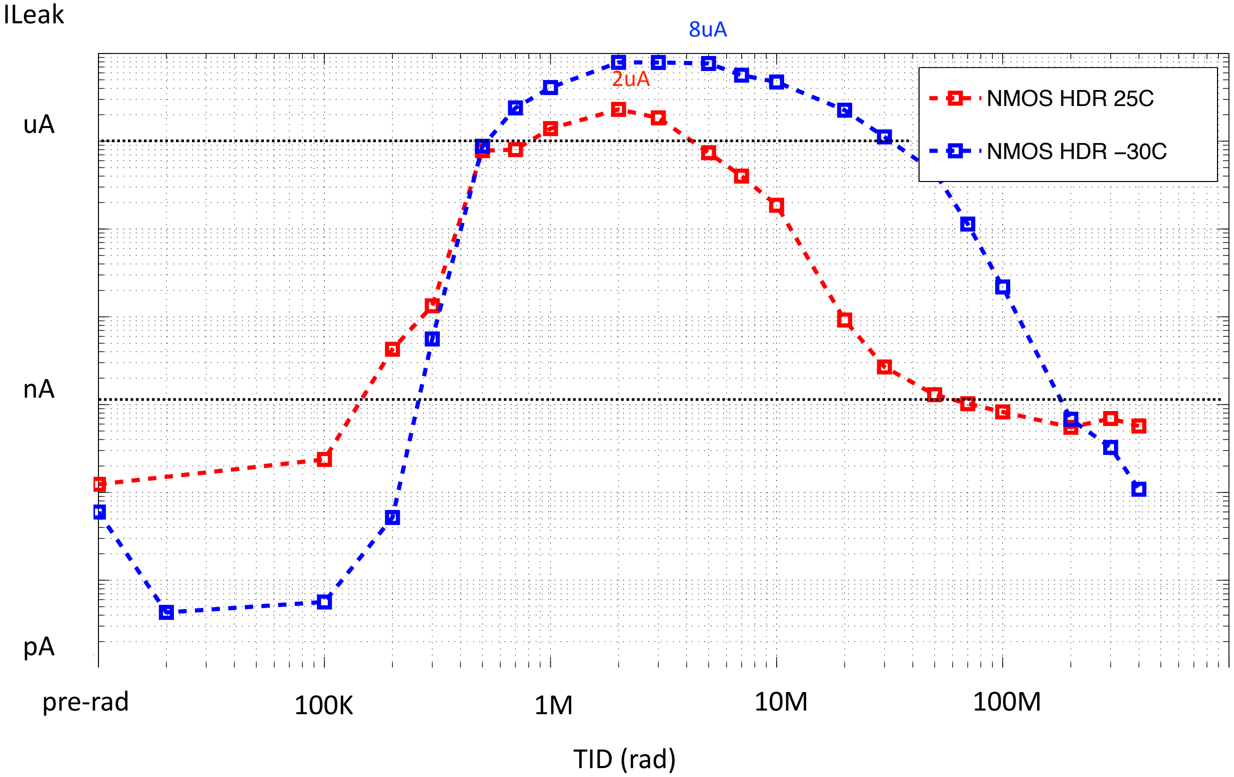


Annealing time:
at 25C is ~hours
at -30C is ~days

plot from Fab14 12inches

NB: Fab14

Differences between irradiation T

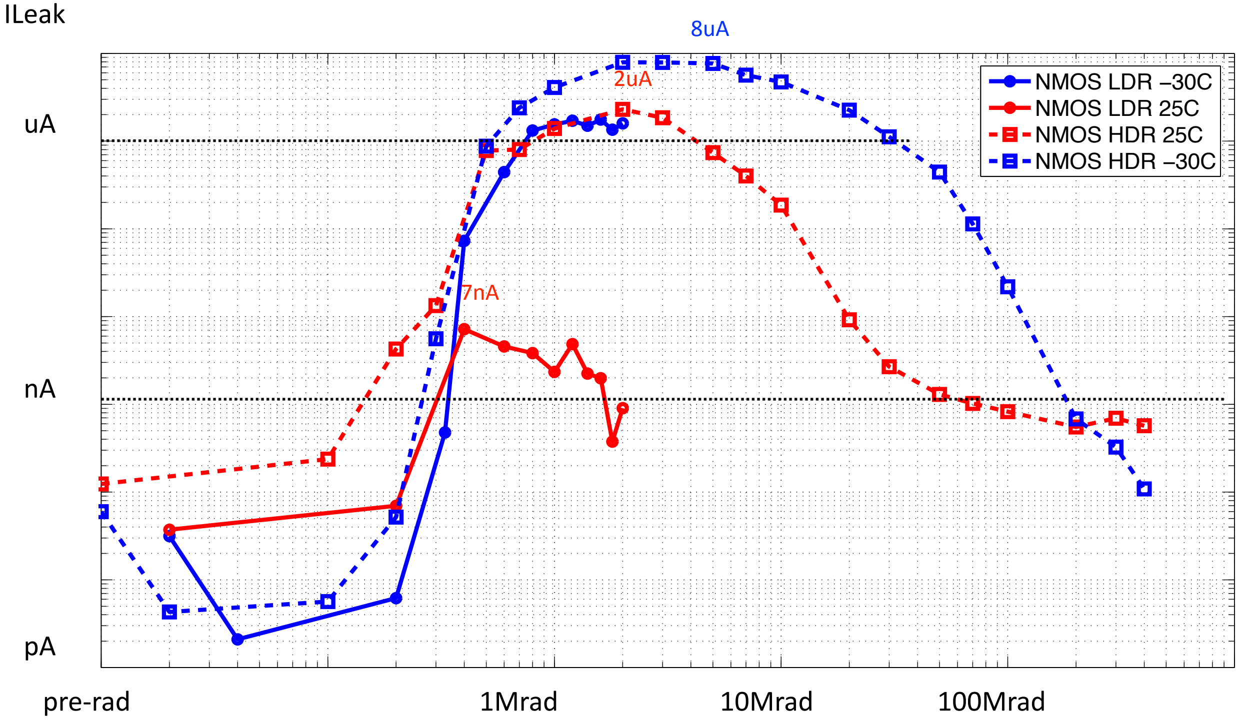


high dose rate (HDR) ~ 9Mrad/h (200Mrad/day)

plot from Fab14 12inches

NB: Fab14

Differences between irradiation T and Dose Rates



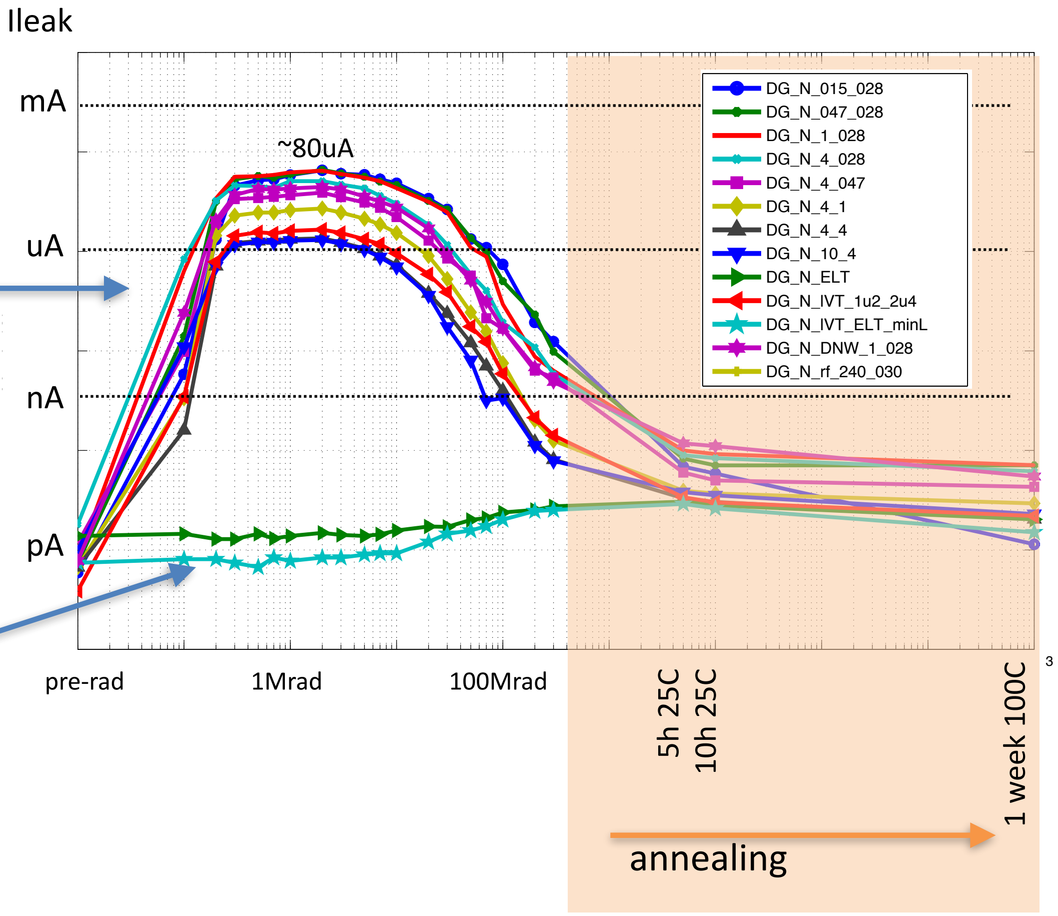
high dose rate (HDR) ~ 9Mrad/h (200Mrad/day)
low dose rate (LDR) ~ 90Krad/h (2Mrad/day)

dose rate for LHCb Velopix application: 0.2Mrad/day (400Mrad over 10years, assuming 200 beam days/year)

plot from Fab14 12inches

NB: Fab14

I/O NMOS Leakage current



Regular I/O NMOS

ELT I/O NMOS

Measurements at 25C

At -30C the peak is
~1.5 times higher

Annealing time:
at 25C is ~days
at -30C is ~weeks

plot from Fab14 12inches

Conclusions

The new 130nm technology from Fab6 (8 inches) is performing better than legacy 130nm technology in term of intrinsic TID tolerance.

The new 130nm technology from Fab14 (12 inches) shows:

- same performance for PMOS
- large increase of leakage current for NMOS, but
  - annealing time is fast and Ileak decreases with dose rate
  - hVth and ELT layout should be used if leakage is a concern

Therefore for production the best choice is Fab6.

For prototyping Fab14 can be used, knowing that during TID tests (with very high dose rate) the ASICs may suffer of the increase of leakage current

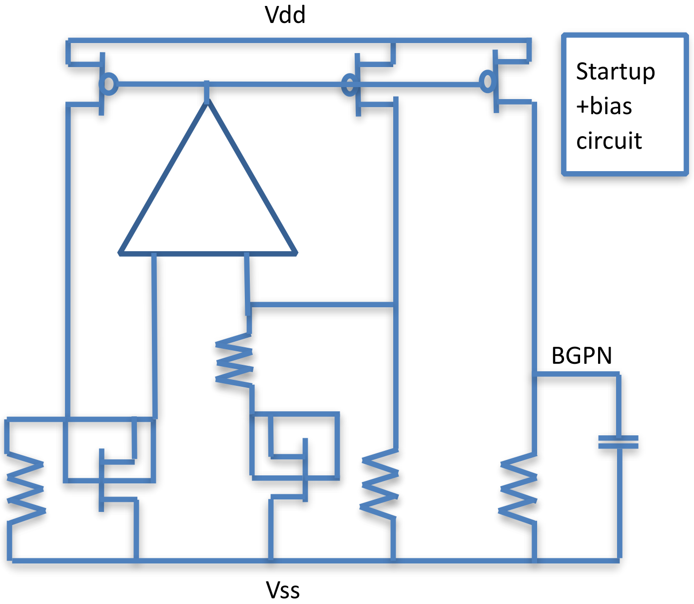
BANDGAP

Bandgap Information

Based on DTNMOS, it provides BGPN=~285mV

Total Idd current (at Vdd=1.2V)= 90uA

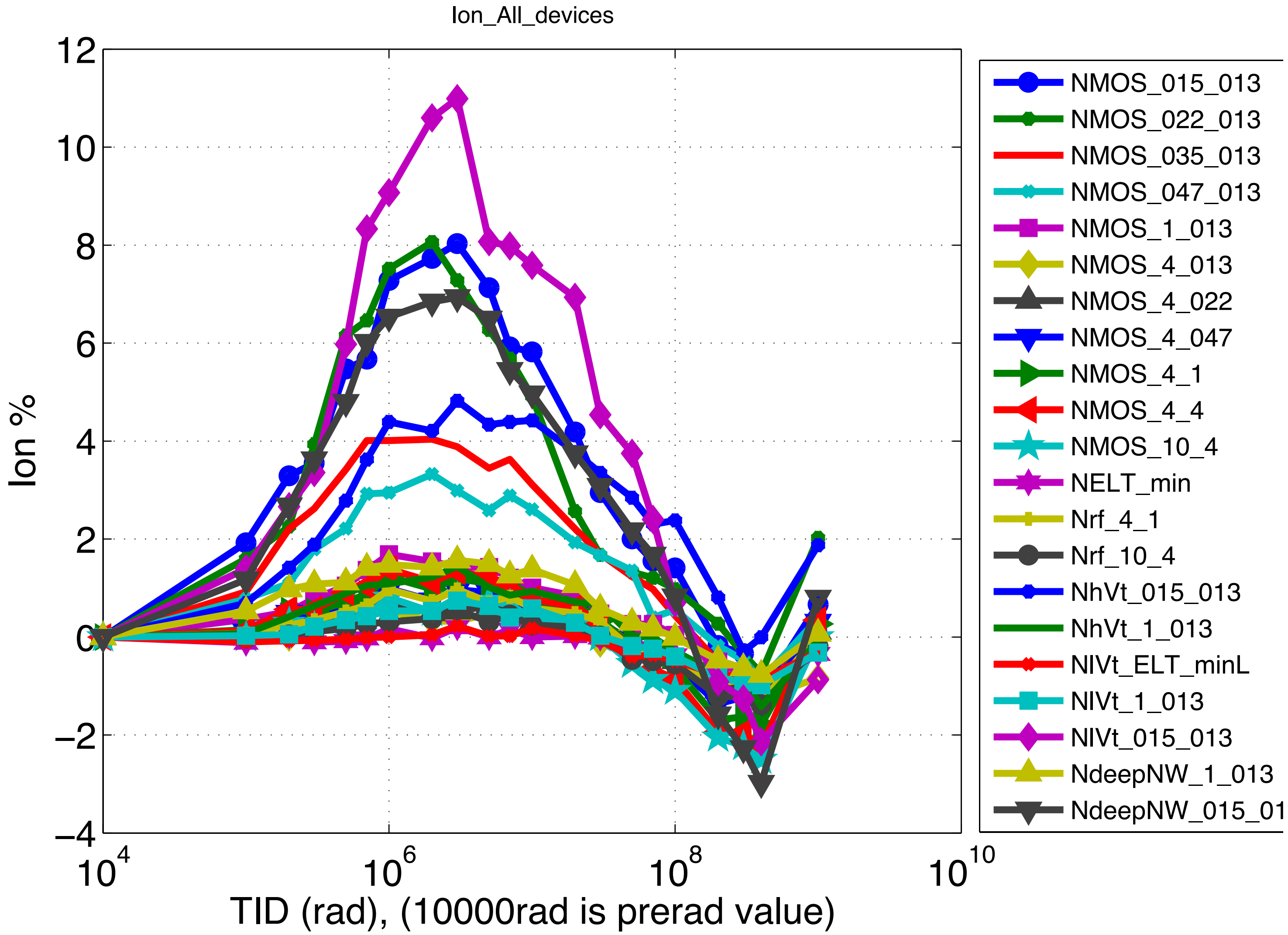
Layout dimensions 160um x 320um



Test Results	Range	Max variation (mV)	Max variation (%)
Temperature	-20C to 30C	1mV	0.3%
	-20C to 100C	5 mV	1.5%
VDD	0.5 to 1.3V	1.5mV	0.5%
TID	up to 400Mrad	3mV	1%

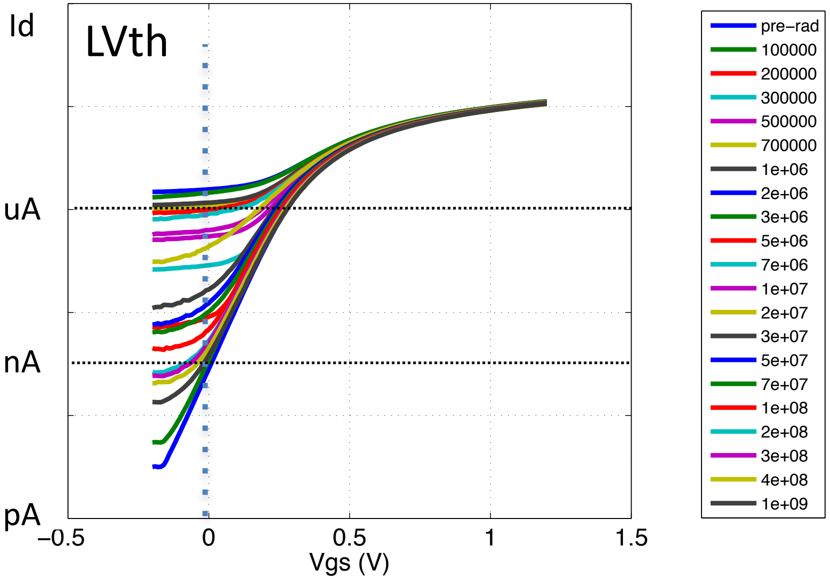
Backup Slides

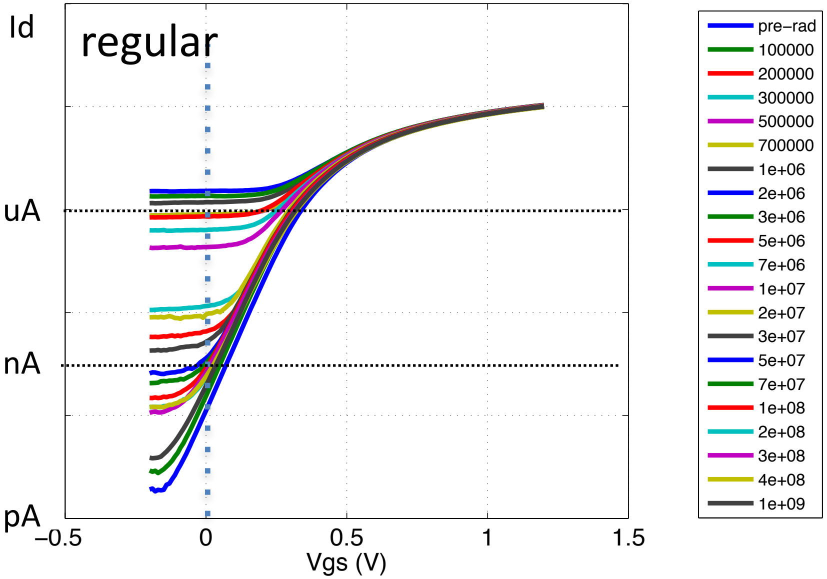
Core NMOS Ion degradation



NMOS 0.15/0.13 Id Vg – HDR,25C

plot from Fab14 12inches

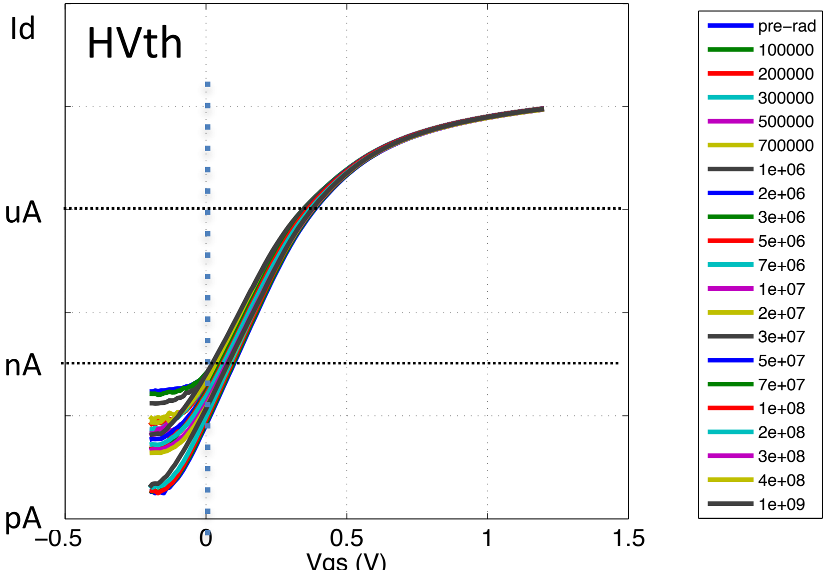




At 25C with high dose rate low Vth and regular transistors suffer of an important increase of the I_leak (up to 2uA)

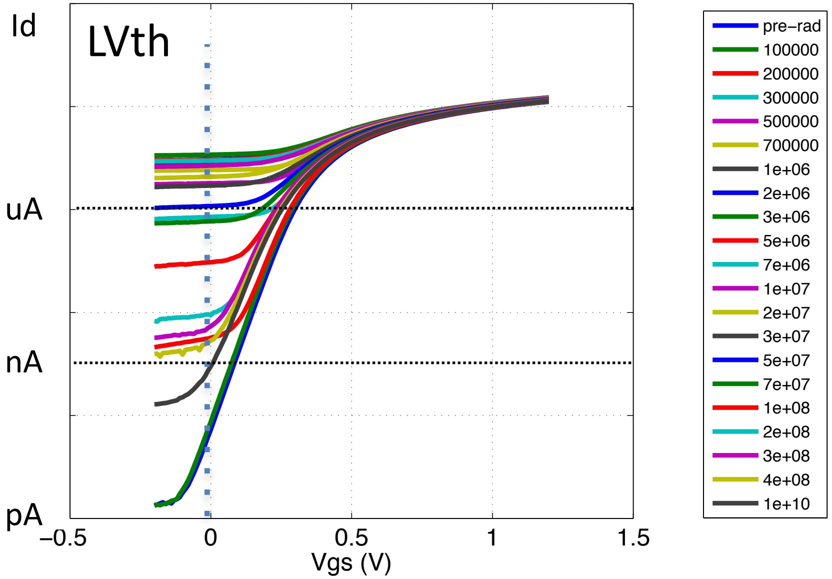
HighVth transistors instead have a negligible increase of the I_leak.

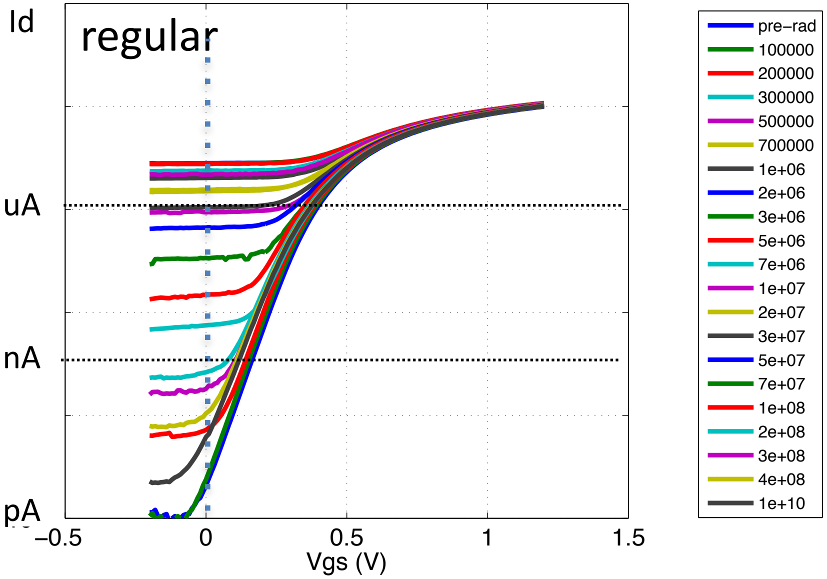
The extraction of the Vth shift is difficult and meaningless with the large increase of leakage current.

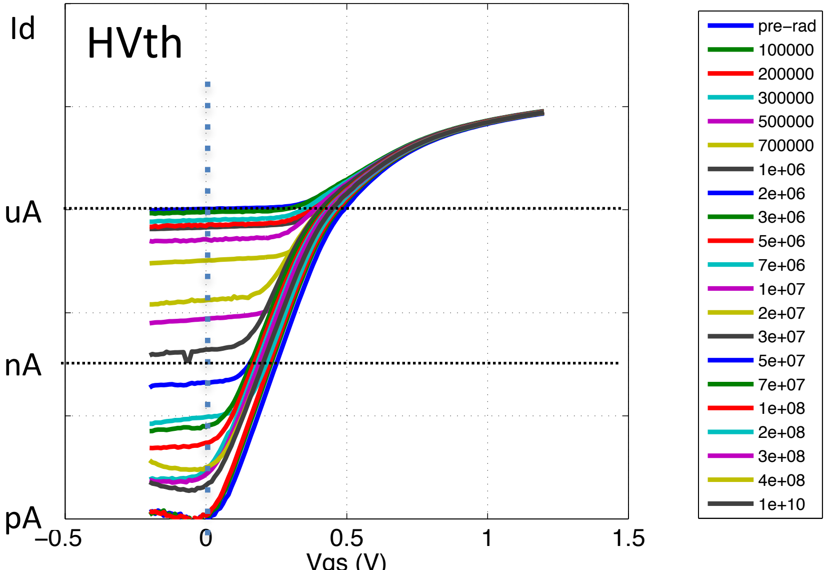


NMOS 0.15/0.13 Id Vg – HDR,-30C

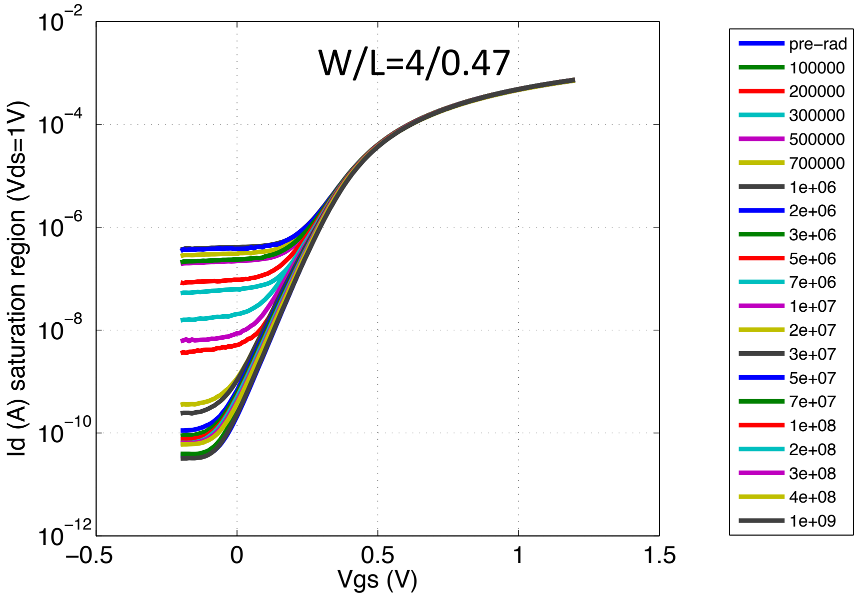
plot from Fab14 12inches

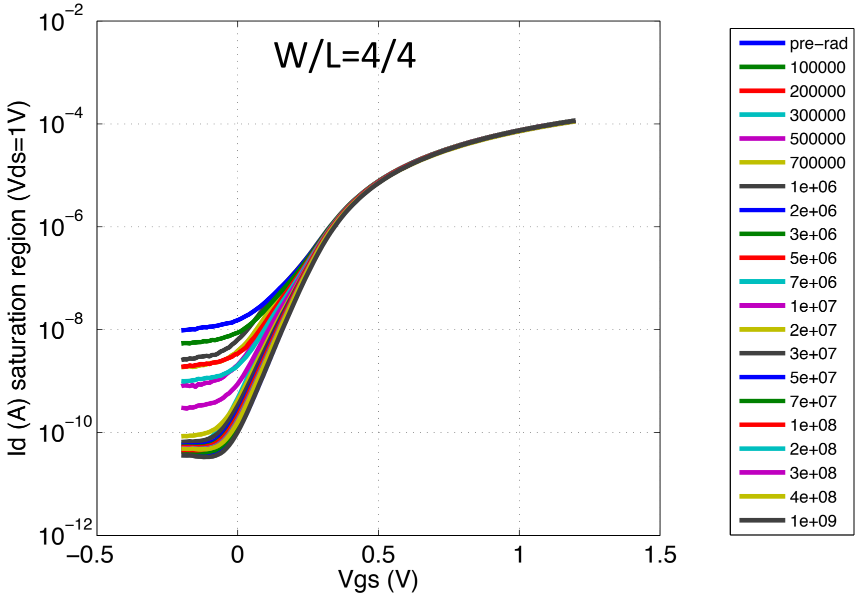


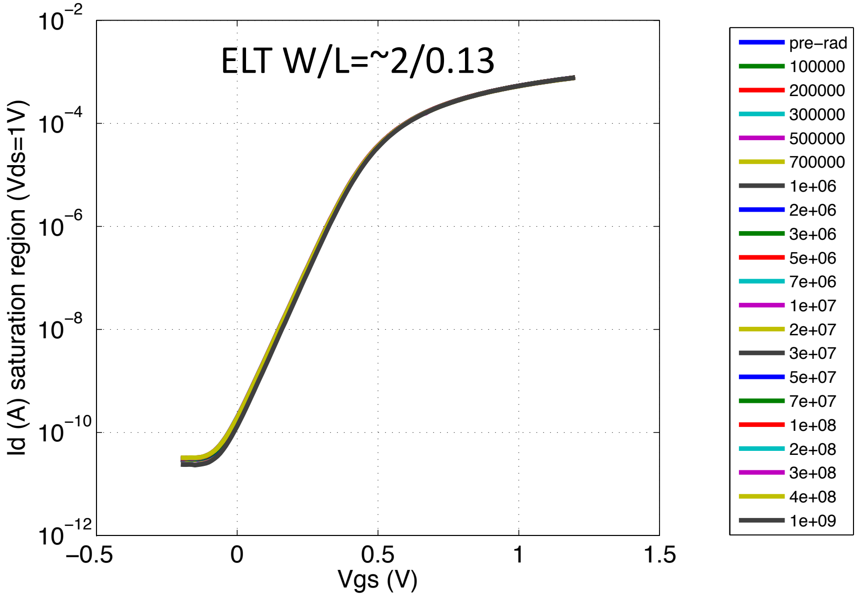




IdVg of ELT and big transistors







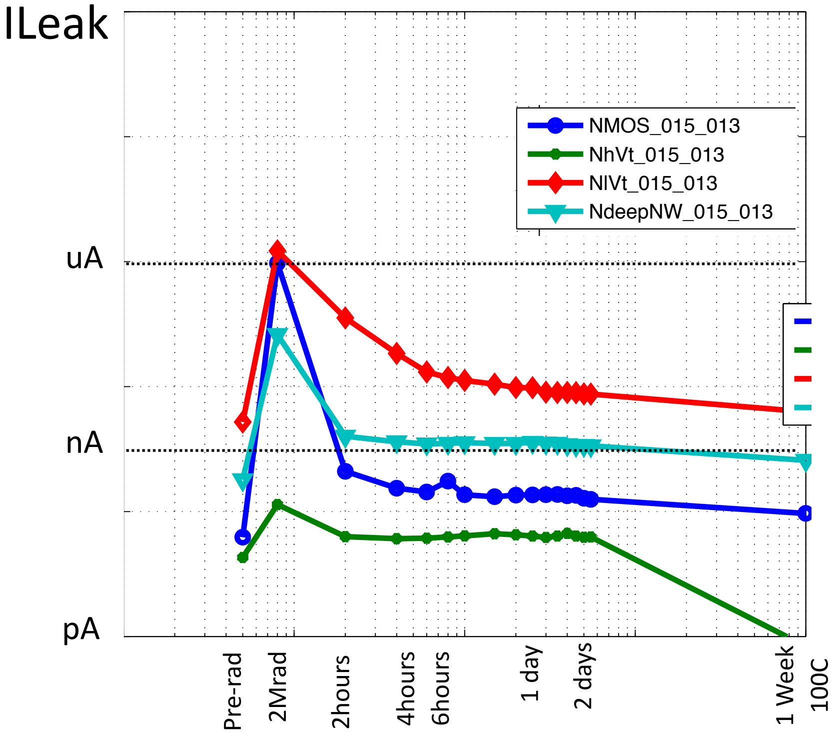
plot from Fab14 12inches

NMOS Leakage current with annealing

We want to see the impact of annealing at 25C and -30C

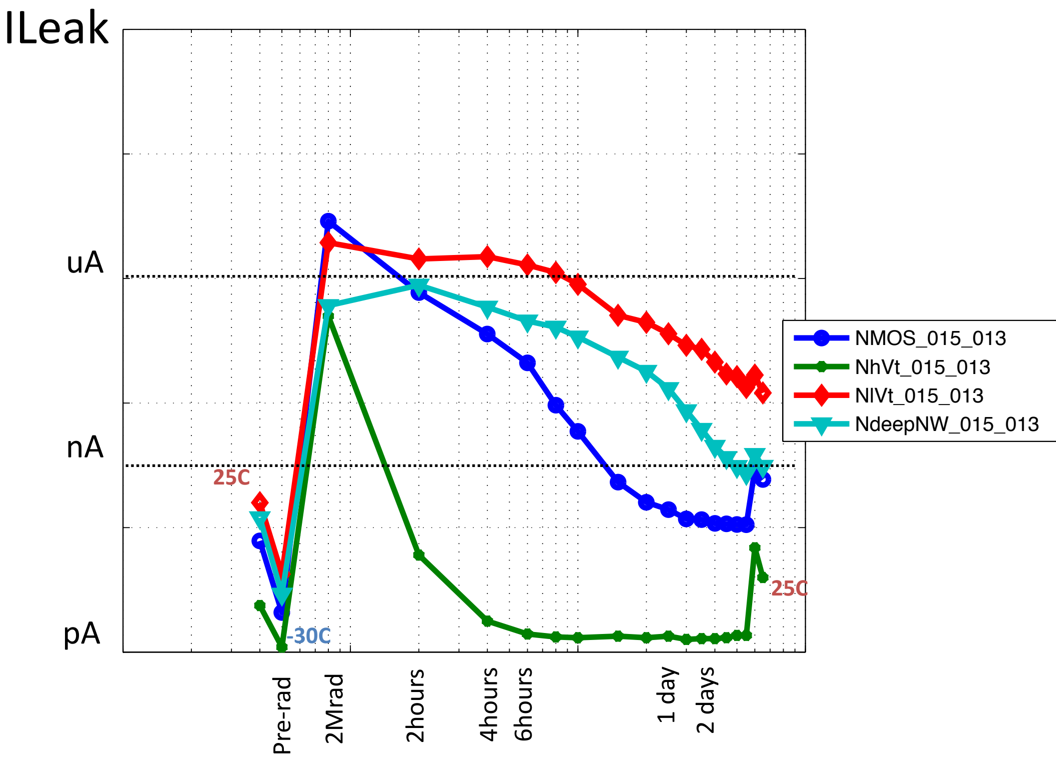
Procedure: irradiation up to 2 Mrad (highest peak)
annealing for 48 hours with 2-5h delay between measurements

25C



Annealing at 25C temp (in hours)

-30C



Annealing at -30C temp (in hours)

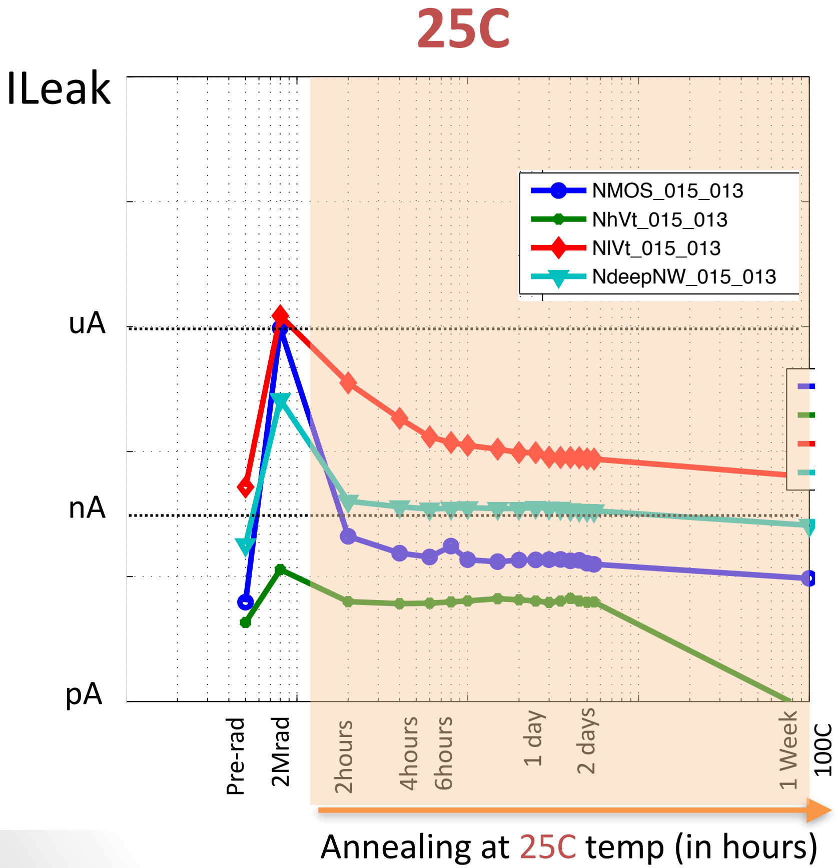
plot from Fab14 12inches

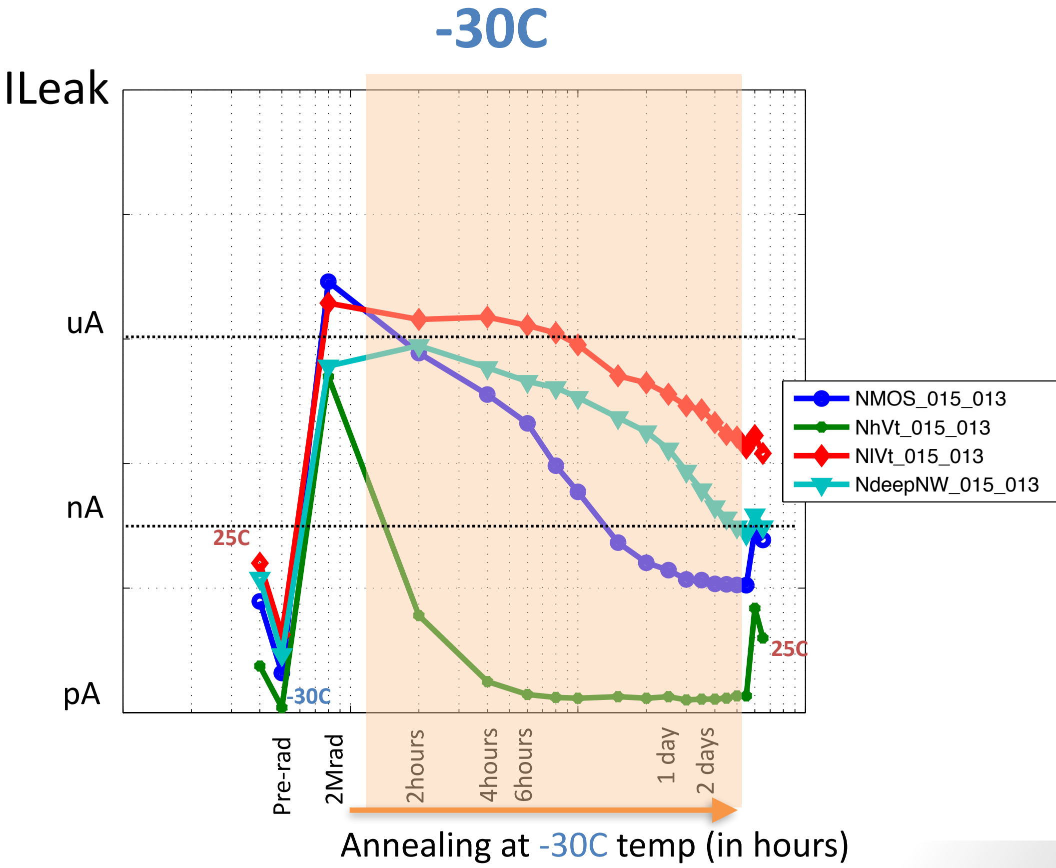
NMOS Leakage current with annealing

We want to see the impact of annealing at 25C and -30C

Procedure: irradiation up to 2 Mrad (highest peak)

annealing for 48 hours with 2-5h delay between measurements





plot from Fab14 12inches

Summary of NMOS core results

All NMOS flavors present a large increase of leakage current with TID (except hVt at 25C)

NMOS I_Leak 25C/-30C	*Pre-rad (A)*	*Peak HDR (A)*	*Peak LDR (A)*
Low Vth	*1n/80p*	*2u/10u*	*800n/8u*
regular	*100p/4p*	*2u/8u*	*7n/2u*
High Vth	*80p/1p*	*700p/1u*	*-/15n*

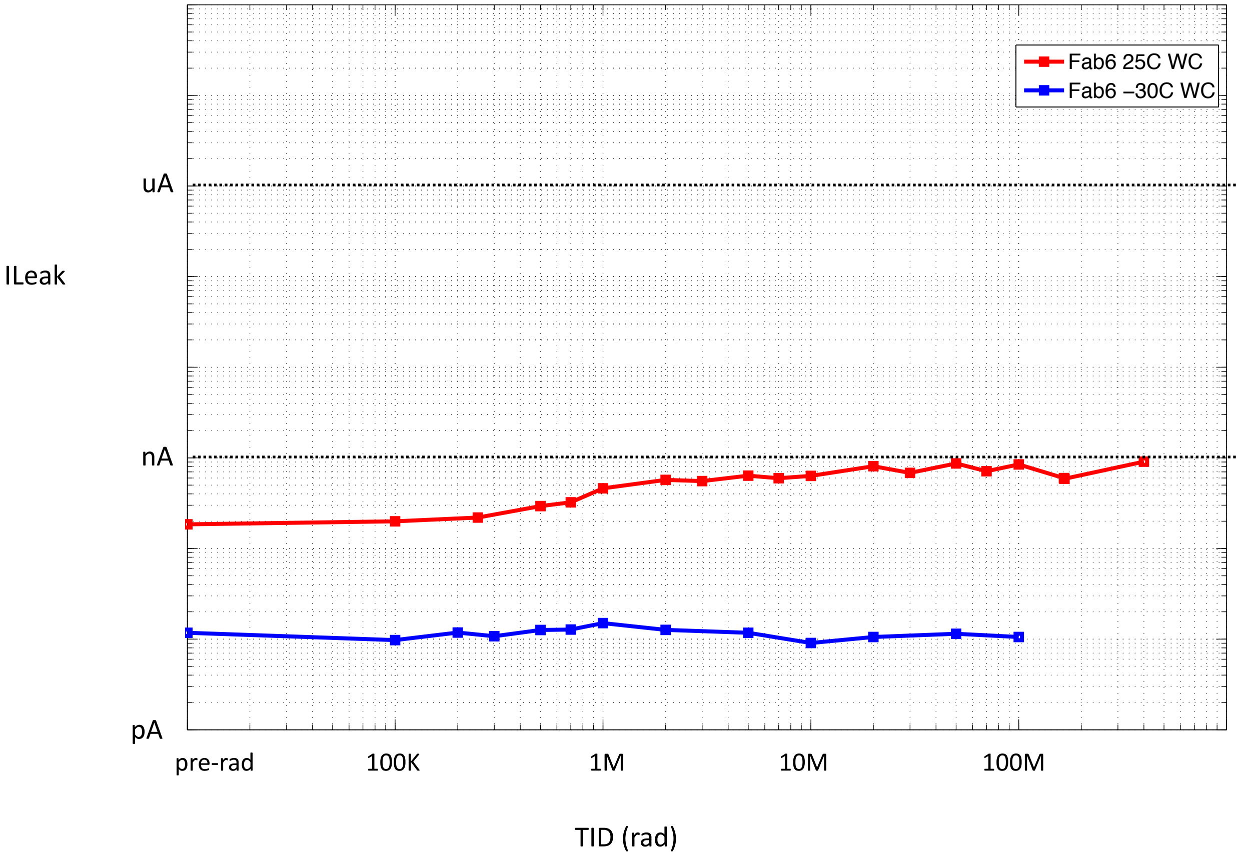
The annealing time is rather fast: hours at 25C, days at -30C (hours for hVt)

There is no degradation of the Ion (-2% at 400Mrad)

It is evident that there will issues for testing ASICs with big digital blocks (large increase of static current)

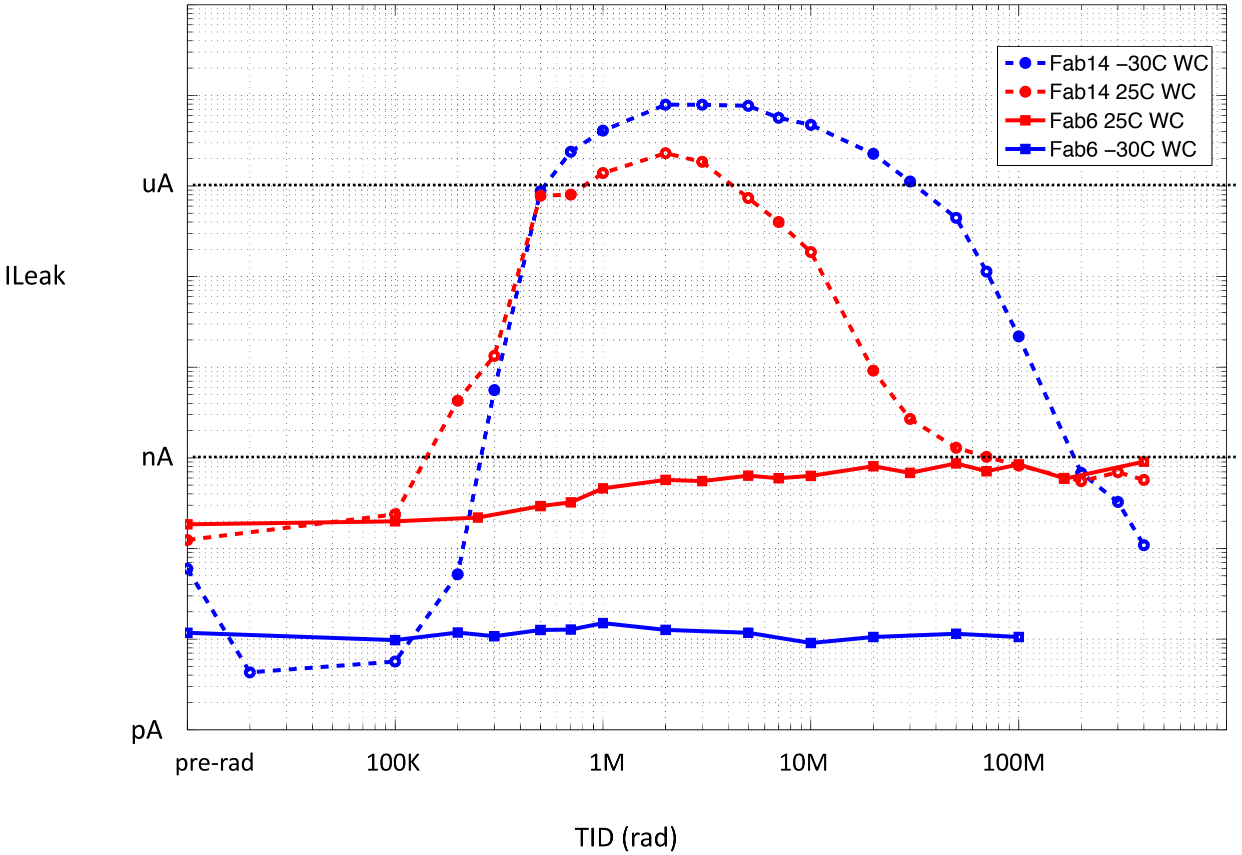
Strong suggestion for using hVt NMOS when possible (no leakage at 25C and at -30C the annealing time is 1-2h)

Leakage current difference between Fabs



NMOS min size
0.15/0.13

Leakage current difference between Fabs



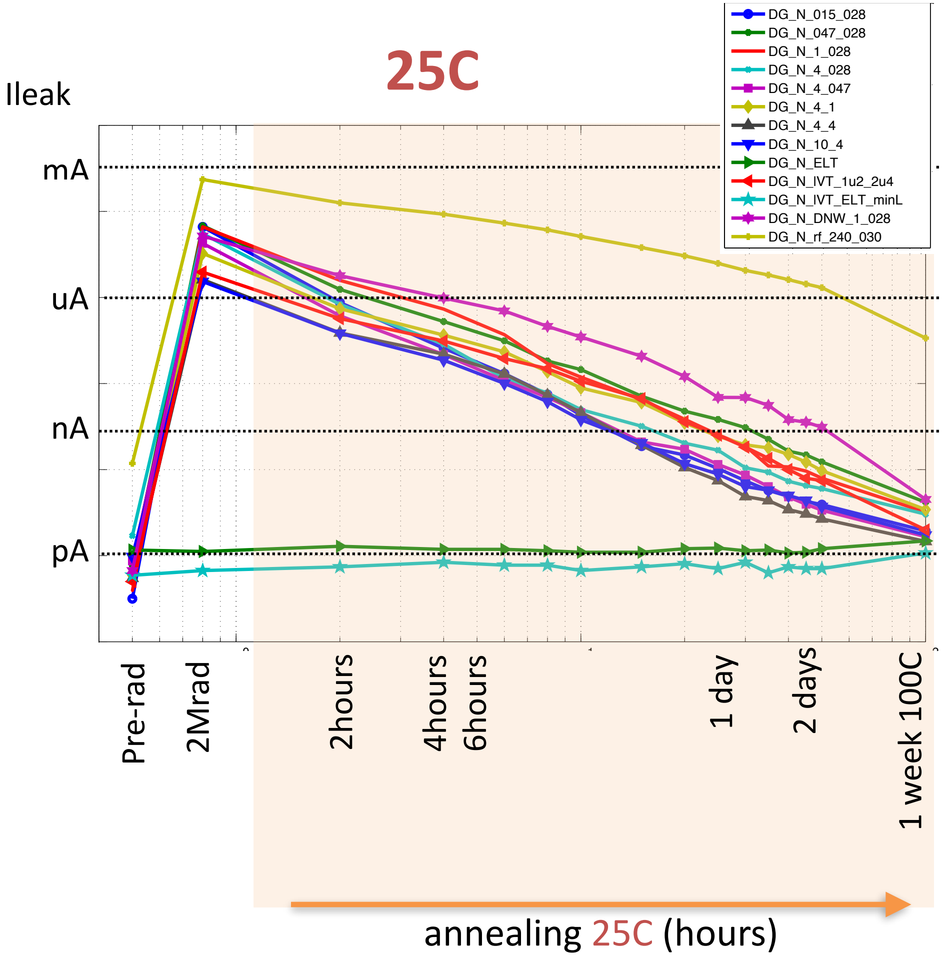
NMOS min size
0.15/0.13

NB: Fab14

I/O NMOS Leakage current with annealing

The aim is the understanding of annealing behavior at 25C and -30C

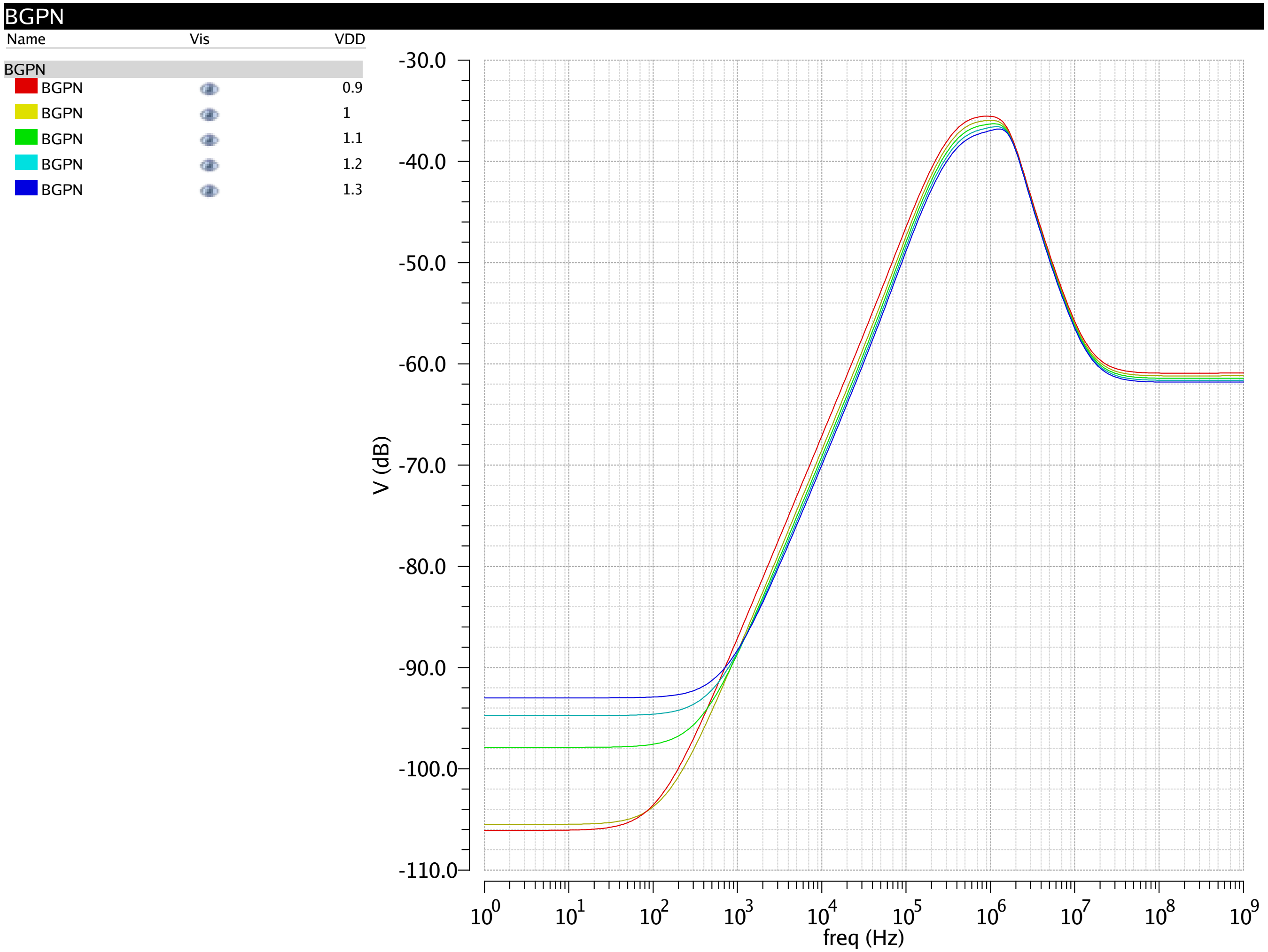
Procedure: irradiation up to 2 Mrad (highest peak)
annealing for several hours with 2-5h delay between measurements



Annealing time:
at 25C is ~days
at -30C is ~weeks

BANDGAP

PSRR simulations

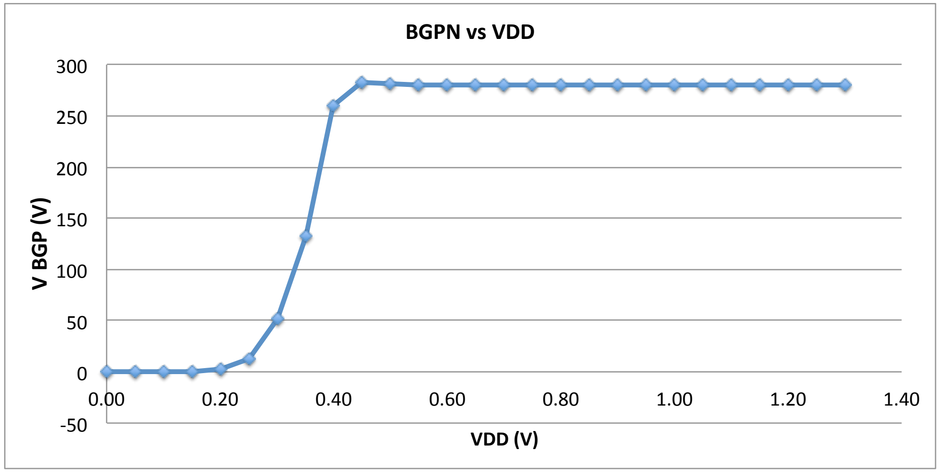


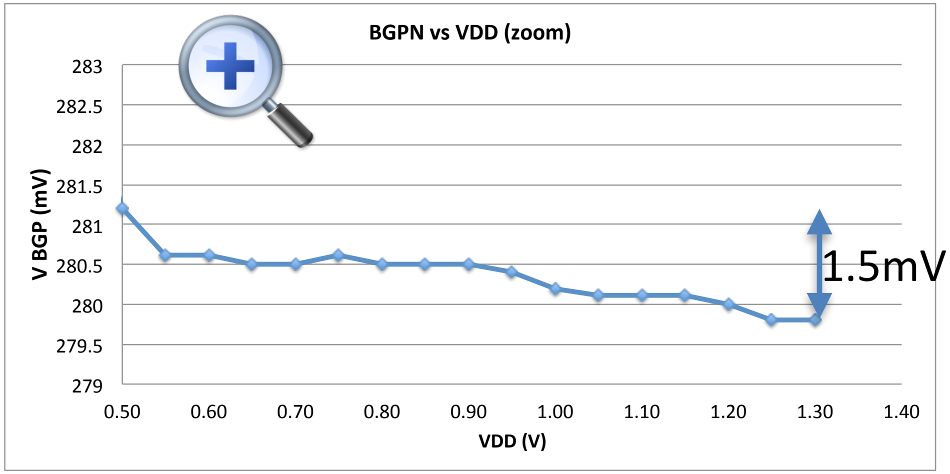
BGPN

Name	Vis	VDD
BGPN		
🟥 BGPN	👁	0.9
🟨 BGPN	👁	1
🟩 BGPN	👁	1.1
🟦 BGPN	👁	1.2
🟦 BGPN	👁	1.3

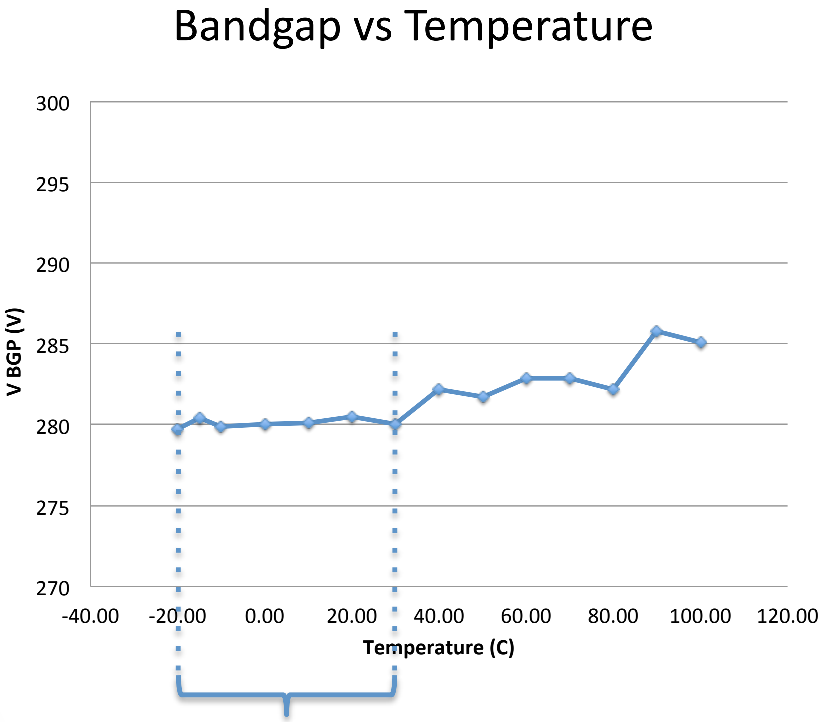
Bandgap vs VDD (real measures)

The bandgap is operative starting from Vdd=0.5V
the variation of the Bandgap in the range of Vdd=0.5-1.3V is 1.5mV

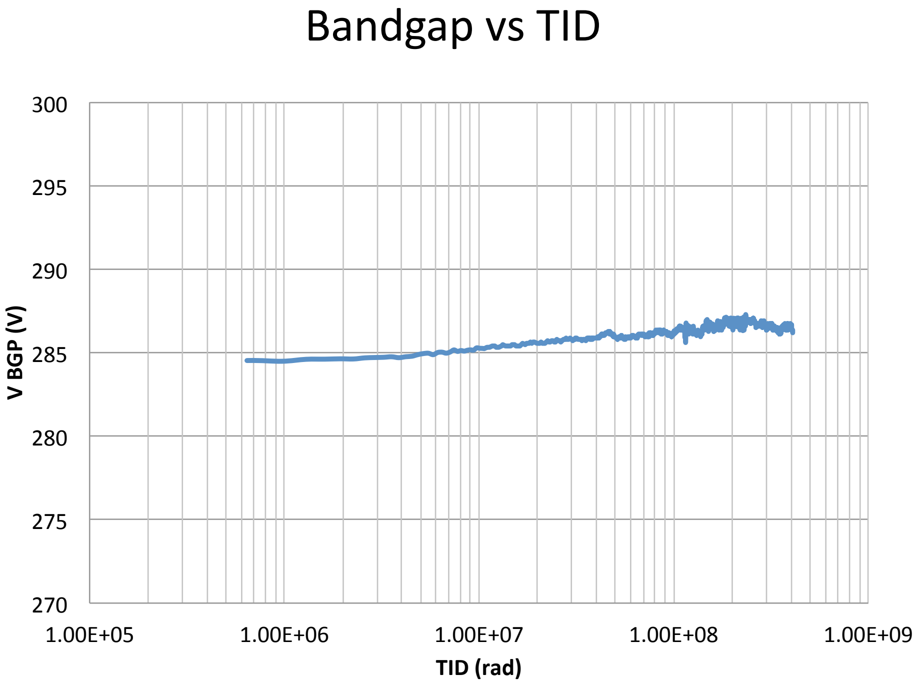




Bandgap vs T and TID



In the range from -20C to 30C the variation is less than 1mV



3 mV variation over 400Mrad