Will anyone care to go to ISSCC 2025 ?

Is Moore's Law still alive?

A. M. / PH-ESE

Integrated Circuits at the (Energy-Constrained) End of Silicon Scaling

Rob A. Rutenbar
Bliss Professor and Head
Computer Science • University of Illinois at Urbana-Champaign

THE END OF CMOS SCALING

Toward the Int
and Structural

Thomas Skotnicki,
H.-S. Philip Wong,

Intel's former chief architect: Moore's law will be dead within a decade

By Joel Hruska on August 30, 2013 at 8:30 am | 50 Comments

DARK SILICON AND THE END OF MULTICORE SCALING

A KEY QUESTION FOR THE MICROPROCESSOR RESEARCH AN
WHETHER SCALING MULTICORES WILL PROVIDE THE PERFORM

Appears in the Proceedings of the 38th International Symposium on Computer Architecture (ISCA '11)

Dark Silicon and the End of Multicore Scaling

Surviving the End of Scaling of Traditional Micro Processors in HPC

Robert G. Clapp
Mencer,

THE END OF DENNARD SCALING

APRIL 15, 2013 ADRIAN MCMENAMIN

The End of Moore's Law?

The current economic boom is likely due to increases in computing speed and decreases in price. Now there are some good reasons to think that the party may be ending.

MYSEMICONDAILY
Semiconductor News and Social Connections

BLOG PHOTOS PARTNERS ABOUT US CONTACT

Posted on July 9, 2014 by sdavis
← Previous Next →

The End of Scaling?

By Jeff Dorsch

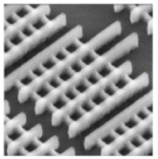
Are we reaching the end of scaling?

Yes and no.

TECH 11/13/2011 @ 5:42PM | 1,300 vie

The End of Semiconductor Scaling

+ Comment Now + Follow Comments



I have repeatedly heard that there is a brick wall facing the world of semiconductors ever since I first worked for National Semiconductor in the late 1970s. Scaling was destined to end, and once it did, the economic force behind the world of semiconductors would come to a grinding halt.

In the early 1980s a co-worker explained to me with conviction that

every
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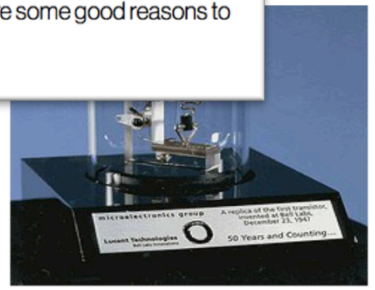
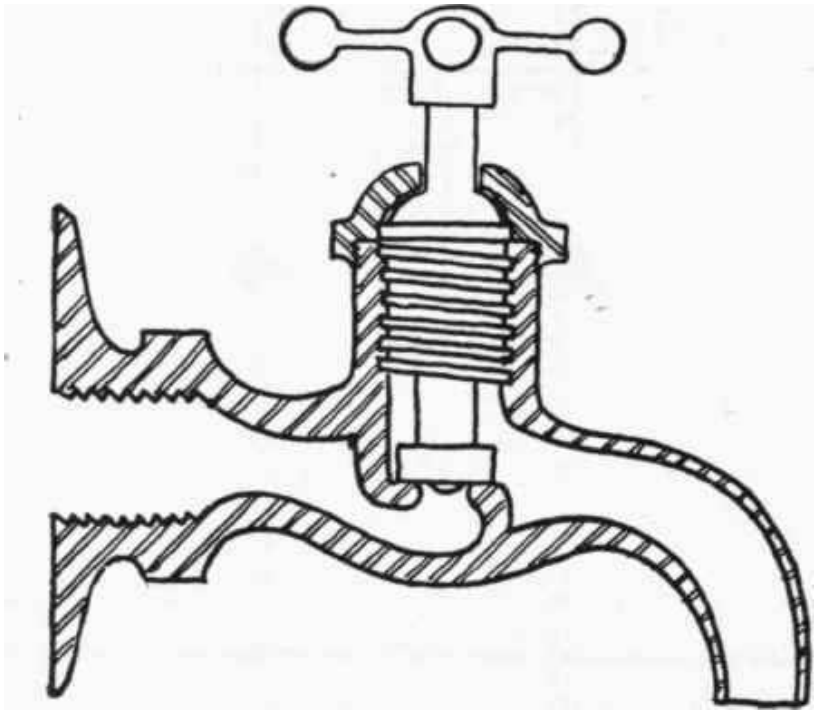


Replica-of-first-transistor (Photo credit: Revol-web)

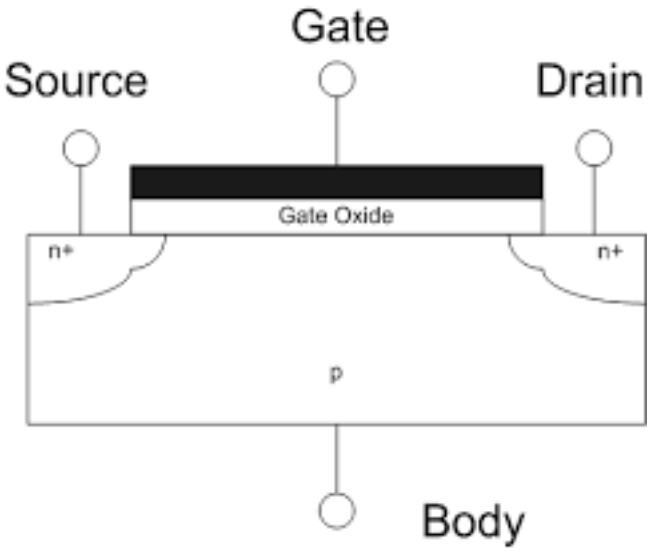
SCALING

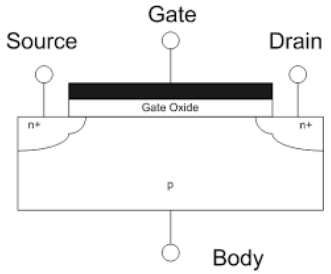
What do we want from a transistor anyway? (sorry engineers…)

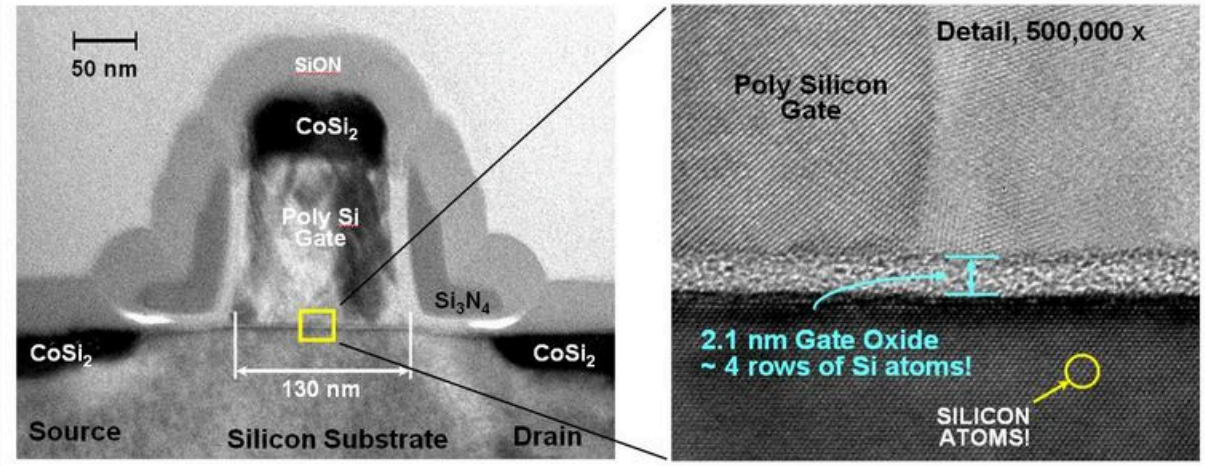
- A transistor (a digital transistor) is a device that has to have the following characteristics:
  - to work as a switch (on or off)
  - make a transition between the two states in a time as short as possible
  - has no leakage current when off
  - has to deliver high current when on (to drive strongly the next stage).
    - Unfortunately this it is not uncorrelated from the previous requirement
  - make a transition between the two states with a voltage drive (Vg) as small as possible
  - control terminal should not be influenced by input/ output terminal(s)
  - be physically small (otherwise other “parasitics” ruin the party)
- Good “analog” characteristics are desirable but by far not necessary or even important for the the majority of applications.



Scaling of FET







Summary of SC and other effects

- High leakage current
- Gate leakage current
- Threshold voltage depends on V_{ds} (DIBL)
- Threshold voltage depends on L
- Mobility degradation (vertical electric field too strong)
- Velocity saturation (carriers can't move faster than thermal velocity)
- Poor r_0 and $g_m * r_0$
- Hot electrons
- Punch-through
- …

Tricks already in use

- Bag of *tricks* already in use (apart from geometrical shrinking):
  - Lithography: many — Print structures << λ
  - High K gate dielectric — *Thicker gate oxide (yes, thicker) to reduce gate leakage*
  - Strained SiGe channels — *Increase mobility, i.e. faster electrons*
  - Metal gate — *Reduces gate resistance*
  - More metallization layers — *Increase density*
  - Low K inter-metal dielectric — *Reduces cross-capacitance*
  - Cu wires — *Reduces interconnect resistance*

What is scaling all about?

- Speed?
  - III-IV materials, Ge
- Low Power?
  - Tunneling effect devices for low ΔV_g switching
- High density?
  - High density multi-chip assembly (many options!)
  - 3D assemblies (wafer on wafer)
  - Fully 3D monolithic ICs (watch what is being done in the area of flash memories!)
- Exotic
  - Ferroelectric memories and resistive RAMs
  - Quantum devices

	Speed	Power	Density
CMOS (until recently)	☺	☺	☺
III-V or Ge	☺	☹	😐
New devices with enhanced Sub Slope	☺	😐	😐
3D	☺	☹	☺
Quantum	?	?	??

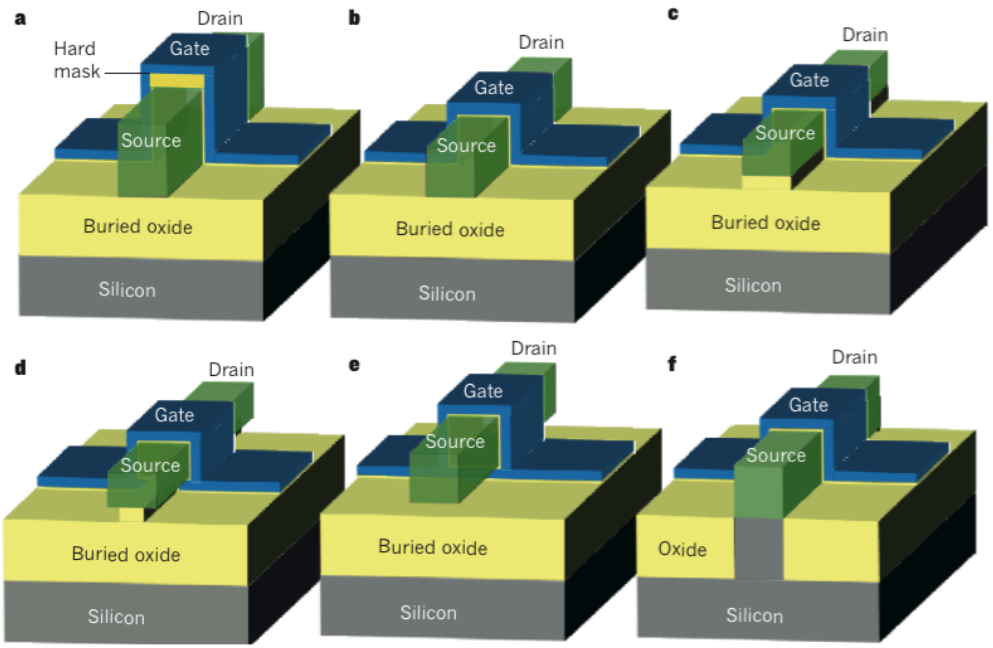
IEDM 2014

- What options are around
  - FinFETs
  - Low subthreshold slope transistors
- Imagers

FINFET AND GATE CONTROL

Multi-gate devices

- Intel Tri-gate
- TSMC Finfet
- STM FDSOI



from: Ferain, **"Multigate transistors as the future of classical metal–oxide–semiconductor field-effect transistors "**,

FinFET History

Prof. Chenming Hu
UC Berkeley

is the silicon substrate. So you really have to do something on both sides so you're pinching against something firm, and that's what the FinFET is doing. We should pinch the channel [where electrons flow] on two sides and on top. The more pinching sides, the better.

Pinching the hose will allow us to use a much, much shorter hose. That's extremely important. Making things small is really the key of making the electronics cheaper, faster, and lower power.

IEEE Spectrum: The idea for FinFETs has been around for a while. How did it all get started?

Chenming Hu: DARPA [the Defense Advanced Research Projects Agency] sent out a request for proposals in 1996 for ideas to develop electronic switches beyond 25 nm. At the time, the industry was using 250-nm transistors, and the general view was that transistors could not be scaled below 100 nm. But my students and I had already been thinking about how to get transistors to scale to 25 nm and beyond.

There was a quick meeting probably lasting only five minutes between myself and two colleagues—Professor Tsu-Jae King Liu and Professor Jeff Bokor. The meeting was short because we already knew what to do.

I was on a flight to a conference in Japan, and I had about 10 hours, so I just wrote down the technical proposal in longhand. I proposed two structures that we'd been thinking about for a while. One was FinFETs, and the other is what we call an ultrathin-body silicon-on-insulator (UTB SOI).

We got the contract in 1997, and that gave us the resources to demonstrate FinFETs experimentally. A young graduate student named Xuejue "Cathy" Huang made the working device, and the team of three professors and 11 students and visiting researchers published it in 1999.

This proves that long flights are useful!

First Berkeley FinFET Paper

Sub 50-nm FinFET: PMOS

Xuejue Huang, Wen-Chin Lee, Charles Kuo, Digh Hisamoto*, Leland Chang, Jakub Kedzierski, Erik Anderson**, Hideki Takeuchi, Yang-Kyu Choi, Kazuya Asano^, Vivek Subramanian, Tsu-Jae King, Jeffrey Bokor and Chenming Hu

Department of Electrical Engineering and Computer Sciences, University of California at Berkeley, CA 94720 USA
Tel: (510) 642-1010; FAX: (510) 643-2636; e-mail: xuejue@eecs.berkeley.edu
*Central Research Laboratory, Hitachi Ltd., Tokyo, Japan
**Lawrence Berkeley National Laboratory, University of California, Berkeley, CA 94720 USA
^NKK Corp., Japan

Abstract

High performance PMOSFETs with gate length as short as 18-nm are reported. A self-aligned double-gate MOSFET structure (FinFET) is used to suppress the short channel effect. 45 nm gate-length PMOS FinFET has an I_{dsat} of 410 μA/μm (or 820 μA/μm depending on the definition of the width of a double-gate device) at Vd = Vg = 1.2 V and Tox = 2.5 nm. The quasi-planar nature of this variant of the double-gate MOSFETs makes device fabrication relatively easy using the conventional planar MOSFET process technologies. Simulation shows possible scaling to 10–nm gate length.

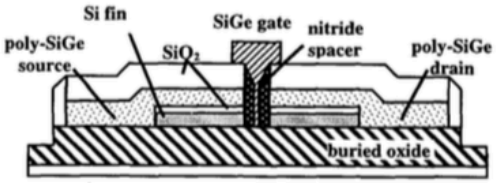


Figure 1: Schematic drawing of FinFET

Fig. 1 shows an exploded view of the FinFET device. The following process sequence was used to fabricate the device. 100 nm SOI film over buried oxide was thinned to 50 nm by thermal oxidation. Ion implantation established a body

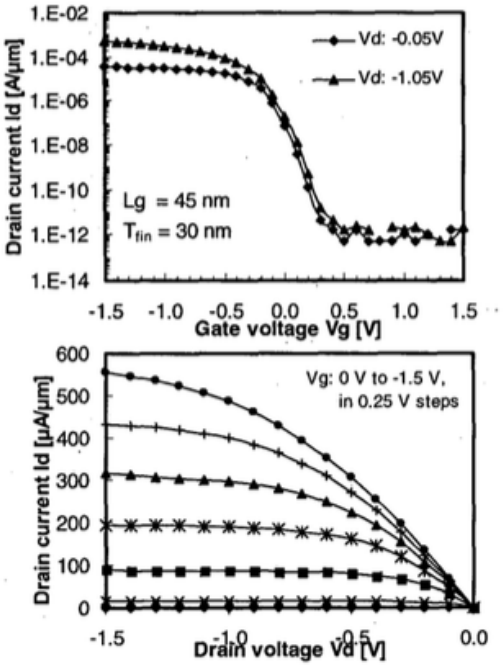


Figure 6: IV characteristics for 45-nm gate length and 30-nm thick Si body PMOS device

Published in:
Electron Devices Meeting, 1999. IEDM '99. Technical Digest. International

More complete LBL FinFET Paper

FinFET—A Self-Aligned Double-Gate MOSFET Scalable to 20 nm

Digh Hisamoto, *Member, IEEE*, Wen-Chin Lee, Jakub Kedzierski, Hideki Takeuchi, Kazuya Asano, *Member, IEEE*, Charles Kuo, Erik Anderson, Tsu-Jae King, Jeffrey Bokor, *Fellow, IEEE*, and Chenming Hu, *Fellow, IEEE*

***Abstract*—MOSFETs with gate length down to 17 nm are reported. To suppress the short channel effect, a novel self-aligned double-gate MOSFET, FinFET, is proposed. By using boron-doped $Si_{0.4}Ge_{0.6}$ as a gate material, the desired threshold voltage was achieved for the ultrathin body device. The quasiplanar nature of this new variant of the vertical double-gate MOSFETs can be fabricated relatively easily using the conventional planar MOSFET process technologies.**

***Index Terms*—Fully depleted SOI, MOSFET, poly SiGe, short-channel effect.**

I. Introduction

TO DEVELOP sub-50-nm MOSFETs, the double-gate structure has been widely studied. This is because

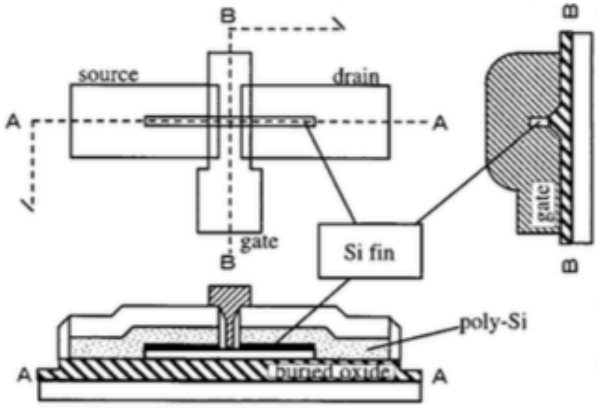


Fig. 1. FinFET typical layout and schematic cross sectional structures.

quasi planar technology. In this paper, the fabrication process and the device characteristics in the sub-50 nm gate-length region are presented. We demonstrate the feasibility of the new device structure named FinFET.

Previous ideas

Monte Carlo Simulation of a 30 nm Dual-Gate MOSFET: How Short Can Si Go?

D. J. Frank, S. E. Laux and M. V. Fischetti

IBM Research Division, T. J. Watson Research Center
P.O. Box 218, Yorktown Heights, NY 10598

Conclusions

In summary, it appears that high performance Si MOSFETs can be scaled down to gate lengths of order 30 nm. Such devices are still suitable for digital circuitry, and may have transconductances as high as 2300 mS/mm and ring oscillator speeds near 1 ps. The technology needed to do this includes thickness control of very thin layers, dual gate alignment, very abrupt doping profiles and gate work function control. A high thermal conductivity method of removing heat from such devices would also need to be found.

References

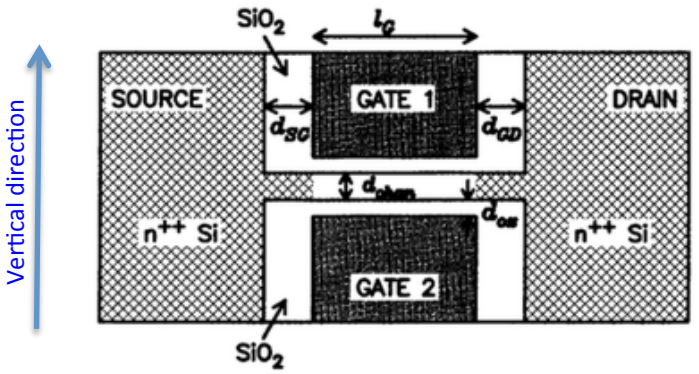


Fig. 1. Dual-gate MOSFET cross-section. Our simulations all use $d_{ox} = 3$ nm, $d_{SG} = d_{GD} = 0.3 \times l_G$, and 10^{20} cm^{-3} n-type source and drain doping.

Previous ideas++

Design and Performance Considerations for Sub-0.1μm Double-Gate SOI MOSFET's

Hon-Sum Wong, David J. Frank, Yuan Taur, and Johannes M.C. Stork[1]

I.B.M. Thomas J. Watson Research Center,
P.O. Box 218, Yorktown Heights, New York 10598, U.S.A.

ABSTRACT

We present a simulation-based analysis of the device design and circuit performance trade-offs between short channel immunity and parasitic device capacitances of sub-0.1μm double-gate SOI MOSFET's. We demonstrate that perfect alignment of the bottom gate to the top gate is not necessary to achieve adequate short channel immunity but is required to maintain short gate delays. Double-gate MOSFET device design guidelines are provided.

in reduced worst-case short-channel immunity and lower current drive for MBG due to the weaker backgate control when the bottom gate is offset from the drain (Fig. 1(d)) or the source (Fig. 1(e)).

DEVICE DESIGN

source/drain doping (Fig. 1(a)). However, fabrication of DG-SOI at the 100 nm regime with this ideal self-aligned structure is difficult. A promising approach presented recently [5] is the "flip-bonded-etchback SOI" method in which the bottom gate is formed prior to the bonded-etchback process and the subsequent formation of the top gate and source/drain structures. In this method, the bot-

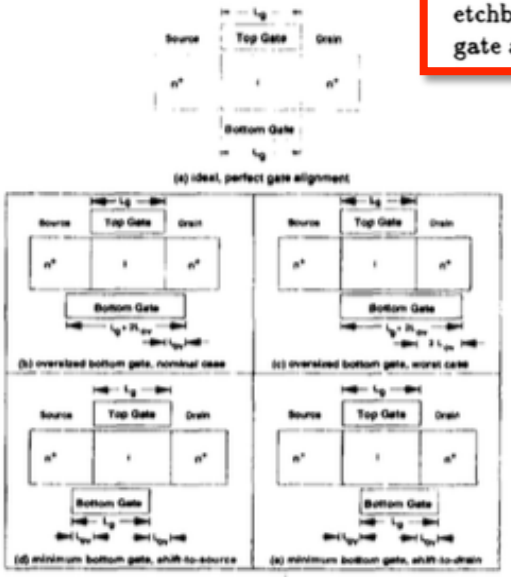


Figure 1: Schematic views of the double-gate SOI MOSFET's.

H. S. Wong, D. J. Frank, Y. Taur, and J. M. C. Stork, "Design and per- formance considerations for sub-0.1 um double-gate SOI MOSFET's," in *IEDM Tech. Dig.*, 1994, pp. 747–750.

…and this?

IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 38, NO. 6, JUNE 1991

Impact of the Vertical SOI "DELTA" Structure on Planar Device Technology

Digh Hisamoto, *Member, IEEE*, Toru Kaga, *Member, IEEE*, and Eiji Takeda, *Senior Member, IEEE*

***Abstract*—A fully depleted lean channel transistor (DELTA) with its gate incorporated into a new vertical ultra-thin SOI structure is presented. In the deep-submicrometer region, selective oxidation produces and isolates an ultra-thin SOI MOSFET that has high crystalline quality, as good as that of conventional bulk single-crystal devices. Experiments and three-dimensional simulations have shown that this new gate structure has effective channel control, and that the vertical ultra-thin SOI structure provides superior device characteristics: reduction in short-channel effects, minimized subthreshold swing, and high transconductance.**

First version of this work at IEDM 1989

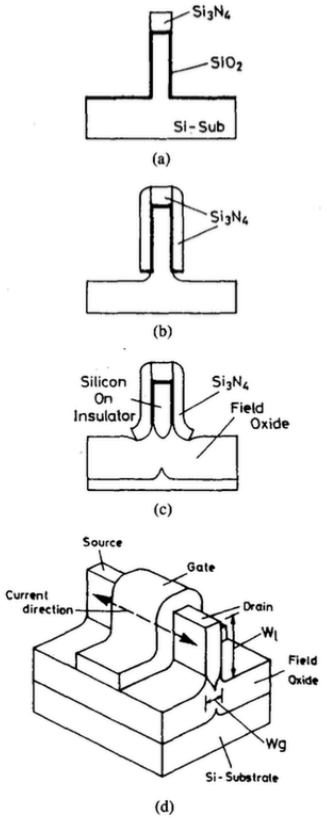


Fig. 1. (a)–(c) Process flow of selective oxidation. (d) Schematic cross section of DELTA.

Authors were with Hitachi Central Research

Ops, another one

NEW EFFECTS OF TRENCH ISOLATED TRANSISTOR USING SIDE-WALL GATES

K. Hieda, F. Horiguchi, H. Watanabe, K. Sunouchi, I. Inoue and T. Hamamoto

VLSI Research Center, Toshiba Corporation
Komukai, Saiwai-ku, Kawasaki, 210 Japan

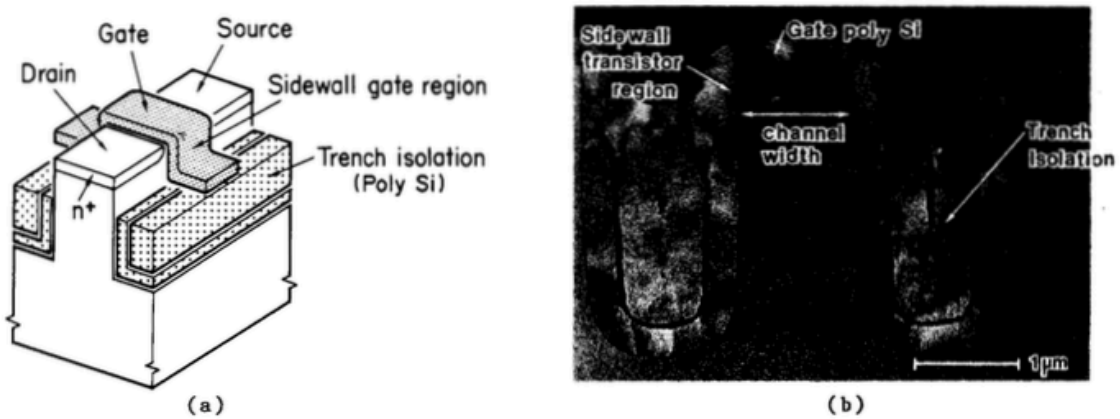


Fig. 1. (a) Schematic cross section of trench isolated transistor using side-wall gates (TIS). (b) SEM micrograph of the cross section along the direction of gate width.

32.2

IEDM 87-737

Huhu, one more

Solid-State Electronics Vol. 27, Nos. 8/9, pp. 827–828, 1984
Printed in Great Britain

0038–1101/84 $3.00 + .00
1984 Pergamon Press Ltd.

CALCULATED THRESHOLD-VOLTAGE CHARACTERISTICS OF AN XMOS TRANSISTOR HAVING AN ADDITIONAL BOTTOM GATE

(*Received* 30 *May* 1983; *in revised form* 24 *August* 1983)

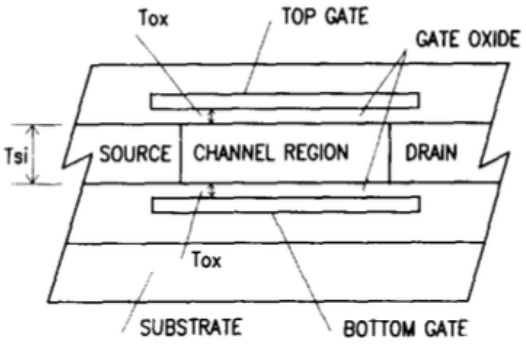


Fig. 1. Schematic cross-sectional structure of an XMOS transistor having an additional bottom gate which is symmetrically placed to a top gate with a channel region between them. "*X*" originates from Greek capital letter of xi as this structure resembles its shape.

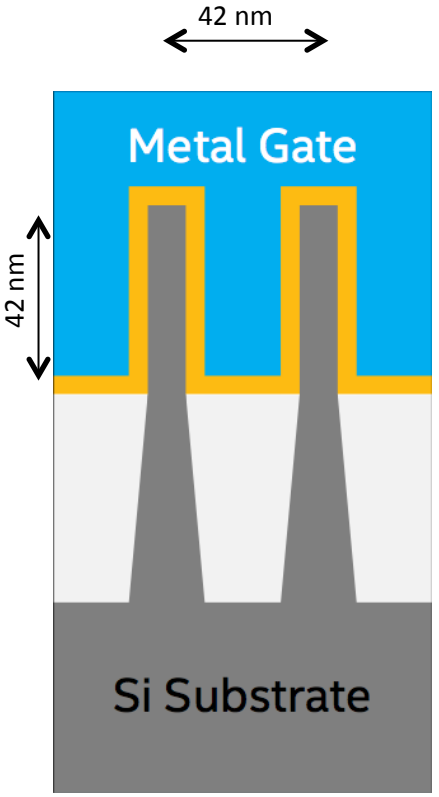
Electronic Device Division,
Electrotechnical Laboratory,
Sakura-mura,
Ibaraki, 305,
Japan

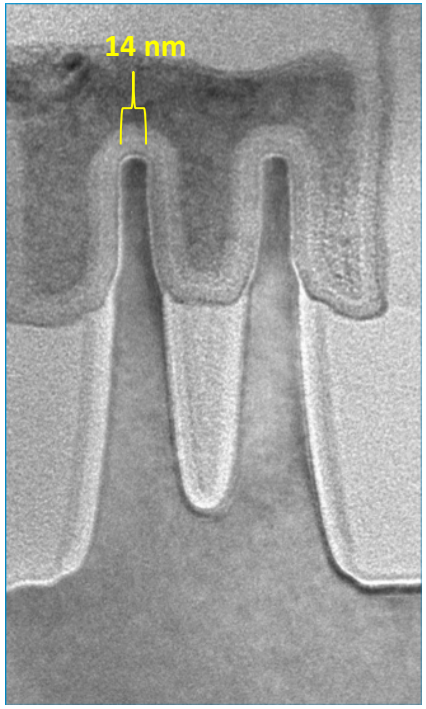
T. SEKIGAWA and
Y. HAYASHI

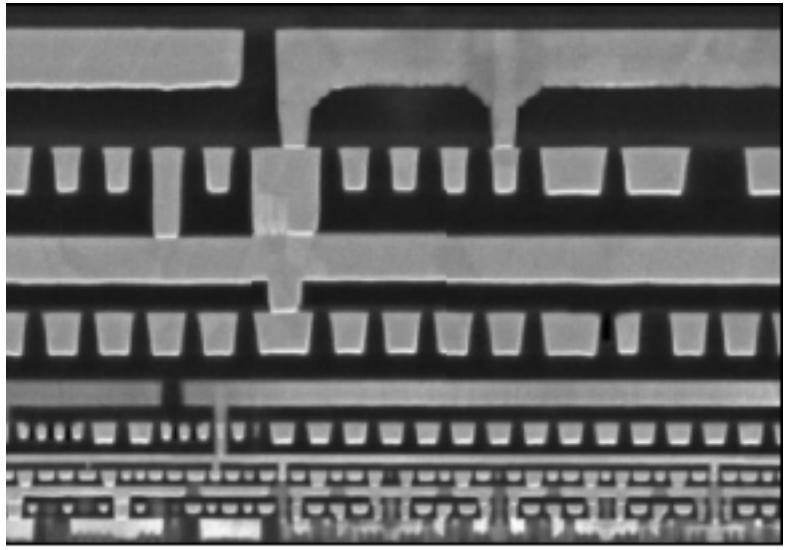
from the conclusions:

It must be said that the proposed device structure does not seem to match well the present LSI technology from a fabrication point of view. However, this problem may be solved when the silicon-on-insulator technology becomes well established. Then this device is expected to be one of the basic elements for the 3D–IC.

Intel TRI-Gate



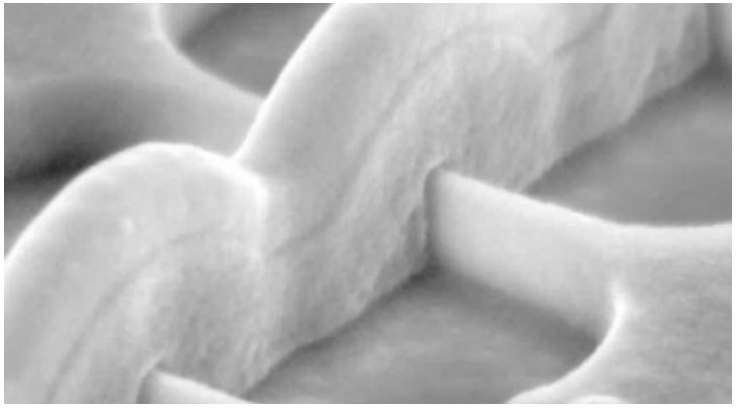




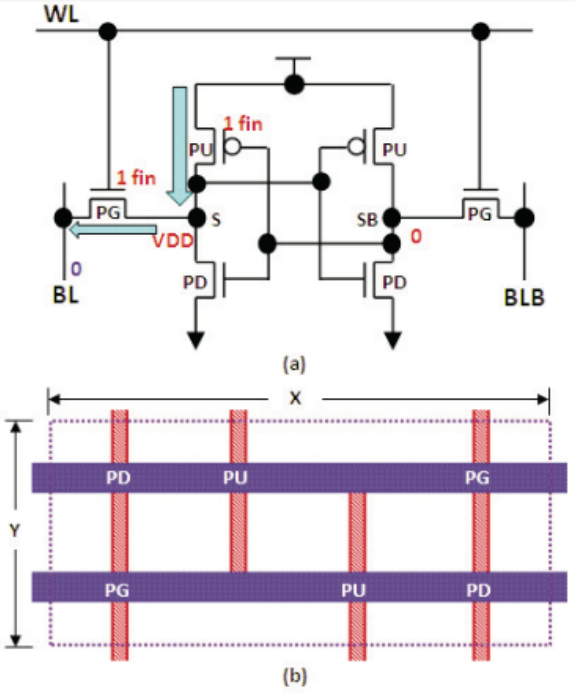
Metalization detail

Source: Intel

TSMC FinFET



16 nm FinFET from TSMC



FinFET based SRAM,
0.07 μm^2 per bit,
presented at ISSCC 2014

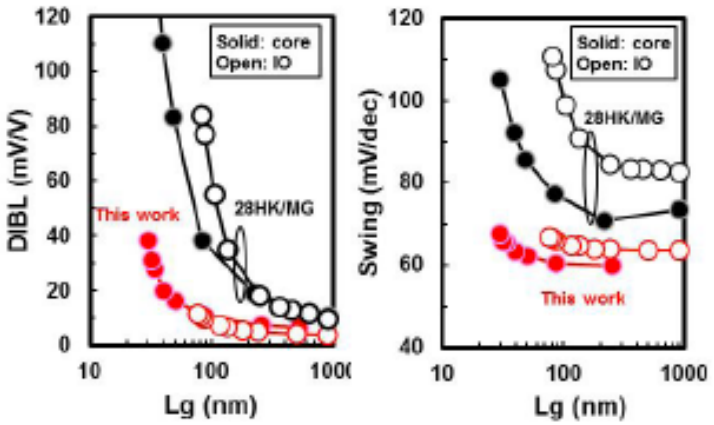
FinFET @ TSMC

An Enhanced 16nm CMOS Technology Featuring 2nd Generation FinFET Transistors and Advanced Cu/low-k Interconnect for Low Power and High Performance Applications

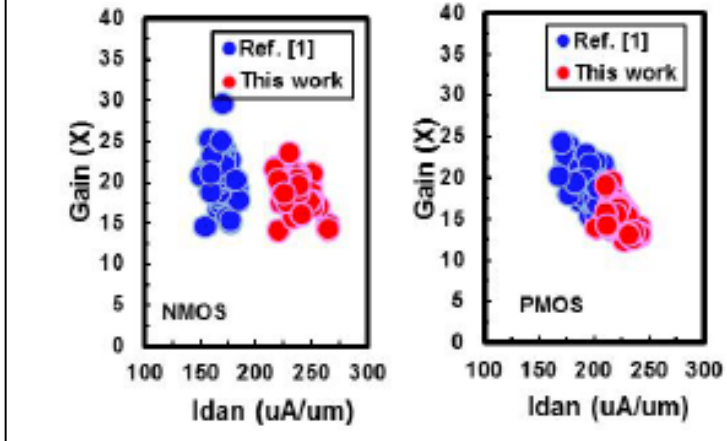
Shien-Yang Wu, C.Y. Lin, M.C. Chiang, J.J. Liaw, J.Y. Cheng, S.H. Yang, S.Z. Chang, M. Liang, T. Miyashita, C.H. Tsai, C.H. Chang, V.S. Chang, Y.K. Wu, J.H. Chen, H.F. Chen, S.Y. Chang, K.H. Pan, R.F. Tsui, C.H. Yao, K.C. Ting, T. Yamamoto, H.T. Huang, T.L. Lee, C.H. Lee, W. Chang, H.M. Lee, C.C. Chen, T. Chang, R. Chen, Y.H. Chiu, M.H. Tsai, S. M. Jang, K.S. Chen, Y. Ku

168, Park Ave. 2, Hsinchu Science Park, Hsinchu, Taiwan, R.O.C., Email: shien-yang_wu@tsmc.com

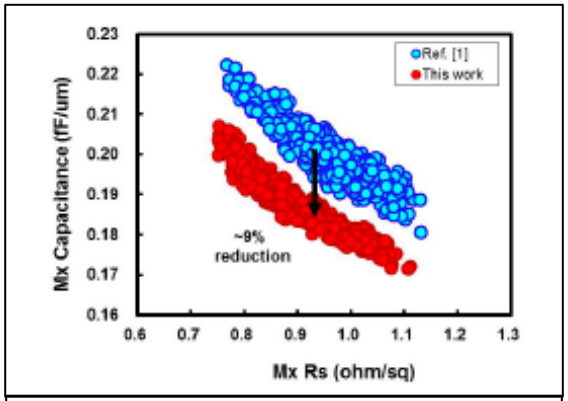
Taiwan Semiconductor Manufacturing Company



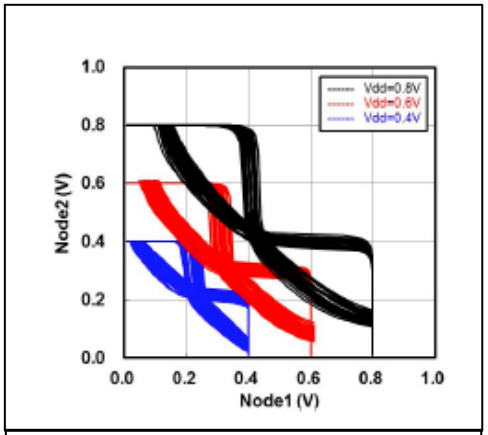
TSMC: 16nm FinFET vs. 28nm HKMG



TSMC: 16nm FinFET gain



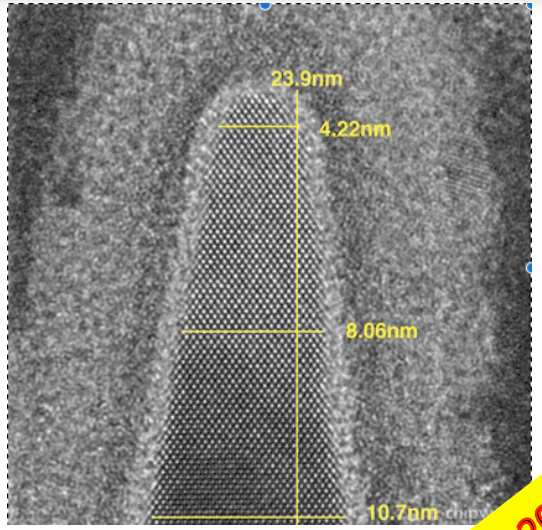
TSMC: 16nm FinFET Low Intermetal C



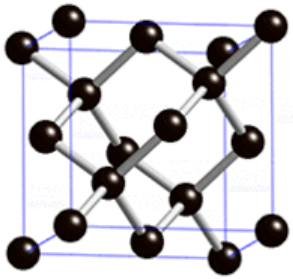
TSMC: 16nm FinFET Low Voltage SRAM

ITRS 2013

Year of Production	2013	2015	2017	2019	2021	2023	2025	2028
FinFET Fin Width (new) (nm)	7.6	7.2	6.8	6.4	6.1	5.7	5.4	5.0



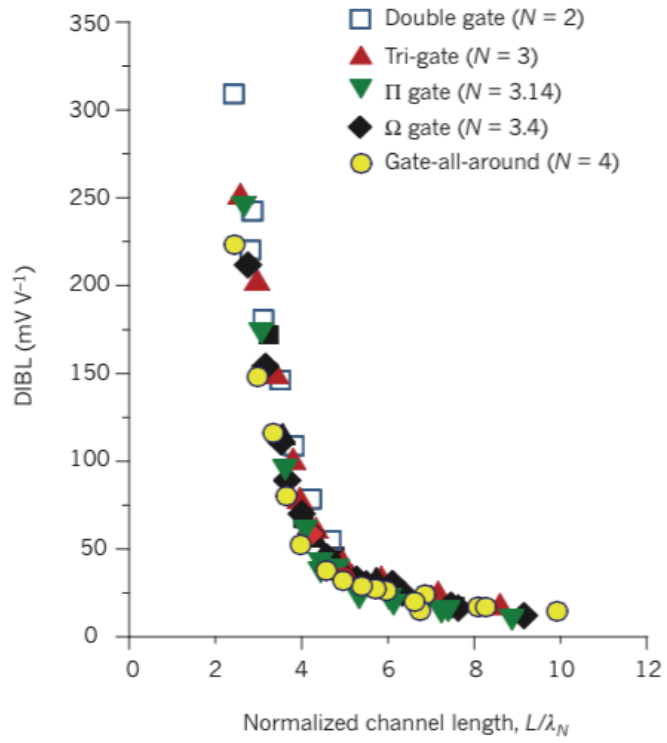
from Wikipedia



diamond cubic crystal structure, with a lattice spacing of 0.5430710 nm (

This FinFET has EXACTLY 20 atoms across at half-height

How big an advantage with multi-gate?



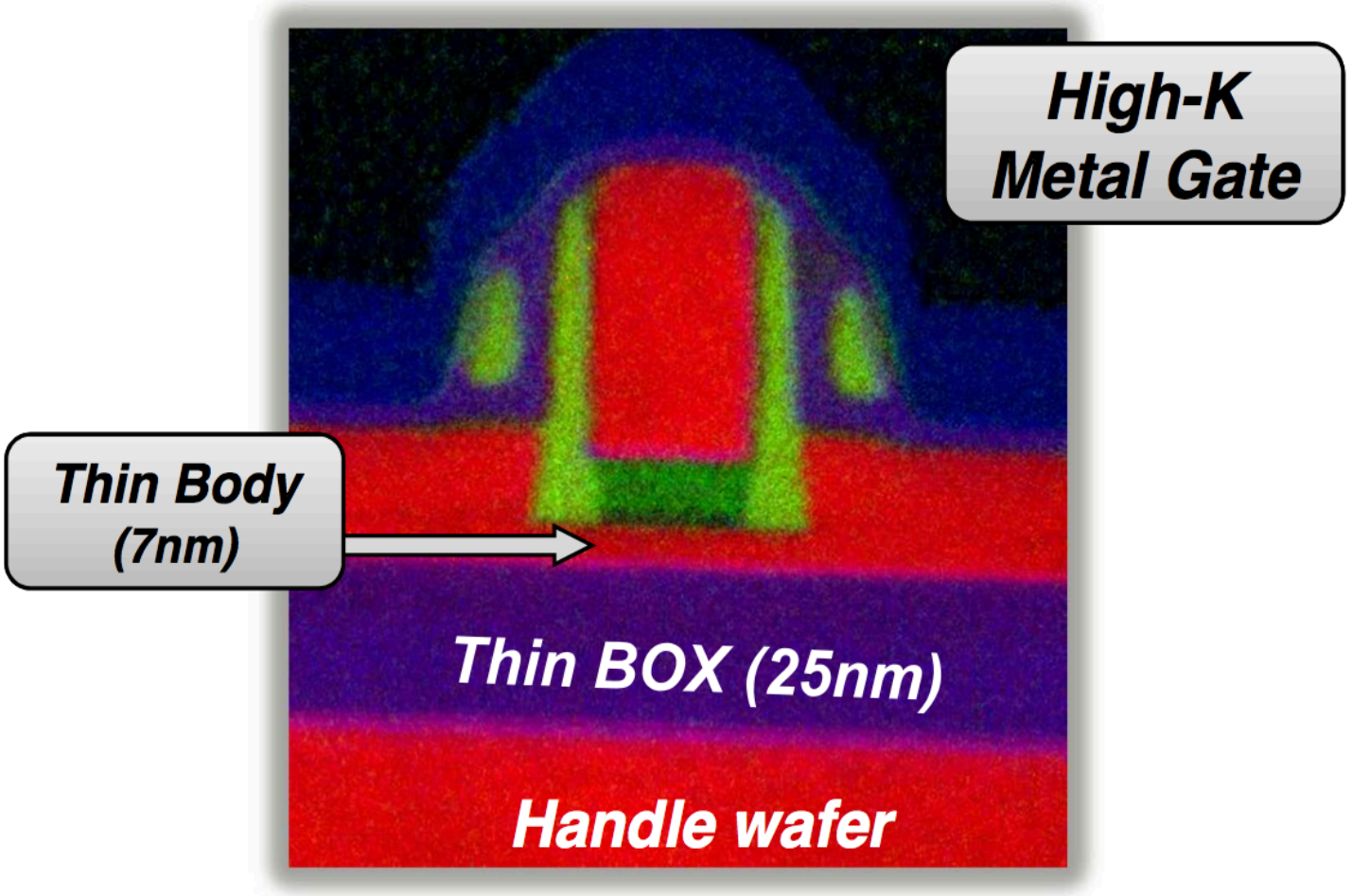
from: Ferain, **"Multigate transistors as the future of classical metal–oxide–semiconductor field-effect transistors"**, 2011

$$\lambda_n = \sqrt{\frac{1}{n}}\sqrt{\frac{\varepsilon_{Si}}{\varepsilon_{ox}} t_{Si} t_{ox}}$$

with n=1...4 the number of lateral gates in the device.

Notice that increasing the number of gates, gives only a square root advantage in λ_n.

STM FDSOI



28nm FDSOI from ST

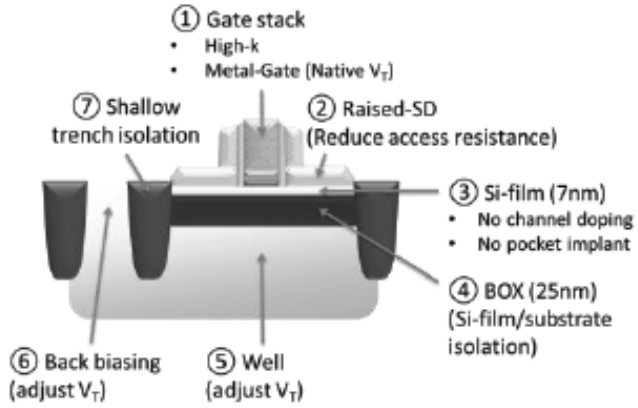


Fig.1: UTBB FD-SOI cross section view. Device V_T is set by the gate stack and adjusted by well doping type [2-3]. Wide V_T tuning is feasible by back-biasing changing the well bias.

Dynamic Single-P-Well SRAM bitcell characterization with Back-Bias Adjustment for Optimized Wide-Voltage-Range SRAM Operation in 28nm UTBB FD-SOI

O. Thomas[1,2], B. Zimmer[1], S. O. Toh[1], L. Ciampolini[3], N. Planes[3], R. Ranica[3] P. Flatresse[3] and B. Nikolić[1]

[1] Berkeley Wireless Research Center, Berkeley, CA, United States, email : olivier.thomas@cea.fr – [2] CEA-LETI Minatec Campus, 38054 Grenoble Cedex 9, France, Crolles – [3] ST Microelectronics, 38926 Crolles, France

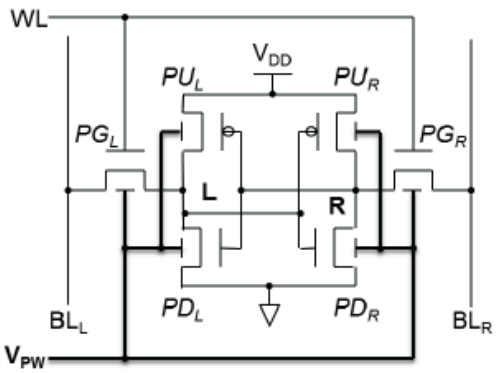


Fig.3: SPW bitcell schematic. Back gate of NMOS (PG, PD) and PMOS (PU) devices are electrically connected by the common P-well.

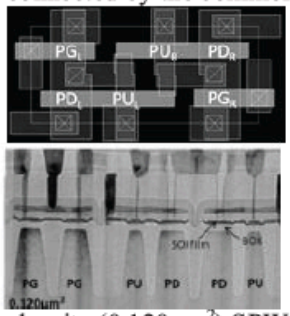


Fig.6: High density (0.120µm^2) SPW bitcell layout and TEM cross section [8]. 28nm High-k metal-gate technology implementing 7nm Si-film relying on 25nm BOX thickness [9].

FDSOI++ from ST

Dynamic Single-P-Well SRAM bitcell characterization with Back-Bias Adjustment for Optimized Wide-Voltage-Range SRAM Operation in 28nm UTBB FD-SOI

O. Thomas[1,2], B. Zimmer[1], S. O. Toh[1], L. Ciampolini[3], N. Planes[3], R. Ranica[3] P. Flatresse[3] and B. Nikolić[1]

[1] Berkeley Wireless Research Center, Berkeley, CA, United States, email : olivier.thomas@cea.fr – [2] CEA-LETI Minatec Campus, 38054 Grenoble Cedex 9, France, Crolles – [3] ST Microelectronics, 38926 Crolles, France

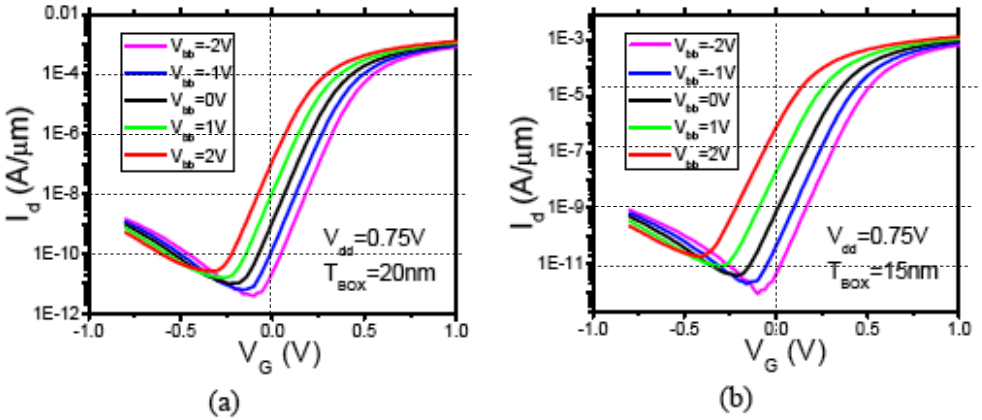


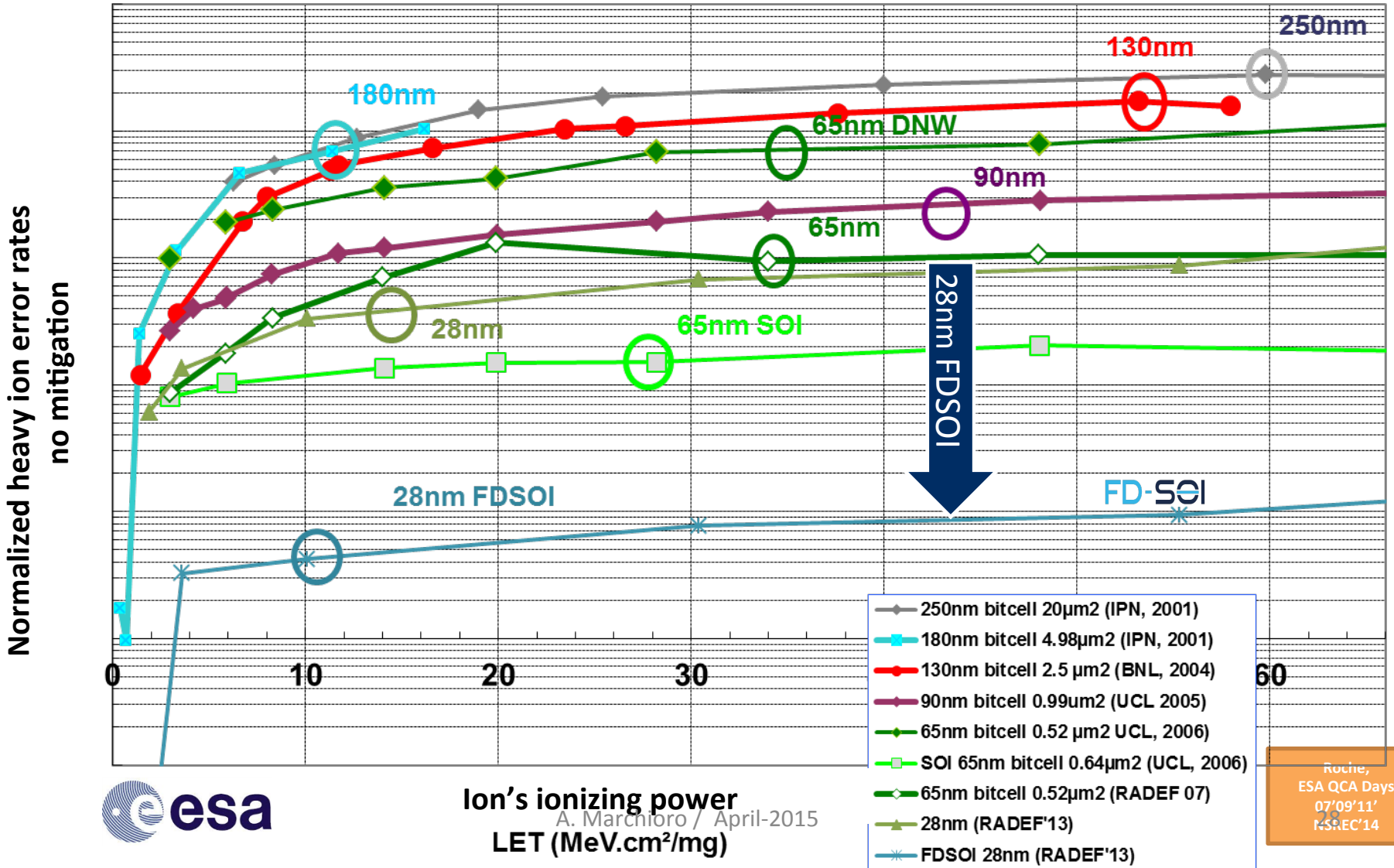
Fig. 17 I_d/V_G curves of NFET on (a)20nm BOX and (b)15nm BOX substrate with back bias from -2V to 2V, showing the larger body factor with thinner BOX.

Table 1 shows a benchmark of device characteristics of this work and other previously reported state-of-the-art Bulk FinFET and FDSOI devices. Competitive electrostatic performance and drive current are achieved at a much smaller L_G, illustrating the capability to extend FDSOI devices to 10nm for both high performance and low power applications.

…but they did not really say how to do it

Soft Error Rate in SRAMs on 28nm FDSOI

- **Lowest (best) error rates against space ions in 28nm UTBB FDSOI**
  - 3 and 2 decades lower respectively than CMOS 65nmn and 28nm (no SEGR/SEL)



Courtesy of P. Roche, STMicroelectronics

Roche, ESA QCA Days 07'09'11' NSREC'14

STEEP SWING DEVICES
(I.E. LOW SUBTHRESHOLD SLOPE)

If oxides leak, eliminate them!

NEM Relay Design for Compact, Ultra-Low-Power Digital Logic Circuits

Tsu-Jae King Liu[1*], Nuo Xu, I-Ru Chen[1], Chuang Qian[1] and Jun Fujiki[2]

[1]Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, CA 94720 USA
[2]Toshiba Corporation, Tokyo 105-8001, Japan
[*]Phone: +1-510-642-0253, Fax: +1-510-643-7846, E-mail: tking@eecs.berkeley.edu

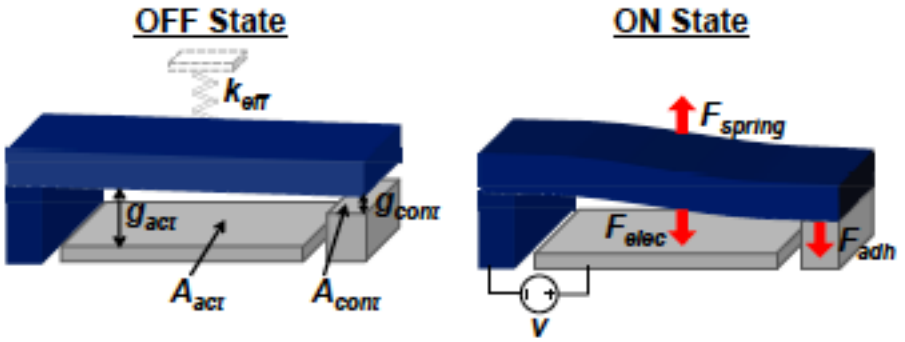


Fig. 1: Schematic isometric views illustrating the operation of a normally-OFF electrostatically actuated mechanical switch. $F_{elec} > F_{spring} > F_{adh}$.

Gate footprint: 0.1 um2

Design rules: 20 nm

Air gap: 1 nm

Operating voltage: 1V

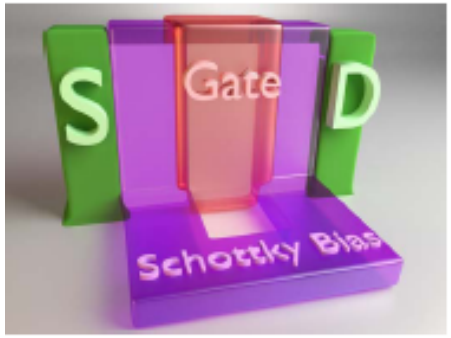
Energy/op: ?

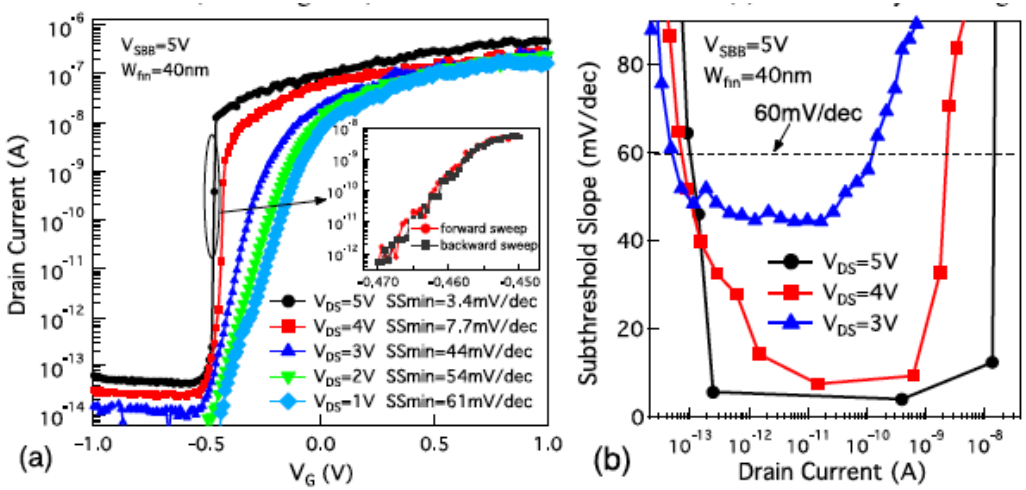
Steep Swing Device example

A Schottky-Barrier Silicon FinFET with 6.0 mV/dec Subthreshold Slope over 5 Decades of Current

Jian Zhang, Michele De Marchi, Pierre-Emmanuel Gaillardon, Giovanni De Micheli

Integrated Systems Laboratory, EPFL, Lausanne, Switzerland
Tel: +41 21 6938164, E-mail: jian.zhang@epfl.ch





(Notice that unfortunately the SS is steep only for high V_{DS}!)

Imagers @ IEDM

- 10.1 Jot Devices and the Quanta Image Sensor (Invited), Jiaju Ma, Donald Hondongwa and Eric R. Fossum
- 10.2 SPAD Based Image Sensors (Invited), Edoardo Charbon
- 10.3 Toward 1Gfps: Evolution of Ultra-High-Speed Image Sensors: ISIS, BSI, Multi-Collection Gates, and 3D-Stacking (Invited), T. G. Etoh, V. T. S. Dao, K. Shimonomura, E. Charbon, C. Zhang, Y. Kamakura and T. Matsuoka
- 10.4 Imaging with Organic and Hybrid Photodetectors (Invited), Sandro F. Tedde, Patric Büchele, Rene Fischer, Frank Steinbacher and Oliver Schmidt
- 10.5 A CMOS-Compatible, Integrated Approach to Hyperand Multispectral Imaging (Invited), Andy Lambrechts, Pilar Gonzalez, Bert Geelen, Philippe Soussan, Klaas Tack and Murali Jayapala
- 10.6 Image Sensors for High-Throughput, Massively- Parallel DNA Sequencing: Requirements and Roadmap (Invited), Annette Grot
- 10.7 High Performance Silicon Imaging Arrays for Cosmology, Planetary Sciences, & Other Applications (Invited), Shouleh Nikzad, Michael E. Hoenk, John Hennessy, April D. Jewell, Alexander G. Carver, Todd J. Jones, Samuel L. Cheng, Timothy Goodsall and Charles Shapiro
- 10.8 Detecting Elementary Particles Using Hybrid Pixel Detectors at the LHC and Beyond (Invited), Michael Campbell

My “strange” pick

Jot Devices and the Quanta Image Sensor

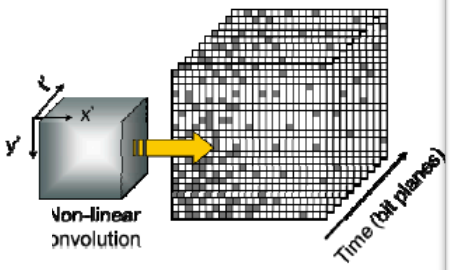
Jiaju Ma, Donald Hondongwa and Eric R. Fossum

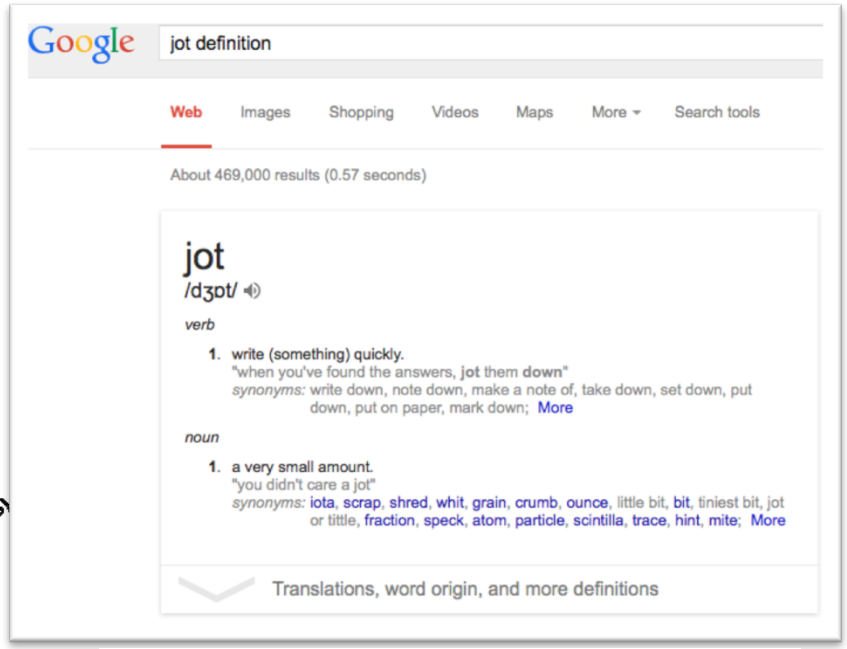
Thayer School of Engineering at Dartmouth
14 Engineering Drive, Hanover, NH 03755 USA

Abstract

The Quanta Image Sensor (QIS) concept and recent work on its associated jot device are discussed. A bipolar jot and a pump-gate jot are described. Both have been modelled in TCAD. As simulated, the pump-gate jot has a full well of 200e- and conversion gain of 480uV/e-.

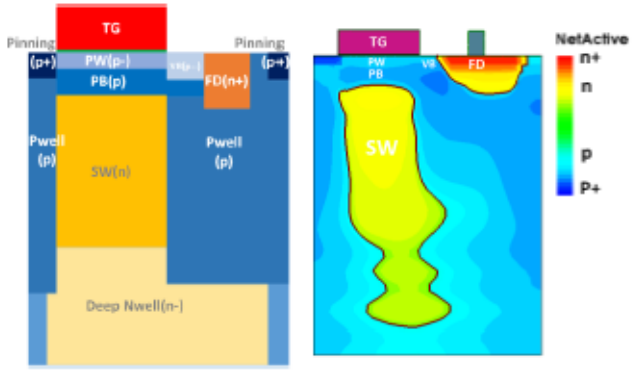
Introduction:





Essentially a single photon discrete counter collecting signal by:

- sampling at very high rate
- counting single photons
- converting 1 e^- -> 1 bit
- adding up in the digital domain



(a) (b)

Figure 4. Schematic of (a) pump gate jot doping and (b) TCAD simulation.

CIRCUITS AT ISSCC2015

ISSCC 2015 Conference's Theme

- The buzzword: IoT (i.e. Internet of Things)
- Comment: Nobody knows what it is precisely, but everybody is convinced that *the IoT* is the next killer-application that will allow the microelectronics industry to move beyond the 10 nm barrier.
- It is a mixture of:
  - Sensors
  - Extremely low power processing
  - Wireless connectivity
  - Power scavenging

Scaling down to sub 5 nm

Fundamentally, transistors as small as 1.5㎚ are possible

Thermodynamic Limit

- SNL expression :
  at least 0.017eV to process a bit

$$E_{bit} = kT \ln 2$$

- Heisenberg's uncertainty principle:
  min. feature ~1.5㎚ (@300K)

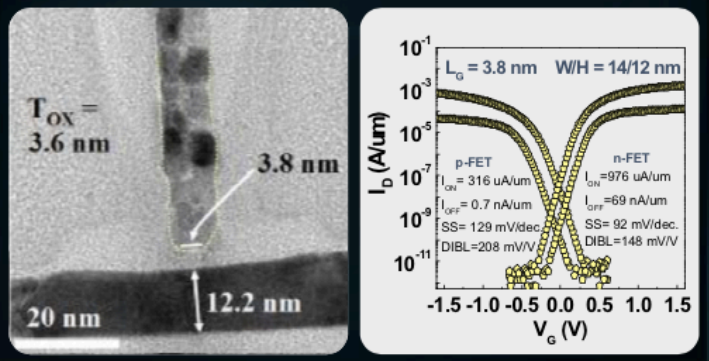
$$d_{min} \approx \frac{\hbar}{\sqrt{2mE_b}}$$

Device Limit

- Possible to have working CMOS transistor down to 3~5㎚

3.8㎚ CMOS FinFET

※ SAMSUNG, VLSI 2009

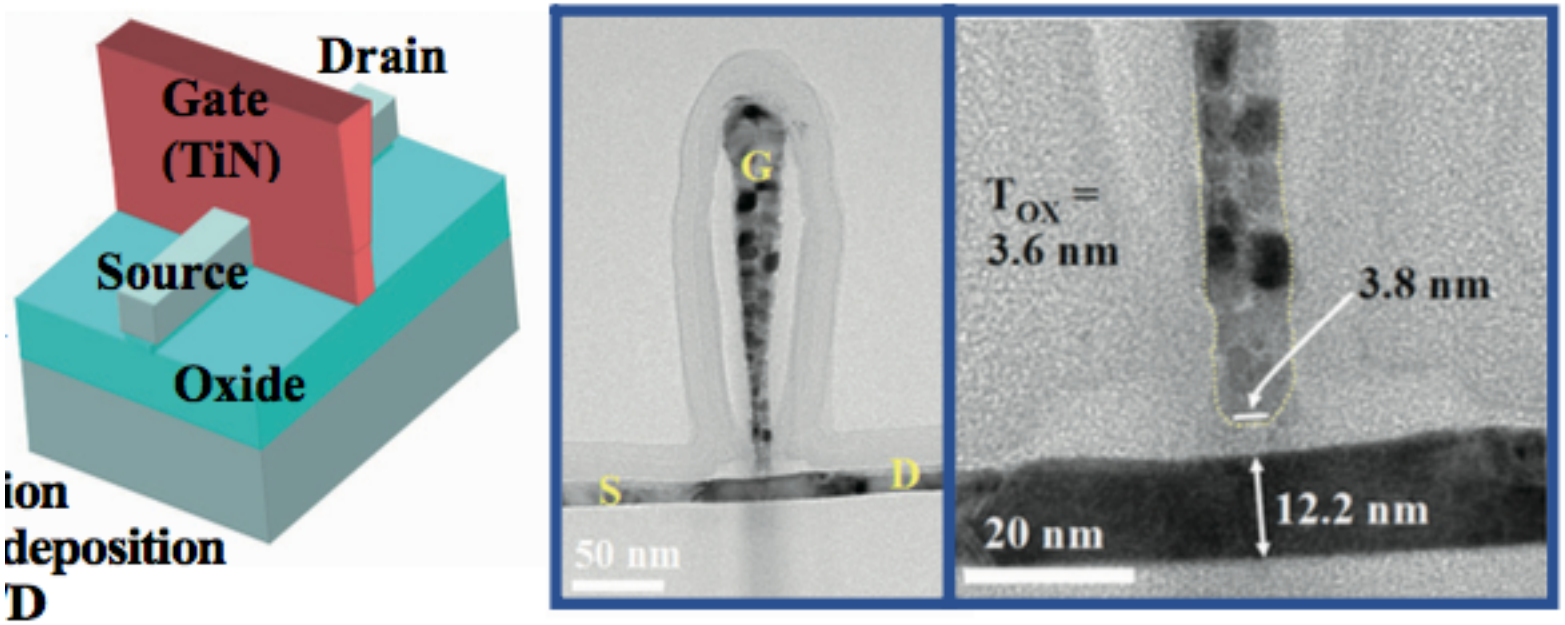


Kinam Kim, PhD
IEEE Fellow, US NAE Foreign Member
President, Samsung Electronics
1.1: Silicon Technologies and Solutions for The Data-Driven World

… details

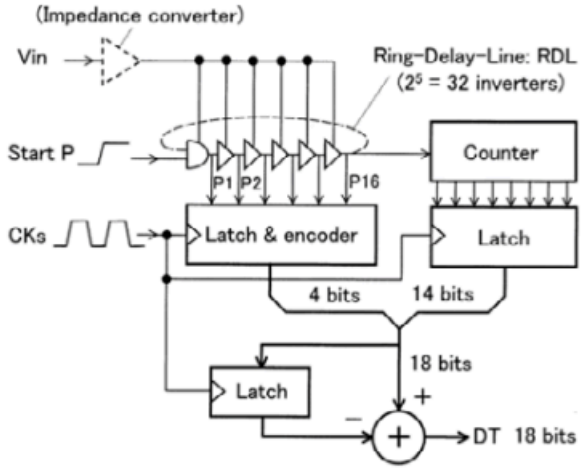
Characteristics of sub 5nm Tri-Gate Nanowire MOSFETs with Single and Poly Si Channels in SOI Structure

Sung Dae Suk, Ming Li, Yun Young Yeoh, Kyoung Hwan Yeo, Jae Kyu Ha*, Hyunseok Lim*, HyunWoo Park**, Dong-Won Kim, TaeYoung Chung, Kyung Seok Oh and Won-Seong Lee
Advanced Technology Development Team 1, PD Team*, MTT2 Team**, Semiconductor R&D Center, Samsung Electronics Co., San 24, Nongseo-Dong, Kiheung-Ku, Yongin-City, Kyoungi-Do, 449-711, KOREA
Phone: +82-31-209-6668, Fax:+82-31-209-3274 E-mail: sd1.suk@samsung.com



Samsung @ VLSI Technology Symposium 2009

Going towards 5nm in analog



100 kHz
11 bits
1mW (2 V)
3 pJ/conv.
0.8 μm CMOS

From Prof. W. Sansen's invited plenary talk

… Déjà vu ?

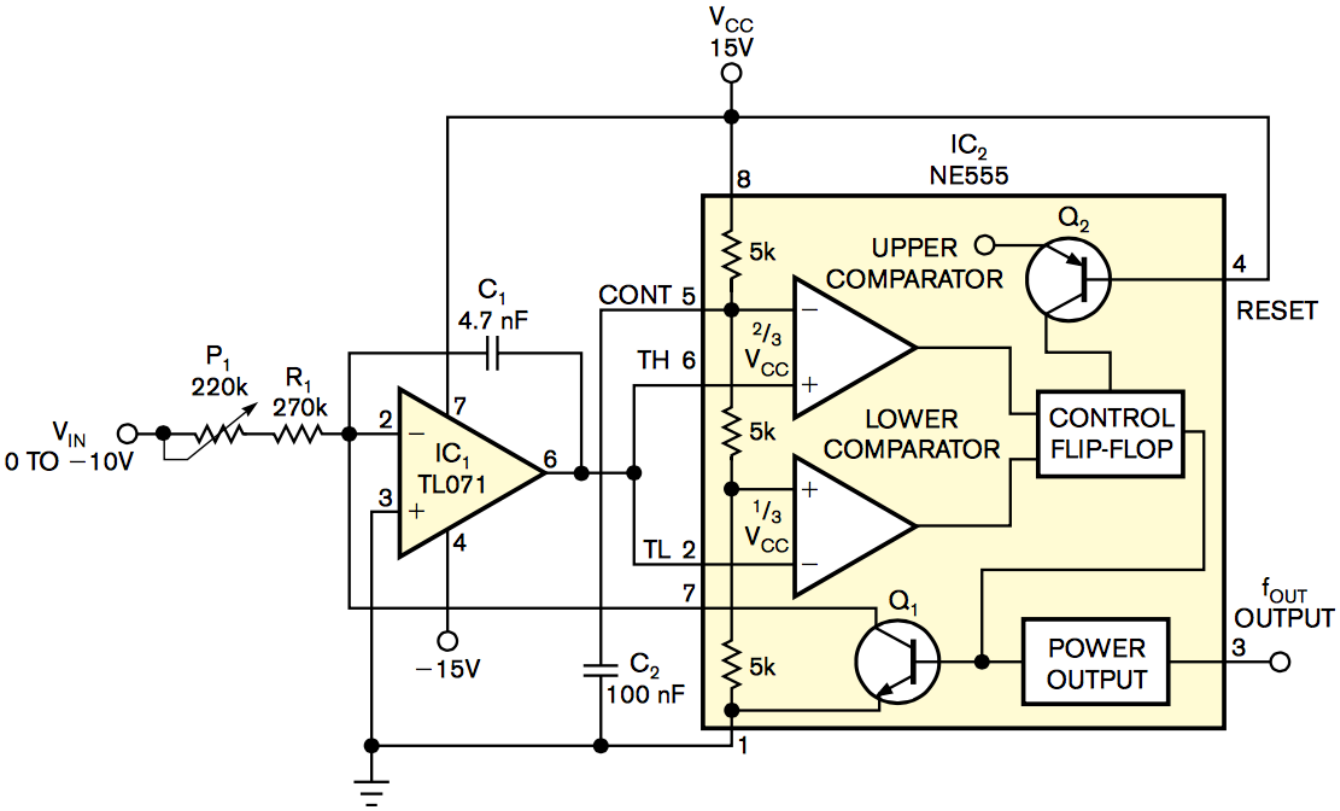


Figure 1 Preceding an NE555 timer with a Miller integrator yields a voltage-to-frequency converter that costs less than 50 cents.

Trends: High Speed Wireline Links

- **3.1 A 28Gb/s Multi-Standard Serial-Link Transceiver for Backplane Applications in 28nm CMOS** (*B. Zhang,* Broadcom, Irvine, CA)
  - 28Gb/s multi-standard transceiver with data rates up to 28Gb/s in 28nm CMOS. The receiver has a linear equalizer and a 14-tap DFE, while the transmitter uses a source-series terminated driver with a 5-tap FFE. The transceiver compensates a 40dB loss backplane channel at 25.78Gb/s; each 0.62mm2 TX/RX consumes 295mW.
- **3.2 Multi-Standard 185fsrms 0.3-to-28Gb/s 40dB Backplane Signal Conditioner with Adaptive Pattern-Match 36-Tap DFE and Data-Rate-Adjustment PLL in 28nm CMOS (***T. Kawamoto,* Hitachi, Tokyo, Japan)
  - A multi-standard backplane transceiver that uses a 36-tap DFE with a pattern-capture CDR and a pattern-matching adaptive equalizer to cancel reflections due to backplane connectors. The 28nm CMOS chip operates from 0.3 to 28.05Gb/s over a 40dB loss backplane with 2 connectors.
- **3.3 A 0.5-to-32.75Gb/s Flexible-Reach Wireline Transceiver in 20nm CMOS** (*P. Upadhyaya,* Xilinx, San Jose, CA)
  - A fully-adaptive 0.5-to-32.75Gb/s transceiver embedded in a 20nm CMOS FPGA. The receiver uses a 15-tap DFE while the clocking circuits consist of fractional-N LC PLLs and poly-phase IQ generation circuits. The transceiver achieves BER <10-15 over a 10.4dB loss short-reach channel at 32.75Gb/s and a 27dB loss backplane at 28Gb/s.
- **3.4 A 36Gb/s PAM4 Transmitter Using an 8b 18GS/s DAC in 28nm CMOS** (*A. Nazemi,* Broadcom, Irvine, CA)
  - A 36Gb/s PAM4 transmitter with a clock-generation circuit. The transmitter is based on an 18GS/s 8b DAC achieving 800mVppdiff. Implemented in 28nm CMOS technology, the measured SFDR is 52 and 43dB at 0.7 and 8GHz outputs, respectively. The DAC-based transmitter consumes 84mW from 1 and 1.5V power supplies.
- **3.5 A 16-to-40Gb/s Quarter-Rate NRZ/PAM4 Dual-Mode Transmitter in 14nm CMOS** (*J. Kim,* Intel, Hillsboro, OR)
  - A 0.0279mm2 NRZ/PAM4 transmitter (TX) operating from 16 to 40 Gb/s in 14nm tri-gate CMOS. The TX includes a feed-forward charge-injected 4:1 serializer and quarter-rate clocking and clock calibration. The TX consumes 195 and 518mW at 28 and 40Gb/s, respectively, in NRZ mode and consumes 141 and 168mW at 33.6 and 40Gb/s in PAM4 mode.
- **3.6 A 10Gb/s Hybrid ADC-Based Receiver with Embedded 3-Tap Analog FFE and Dynamically-Enabled Digital Equalization in 65nm CMOS (***A. Shafik,* Texas A&M University, College Station, TX)
  - A 65nm 10Gb/s hybrid ADC-based receiver employing a 3-tap analog FFE embedded inside a 6b asynchronous SAR ADC, as well as a per-symbol dynamically-enabled digital equalizer. Applying the latter technique to the digital 4-tap FFE and 3-tap DFE results in ~30mW savings on a 36.4dB loss channel.
- **3.7 A 7Gb/s Rapid On/Off Embedded-Clock Serial-Link Transceiver with 20ns Power-On Time, 740µW Off-State Power for Energy-Proportional Links in 65nm CMOS (***T. Anand,* University of Illinois, Urbana, IL)
  - A 7Gb/s embedded clock burst-mode transceiver to achieve energy proportional operation. Using a fast-locking LC PLL the design achieves effective throughput scaling over a 100× range (7Gb/s to 70Mb/s) while scaling the power by 44× (63.7mW to 1.43mW).
- **3.8 A 0.45-to-0.7V 1-to-6Gb/s 0.29-to-0.58pJ/b Source-Synchronous Transceiver Using Automatic Phase Calibration in 65nm CMOS (***W-S. Choi,* University of Illinois, Urbana, IL)
  - A source-synchronous transceiver with aggressive supply voltage scaling to achieve energy efficiency ranging from 0.29 to 0.58pJ/b at data rates of 1 to 6Gb/s, as the supply voltage varies from 0.45 to 0.7V. Phase-spacing errors resulting from device mismatches are corrected using self- calibration.

Summary for Wireline Links

Session 3							
Paper	Speed [GB/s]	Tech [nm]	Design	Mode	Power [mW]	Power/bit [pJ]	Converter Power [pJ/bit]
3-1	28	28	Broadcom	TXRX	295	10.5	
3-2	28	28	Hitachi	TXRX	702.8	25.1	
3-3	32.75	20	Xilinx	TXRX	785	24.0	
3-4	36	28	Broadcom	TX (DAC)			0.017
3-5	40	14	Intel	TX	518	13.0	
3-6	10	65	Texas A&M	RX (ADC)			8.9
3-7	7	65	Univ Illinois	TXRX	63	9.0	
3-8	6	65	Univ Illinois	TXRX		0.47	

Trends: Imagers

- **6.1 A 1/1.7-inch 20Mpixel Back-Illuminated Stacked CMOS Image Sensor for New Imaging Applications (***A. Suzuki,* Sony, Atsugi, Japan)
  - A 1/1.7-inch 20Mpixel back-illuminated stacked CMOS image sensor. The sensor achieves 1.3e-rms random noise with multiple sampling at 20Mpixel 30fps in addition to 16Mpixel 120fps readout with visually lossless data compression and two simultaneous output streams.
- **6.2 133Mpixel 60fps CMOS Image Sensor with 32-Column Shared High-Speed Column-Parallel SAR ADCs (***R. Funatsu,* NHK Science & Technology Research Laboratories, Tokyo, Japan)
  - A 133Mpixel 60fps 12b image sensor for 8K video. The pixel size in 0.18µm technology is 2.45×2.45µm2. Front-end multiplexing analog readout circuitry and column-parallel successive approximation register ADCs are used.
- **6.3 A 45.5µW 15fps Always-On CMOS Image Sensor for Mobile and Wearable Devices** (*J. Choi,* Samsung Advanced Institute of Technology, Suwon, Korea)
  - An always-on image sensor that enables smart sensing in addition to a photograph- shooting mode. Switchable always-on and photo-shooting modes are implemented using dynamic voltage-scaling and reconfigurable ADC circuits. The sensor has 640×480 pixels and consumes 45.5µW at 15fps in the always-on mode.
- **6.4 Single-Shot 200Mfps 5×3-Aperture Compressive CMOS Imager (***F. Mochizuki,* Shizuoka University, Hamamatsu, Japan)
  - A CMOS image sensor fabricated in a 0.11µm process with 5×3 apertures. The sensor performs single-shot and burst-readout image acquisition at a frame rate of 200Mfps employing image reproduction based on compressive sensing.

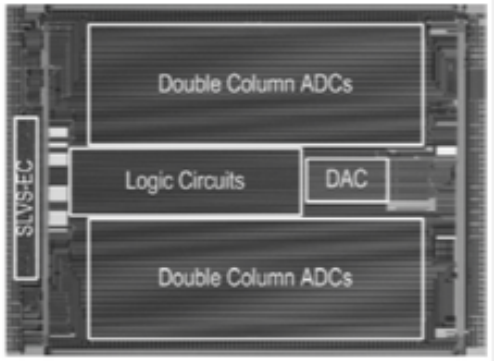
Back-Illuminated, Stacked Sony Imager

6.1 A 1/1.7-inch 20Mpixel Back-Illuminated Stacked CMOS Image Sensor for New Imaging Applications

Atsushi Suzuki[1], Nobutaka Shimamura[1], Toshiki Kainuma[1], Naoki Kawazu[1], Chihiro Okada[1], Takumi Oka[1], Kensuke Koiso[2], Atsushi Masagaki[1], Yoichi Yagasaki[3], Shigeru Gonoi[4], Tatsuya Ichikawa[1], Masatoshi Mizuno[5], Tatsuya Sugioka[1], Takafumi Morikawa[1], Yoshiaki Inada[1], Hayato Wakabayashi[1]

Fabrication Process		90nm 1P4M MOS / 65nm 1P7M Logic
Supply Voltage		2.9V / 1.8V / 1.1V
Image size		Diagonal 9.325mm (Type 1/1.7)
Number of effective pixels		5256 (H) x 3934 (V) 20.68Mpixels
Pixel size		1.43μm (H) x 1.43μm (V)
Frame rate	Still (4:3)	30fps at 20Mpix 12b with multiple sampling 60fps at 20Mpix 10b 90fps at 20MPix 10b with data compression
	Movie (16:9)	120fps at 16Mpix 10b with data compression 240fps at 4Mpix 10b 960fps at 0.7Mpix 10b
	Movie & Still (16:9)	60fps at 4Mpix 12b and 16Mpix 10b
Power consumption		532mW at 20Mpix 12b 30fps with multiple sampling 428mW at 20Mpix 10b 60fps
Saturation signal		9700e⁻ at 60°C
Sensitivity (typical value F5.6)		7922e⁻/lx-s (Green pixel, 3200K light source with IR cut filter of 650nm cut-off)
Conversion gain		76.6μV/e⁻
RMS random noise		1.3e⁻ (AnalogGain:27dB)
Dynamic range		72dB at 12b

A micrograph of the chip



A micrograph of bottom part

Chips in two different technologies
Wafer-to-wafer bonding

News & Analysis

Sony to Ramp CMOS Image Sensor Production

Peter Clarke

2/3/2015 08:49 PM EST

Post a comment

NO RATINGS
LOGIN TO RATE

LONDON — Sony Corp., the world's leading supplier of CMOS image sensors, has said it will invest 105 billion yen (about US$895 million) in the next financial year to increase its production capacity for stacked CMOS image sensors.

Sony said it would take production across three production sites current level of approximately 60,000 wafers per month to approximately 80,000 wafers per month by the end of June 2016. Previously Sony had a mid-term target of 75,000 wafers per month but demand for sensors in smartphones has prompted Sony to accelerate its investment, the company said.

The investment will take place at Sony Semiconductor's Nagasaki Technology Center ("Nagasaki TEC"), Yamagata Technology Center ("Yamagata TEC"), and Kumamoto Technology Center ("Kumamoto TEC"). The investment of approximately 105 billion yen comprises approximately 78 billion yen for Nagasaki TEC, approximately 10 billion yen at Yamagata TEC and approximately 17 billion yen in Kumamoto TEC.

Sony's Kumamoto Technology Center. (Source: Sony)

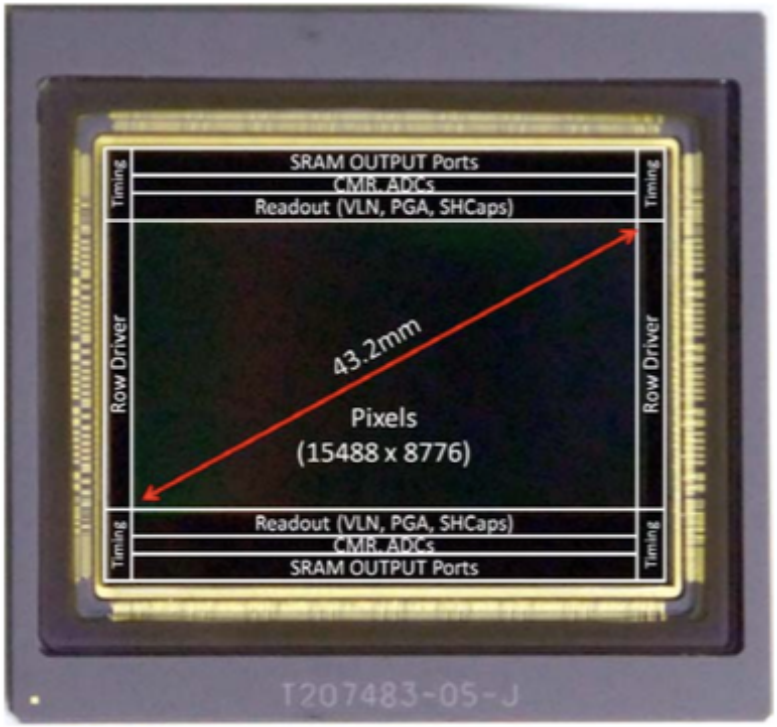
Sony's Nagasaki Technology Center. (Source: Sony)

Data Monster:
133Mp x 60fps x 14 bit/p = 120 Gbps

6.2 133Mpixel 60fps CMOS Image Sensor with 32-Column Shared High-Speed Column-Parallel SAR ADCs

Ryohei Funatsu[1], Steven Huang[2], Takayuki Yamashita[1], Kevin Stevulak[2], Jeff Rysinski[2], David Estrada[2], Shi Yan[2], Takuji Soeno[1], Tomohiro Nakamura[1], Tetsuya Hayashida[1], Hiroshi Shimamoto[1], Barmak Mansoorian[2]

[1]NHK Science & Technology Research Laboratories, Tokyo, Japan
[2]Forza Silicon, Pasadena, CA



- 484 SAR 17.95 MS/s ADC
- Total power: 11 W

- Chip is very large, cap on lines must be significant during read-out

The other side of the spectrum…

6.3 A 45.5μW 15fps Always-On CMOS Image Sensor for Mobile and Wearable Devices

Jaehyuk Choi, Jungsoon Shin, Dongwu Kang, Du-Sik Park

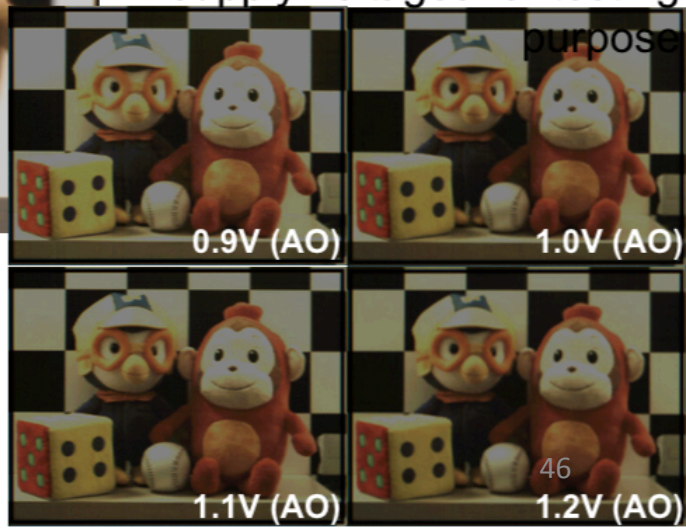
Samsung Advanced Institute of Technology, Suwon, Korea

Sample Images

PS mode
640 × 480, 15 fps
V_{DDA} = 3.3 V / V_{DD} = 1.8 V

AO mode
320 × 240, 15 fps
V_{DDA} = V_{DD} = 0.9 V

Four images with various supply voltages for testing purpose

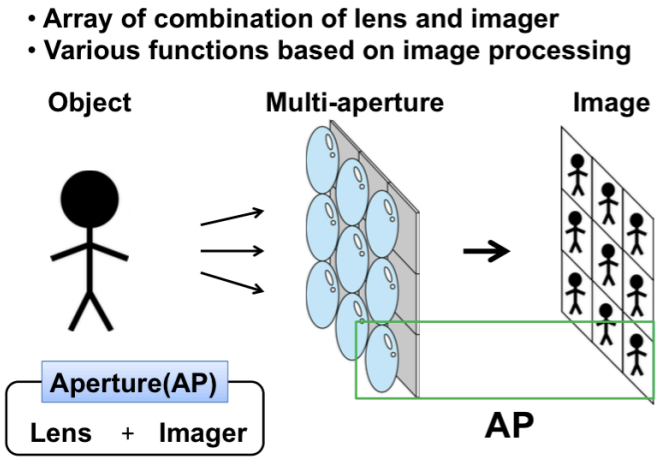


A 200 MS/s imager

6.4 Single-Shot 200Mfps 5×3-Aperture Compressive CMOS Imager

Futa Mochizuki[1], Keiichiro Kagawa[1], Shin-ichiro Okihara[2],
Min-Woong Seo[1], Bo Zhang[1], Taishi Takasawa[1],
Keita Yasutomi[1], Shoji Kawahito[1]

[1]Shizuoka University, Hamamatsu, Japan,
[2]The Graduate School for the Creation of New Photonics Industries, Hamamatsu, Japan

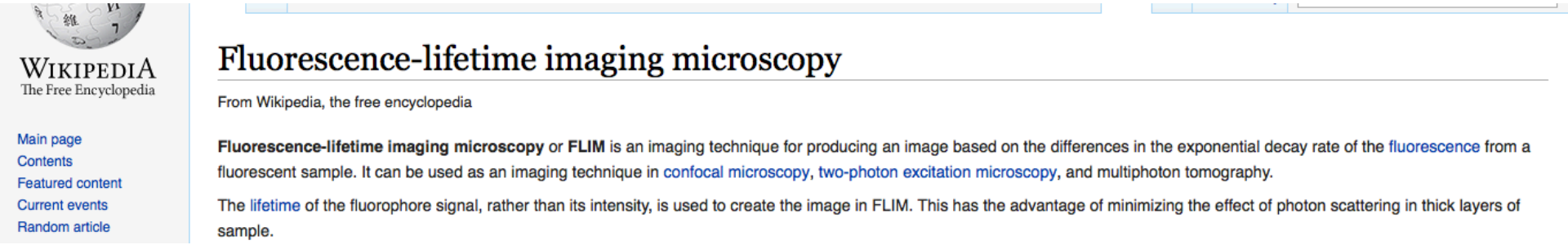


Pixel count	$64^H \times 108^V$
Pixel pitch	$11.2\mu m^H \times 5.6\mu m^V$
Aperture count	$5^H \times 3^V$
Chip size	7.0mm × 9.3mm
Technology	0.11µm CIS
Frame count	15
Frame count after reproduction	32 (comp. ratio≃47%)
Frame rate	200Mfps
Power consumption	1.62W@200Mfps

Imagers for FLIM

FLIM: Fluorescence Lifetime Imaging Microscopy

– A technique used to obtain images in the time-dimension (not intensity or color dimension!)



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Fluorescence-lifetime imaging microscopy

From Wikipedia, the free encyclopedia

Fluorescence-lifetime imaging microscopy or **FLIM** is an imaging technique for producing an image based on the differences in the exponential decay rate of the fluorescence from a fluorescent sample. It can be used as an imaging technique in confocal microscopy, two-photon excitation microscopy, and multiphoton tomography.

The lifetime of the fluorophore signal, rather than its intensity, is used to create the image in FLIM. This has the advantage of minimizing the effect of photon scattering in thick layers of sample.

Sub-ns Imager

ISSCC 2015 / SESSION 11 / SENSORS AND IMAGERS

11.3 A 160×120-Pixel Analog-Counting Single-Photon Imager With Sub-ns Time-Gating and Self-Referenced Column-Parallel A/D Conversion for Fluorescence Lifetime Imaging

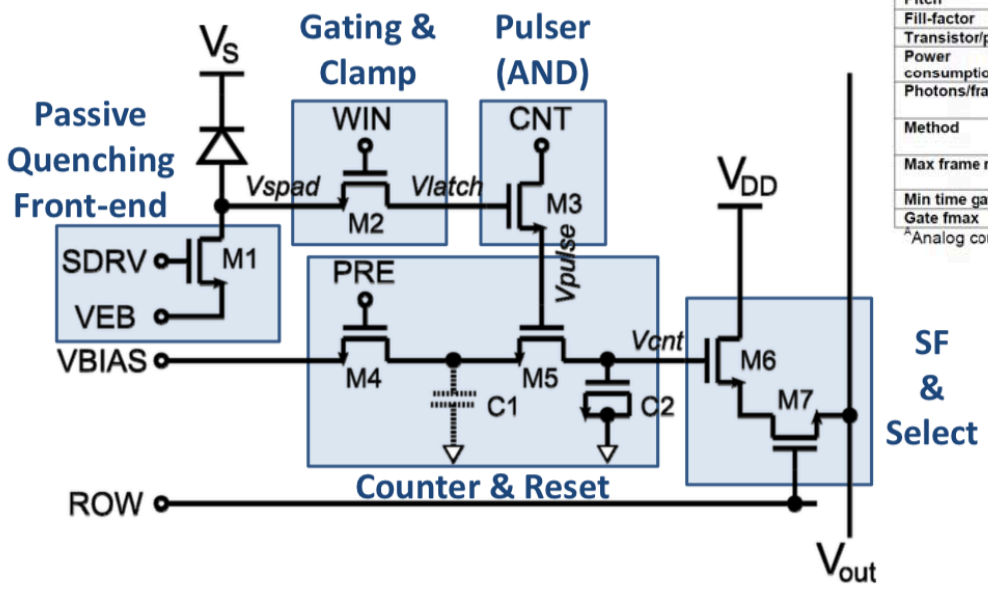
Matteo Perenzoni, Nicola Massari, Daniele Perenzoni, Leonardo Gasparini, David Stoppa

Fondazione Bruno Kessler, Povo, Italy

Chip features			Time gating		
Chip size	3.42×3.55 mm²		Time width stddev	80.2 ps	*Twin = 1.4ns*
Transistors/pixel	7 T + 1 MOSCAP		Delay resolution	194 ps	
Median DCR	580 Hz	*Vexc = 2.5 V*	Gating windows	200 cycles/frame	
Analog output			**Digital output**		
Sensitivity	16.5 mV/photon		Sensitivity	1 LSB/photon	
Pixel noise	1.3 mV		Pixel noise	0.55 LSB	
Step uniformity	2.6 mV		DNL	<1 LSB	
			INL	<1.01 LSB	
Output range	1.15 V (70 photons)		Output range	5.4 bit (41 photons)	
Output rate	5 MS/s		Output rate	50 MHz	
Power	20.6 mW	*Total*	Power	156.7 mW	*Total*
	4.5 mW	*Digital 5V*		123.2 mW	*Digital 5V*
	0.6 mW	*Digital 3.3V*		18.0mW	*Digital 3.3V*
	15.5 mW	*Analog 3.3V*		15.5 mW	*Analog 3.3V*

Reference →	[1]	[2]	[3]	[4]	[5]	[6]	This Work
Technology	0.13µm CIS	0.35µm HV	0.15µm	0.13µm CIS	0.13µm	0.35µm	0.35µm HV
Array resolution	160×128	32×32	n.a.	320×240	64×64	128×128	160×120
Pitch	50µm	25µm	n.a.	8µm	48µm	25µm	15µm
Fill-factor	1%	20.8%	n.a.	26.8%	0.77%	4.5%	21%
Transistor/pixel	>50T	12T + 1C	12T + 2C	8T+1C	>30T	12T	7T + 1C
Power consumption	550 mW	33 mW	n.a.	69.5 mW[A] 69.0 mW[D]	8.79 W	363 mW	20.6 mW[A] 156.7 mW[D]
Photons/frame	128 ph	150 ph	90 ph	400 ph[A] 1 ph[D]	n.a.	1 ph	70 ph[A] 41 ph[D]
Method	Counting[D] Timestamp	Counting[A] Gating	Counting[A] Gating	Counting[A,D]	Counting[D] Timestamp	Gating	Counting[A,D] Gating
Max frame rate	500 kfps	180 fps	n.a.	7 fps[A] 5.1 kfps[D]	466 fps	2441 fps	231 fps[A] 486 fps[D]
Min time gating	n.a.	1.1 ns	0.53 ns	n.a.	n.a.	n.d.	0.75 ns
Gate fmax	1 MHz	40 MHz	50 MHz	n.a.	20 MHz	40 MHz	50MHz

[A]Analog counting mode, [D]Digital counting mode



SPAD + Histo + TDC

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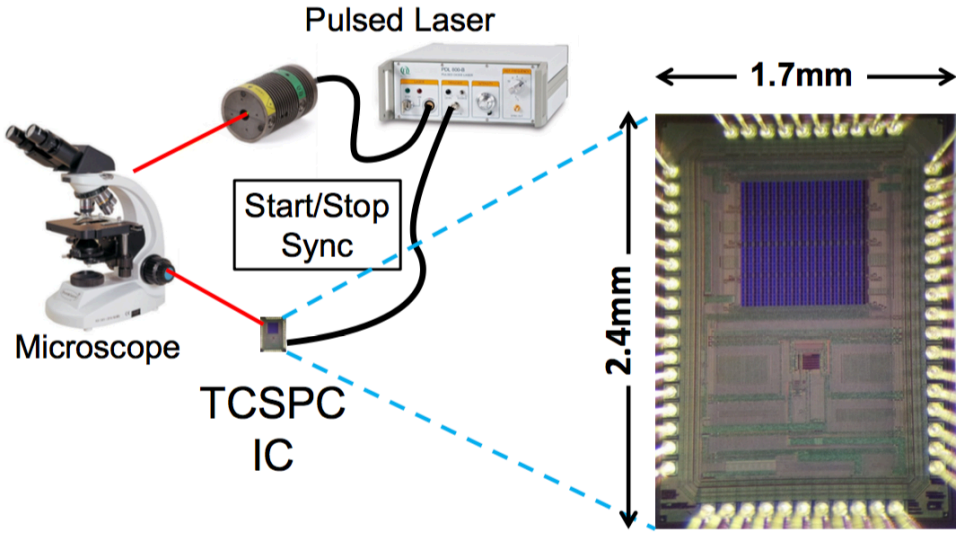
11.5 A Time-Correlated Single-Photon-Counting Sensor with 14GS/s Histogramming Time-to-Digital Converter

Neale A. W. Dutton[1,2], Salvatore Gnecchi[1,2], Luca Parmesan[1,2], Andrew J. Holmes[2], Bruce Rae[2], Lindsay A. Grant[2], Robert K. Henderson[1]

[1]University of Edinburgh, Edinburgh, United Kingdom,
[2]STMicroelectronics, Edinburgh, United Kingdom

Miniaturized TCSPC System



	This Work	
Architecture	Histogramming Folded Flash TDC	
Application	TCSPC	
Channels	1ch	
Tech.	130nm	
Supply	1.2V	
Conv. Rate	11.7GS/s	14GS/s
TDC Power	14.1 mW	

ADCs

	Type	Design	Tech	# bits	Rate [MS/s]	Energy [fJ/conv]
26.1	SAR	UMichigan	65 nm	13	50	6.9
26.2	SAR	Holst, Eindhoven	130 nm	12	22	50.8
26.4	SAR	KAIST	45 nm	10	1600	21
26.5	SAR	UMacau	65 nm	6	5000	39
26.6	Pipe/SAR	Broadcom	28 nm	10	5000	153
26.7	SAR	KAIST	45 nm	10	1700	30

Take home messages

- There is NO obvious successor to CMOS, yet.
  - CMOS will definitively saturate at … nm, but after the trains mankind invented the airplanes!
- Despite 20 years of whining, analog is NOT dead below 65 nm.
- … but if you want to make efficient low power electronics, think digital.

- Remember to ask Philippe to save travel money for the 2025 trip to ISSCC, you will still learn something interesting!

THANK YOU