Signal and Power Integrity Design Practices

Csaba SOOS

PH-ESE-BE
Outline

• Introduction
• Signal and interconnect bandwidth
• Time and frequency
  • Scattering parameters
• Transmission lines
  • Theory
  • Losses, ISI, discontinuities, crosstalk, mode conversion
• Power Delivery Network
• Related activities in the group
Introduction

• High-speed design challenges:
  • Front-end electrical links: very light cables and flexible circuits
  • Readout and control systems: complex FPGA boards, backplanes

• Data rate from 100’s of Mbits to 10Gbits per sec per channel
  • Maximum speed increases rapidly in back-end systems, >10Gb/s soon

• Design iterations cost money and take extra time (=money)

• Activities in the group offer the possibility to gather, share and preserve know-how
Sources

• Istvan Novak’s courses
  • Signal Integrity: Advanced High-Speed Design and Characterization
  • Power Distribution Design

• Eric Bogatin’s courses
  • Essential Principles of Signal Integrity
  • Advanced Gibabit Channel Design
  • http://www.bethesignal.com/bogatin/

• Eric’s book
Signal bandwidth

- Time domain: periodic signal (e.g. clock)
  - Period, $T$
  - Rise/fall times, $t_r/t_f$
  - Duty cycle, $D$

- Time-domain to frequency domain using Fourier transformation

- Spectrum of an ideal square wave ($D=0.5$, $t_r/t_f = 0$)
  - DC ($0^{th}$ harmonic) + infinite odd harmonics (1,3,5,...)
  - Amplitudes decrease with 1/f (-6dB/octave), $A_n=(2 \times A)/(\pi \times n)$
Signal bandwidth

- Trapezoidal signal (duty cycle $D$, $t_r/t_f > 0$)
- DC ($0^{th}$ harmonic) + infinite harmonics
- If $D$ is not 0.5, we have even harmonics too
- First corner frequency ($f_1$) depends on the duty cycle, but has less impact than rise/fall times
- Second corner frequency ($f_2$) depends ONLY on rise/fall times, $f_2 = 1/(\pi \times t_r)$
Signal bandwidth

• How many harmonics should be preserved?

• First approach
  • Use only harmonics which are more than 70% of the amplitude (-3dB) of the equivalent ideal square wave => e.g. up to 5\textsuperscript{th} harmonic

• Second approach
  • Sum up harmonics until the rise/fall time reaches required value => BW=0.35/t_{r(10-90)}, or BW=0.22/t_{r(20-80)} which is about the same as the second corner frequency

• Do not use higher bandwidth than required, because it costs money
Bandwidth of the interconnect

- The bandwidth definition is subjective
  - Highest sine-wave frequency at which the interconnect still meets the specs.
- We typically use -3 dB => 70% of the incident amplitude
- Bandwidth limitation increases rise time
  \[ RT_{out} = \sqrt{RT_{in} + RT_{channel}} \]
- To quantify, we can use the frequency dependent Insertion Loss of the interconnect
Time-domain and frequency-domain

- Time-domain is our real world where the design has to meet the specifications
- Frequency-domain is a mathematical ‘world’ where we can solve some problems faster than in the time-domain
- Different interpretations of the SAME thing
- Fourier transform links the two domains
Scattering or S-parameters

• Behavioural model of N-port linear electrical networks
• Frequency domain description
  • Sine wave in, sine wave out
• Inherited from RF and now widely used by SI/PI engineers

\[
\begin{align*}
\vec{b} &= S\vec{a} \\
\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} &= \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \\
b_1 &= S_{11}a_1 + S_{12}a_2 \\
b_2 &= S_{21}a_1 + S_{22}a_2
\end{align*}
\]
S-parameter plots (frequency domain)

- $S_{11}$ should be a large negative number if the port is matched to the reference impedance.
- $\text{Mag}(S_{21})$ shows the frequency dependent loss (FOM $\text{dB/inch/Hz}$).
- $\text{Ang}(S_{21})$ should start from 0 and decrease with increasing frequency (saw tooth).
S-parameters (time domain)

S parameters can be converted back to time domain (IFFT). Some artifacts may appear if the S parameter data does not meet certain criteria.
Mixed-mode S-parameters

Single-ended S parameters can be converted to mixed-mode S parameters to describe differential signals.
Transmission line

- Critical part of the channel that connects the source (driver) to the destination (receiver)
- It can be described with its electrical characteristics: $Z_0$, $t_{pd}$, loss, etc.
  - Do not uniquely determine the geometry (no solution or many solutions)
- Typical aspect ratio (trace width/dielectric height) of 50 ohm traces: from 2 (microstrip) to 1 (stripline)

\[ Z_0 = \frac{\Delta R + j\omega\Delta L}{\Delta G + j\omega\Delta C} \]
\[ \gamma = \sqrt{(\Delta R + j\omega\Delta L)(\Delta G + j\omega\Delta C)} \]
\[ \gamma = \alpha + j\beta = \alpha + j\omega t_{pd} \]

Lossless case ($R = 0$, $G = 0$)

\[ Z_0 = \sqrt{\frac{L}{C}} \]
\[ t_{pd} = \sqrt{LC} \]
\[ t_{pd} = \frac{l}{v}, \quad v = \frac{c}{\sqrt{\varepsilon_{eff}}} \]
Losses, resistive vs. dielectric

Standard FR4 dielectric, Dk=4.3, tanδ=0.02
h=150um, w=250um, Z₀ ~ 50 Ohm
dielectric loss dominates above 900MHz

Better dielectric, Dk=3.7, tanδ=0.002
h=150um, w=300um, Z₀ ~ 50 Ohm
conductor loss dominates, wasting the expensive dielectric
with tight coupling and surface roughness it gets worse

Surface roughness of the conductor increases the resistive loss at higher frequency. Use wider traces to reduce the impact.

\[ atten [dB/in] \sim \frac{1}{w[mils]} \sqrt{f[GHz]} + 2.3 \times f[GHz] \times Df \times \sqrt{Dk}, \text{Figure of Merit} \sim 0.1 - 0.3 \text{ dB/in/GHz} \]
Coupled traces, differential impedance

FR4, Dk=4.3, tanδ=0.02

Coupled microstrip traces

Coupled stripline traces
Tight vs loose coupling

Tight coupling decreases differential impedance. Need either narrower traces, or higher dielectric. This may lead to more losses. Loose coupling may compromise routing density.
Loss in coupled microstrip traces

Judging the loss of the interconnect using only $S_{21}$ is difficult, if traces are coupled. If the coupling is intentional (differential trace), use $S_{DD21}$ instead.
Inter-symbol Interference (ISI)

Frequency dependent (!) loss causes rise time degradation.

Rise time degradation causes vertical and horizontal eye collapse. State of the signal is influenced by previously transmitter bits.
Attenuation at Nyquist

10Gb/s, 5GHz Nyquist

Practical limits:
- -8dB limit without EQ,
- -15dB CTLE,
- -25dB CTLE+FFE+DFE
Mode conversion, frequency domain

Mixed-mode S parameters

Mode conversion (differential skew), check SCD terms
Mode conversion, time domain

No skew

18ps skew
Mode conversion summary

• There is no perfect interconnection, there is always mode conversion
  • Skew (driver, traces, connectors, PCB dielectric etc.), asymmetries

• Issues related to mode conversion
  • Distorted differential signal, EMI, ISI (reflected common signal converts back to differential)

• Solutions
  • Reduce skew to achieve << 10% UI, match near mismatch
  • Terminate common signal (no conversion back to differential)
  • Use symmetrical ground return vias (GSSG)
  • Use better dielectric glass weave (1086, 3313), better glass fill or zig-zag routing
Crosstalk

• Near-end crosstalk (NEXT)
  • In all forms of coupled lines
  • Depends on the mutual capacitance and inductance
    \[ K_{\text{next}} = \left( \frac{C_M}{C} + \frac{L_M}{L} \right) / 4 \]
  • Does not depend on coupled length for long traces \((t_r < 2t_{pd})\)
    \[ V_{\text{next}} = K_{\text{next}} V \]
  • Proportional to the coupled length for short traces \((t_r > 2t_{pd})\)
    \[ V_{\text{next}} = K_{\text{next}} V \left( \frac{2t_{pd}}{t_r} \right) \]
Crosstalk

• Far-end crosstalk (FEXT)
  • Only in inhomogeneous coupled lines (e.g. MS)
  • Depends on the difference in velocity between even and odd propagation modes (no difference in stripline, no FEXT)
    
    \[ K_{fext} = (C_M/C - L_M/L)/4 \]

• Proportional to the coupled length
  
  \[ V_{fext} = K_{fext} V(2t_{pd}/t_r) \]
Crosstalk, frequency and time domain

Microstrip

Stripline

NEXT lasts for 2TD
Crosstalk, frequency and time domain

Microstrip

Stripline

S21
S31
S41

FEXT in UI

No FEXT
Crosstalk, mitigation

- Use stripline, no FEXT
  - Loosely coupled allows to reduce dielectric height, less fringe fields

- Microstrip should be very short
  - If you need microstrip traces, use large separation \((s > 3w)\)
  - Reduce coupled length as much as possible

- Use 2D field solver for estimating the crosstalk
Discontinuities

• Discontinuities cause reflections
  • May impact the channel for MANY bit periods (difficult to compensate with equalization)

• Depends on many factors
  • Rise time, data rate, length and location of the discontinuity, losses

• Single reflection is tolerated if driver is terminated
  • Multiple discontinuities are much worse

• Losses could help, if you cannot avoid a discontinuity make the reflected signal travel longer

• Typical discontinuities
  • Stubs (routing, termination), via, imperfect return, connectors, packages
Routing via

- Provide connection between different PCB layers
- Consists of the thru and stub part
- Features:
  - Hole diameter
  - Capture pad size
  - Clearance diameter
  - Non-functional pads (NFP)
  - Differential via pitch
  - Via length
- LC pi approximation only at low frequencies
- Use 3D field solver to explore design space
Via optimization

• Get rid of stubs - first priority
  • $f_{res} = \frac{1}{4} \frac{1}{t_{pd}} = \frac{1}{4} \frac{c}{l_{stub} \sqrt{Dk_{eff}}}$ should be > 2 x signal bandwidth (@TX)

• Try to match impedance
  • Capture pads, and clearance hole diameter affect capacitance
  • Drill diameter affect inductance
  • Remove NFPs, they increase C and Dk_{eff} (electrical length increase)

• Differential via pitch
  • Tight spacing will reduce noise injected into cavity
  • BUT, also decreases differential impedance => compensate

• Return vias help to reduce ground bounce from common signal
  • No impact on differential signals
Power Delivery Network

• Deliver power from source to ICs
• Provide return path for signals
• Keep radiation within EMI limits
• Complex system consisting of:
  • Voltage Regulator Module(s) (VRM)
  • Decoupling capacitors
  • Vias, traces, planes on the PCB
  • Packages, etc.
• Need to design \( Z(f) \) according to the power rail requirements =>
• Take into account the limits set by the package and chip

\[
V_{\text{ripple}} > V_{PDN} = I(f) \times Z_{PDN}(f)
\]
\[
Z_{\text{target}}(f) = Z_{PDN}(f) < \frac{V_{\text{ripple}}}{I(f)}
\]

Assuming:
\[
I_{\text{transient}} \approx 0.5I_{\text{peak}}, I_{\text{peak}} = \frac{P_{\text{max}}}{V_{dd}}, \text{ripple} = 5\%
\]
\[
Z_{\text{target}} < \frac{V_{dd} \times 5\%}{0.5I_{\text{peak}}} = 0.1 \times \frac{V_{dd}^2}{P_{\text{max}}}
\]
PDN design challenge

We can influence this region.

On-die Capacitance
130nm technology:
\[ 130 \frac{nF}{cm^2} \]
Decoupling

- **Bulk capacitors**
  - Electrolytic: high C, high ESR, high L
  - Tantalum: high C, medium ESR, medium L

- **Multi-layer Ceramic Capacitors (MLCC)**
  - Medium C, low ESR, low L
  - Low ESR could mean high Q, which is not always good
  - ESL depends also on mounting

- **How to achieve ESL = 0.5-2nH**
  - We have to reduce parasitic inductances
  - Bring planes close to the IC
  - Use thin dielectric between planes
  - Use short and wide surface traces
Ansys Capacitor Library Browser

- Define VRM
- Define target Z
- Select capacitors
  - Vendor
  - Size
- Use automatic optimization
- Adjust manually
Tools

• Impedance calculators
  • Quick answer but not always accurate, good for estimation
  • PCB Saturn, Qucs

• Field solvers
  • 2D/3D, hybrid
  • Slightly more complicated to set up, but accurate

• CERN
  • ANSYS EM (HFSS, Q3D, Siwave, Designer, Via wizard, PI advisor)
  • HyperLynx (not supported)
  • Cadence
  • Other tools: CST (3D EM solver), Qucs
Measurement

• TDR uses voltage step with certain rise time (=> BW)
• TDR has a broadband receiver
  • Higher noise floor
• TDR source power roll-off limits dynamic range
• VNA uses single-tone sine wave
• VNA has narrow IF bandwidth
  • Lower noise floor
  • Higher dynamic range
TDR vs VNA, dynamic range

S-parameters (measurement)

Eye diagram (simulation, ANSYS)

5Gb/s PRBS-7 (PNA)

5Gb/s PRBS-7 (TDR)
Controlled impedance on very high density flex circuits

- G. Blanchot, M. Kovacs, T. Gadek, Gianluca Traversi, Francesco De Canio
- Investigated the impedance of various routing topologies
- Built test board to measure impedances and compared with previously calculated values

**Diagram:**
- Edge coupled microstrip
- Edge coupled stripline
- Broadside coupled stripline
- Broadside coupled offset stripline

**Dimensions:**
- Shorter test line = 101 mm
- Longer test line = 113 mm
Controlled impedance on very high density flex circuits, measurement

- Impedance measurements are well in line with simulation results, small difference observed for the broadside coupled striplines.

- Edge-coupled microstrip and stripline differential pairs showed 80 Ω – 90 Ω impedance, close to the target 100 Ω value.
Light weight readout cable for inner barrel pixel readout
Light weight readout cable for inner barrel pixel readout, S parameters
Light weight readout cable for inner barrel pixel readout, time domain

Eye diagram simulation on built-in cable model, $L=2.7\,\text{m}$ $TD=0.008$, 1.2Gbps

Eye diagram simulation using FFE on built-in cable model, $L=2.7\,\text{m}$ $TD=0.008$, 1.2Gbps

Eye diagram simulation on measured S parameters, $L=2.7\,\text{m}$ $TD=0.008$, 1.2Gbps

Eye diagram simulation using FFE on measured S parameters, $L=2.7\,\text{m}$ $TD=0.008$, 1.2Gbps

Simulation

Simulation using measured model

Simulation

Simulation using measured model
ALICE ITS upgrade, Outer Barrel

• Gianluca Aglieri, Antoine Junique

• Transmission lines on Flexible Printed Circuits (Al/Polyimide or Cu/Polymide)
  • specifications, design, modelling
  • identification of critical parameters (resistive losses in ITS case)
  • identification of architectural trade-offs e.g. bit-rate vs physical constraints (material, thickness, lengths) and definition of system specs

• Frequency domain synthesis/analysis, S parameters models transient domain simulation (including the "virtual" eye-diagrams)
ALICE ITS upgrade, Outer Barrel

Frequency domain

Time domain

Phased Array System Engineering seminar, 9/6/2015
Csaba SOOS, Signal and Power Integrity Design Practices
ALICE ITS upgrade, Outer Barrel

- Transmission of 1.2 Gb/s on Al Flex over 27cm robust
- Transmission of 160 Mb/s on Al/Cu Flex over 1.5m robust
  - Pre-emphasis desirable
- Transmission of 320 Mb/s on Flex over 1.5m possible
  - Pre-emphasis necessary
  - Copper and differential microstrips facilitate
GBTx test board PDN

• 4-port sensing (Kelvin method) for measuring low impedance (plane)
• Simulation carried out using Ansys SIwave
• Nice match above 1 MHz
• Mismatch at low frequency could be due to capacitor model
PCle40 PDN, current density

Jean-Pierre Cachemiche, Fred Rethore (CPPM)
Cadence Sigrity

Current density too high

Reshaping and splitting planes to reduce current
PCle40 PDN, IR drop

VCCT (0.9V, 5A) ~ 60mV
VCCR (0.9V, 13A) ~ 160mV

Redesigned shapes to reduce drop

VCCT (0.9V, 5A) ~ 15mV
VCCR (0.9V, 13A) ~ 50mV

Jean-Pierre Cachemiche, Fred Rethore (CPPM)
Cadence Sigrity

PH-ESE seminar, 9/6/2015
Csaba SOOS, Signal and Power Integrity Design - Cadence
Backup slides
PDN analysis, mounting inductance

<table>
<thead>
<tr>
<th>Capacitor Model</th>
<th>Mounting Quality</th>
<th>Total Mounting Inductance, nH</th>
<th>Estimated ESL, nH</th>
<th>Actual Resonance Frequency, MHz</th>
<th>Resonance Frequency w/o Mounting, MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>C6 C=0.1uF, ESL=Auto, ESR=25mOhms</td>
<td>good</td>
<td>1.52</td>
<td>0.31</td>
<td>12.89</td>
<td>27.71</td>
</tr>
<tr>
<td>C10 C=0.1uF, ESL=Auto, ESR=25mOhms</td>
<td>good</td>
<td>0.63</td>
<td>0.28</td>
<td>19.98</td>
<td>27.71</td>
</tr>
</tbody>
</table>
PDN analysis, laminate thickness

- Thinner laminate helps to reduce the impedance, but watch out for anti-resonance (Cplane + decoupling inductance)
Unwanted coupling seen on S21
HyperLynx, PCIe Gen3 channel