Commissioning and Performance of the upgraded ATLAS Pixel Detector for Run II

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Ann Arbor, MI
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Run 1 Pixel
3-Layers pixel with 80M pixels (5cm radius B-layer)

Insertable B-Layer (IBL)
4th Pixel layer with 12M pixels (3.3 cm radius)
Motivation for a 4th Pixel Layer

Run II conditions after LS1 will be very different

- centre-of-mass energy is increased from 8 TeV to 13 TeV
- luminosity is increased from $10^{34} \text{ cm}^{-2}\text{s}^{-1}$ by a factor of 2-3
  → readout inefficiency in B-Layer will reach 5% to 10%

Aim for IBL

- compensate readout inefficiencies
- add redundancy against radiation damage
  → improve vertex reconstruction, tracking and b-tagging performance
New 4th silicon layer the the ATLAS Pixel

- 14 staves organized in a turbine-like fashion with $\Phi = 14^\circ$ tilt angle
- New FEI4 readout chip
  130nm CMOS modules
- New sensor technologies
  planar slim edge and 3D
- New readout system, to be used for
  Pixel bandwidth upgrade in Run II
- Low material budget
  - radiation length $< 1.9\% X_0$
  - carbon foam support
  - evaporative CO$_2$ cooling

IBL Overview

IDTR-2015-007
IBL Staves/Modules

- 20 pixel sensors per stave
- 12 double-chip modules, 8 single chip modules
- 32 front-ends per stave

26880 pixel

12 planar Sensors

4 x 3D Sensors

4 x 3D Sensors

2 FE + planar sensor

230 μm thick n⁺-in-p sensor
- short collection time
- lower depletion voltage
- higher capacitance, noise
- two vendors (FBK & CNM)

200 μm thick n⁺-in-n sensor
- slime edge (200 μm)
- one vendor (CiS)
New Front-end

- Smaller pixel size improves resolution and lowers occupancy
- Larger chip with increased active area
  - simpler module design
  - less material in detector
  - cheaper module production
- Increased radiation tolerance to withstand 2.5 MGy/5·10^{15} neq cm^{-2}
- Local hit processing and data storage
  - higher occupancies without saturation
  - reduced bandwidth use
  - lower power consumption

<table>
<thead>
<tr>
<th></th>
<th>FE-I3</th>
<th>FE-I4</th>
</tr>
</thead>
<tbody>
<tr>
<td>CMOS Technology</td>
<td>250 nm</td>
<td>130 nm</td>
</tr>
<tr>
<td>Chip size</td>
<td>8×11 mm^2</td>
<td>20×19 mm^2</td>
</tr>
<tr>
<td>Pixel size</td>
<td>50×400 μm^2</td>
<td>50×250 μm^2</td>
</tr>
<tr>
<td>Pixel array</td>
<td>18×160</td>
<td>80×336</td>
</tr>
<tr>
<td>Active area</td>
<td>74%</td>
<td>89%</td>
</tr>
<tr>
<td>Readout rate</td>
<td>40 Mb/s</td>
<td>160 Mb/s</td>
</tr>
<tr>
<td>Threshold</td>
<td>3500e</td>
<td>1500e</td>
</tr>
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</table>
• **Pixel** was extracted from ATLAS in Apr 2013
• **New Service Quarter Panels (nSQP):** new on-detector services, new optical links, module failure repairment
• **IBL:** additional layer with advanced technology
• **Diamond Beam Monitoring (DBM):** FEI4 with diamond and silicon sensors, installed in the pixel volume.
• **New readout chain** for Layers 1 and 2 (on-going)
New Readout Chain

- New 9U-VME Readout Driver (ROD) and Back-of-Crate Card (BOC)
- Ethernet-based communication to overcome VME bandwidth limitations for off-detector calibration (6 GBit/s)
- Capability of processing all FE data at 200KHz trigger rate (IBL expects to run at 100kHz)
Pixel Improvement

Pixel Perf 2015/06/01

- Pixel: 3% of modules recovered since Run 1 (now 98% of modules active)
- IBL: 99.5% of modules active for Run2

Pixel Disabled Modules [%]

- **ATLAS** Pixel Preliminary
  - End of Run 1
  - After Re-installation

![Bar chart showing PixelDisabled Modules][1]

![Graph showing PixelLayer 0][2]

B-Layer

Run II

K. Potamianos (LBNL)

By: Alice

July 22-29, 2015 7 / 17
Lessons Learned

- **Bump-bonding**
  - problems with the first batch of sensors
  - open bumps and shorted pixels
  - solved by performing flux free flip-chip
- **Module replacement**
  - 28 modules had to be replaced
  - extremely delicate operation
  - successfully managed to perform the procedure
- **Wire-bonds corrosion**
  - Mid-way during production discovered corrosion of wire bonds
  - Halogen (Cl or F) associated with the corrosion product (residue)
  - half of the staves were cleaned, wire-bonds redone
  - On few samples discovered Fluorine into the gold layer
Pixel re-installed into ATLAS, Dec 2013

Pixel Detector status after LS1

- Pixel detector re-installed into ATLAS Experiment on 9th December 2013
- Outstanding recovery of modules
- 75% of modules recovered on the surface
- Few new modules found faulty after the reconnection

IBL lowered down, May 5th 2014

- IBL was lowered down in the ATLAS cavern on May 5th, 2014
- IBL installed, May 7th 2014
First Run2 Collisions with a 4-Layer Pixel
• Distortion is driven by the difference of CTE (coeff. of thermal expansion) between the carbon foam and stave flex where they are glued together in one side of the omega-shaped stave
• Thermo-mechanical asymmetry between two sides of the carbon foam
• Carbon foam: ~0ppm  Stave flex ~ several tens of ppm
• Thermo-mechanical FEA analysis confirmed qualitative nature of bowing
• Dedicate temperature scan during Cosmic commissioning show a nice m
• The distortion can be corrected using track-based alignment procedure.
• Good stability of CO$_2$ cooling is observed and monitored.

\[
\frac{dM}{dT} = -10.6 \pm 0.7 \text{ [\(\mu\text{m/K}\)]}
\]
Pixel Detector Performance

- Pixel cluster on-track in-line well with Run I
- IBL cluster on-track ToT distribution as expected, with the difference in peak position due to different sensor thickness (200 μm for Planar and 230 μm for 3D sensors)
- Minimum cluster width for IBL around 240 mrad as expected from the silicon bulk properties and the 2T uniform field from the ATLAS solenoid

Pixel Perf 2015/06/01

ATL-PHYS-PUB-2015-012
b-Tagging Performance Enhancement

- Significant improvement to b-tagging for Run II
- Improved light-flavor jet rejection due to IBL and algorithm improvements (new multivariate tagger MV2, tracking, in particular TIDE)

See M. Clark's DPF talk

ATL-INDET-PUB-2014-006

ATL-PHYS-PUB-2015-022
Summary

• Re-furbished pixel detector since Run I
  • Improved services and optical links for high occupancy
  • Recovered about 3% of the 3-layer pixel
• Improved pixel detector for Run II
  • New IBL is well under control and still in performance optimization
  • New read-out system for IBL to be used for Pixel bandwidth upgrade
• Looking forward to an exciting and challenging Run II
Backup
Pixel Bandwidth Upgrade

- The 40 Mbps readout of Layer 2 will be a bottleneck when running at Run 2 luminosities
- Use the IBL ROD and BOC cards with pixel modules to increase the bandwidth

<table>
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<tr>
<th>Link occupancy at 100 kHz L1 trigger rate</th>
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<tr>
<td></td>
</tr>
<tr>
<td>$\mu$</td>
</tr>
<tr>
<td>50ns</td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td>25ns</td>
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Most significant improvements:
- B-Layer dead modules from 6.3% to 1.4%
- Layer2 dead modules from 7% to 1.9%

In Run2, 98% of Pixel in functional.
Planar sensor (CiS)  
Slim edge

3D sensor

Sensors technology
# ROD: Pixel vs IBL

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<thead>
<tr>
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<th>Pixel ROD</th>
<th>IBL ROD</th>
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<tbody>
<tr>
<td><strong>FPGAs</strong></td>
<td>1 Master + 8 Formatter + 1 EFB + 1 Router + 1 PRM</td>
<td>1 Master + 2 Slaves + 1 PRM</td>
</tr>
<tr>
<td><strong>Control</strong></td>
<td>Master DSP + 4 Slave DSP</td>
<td>Embedded PPC &amp; MicroBlaze</td>
</tr>
<tr>
<td><strong>Memory</strong></td>
<td>Many External</td>
<td>Mostly Internal to FPGA except SSRAMs + DDR2s</td>
</tr>
<tr>
<td><strong>Components</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Data RX rate</strong></td>
<td>40 MHz (all channels enabled)</td>
<td>80 MHz</td>
</tr>
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Stave Quality Assurance

- Extensive tests performed before installation of the IBL
- optical inspection
- electrical tests
- tuning and calibration 1500e/10ToT (16 ke)
- source scan (Sr$^{90}$)
- thermal cycle
- ranking of the staves based on equivalent number of bad pixels
- (< 0.2%/stave)
- Stave integration order based on minimization of $\eta$-$\phi$ structure