FELIX: the detector readout upgrade of the ATLAS experiment

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Brief about FELIX

• What is FELIX?
  ▶ Front End Link Interface eXchange
  ▶ the new ATLAS Readout for Run4(2023)
  ▶ a heterogeneous switch

• Why we change?
  ▶ Upon the change of link protocol on FE side from S-Link to GBT-Link
  ▶ To introduce Commercial Off-The-Shelf (COTS) products → convenient to scale up the electronic components

GBT-link: radiation hard bi-directional optical link protocol developed by CERN
https://espace.cern.ch/GBT-Project/GBT-FPGA/default.aspx
ATLAS TDAQ : Current (2015)

40.08 MHz

L1 trigger

trigger rate : 100 kHz

FE : Front-End
ROD : Read Out Driver
ROS : Read Out System (buffer)
HLTPU: High Level Trigger Processing Unit

Ethernet

Custom Link

S-Link

COTS network

Custom Components

PC

HLTPU

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ROD-like features can be implemented in downstream of FELIX either in software or in hardware.
A new TDAQ architecture based on FELIX will become
1. Scalable
2. Heterogeneous

Routing of multiple traffic types:
(physics events, detector control, configuration, calibration, monitoring)
Reconfigurable data path
Multicasting, Cloning, QoS

Automatic failover and load balancing
Trigger data, LHC clock distribution

E-link: variable-width logical link on top
GBT. Can be used to logically separate different streams on a single link.

Feature and functionality

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FELIX Architectural View

- **Front End Board**
  - GBTx

- **Optical Receiver**
  - Xilinx Virtex7

- **FPGA PCIe Card**
  - PCIe Gen. 3 x 8 Lane

- **Mezzanine card**

- **FELIX PC**
  - PCIe Gen3 Slot x6
  - Network Card

- **PC**
  - network Switch

Optical Link: 4.8 (9.6) Gbps / link

Trigger data / LHC clock 40.08 MHz

PCIe Gen. 3 x 8 Lane 64 Gbps

40 Gbps / port
Development Platform

High Tech Global 710
Xilinx Virtex 7
CXP module: 12ch

Mezzanine card

FELIX PC
PCIe Gen3 Slot x6
Network Card

Mellanox ConnectX-3 EN
40Gbps x 2port

SuperMicro X10DRG-Q
Haswell CPU 10 cores x2

KC705/GLIB

HTG-710
CXP1
CXP2
Xilinx Virtex7

PC
gbtX

12ch

PCle Gen. 3 x 8 Lane

Network Switch

2 port
FELIX Functional View

FELIX Firmware design

Time, Trigger & Control

Decode trigger data and recover LHC clock

FELIX PC

Buffer

Network Card

Software Pipeline

Data Storage

Data Storage

Network Switch

Send/Receive GBT data

Map GBT data to E-Link format

Push data to the memory

Repack E-link data to Industry standard network packet

Front End Board

Giga-Bit Transceiver

Central Router

PCle DMA Engine

GBTx

FELIX PC

Network Card

Software Pipeline

Repack E-link data to Industry standard network packet

Data Storage

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Send/Receive GBT data

Map GBT data to E-Link format

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Decide trigger data and recover LHC clock

FELIX Firmware design

Time, Trigger & Control

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GBTx

FGTb
• Split functional Test
  • Forwarding trigger signal and LHC clock (TTC – CR – GBT – FE)
  • PCI DMA performance
  • Network throughput

• Combined test : Full FPGA chain
Trigger/Clock Forwarding test

- Split functional Test
  - Forwarding trigger signal and LHC clock (TTC – CR – GBT – FE)
  - PCI DMA performance
  - Network throughput

- Combined test: Full FPGA chain
Trigger/Clock Forwarding test

- Constant latency: 247 ns (including cable delay: 5 ns)
- Jitter in LHC clock @ HTG710: 6.5 ps
  @ GBTx chip: 9 ps
PCIe DMA performance

- **Split functional Test**
  - Forwarding trigger signal and LHC clock
  - **PCI DMA performance**
    - a. PCIe – Memory : throughput test
    - b. Data Emulator – PCIe – Memory : stability test
  - Network throughput

- Combined test : Full FPGA chain
PCIe DMA performance

Throughput test

Working point
6.3 GB/s

Stability test

Stable readout from PCIe card possible over long timespan

(Throughput speed is only limited by Internal pseudo-data generator’s throughput)
Network throughput test

- Split functional Test
  - Forwarding trigger signal and LHC clock
  - PCI DMA performance
  - Network throughput (Memory – Pipeline – NIC – Switch – PC)

- Combined test: Full FPGA chain
Network throughput test

- Input from files
- Hardware limit: 40 Gbps
- Achieved maximum throughput for large data fragments: 36 Gbps
- Need more efforts for smaller fragments
**Combined test : Full FPGA chain**

- Data Emulator – GBT – FE – CR – PCIe – Memory
- pseudo data loop back through Front End forwarded to host memory
- FE and FELIX are synced in LHC clock
- Received data is matched to the generated data
Summary & Outlook

• Summary
  ● FELIX is a new readout system of ATLAS DAQ for the next LHC runs
  ● FELIX is a heterogeneous switch
  ● First integration test is done and achieved reasonable results

• Upcoming Tasks
  ● Establish multiple GBT link design and clocking scheme
  ● Implement all functionality (TTC Busy, HDLC encode/decode ... )
  ● Prove no data congestion between GBT and Central Router
  ● Optimize host software functionality and performance

• UC Irvine is going to join for software development

• Production and test plan
  A few FELIX prototypes will be produced and tested with several prototypes for new detector components foreseen for Run4
Evolution of Readout Architecture

ROD (readout driver): is an off-detector end point that processes incoming data to send via ethernet.

FELIX routes physics data to off-detector endpoint through industry standard network.

ROD-like functionality can be implemented either in software or in dedicated hardware.
FELIX Firmware Design

Legend:
- Main data path
- Slow control and monitor

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Development team

FELIX FPGA
- GBT
- Central Router

Time, Trigger & Control
- PCIe DMA Engine

FELIX PC
- Software Pipeline

FPGA Firmware development
- Time, Trigger & Control
- Giga-bit Transceiver (GBT)
- PCIe DMA engine
- Central Router

Software development
- Independent implementation
- First integration efforts in May 2015

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