

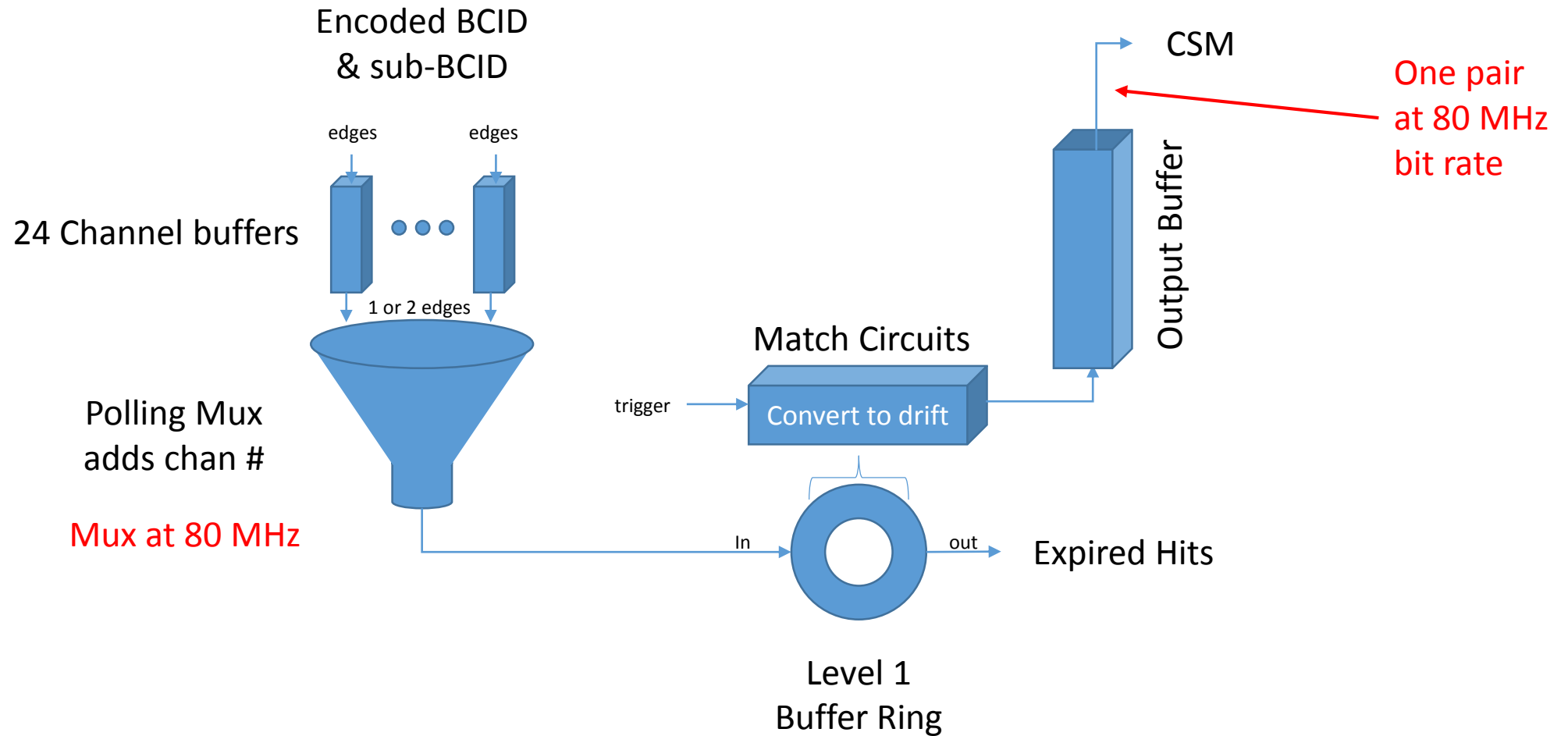
Design Study of the Options for the ATLAS Muon Drift Tube (MDT) Electronics for Phase-II

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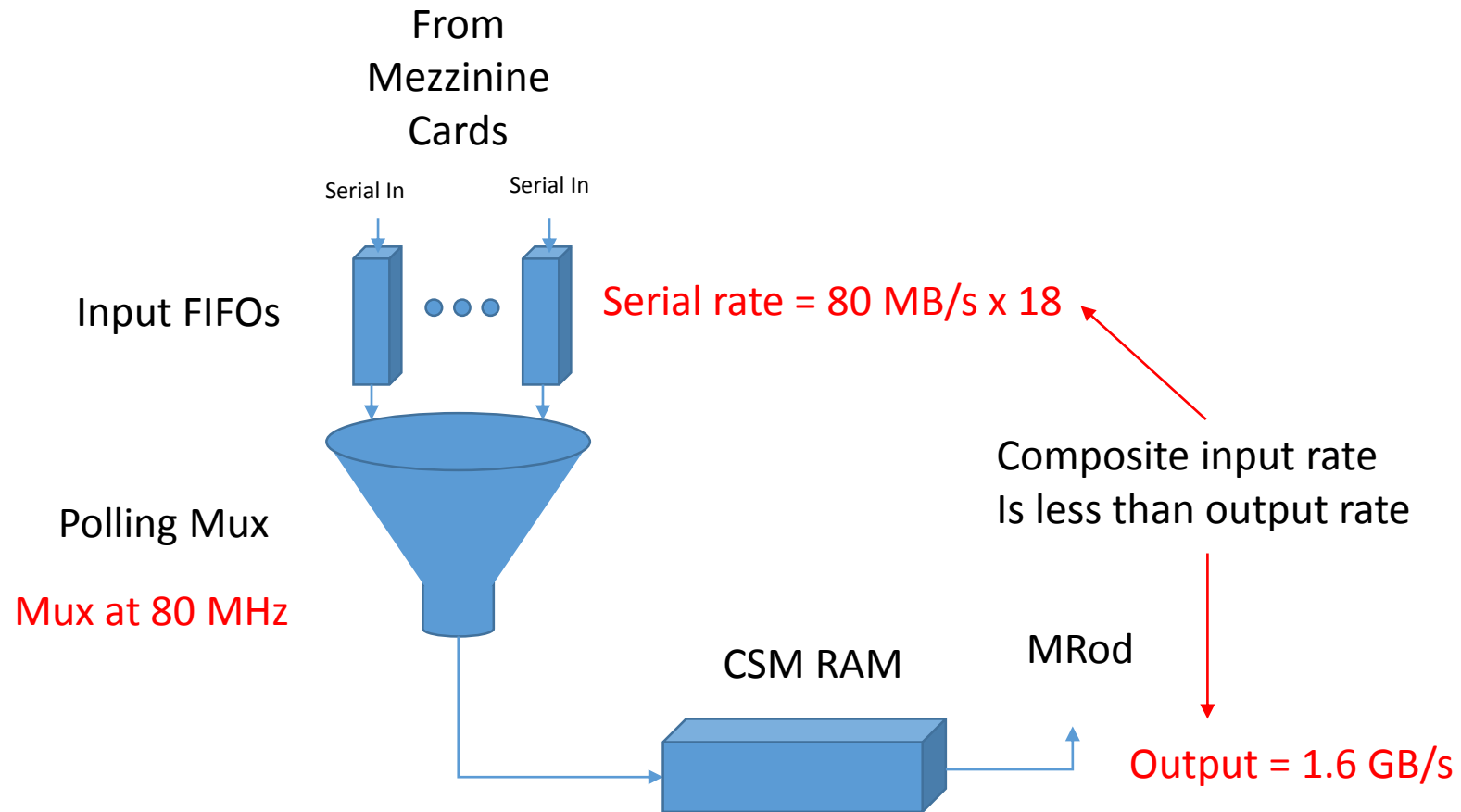
Goals (of the work & presentation)

- Characterize each design being considered for a new MDT front-end
- Simulate the latency for data arriving at USA-15 for MDT trigger
- Determine any bottlenecks in the flow of data
- Check the bandwidth available with the existing cables
- Determine the highest tube rate sustainable with each option
- Examine the capability of the current (legacy) electronics
- Show cable tests of the current mezzanine to CSM cables

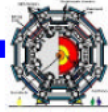
Front-end Cards Now



CSM (second multiplexer) Now

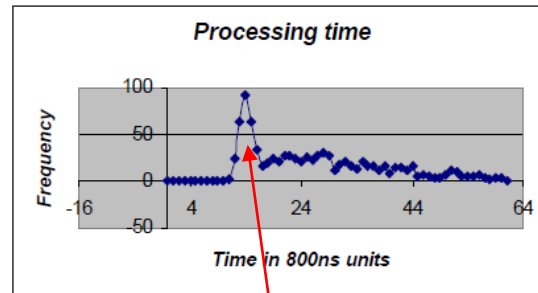
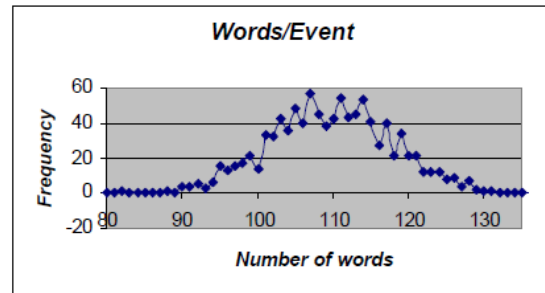
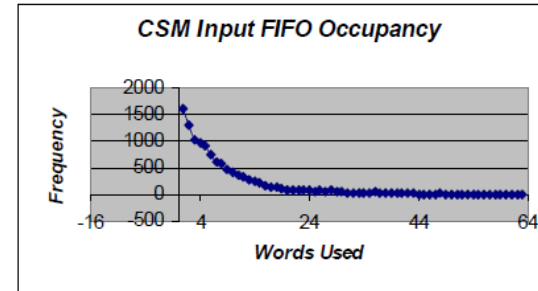
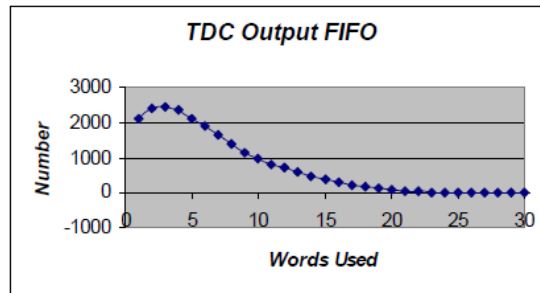


Latency in the Current CSM Readout



ATLAS

Buffer Occupancies from Performance Monitoring



Can't just
run what
we have

Note Date
September
1999

Minimum time 15us

September 19, 1999 - J. Wehrley Chapman



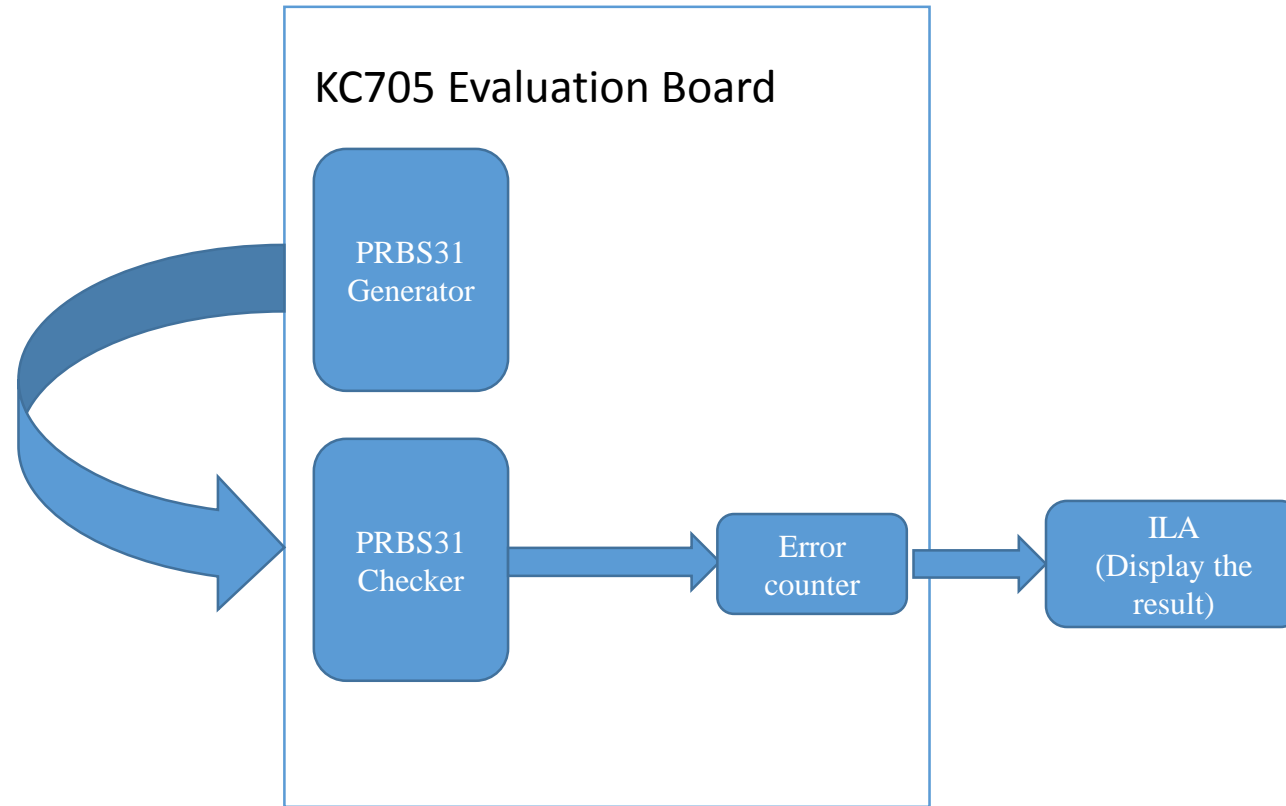
Design Methodology for Simulation

- Not a Design but an Evaluation & Consideration of Options
- A Specific Design is considered but it is not chosen at this time
- Detailed Electronics implemented in Behavioral Verilog
- Data Rates taken from Physics MC or extrapolated measurements
- Data Movement times (Latency) evaluated for realistic data rates
 - Starting time represented as BCID + sub-BCID (0.78ns) at it arrival #1
 - Ending time represented as BCID when hit handed off to fiber driver #4
 - For complete transit time need to add fiber transit time and receiver time
- Data Buffer requirements evaluated

Why Consider Send-Immediately Design

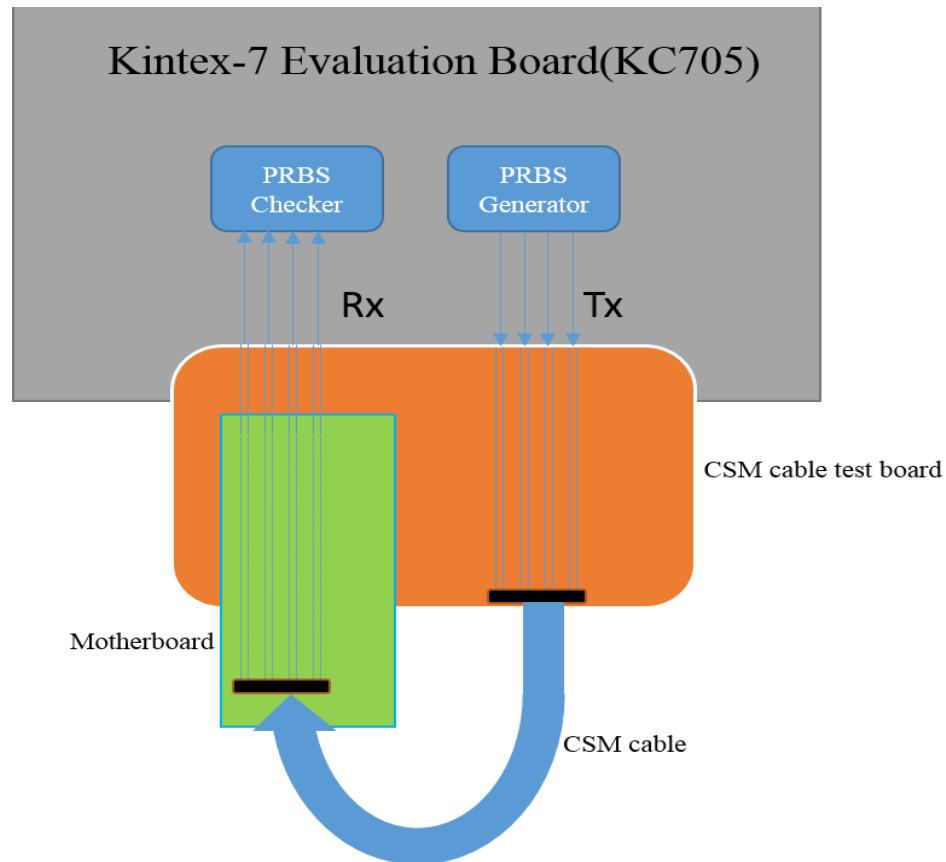
- The $\sim 800\text{ns}$ MDT drift time & 1 MHz L0 trigger selects everything!
 - Current design selects a $1\mu\text{s}$ window each trigger. Overlaps read same hits!
- A single path for trigger & data is simple if fast enough.
- Current mezzanines send data on one pair at 80 MHz bit rate
- Cables have 2 pairs available: Will show test to 320 MHz
- Generate random hits at rates up to 400 KHz/tube
 - Multiplex these hits from 24 channels into RAM and onto 2 pairs to CSM
 - Receive & multiplex the 18 mezzanines into CSM RAM & onto fast fiber
- Examine the distribution of transfer times, hit time to fiber entry
- Determine the highest tube rate that can be sustained

Current Cables Tested to 320MHz

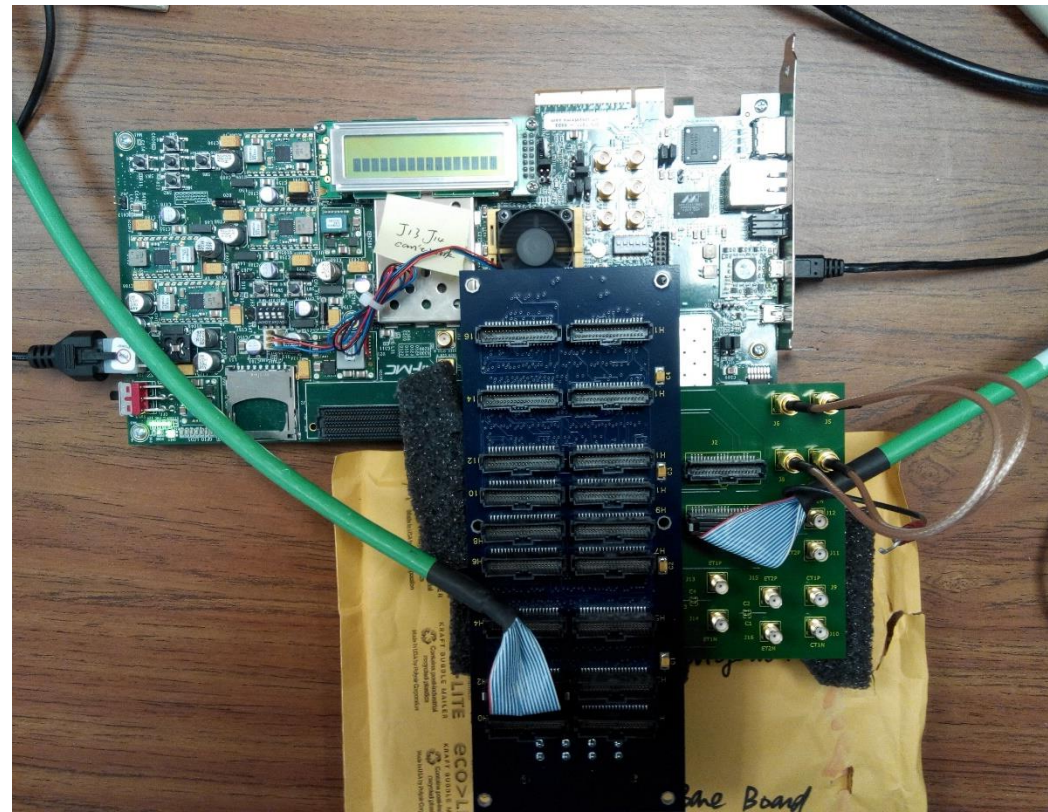


Setup for BER test

- ◆ Kintex-7 Evaluation board used as a Bit Error Ratio (BER) Tester.
- ◆ CSM cable test board is used for cable test interfaces. Four differential pairs(CH1-CH4) of cable can be tested at the same time by using test board.
- ◆ Cable's length is 1.33 m.



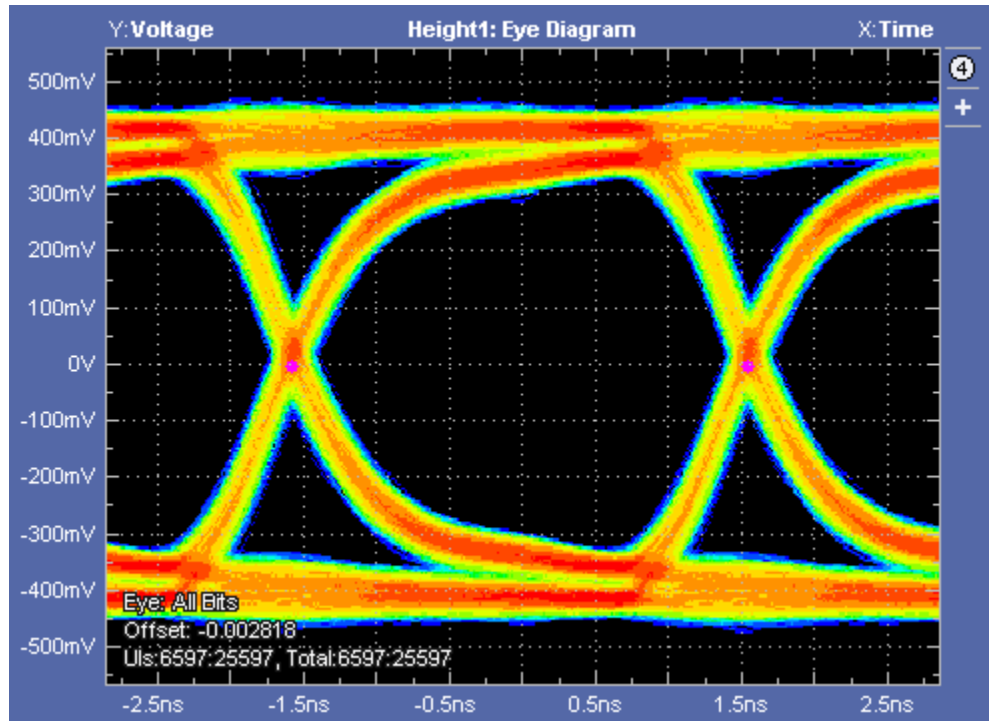
Testing schematic of CSM cable and MB



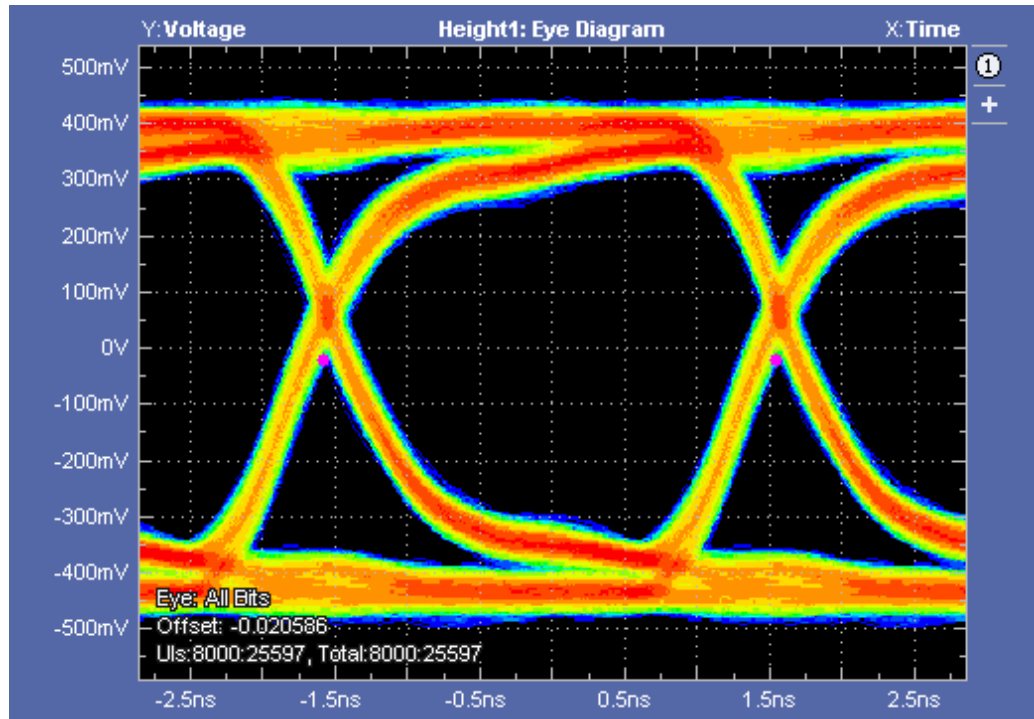
Connection diagram

Eye diagram measurements for 1.33m cable

- At the beginning, we tested CH1's eye diagram. No data transmission in other channels.
- Next, tested CH1's eye diagram again. This time, there is data transmission in CH2 at the speed of 320Mbps and no data transmission in CH3 and CH4.
- Even if data transmit in CH2 at 320Mbps, CH1's eye diagram is also good.



CH1's eye diagram, no data transmit in CH2(1.33m cable)



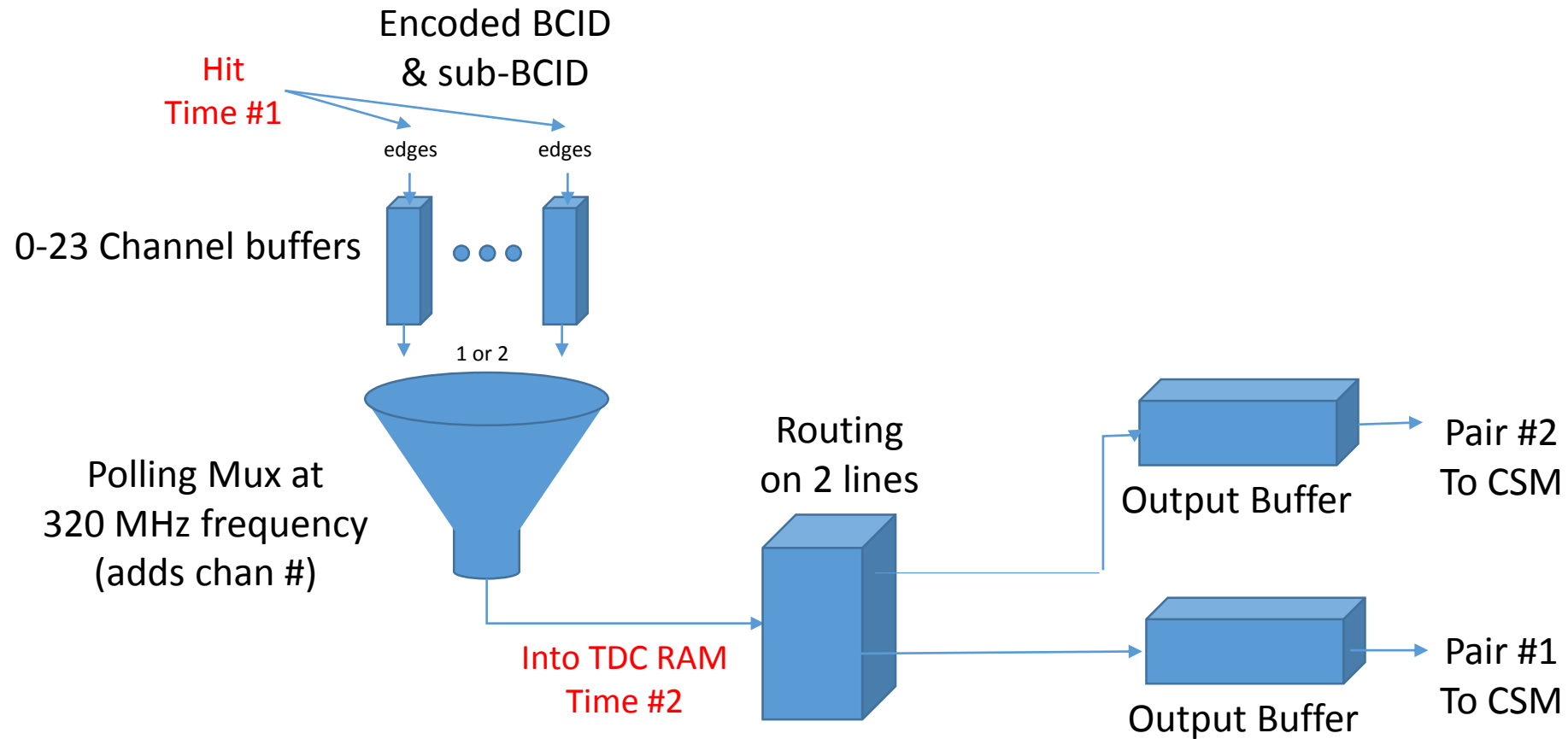
CH1's eye diagram when data transmit in CH2 at the speed of 320Mbps(1.33m cable)

BER results for 1.33m cable

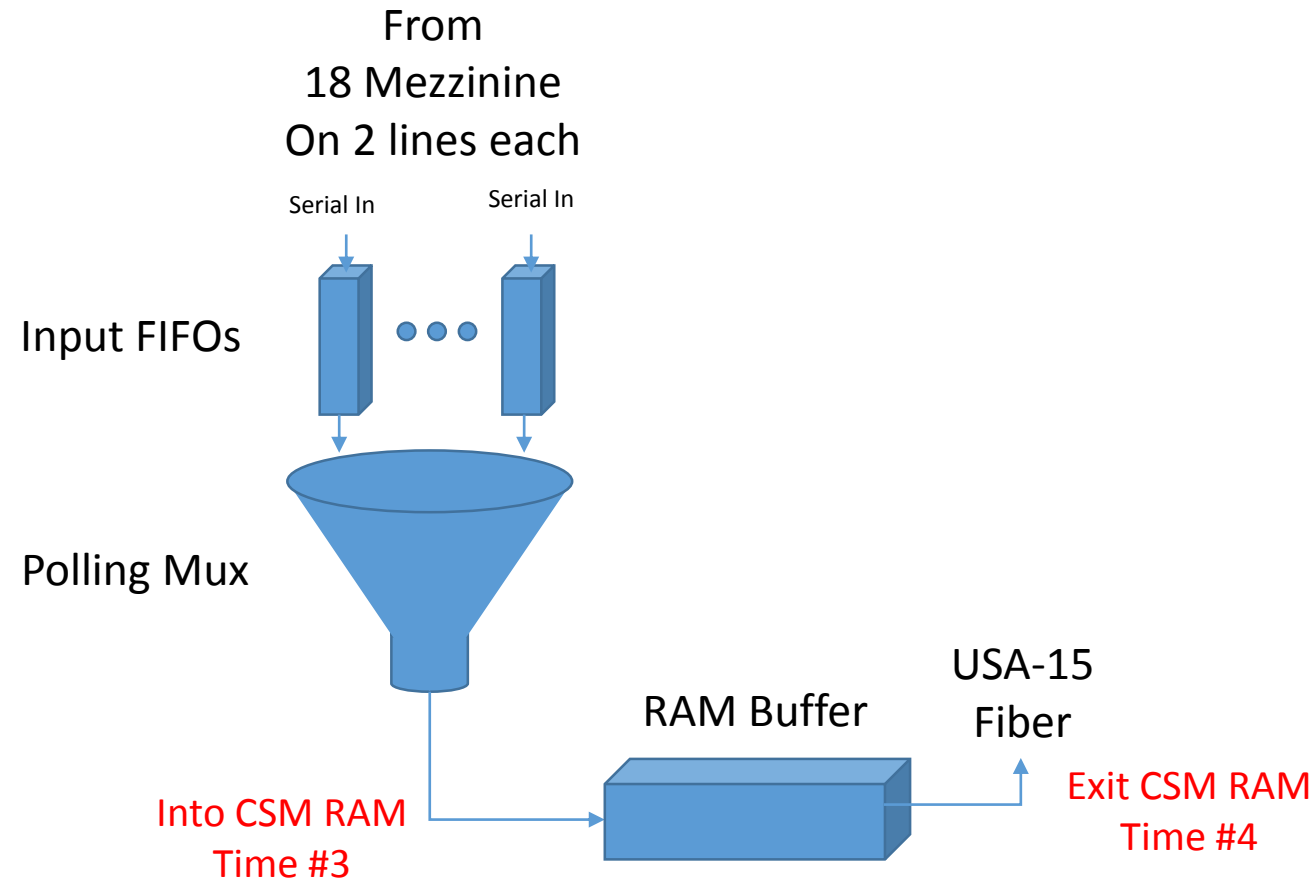
- We have run the BER test program in four channels with different data pattern at the speed of 320Mbps about 67 hours.
- Results are listed below:

Channel	Data pattern	Polynomial	Data bits	Errors	BER
CH1	PRBS31	$X^{31}+X^{28}+1$	7.76E13	0	1.29E-14
CH2	PRBS31	$X^{31}+X^{29}+1$	7.76E13	0	1.29E-14
CH3	PRBS29	$X^{29}+X^{27}+1$	7.76E13	0	1.29E-14
CH4	PRBS23	$X^{23}+X^{18}+1$	7.76E13	0	1.29E-14

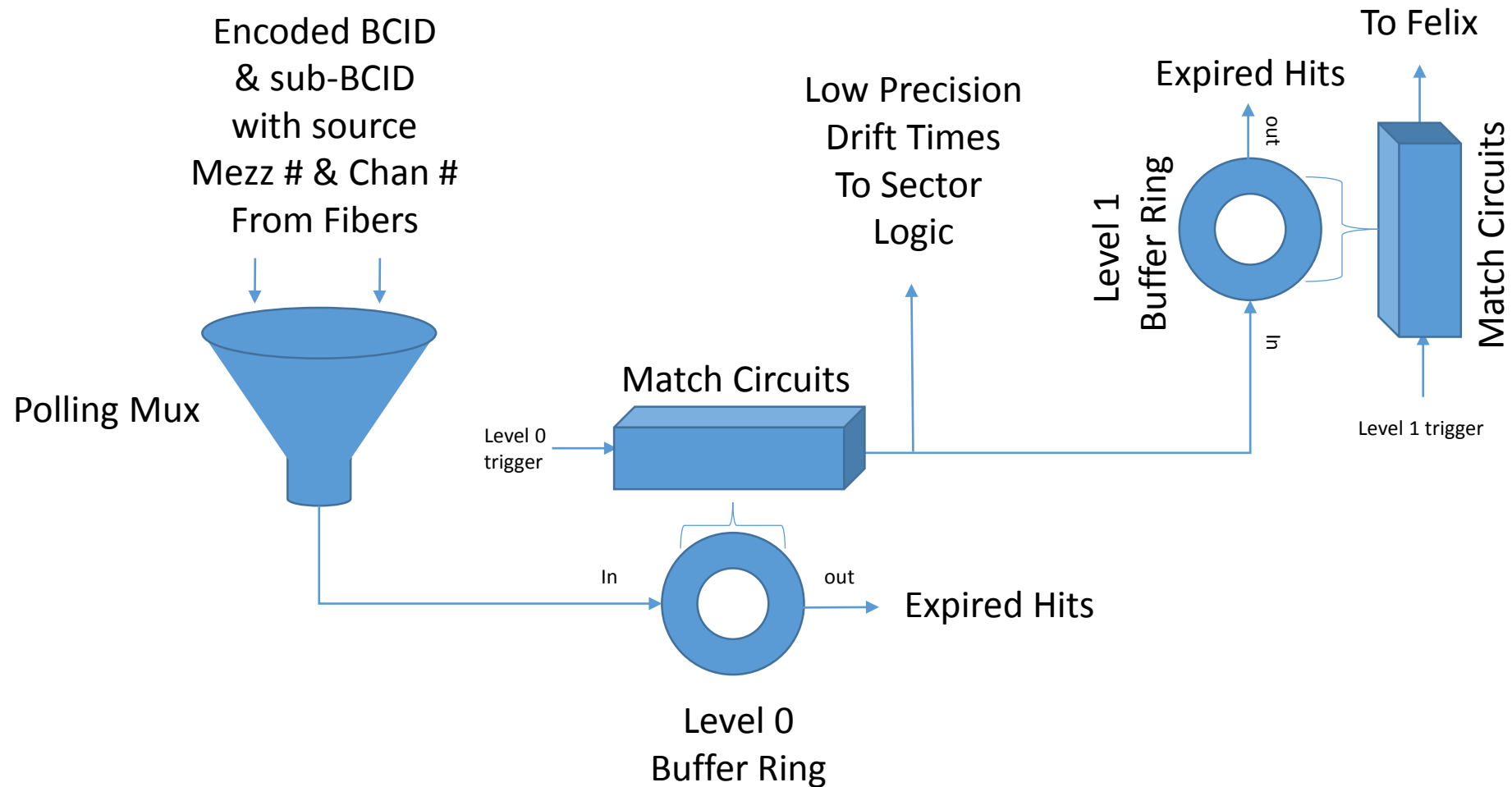
Design Considered in Simulation



New CSM, Much the Same



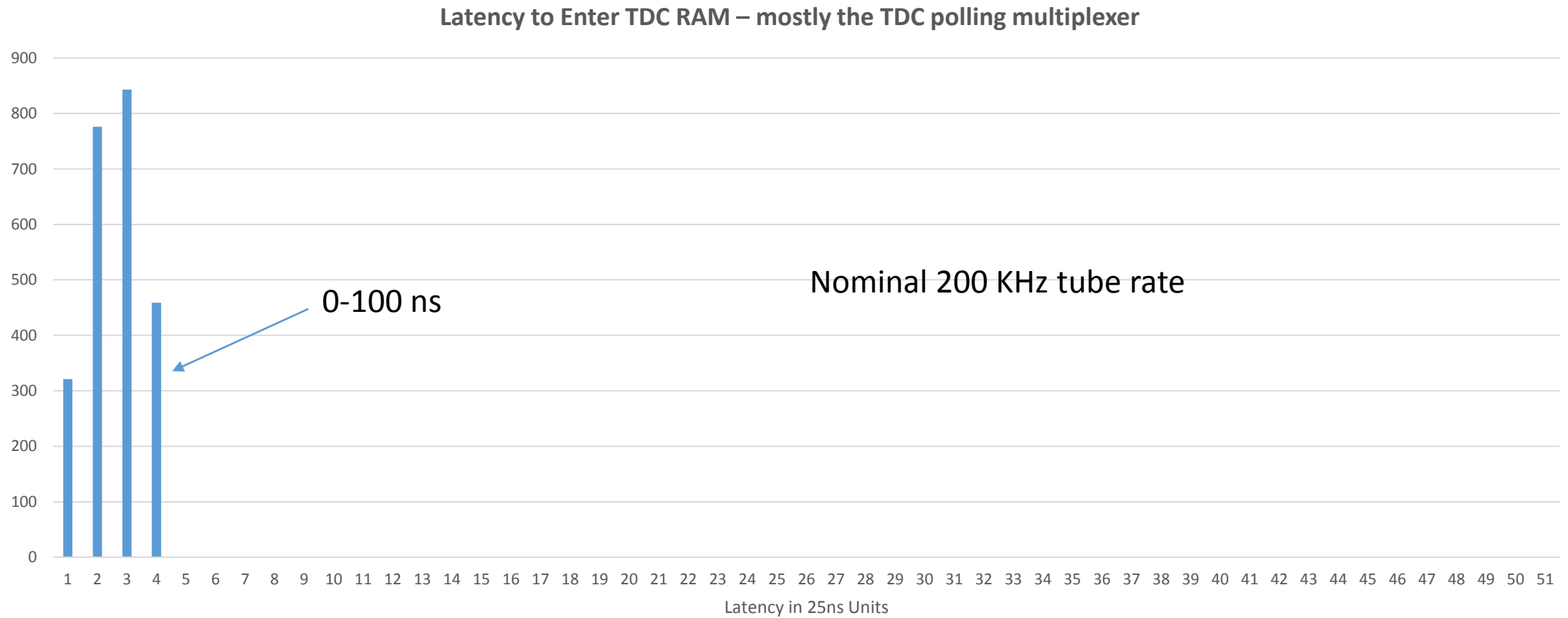
New Trigger Match in USA-15



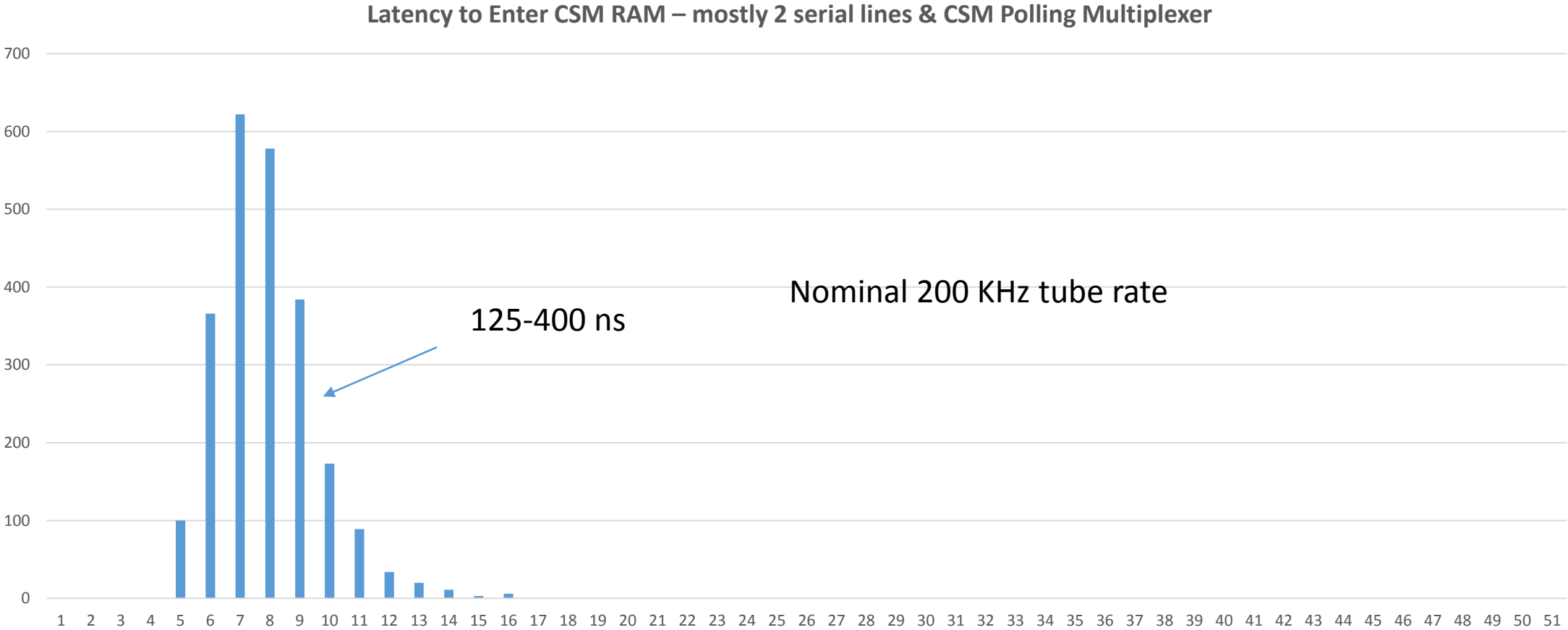
Simulation Details (4 separate entries)

- #1 Hit bcid=1 tdc=15 chan=12 sub=26 amp=21 (time #1 of hit with channel, tdc, sub-time, & amplitude)
- #2 Hit bcid=1 tdc=8 chan=18 sub=8 amp=18
- #3 Hit bcid=1 tdc=6 chan=20 sub=17 amp=12
- #4 Hit bcid=1 tdc=0 chan=19 sub=18 amp=13
- #1 Into TDC RAM=2 bcid=1 tdc=15 chan=12 sub=26 amp=21 (time #2 of entry into TDC RAM & data unit for hit as before)
- #2 Into TDC RAM=3 bcid=1 tdc=8 chan=18 sub=8 amp=18
- #4 Into TDC RAM=3 bcid=1 tdc=0 chan=19 sub=18 amp=13
- #3 Into TDC RAM=3 bcid=1 tdc=6 chan=20 sub=17 amp=12
- #1 Into CSM RAM=7 bcid=1 tdc=15 chan=12 sub=26 amp=21 (time #3 of entry into CSM RAM & data unit for hit as before)
- #4 Into CSM RAM=7 bcid=1 tdc=0 chan=19 sub=18 amp=13
- #1 Exit CSM RAM=7 bcid=1 tdc=15 chan=12 sub=26 amp=21 (time #4 of exit from CSM RAM & data unit for hit as before)
- #4 Exit CSM RAM=8 bcid=1 tdc=0 chan=19 sub=18 amp=13
- #2 Into CSM RAM=8 bcid=1 tdc=8 chan=18 sub=8 amp=18
- #2 Exit CSM RAM=9 bcid=1 tdc=8 chan=18 sub=8 amp=18
- #3 Into CSM RAM=10 bcid=1 tdc=6 chan=20 sub=17 amp=12
- #3 Exit CSM RAM=11 bcid=1 tdc=6 chan=20 sub=17 amp=12

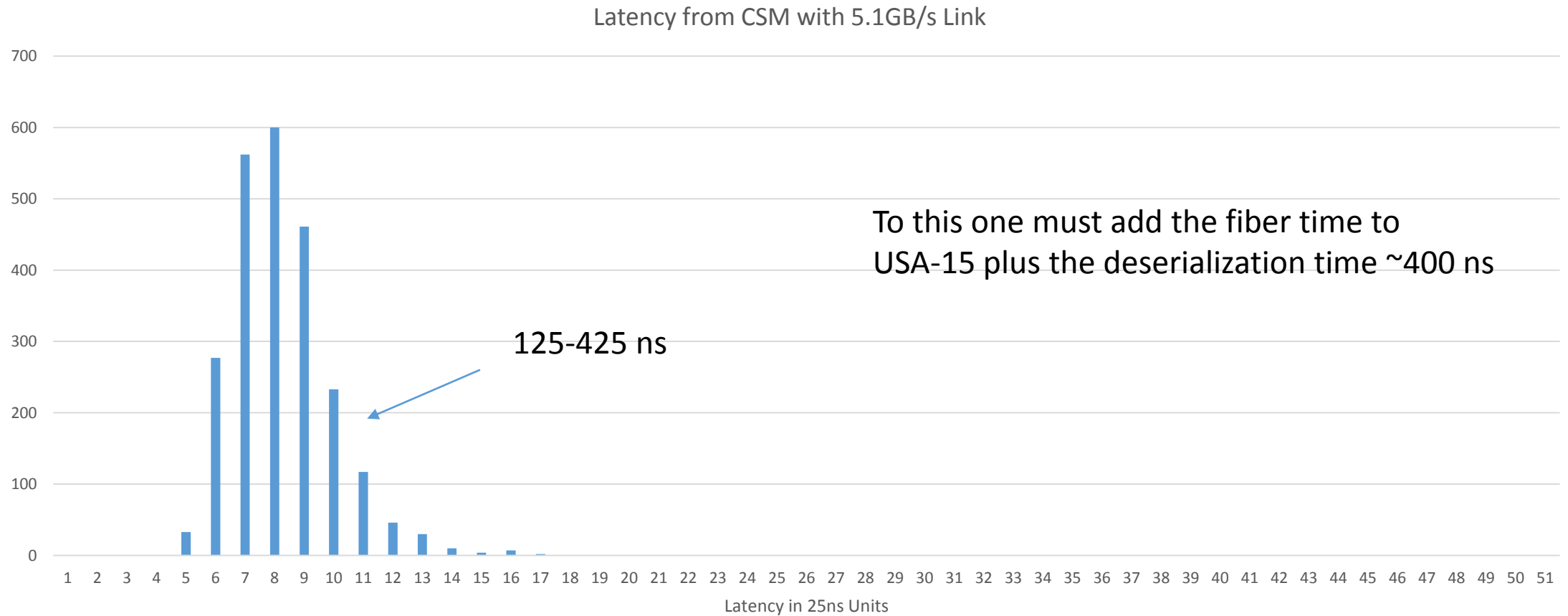
TDC Internal Latency



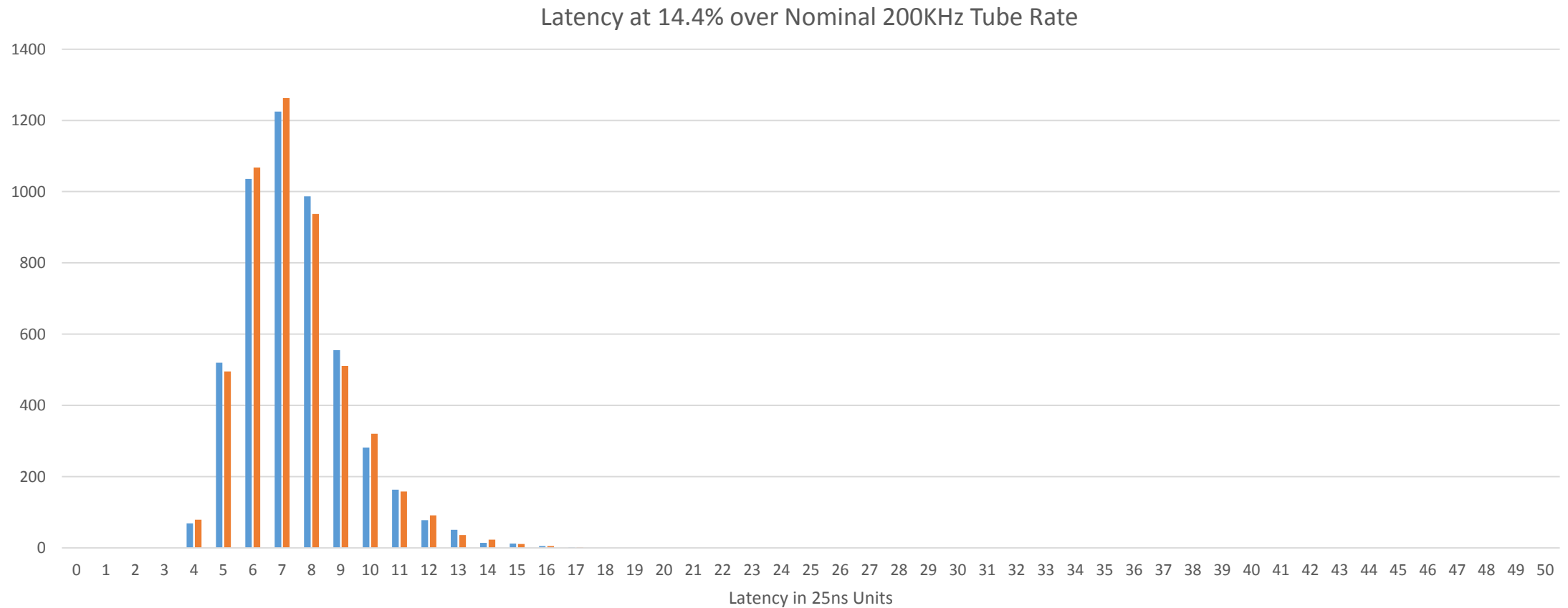
Latency to Enter CSM RAM



Latency Exiting CSM at 160MHz

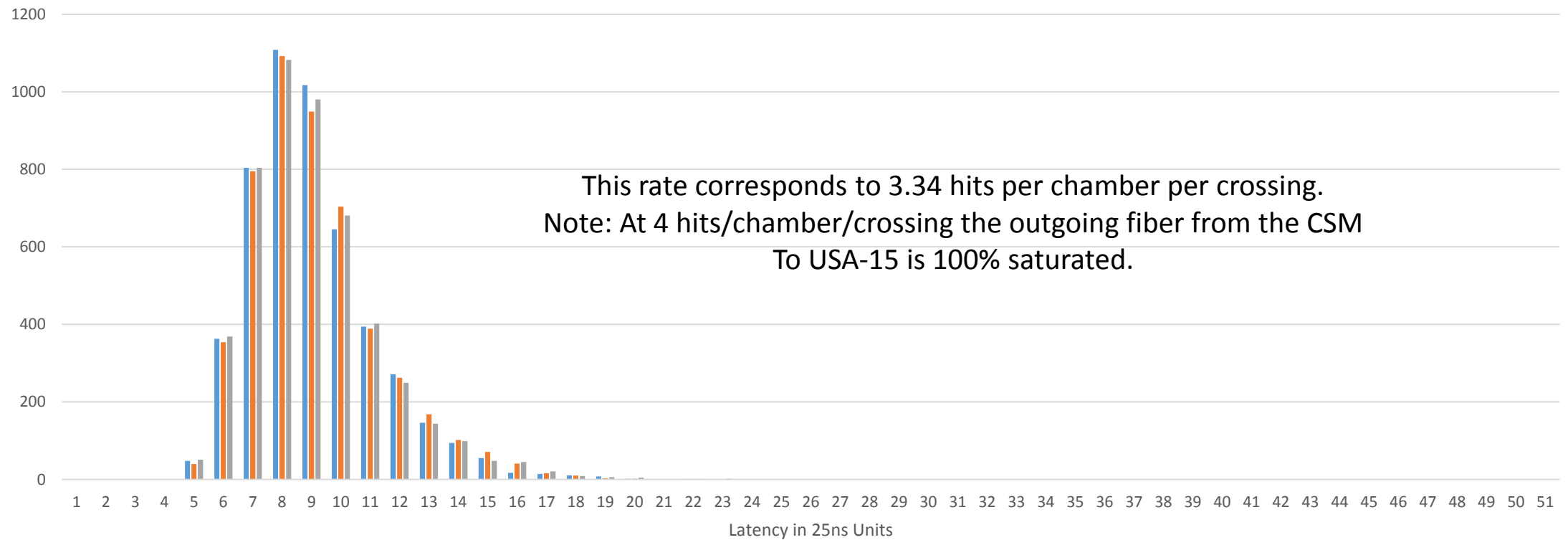


Latency after 50 μ s & 100 μ s

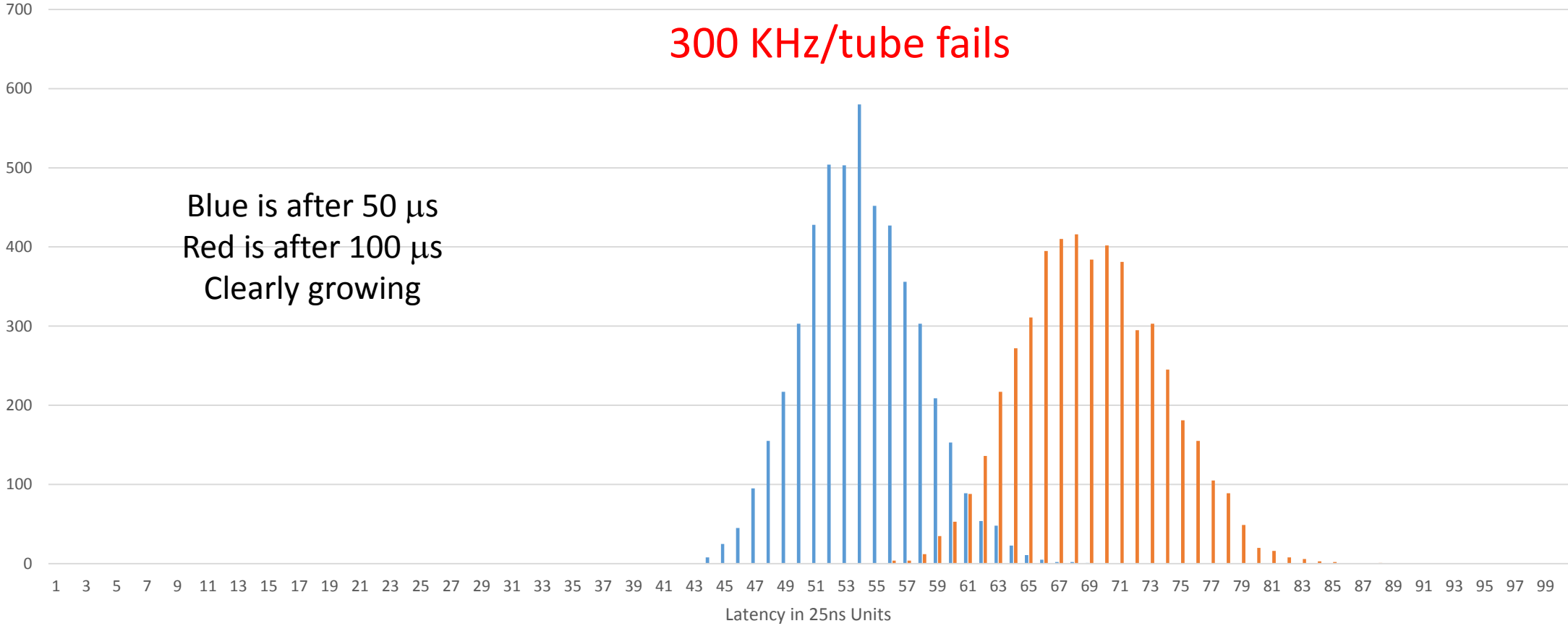


Latency after 50μs, 100μs, & 150μs

Latency at 46% over Nominal after 50μs, 100μs, & 150μs
This is the highest rate for which the latency does not grow.



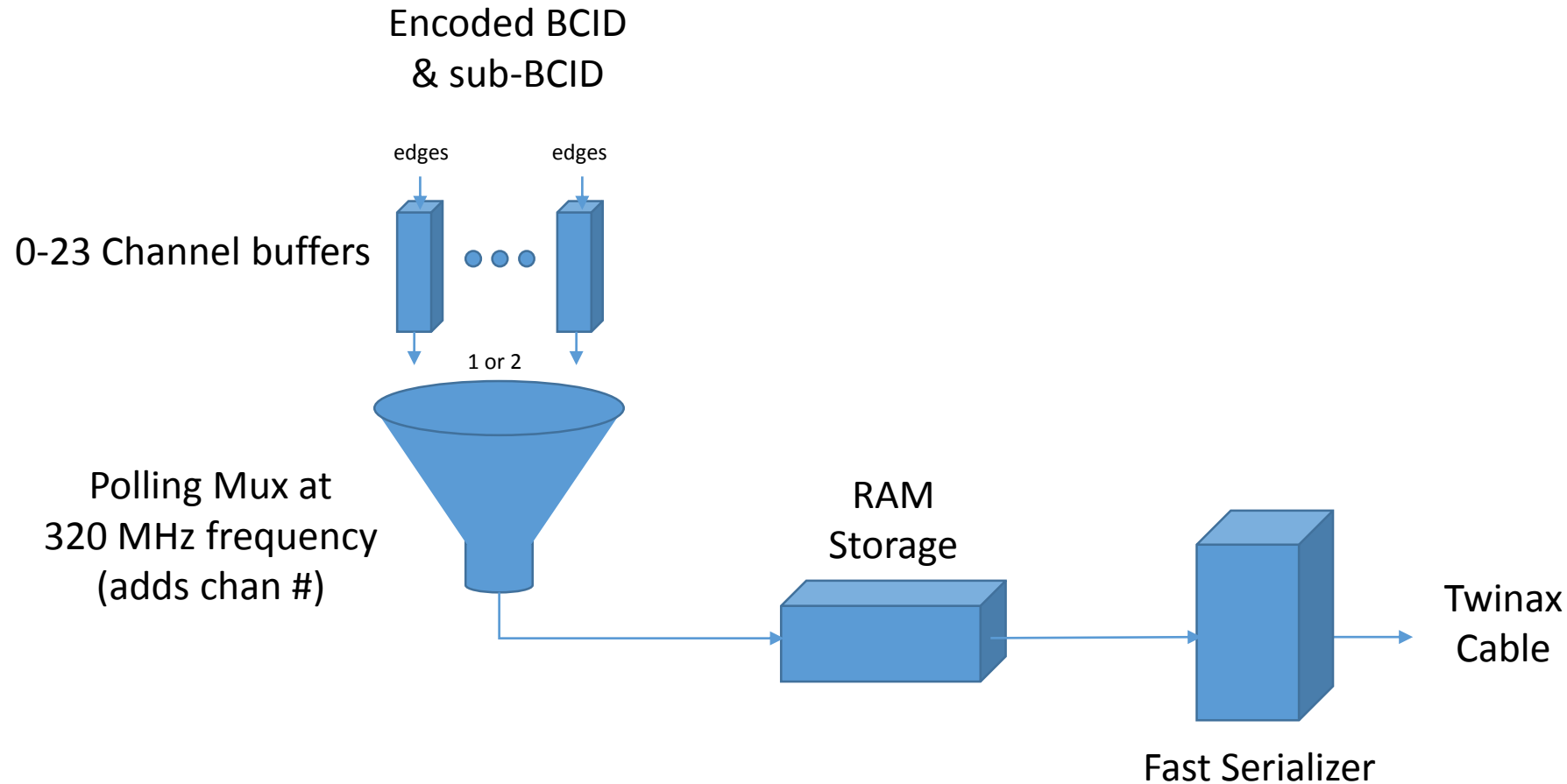
Latency for Overload Rates



What's Next for Simulation

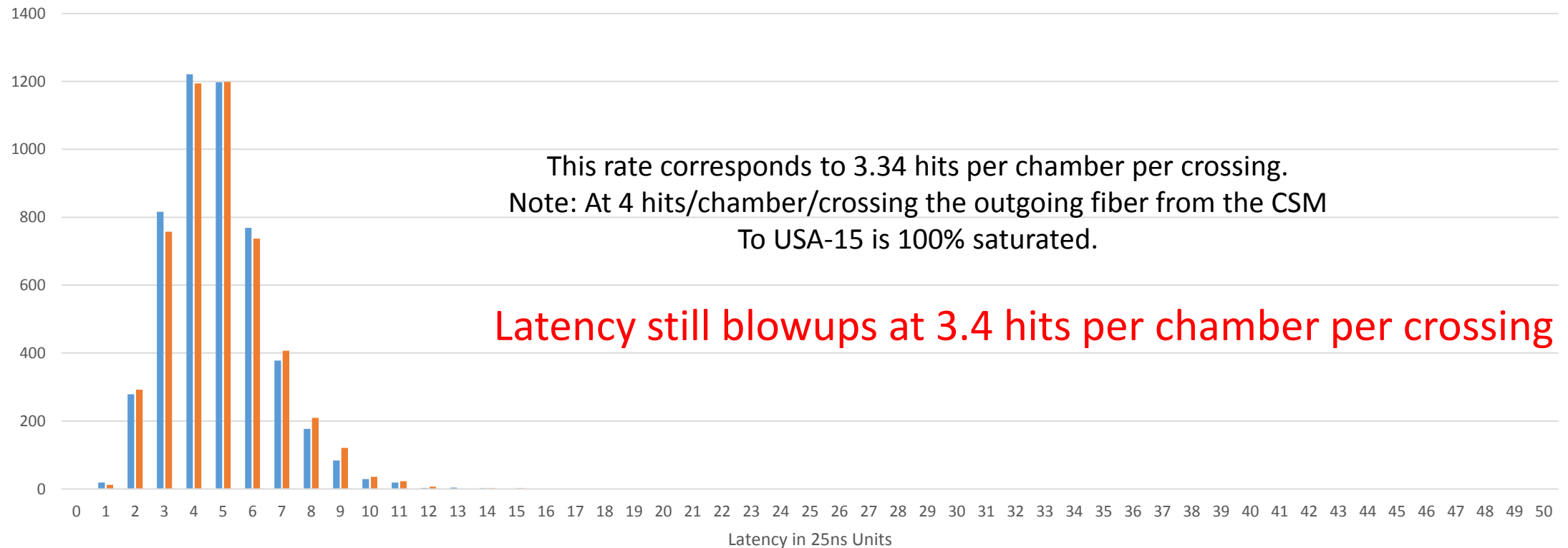
- Look at the bandwidth balance along the data flow chain
 - Tube rate max at 200 KHz/tube = 0.14 hits/crx/tdc = 2.44 hits/crx/chamber
 - 640 MB/s from each mezzanine = 11 GB/s composite rate
 - 5.1 GB/s CSM to USA-15 saturates at 4 hits per chamber per crossing
 - Note that 300 KHz/tube = 3.4 hits/crx/chamber, latency grows unbounded
- How might we go beyond 300 KHz/tube rate?
 - Change mezzanine cables to fast twinax (MiniDisplay Port)
 - Change to lpGBT at 9.6 GB/s CSM to USA-15
 - Change from polling multiplexer to token passing at TDC & CSM
 - Separate trigger & readout data paths
- We examined these options

What does this look like with Fast Serial Line?



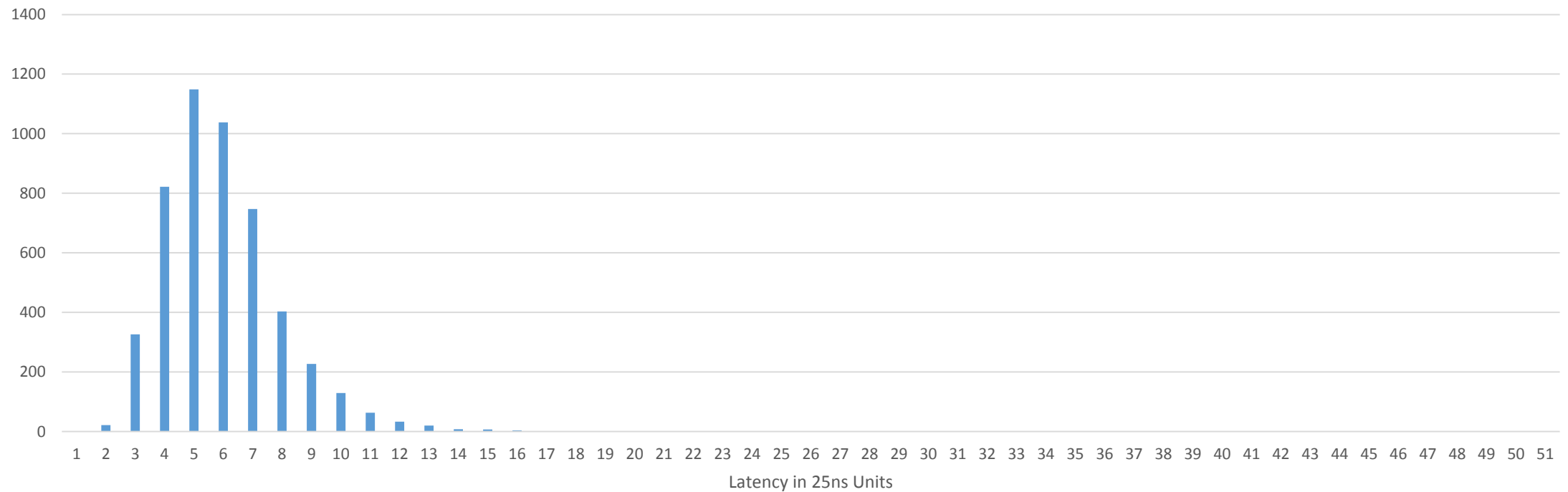
Latency after 50 μ s & 100 μ s

Latency with Fast Mezzanine to CSM cable



At 9.6 GB/s IpGBT “great” at 400 KHz/tube

Latency after 50 μ s at 2x Nominal = 400 KHz/tube
with Fast mezzanine to CSM cables

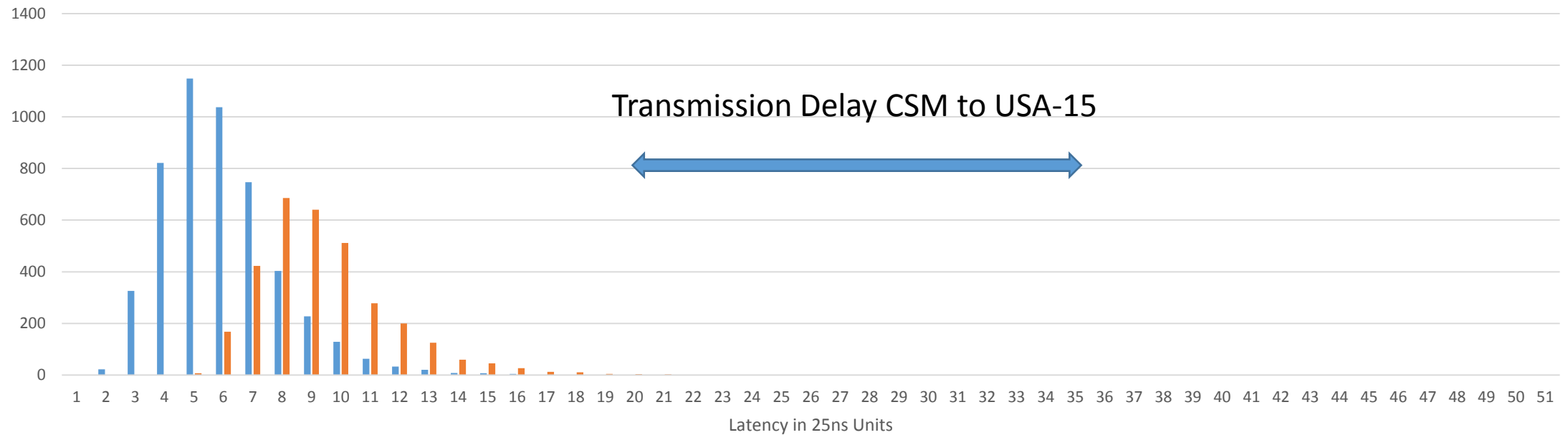


What about Existing Cables?

Latency after 50 μ s at 400 KHz/tube

blue = fast cable mezz to CSM

red=current pairs

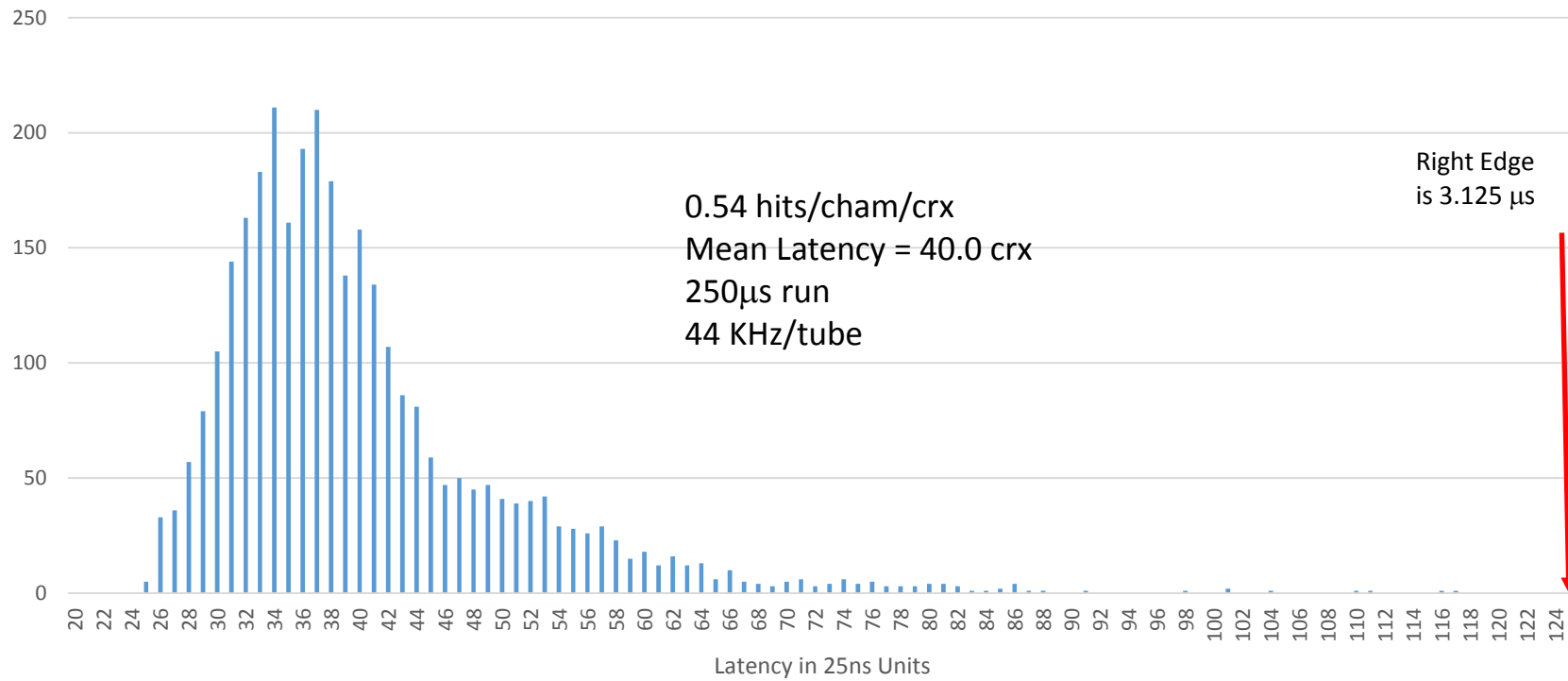


What can be done for inaccessible chambers?

- We have a test setup that can be run in “No Match Mode” (AMT)
 - L0 at MHz is not much different than reading everything.
 - Problem with encoded trigger (only every 3rd) goes away
 - Buffer overflow is likely to be less problematic since we don't hold anything.
- Read actual hardware in “No Match Mode” & determine latency
- Run the simulation at speed of current electronics to compare results
- We check latency to USA-15 for inclusion in L1 trigger match.
- The bottleneck will be the single pair mezzanine to CSM at 80 MHz.
- This is 100 KHz/tube. Simulation will tell us the maximum latency.

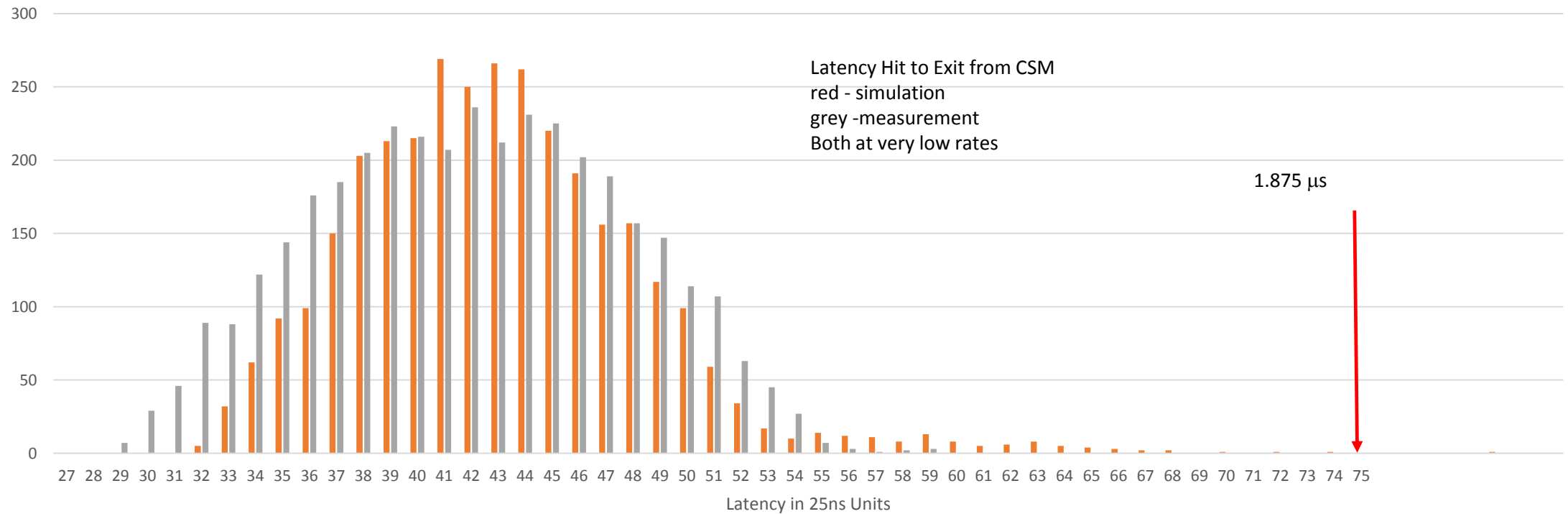
Existing Electronics in “no match mode”

Current MDT Readout Latency



Simulation & Hardware Comparison

Low Rate Comparison Hardware (Grey) &
Simulation (Red) for Current AMT System



Backup Slides

Begin with a Full Simulation for a Send-All Design

- A simulation based on HDL (hardware description language)
 - Simulate the detector output & describe how it flows clock tick by clock tick
 - Examine the buffer occupancy at each stage in the data chain
 - Calculate the transit time (latency) from the original hit to its arrival in USA-15
 - Look at the distribution of latency times for all anticipated rates
 - Note this same code can serve to develop the design once it is accepted
- Build nothing until the design meets the requirements
- Optimize the design wherever there is a bottleneck in the flow
- Target goal for Phase II needs to handle 200 KHz/tube
- Note this was done for the current MDT which behaves as simulated

Summary of Hardware Testing

- Timing summary, Triggerless
 - Serial_to_parallel at CSM complete 860-880ns (34-35)
 - Data ready at output of RAM in CSM 1160-1330ns (46-53)
 - Data presented to GOL for transmission 1700-1800ns (68-72)
 - Compare to simulation where median for low rates is at 40 (1000ns)
- Timing summary, Triggered
 - Serial_to_parallel at CSM complete 2600ns (104)
 - Data ready at output of BRAM 2900-3100ns (116-124)
 - Data presented to GOL for transmission 3500-3600ns (140-144)

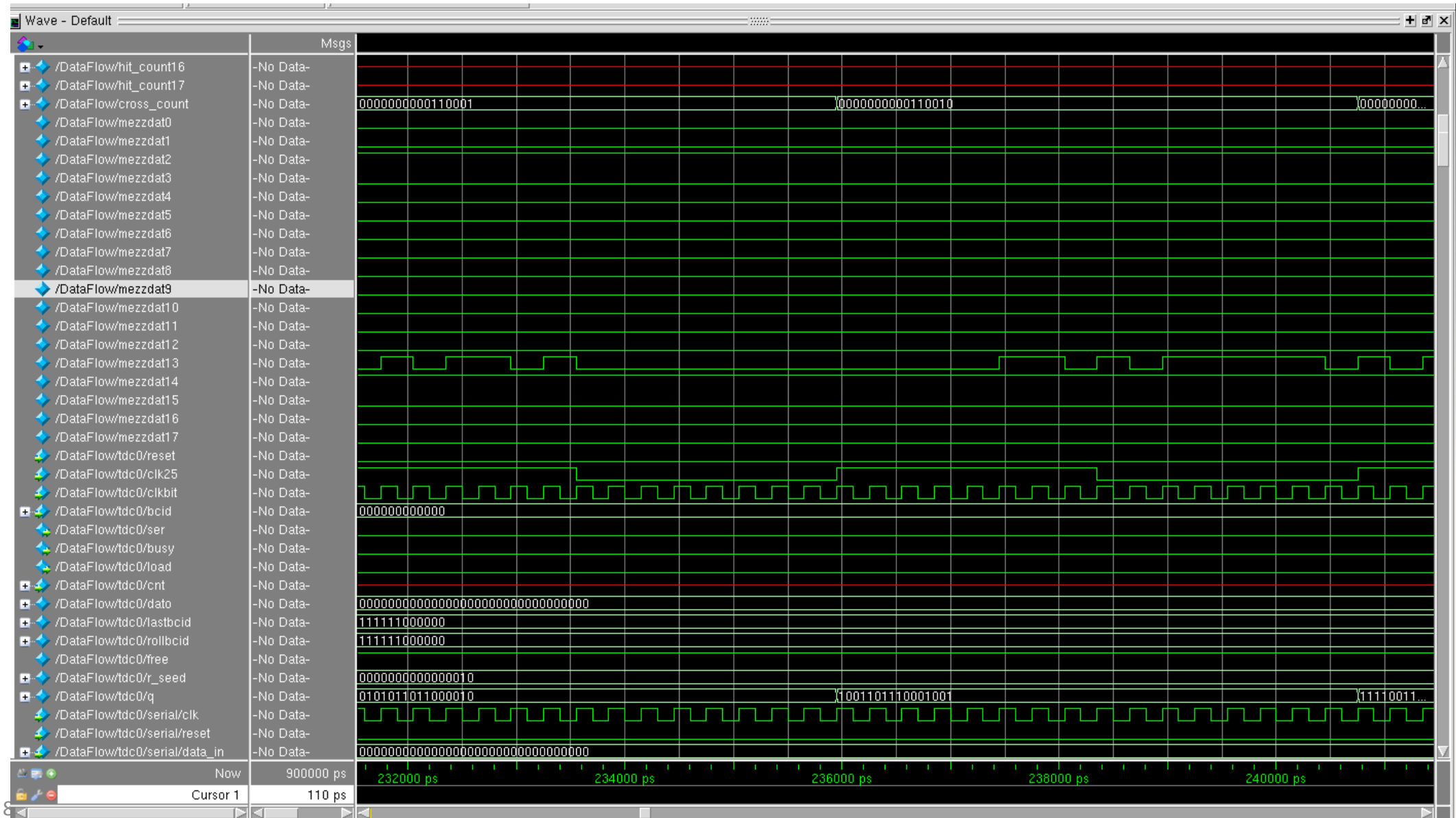
Characteristics of Simulation Runs

- First set of runs
 - Polling Multiplexers running at 320 MHz
 - Two mezzanine to CSM pairs running at 320 MB/s
 - Outgoing fiber 32- bit words loaded at 160 MHz
- Final set of runs
 - Polling Multiplexers running at 320 MHz
 - Two mezzanine to CSM pairs running at 320 MB/s
 - Outgoing fiber 32- bit words loaded at 320 MHz

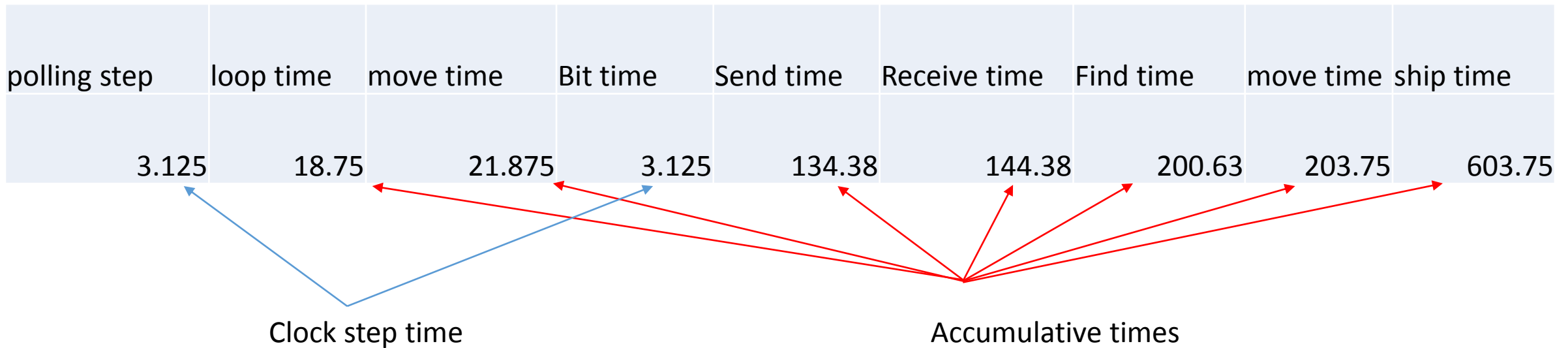
Simulate what for BIS78 is the Question?

- Others (MPI, Rome 1, Rome 2, Napoli, Bologna, & USTC)
 - system layout, mechanics, integration, trigger, station assembly and test
- UMICH 2.5 FTE out of 4 Physicists and Engineers
 - **trigger & readout simulation**, serializer, readout and DAQ
- - concerning the FE design:
 - * 8ch FE chip
 - * 2 FE chips per board
 - * 1 16 ch TDC per board
 - * 1 serializer per board – 4.8 GB/s (trigger & readout)
 - * Concerning the TDC, 32 channel HPTDC mentioned?

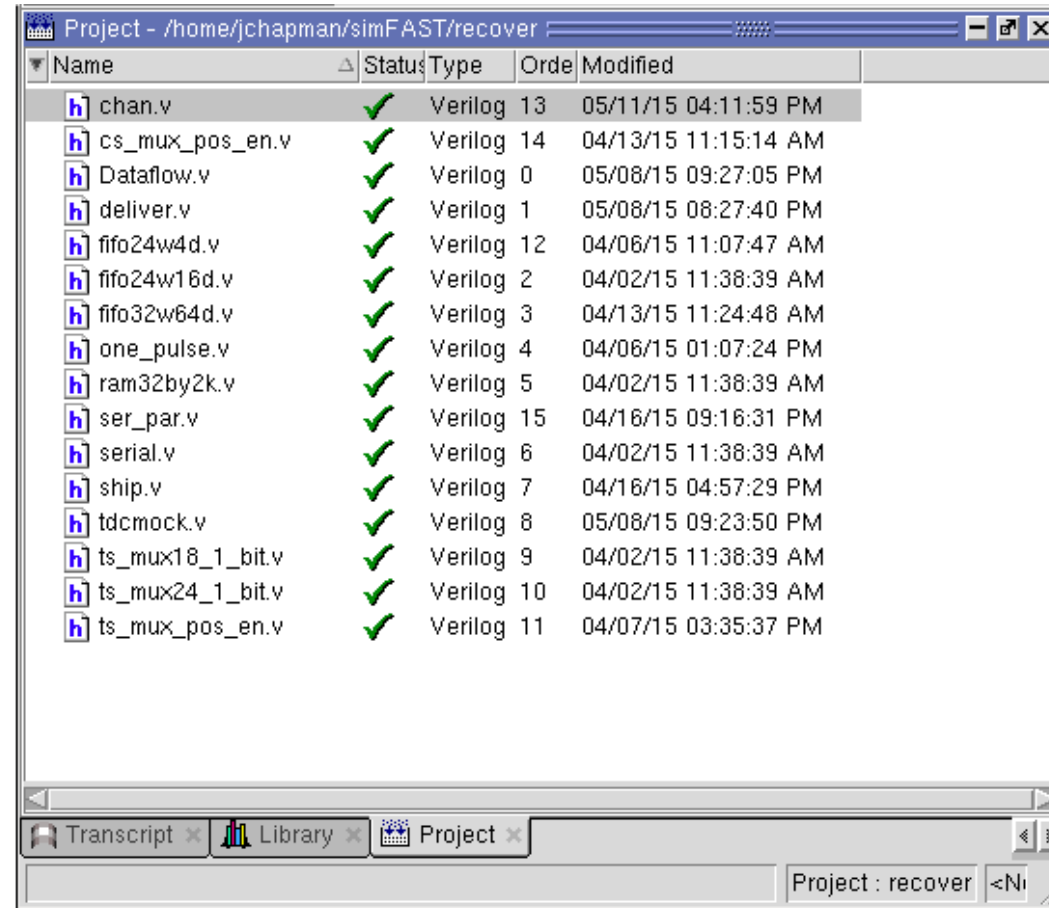
Example Screenshot



Estimate of Minimal Time (ns) to USA-15



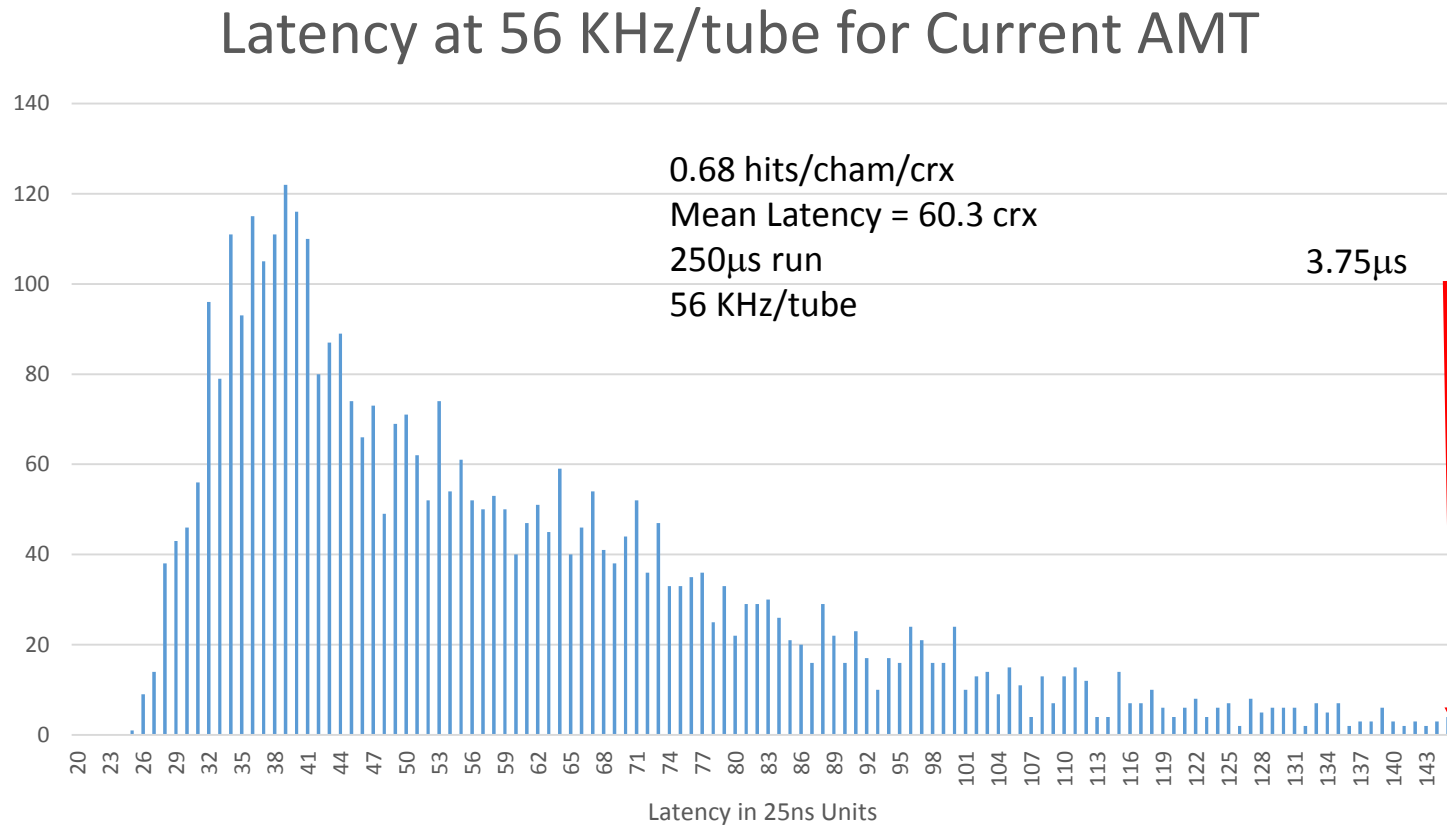
Questa Modules for Simulation



The screenshot shows the 'Project' window in the Questa tool, titled 'Project - /home/jchapman/simFAST/recover'. It displays a table of modules with columns for Name, Status, Type, Order, and Modified. All modules are Verilog files and have a green checkmark in the Status column, indicating they are ready for simulation. The modules listed are: chan.v, cs_mux_pos_en.v, Dataflow.v, deliver.v, fifo24w4d.v, fifo24w16d.v, fifo32w64d.v, one_pulse.v, ram32by2k.v, ser_par.v, serial.v, ship.v, tdcmock.v, ts_mux18_1_bit.v, ts_mux24_1_bit.v, and ts_mux_pos_en.v. The bottom of the window shows tabs for 'Transcript', 'Library', and 'Project', with 'Project' currently selected. A status bar at the bottom right indicates 'Project : recover'.

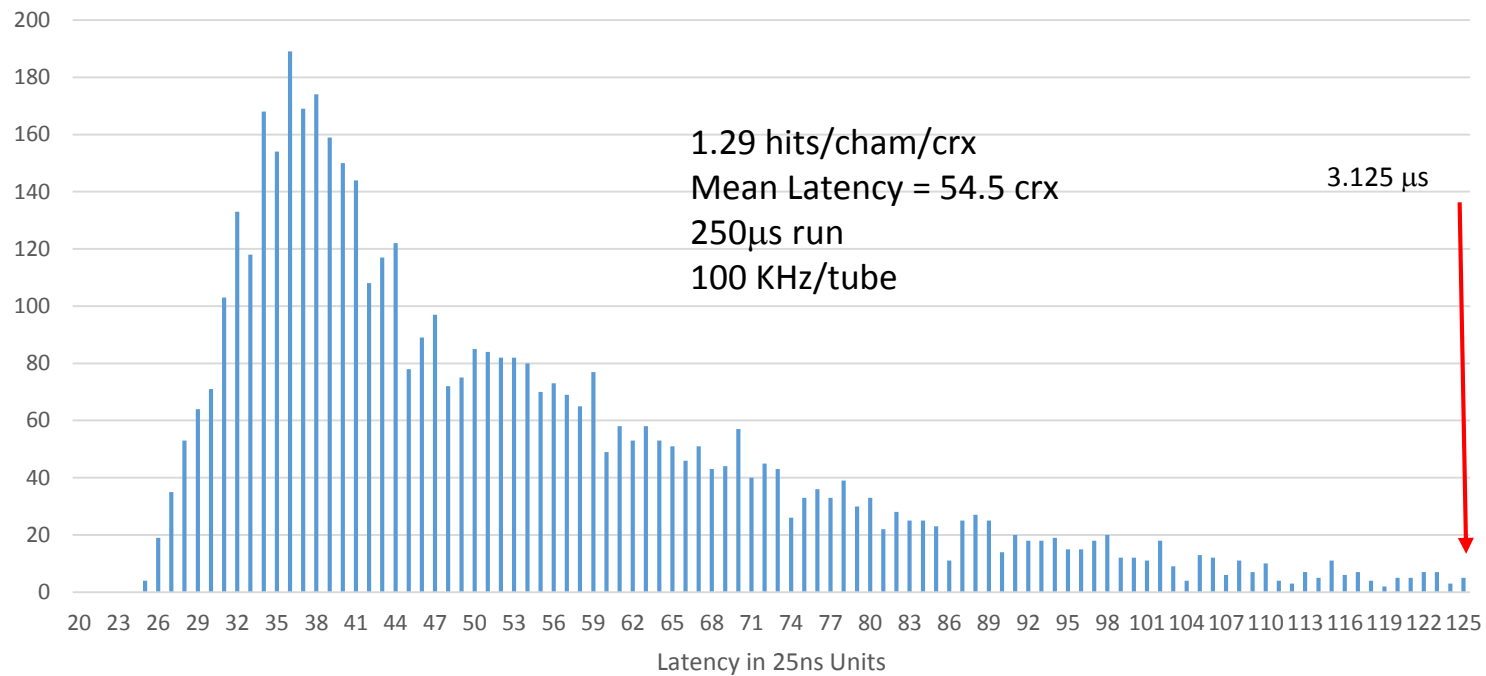
Name	Status	Type	Order	Modified
chan.v	✓	Verilog	13	05/11/15 04:11:59 PM
cs_mux_pos_en.v	✓	Verilog	14	04/13/15 11:15:14 AM
Dataflow.v	✓	Verilog	0	05/08/15 09:27:05 PM
deliver.v	✓	Verilog	1	05/08/15 08:27:40 PM
fifo24w4d.v	✓	Verilog	12	04/06/15 11:07:47 AM
fifo24w16d.v	✓	Verilog	2	04/02/15 11:38:39 AM
fifo32w64d.v	✓	Verilog	3	04/13/15 11:24:48 AM
one_pulse.v	✓	Verilog	4	04/06/15 01:07:24 PM
ram32by2k.v	✓	Verilog	5	04/02/15 11:38:39 AM
ser_par.v	✓	Verilog	15	04/16/15 09:16:31 PM
serial.v	✓	Verilog	6	04/02/15 11:38:39 AM
ship.v	✓	Verilog	7	04/16/15 04:57:29 PM
tdcmock.v	✓	Verilog	8	05/08/15 09:23:50 PM
ts_mux18_1_bit.v	✓	Verilog	9	04/02/15 11:38:39 AM
ts_mux24_1_bit.v	✓	Verilog	10	04/02/15 11:38:39 AM
ts_mux_pos_en.v	✓	Verilog	11	04/07/15 03:35:37 PM

Existing Electronics in “no match mode”



Existing Electronics in “no match mode”

Current MDT Readout Latency

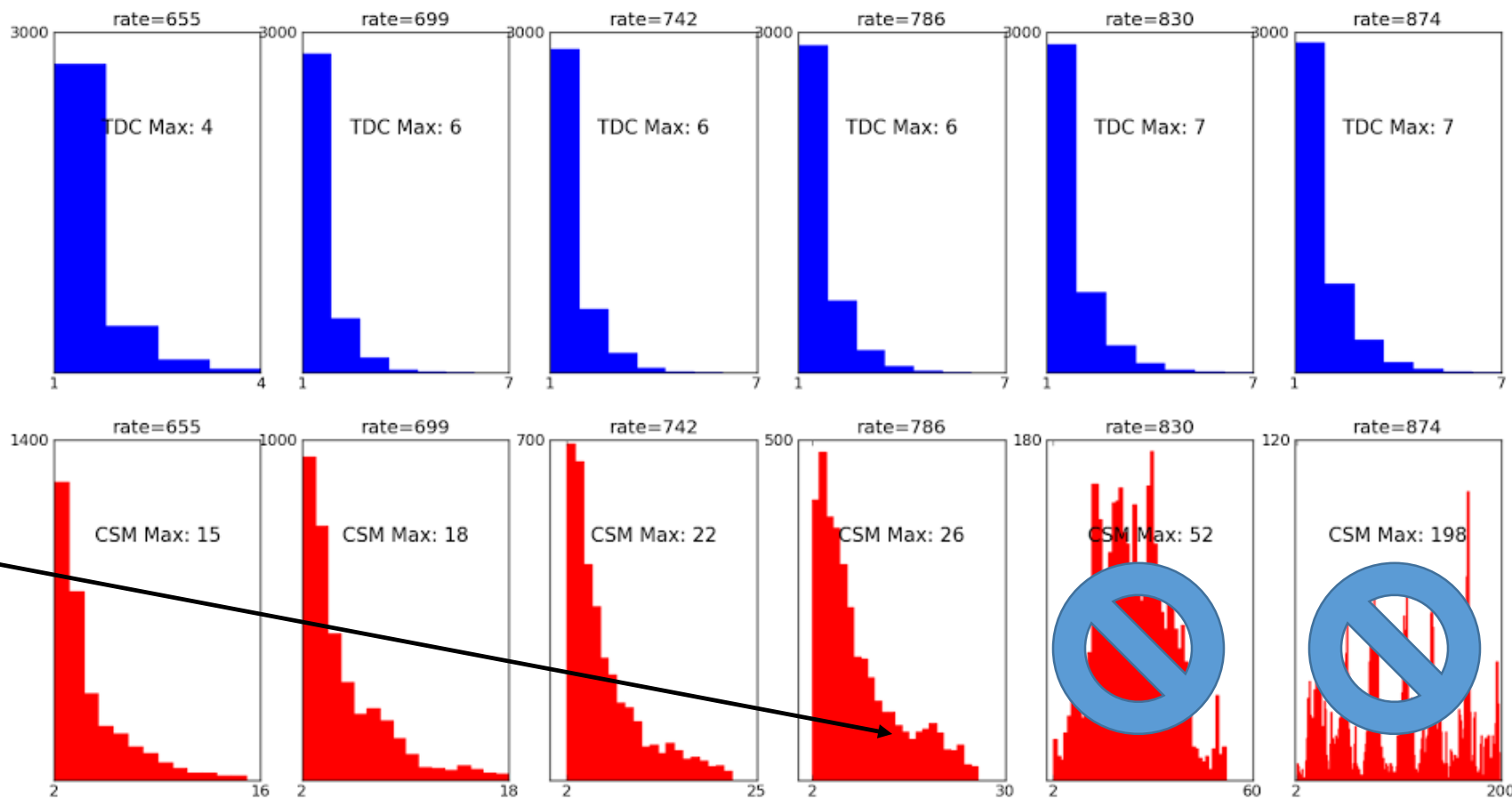


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Buffer Occupancy at 50% Above Nominal to 2x Nominal

TDC (blue) and CSM (red) Occupancy at Multiple TDC Rates, 2cbl Setup



Max Rate
is 380 KHz
per tube
limited by
outgoing
fiber