Design Study of the Options for the ATLAS Muon Drift Tube (MDT) Electronics for Phase-II

Jay Chapman, Junjie Zhu, Tom Schwarz, Aaron White, and Xianting Meng
University of Michigan, Ann Arbor
Goals (of the work & presentation)

• Characterize each design being considered for a new MDT front-end
• Simulate the latency for data arriving at USA-15 for MDT trigger
• Determine any bottlenecks in the flow of data
• Check the bandwidth available with the existing cables
• Determine the highest tube rate sustainable with each option
• Examine the capability of the current (legacy) electronics
• Show cable tests of the current mezzanine to CSM cables
Front-end Cards Now

24 Channel buffers

Polling Mux adds chan #

Mux at 80 MHz

Encoded BCID & sub-BCID

Match Circuits

Convert to drift

Level 1 Buffer Ring

Expired Hits

Output Buffer

CSM

One pair at 80 MHz bit rate

Send All Scheme
CSM (second multiplexer) Now

- Input FIFOs
- Polling Mux
- Mux at 80 MHz
- Serial rate = 80 MB/s x 18
- CSM RAM
- MRod

Serial rate = 80 MB/s x 18
Composite input rate is less than output rate
Output = 1.6 GB/s

8/5/2015
Latency in the Current CSM Readout

- Minimum time 15us

Note Date: September 1999

Can’t just run what we have

Minimum time 15us
Design Methodology for Simulation

• Not a Design but an Evaluation & Consideration of Options
• A Specific Design is considered but it is not chosen at this time
• Detailed Electronics implemented in Behavioral Verilog
• Data Rates taken from Physics MC or extrapolated measurements
• Data Movement times (Latency) evaluated for realistic data rates
  • Starting time represented as BCID + sub-BCID (0.78ns) at it arrival #1
  • Ending time represented as BCID when hit handed off to fiber driver #4
  • For complete transit time need to add fiber transit time and receiver time
• Data Buffer requirements evaluated
Why Consider Send-Immediately Design

• The ~800ns MDT drift time & 1 MHz L0 trigger selects everything!
  • Current design selects a 1µs window each trigger. Overlaps read same hits!
• A single path for trigger & data is simple if fast enough.
• Current mezzanines send data on one pair at 80 MHz bit rate
• Cables have 2 pairs available: Will show test to 320 MHz
• Generate random hits at rates up to 400 KHz/tube
  • Multiplex these hits from 24 channels into RAM and onto 2 pairs to CSM
  • Receive & multiplex the 18 mezzanines into CSM RAM & onto fast fiber
• Examine the distribution of transfer times, hit time to fiber entry
• Determine the highest tube rate that can be sustained
Current Cables Tested to 320MHz
Setup for BER test

- Kintex-7 Evaluation board used as a Bit Error Ratio (BER) Tester.
- CSM cable test board is used for cable test interfaces. Four differential pairs(CH1-CH4) of cable can be tested at the same time by using test board.
- Cable’s length is 1.33 m.
**Eye diagram measurements for 1.33m cable**

- At the beginning, we tested CH1’s eye diagram. No data transmission in other channels.
- Next, tested CH1’s eye diagram again. This time, there is data transmission in CH2 at the speed of 320Mbps and no data transmission in CH3 and CH4.
- Even if data transmit in CH2 at 320Mbps, CH1’s eye diagram is also good.

[Images of eye diagrams: one showing CH1’s eye diagram with no data transmit in CH2, and another showing CH1’s eye diagram with data transmit in CH2 at the speed of 320Mbps.]
We have run the BER test program in four channels with different data pattern at the speed of 320Mbps about 67 hours.

Results are listed below:

<table>
<thead>
<tr>
<th>Channel</th>
<th>Data pattern</th>
<th>Polynomial</th>
<th>Data bits</th>
<th>Errors</th>
<th>BER</th>
</tr>
</thead>
<tbody>
<tr>
<td>CH1</td>
<td>PRBS31</td>
<td>$X^{31}+X^{28}+1$</td>
<td>$7.76\times10^{13}$</td>
<td>0</td>
<td>$1.29\times10^{-14}$</td>
</tr>
<tr>
<td>CH2</td>
<td>PRBS31</td>
<td>$X^{31}+X^{29}+1$</td>
<td>$7.76\times10^{13}$</td>
<td>0</td>
<td>$1.29\times10^{-14}$</td>
</tr>
<tr>
<td>CH3</td>
<td>PRBS29</td>
<td>$X^{29}+X^{27}+1$</td>
<td>$7.76\times10^{13}$</td>
<td>0</td>
<td>$1.29\times10^{-14}$</td>
</tr>
<tr>
<td>CH4</td>
<td>PRBS23</td>
<td>$X^{23}+X^{18}+1$</td>
<td>$7.76\times10^{13}$</td>
<td>0</td>
<td>$1.29\times10^{-14}$</td>
</tr>
</tbody>
</table>
Design Considered in Simulation

0-23 Channel buffers

Polling Mux at 320 MHz frequency (adds chan #)

Hit Time #1

Encoded BCID & sub-BCID

Routing on 2 lines

Into TDC RAM Time #2

Output Buffer

Pair #1 To CSM

Output Buffer

Pair #2 To CSM

Send All Scheme
New CSM, Much the Same

From 18 Mezzanine
On 2 lines each
Serial In
Serial In

Input FIFOs
Polling Mux

Into CSM RAM
Time #3

RAM Buffer
USA-15 Fiber
Exit CSM RAM
Time #4

Send All Scheme
New Trigger Match in USA-15

- Polling Mux
  - Encoded BCID & sub-BCID with source Mezz # & Chan # From Fibers

- Level 0 Buffer Ring
  - Level 0 trigger
  - In
  - Out
  - Expired Hits

- Level 1 Buffer Ring
  - In
  - Out
  - Expired Hits

- Low Precision Drift Times To Sector Logic

- Level 1 trigger

- To Felix

- Level 1 trigger

- Match Circuits

- Send All Scheme
Simulation Details (4 separate entries)

- **#1** Hit bcid=1 tdc=15 chan=12 sub=26 amp=21 (time #1 of hit with channel, tdc, sub-time, & amplitude)
- **#2** Hit bcid=1 tdc=8 chan=18 sub=8 amp=18
- **#3** Hit bcid=1 tdc=6 chan=20 sub=17 amp=12
- **#4** Hit bcid=1 tdc=0 chan=19 sub=18 amp=13
- **#1** Into TDC RAM=2 bcid=1 tdc=15 chan=12 sub=26 amp=21 (time #2 of entry into TDC RAM & data unit for hit as before)
- **#2** Into TDC RAM=3 bcid=1 tdc=8 chan=18 sub=8 amp=18
- **#4** Into TDC RAM=3 bcid=1 tdc=0 chan=19 sub=18 amp=13
- **#3** Into TDC RAM=3 bcid=1 tdc=6 chan=20 sub=17 amp=12
- **#1** Into CSM RAM=7 bcid=1 tdc=15 chan=12 sub=26 amp=21 (time #3 of entry into CSM RAM & data unit for hit as before)
- **#4** Into CSM RAM=7 bcid=1 tdc=0 chan=19 sub=18 amp=13
- **#1** Exit CSM RAM=7 bcid=1 tdc=15 chan=12 sub=26 amp=21 (time #4 of exit from CSM RAM & data unit for hit as before)
- **#4** Exit CSM RAM=8 bcid=1 tdc=0 chan=19 sub=18 amp=13
- **#2** Into CSM RAM=8 bcid=1 tdc=8 chan=18 sub=8 amp=18
- **#2** Exit CSM RAM=9 bcid=1 tdc=8 chan=18 sub=8 amp=18
- **#3** Into CSM RAM=10 bcid=1 tdc=6 chan=20 sub=17 amp=12
- **#3** Exit CSM RAM=11 bcid=1 tdc=6 chan=20 sub=17 amp=12
TDC Internal Latency

Latency to Enter TDC RAM – mostly the TDC polling multiplexer

0-100 ns

Nominal 200 KHz tube rate
Latency to Enter CSM RAM – mostly 2 serial lines & CSM Polling Multiplexer

Latency to Enter CSM RAM

Nominal 200 KHz tube rate

125-400 ns
Latency Exiting CSM at 160MHz

Latency from CSM with 5.1GB/s Link

To this one must add the fiber time to USA-15 plus the deserialization time ~400 ns

125-425 ns
Latency after 50µs & 100µs

Latency at 14.4% over Nominal 200KHz Tube Rate
Latency after 50µs, 100µs, & 150µs

Latency at 46% over Nominal after 50µs, 100µs, & 150µs
This is the highest rate for which the latency does not grow.

This rate corresponds to 3.34 hits per chamber per crossing.
Note: At 4 hits/chamber/crossing the outgoing fiber from the CSM To USA-15 is 100% saturated.
Latency for Overload Rates

300 KHz/tube fails

Blue is after 50 μs
Red is after 100 μs
Clearly growing
What’s Next for Simulation

• Look at the bandwidth balance along the data flow chain
  • Tube rate max at 200 KHz/tube = 0.14 hits/crx/tdc = 2.44 hits/crx/chamber
  • 640 MB/s from each mezzanine = 11 GB/s composite rate
  • 5.1 GB/s CSM to USA-15 saturates at 4 hits per chamber per crossing
  • Note that 300 KHz/tube = 3.4 hits/crx/chamber, latency grows unbounded

• How might we go beyond 300 KHz/tube rate?
  • Change mezzanine cables to fast twinax (MiniDisplay Port)
  • Change to lpGBT at 9.6 GB/s CSM to USA-15
  • Change from polling multiplexer to token passing at TDC & CSM
  • Separate trigger & readout data paths

• We examined these options
What does this look like with Fast Serial Line?

- 0-23 Channel buffers
- Encoded BCID & sub-BCID
- Polling Mux at 320 MHz frequency (adds chan #)
- RAM Storage
- Fast Serializer
- Twinax Cable

Send All Scheme
Latency after 50µs & 100µs

Latency with Fast Mezzanine to CSM cable

This rate corresponds to 3.34 hits per chamber per crossing. 
Note: At 4 hits/chamber/crossing the outgoing fiber from the CSM To USA-15 is 100% saturated.

Latency still blowups at 3.4 hits per chamber per crossing
At 9.6 GB/s lpGBT “great” at 400 KHz/tube

Latency after 50μs at 2x Nominal = 400 KHz/tube with Fast mezzanine to CSM cables
What about Existing Cables?

Latency after 50µs at 400 KHz/tube
blue = fast cable mezz to CSM
red=current pairs

Transmission Delay CSM to USA-15
What can be done for inaccessible chambers?

• We have a test setup that can be run in “No Match Mode” (AMT)
  • L0 at MHz is not much different than reading everything.
  • Problem with encoded trigger (only every 3\textsuperscript{rd}) goes away
  • Buffer overflow is likely to be less problematic since we don’t hold anything.
• Read actual hardware in “No Match Mode” & determine latency
• Run the simulation at speed of current electronics to compare results
• We check latency to USA-15 for inclusion in L1 trigger match.
• The bottleneck will be the single pair mezzanine to CSM at 80 MHz.
• This is 100 KHz/tube. Simulation will tell us the maximum latency.
Existing Electronics in “no match mode”

Current MDT Readout Latency

- 0.54 hits/cham/crx
- Mean Latency = 40.0 crx
- 250μs run
- 44 KHz/tube

Right Edge is 3.125 μs
Simulation & Hardware Comparison

Low Rate Comparison Hardware (Grey) & Simulation (Red) for Current AMT System

Latency Hit to Exit from CSM
- red - simulation
- grey - measurement
Both at very low rates

1.875 μs
Backup Slides
Begin with a Full Simulation for a Send-All Design

• A simulation based on HDL (hardware description language)
  • Simulate the detector output & describe how it flows clock tick by clock tick
  • Examine the buffer occupancy at each stage in the data chain
  • Calculate the transit time (latency) from the original hit to its arrival in USA-15
  • Look at the distribution of latency times for all anticipated rates
  • Note this same code can serve to develop the design once it is accepted

• Build nothing until the design meets the requirements

• Optimize the design wherever there is a bottleneck in the flow

• Target goal for Phase II needs to handle 200 KHz/tube

• Note this was done for the current MDT which behaves as simulated
Summary of Hardware Testing

• Timing summary, Triggerless
  • Serial_to_parallel at CSM complete 860-880ns (34-35)
  • Data ready at output of RAM in CSM 1160-1330ns (46-53)
  • Data presented to GOL for transmission 1700-1800ns (68-72)
  • Compare to simulation where median for low rates is at 40 (1000ns)

• Timing summary, Triggered
  • Serial_to_parallel at CSM complete 2600ns (104)
  • Data ready at output of BRAM 2900-3100ns (116-124)
  • Data presented to GOL for transmission 3500-3600ns (140-144)
Characteristics of Simulation Runs

• First set of runs
  • Polling Multiplexers running at 320 MHz
  • Two mezzanine to CSM pairs running at 320 MB/s
  • Outgoing fiber 32- bit words loaded at 160 MHz

• Final set of runs
  • Polling Multiplexers running at 320 MHz
  • Two mezzanine to CSM pairs running at 320 MB/s
  • Outgoing fiber 32- bit words loaded at 320 MHz
Simulate what for BIS78 is the Question?

- Others (MPI, Rome 1, Rome 2, Napoli, Bologna, & USTC)
  - system layout, mechanics, integration, trigger, station assembly and test

- UMICH 2.5 FTE out of 4 Physicists and Engineers
  - trigger & readout simulation, serializer, readout and DAQ

- concerning the FE design:
  - * 8ch FE chip
  - * 2 FE chips per board
  - * 1 16 ch TDC per board
  - * 1 serializer per board – 4.8 GB/s (trigger & readout)
  - * Concerning the TDC, 32 channel HPTDC mentioned?
Estimate of Minimal Time (ns) to USA-15

<table>
<thead>
<tr>
<th>polling step</th>
<th>loop time</th>
<th>move time</th>
<th>Bit time</th>
<th>Send time</th>
<th>Receive time</th>
<th>Find time</th>
<th>move time</th>
<th>ship time</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.125</td>
<td>18.75</td>
<td>21.875</td>
<td>3.125</td>
<td>134.38</td>
<td>144.38</td>
<td>200.63</td>
<td>203.75</td>
<td>603.75</td>
</tr>
</tbody>
</table>

Clock step time  
Accumulative times
Questa Modules for Simulation
Existing Electronics in “no match mode”

Latency at 56 KHz/tube for Current AMT

0.68 hits/cham/crx
Mean Latency = 60.3 crx
250μs run
56 KHz/tube

Latency in 25ns Units

3.75μs
Existing Electronics in “no match mode”

Current MDT Readout Latency

- 1.29 hits/cham/crx
- Mean Latency = 54.5 crx
- 250μs run
- 100 KHz/tube

Latency in 25ns Units
What’s Next for Simulation

• Look at the bandwidth balance along the data flow chain
  • Tube rate max at 200 KHz/tube = 0.14 hits/crx/tdc = 2.44 hits/crx/chamber
  • 640 MB/s from each mezzanine = 11 GB/s composite rate
  • 5.1 GB/s CSM to USA-15 saturates at 4 hits per chamber per crossing
  • Note that 300 KHz/tube = 3.4 hits/crx/chamber, latency grows unbounded

• How might we go beyond 300 KHz/tube rate?
  • Change mezzanine cables to fast twinax (MiniDisplay Port)
  • Change to lpGBT at 9.6 GB/s CSM to USA-15
  • Change from polling multiplexer to token passing at TDC & CSM
  • Separate trigger & readout data paths

• We are examining these options
Buffer Occupancy at 50% Above Nominal to 2x Nominal

Max Rate is 380 KHz per tube limited by outgoing fiber