PILOT SYSTEM FOR THE CMS PHASE I PIXEL UPGRADE

Robert Stringer, on behalf of the CMS Collaboration
Phase I Upgrade to be installed end 2016/early 2017

- Adds 4th barrel layer and 3rd forward disk.
- Features new digital readout system
- New digital ROC has larger buffer (for PU)
- Smaller beampipe (22.5mm)
Pilot System Goals

- Validate new Digital Readout system.
  - More pixels and higher occupancy

- New powering scheme
  - DC-DC conversion

- Development of the online software
  - Validate operation using the CMS infrastructure

- Phase 1 Pixel Detector will be installed during extended technical stop
  - DAQ system must be ready to take data immediately
PSI46dig Read Out Chip (ROC)

- Based on the original Pixel ROC
  - Now with 8-bit readout ADC
  - Designed for higher LHC luminosity ($2 \times 10^{34}$)
  - Larger Buffer
    - 32 -> 80
    - Reduced min. threshold of 1600e (previously 3400e)
  - 160 Mb/s digital readout
High Rate Performance

- Simulated
- Xray Testing
- Prototype Modules agree with simulation

Avg. Hit Rate for Disk 3:
\(~100\, \text{MHz/cm}^2\)
Pilot System contains 8 Phase 1 Pixel Modules
- Token Bit Manager (TBM08b) (Rutgers)
- High Density Interconnect (HDI) (Fermilab)
- PSI46dig ROC (PSI)
- Produced at UNL & Purdue
- Tested at:
  - Fermilab
  - UIC & KU (X-ray)
Infrastructure exists for 3rd forward disk in present detector

- Cooling, Power, etc..
- One pilot assembly inserted in each end.
  - 2 Blades
  - 4 Modules
- VME based readout using modified Pixel Front End Driver (FED)
  - Two Deserializer “Piggy” Cards
    - Each with Zarlink 12-ch optical receiver
Power

- One assembly powered by DC-DC converter
- DC-DC mount board (Femilab)
  - 4 Converters per board
- FEAST2 ASIC DC-DC converters (CERN & Aachen)
  - Digital: 10V->3V
  - Analog: 10V->2.4V
- Two converters power 4 modules
- Other converters used for SEU study in LHC environment

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Optical Links

- Pilot Port Cards
  - New QPLL
    - Reduces Jitter
    - Good “Eye”

400 Mb/s signal w/100 KHz triggers
Installation

- Pilot System installed in December 2014
  - Readout tests and calibration have begun
Calibration

- Calibration has been performed
  - “PixelAlive” test confirms readout is working
  - Charge is injected, efficiency measured

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New software has been developed for digital readout
- New FED
- New Deserializer

New control systems added
- Control DC-DC Converters
- New powering sequences

Modified calibration algorithms
- Analog link replaced by digital link
Pilot Detector has been included in MC simulations.
Efficiency will be measured using reconstructed tracks.
Test tracking algorithm with additional hits.
Phase 1 Upgrade will feature new DAQ system based on μTCA architecture.

Phase 1 Readout use new Common Tracker AMC (CTA) board.

- Virtex 7 FPGA
- 2x12-ch optical receivers on mezzanine board
µTCA

- µTCA crate to be installed during TS2
  - Parasitic operation w/VME
    (Oct '15)

- Full µTCA operation
  - In Central DAQ (Nov '15)
    - Compare VME & µTCA
  - Operation under µTCA
    (Jan '16-Nov '16)
Summary

- Pilot Blade System provides an opportunity to test Phase I technologies in the experiment
  - Gain experience in operation
  - Reduce downtime after installing Phase I Pixel
- New TBM, ROCs, digital readout
  - Larger buffers for high pile-up
  - Tested at high rate
- New powering scheme
  - DC-DC converters
- DAQ system will move to μTCA at the end of the year
- Will take collision data in LHC Run 2
Backup
Phase I $\mu$TCA Readout

- **Forward Pixels**
  - 14 ch (x672)
  - FPix Modules
    - TBM08c
    - HDI
    - 2x8 ROCs
  - 3 disks/side Double-sided Blades:
    - 22 inner/34 outer

- **Half Disks**
  - DC-DC
  - x(4) CCU

- **Service Cylinders**
  - Dual Port Card (A)
  - Port Card (B)
  - 7ch POH
  - 7ch PD OH

- **USC Racks $\mu$TCA**
  - 12ch fiber ribbons
  - (FPix+BPix)
  - 2x10 Gbps
  - Central DAQ
  - AMC13 (2+4)

- **Other**
  - Clk, L1A
  - TTS
  - TCDS (1+1)

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Pilot Power Supplies

- Modified Pixel Power Supplies
  - 10V output to DC-DC board
- Second assembly uses unmodified supply