A Level-1 Track Trigger for the CMS Phase 2 Upgrade

Brian Winer
The Ohio State University

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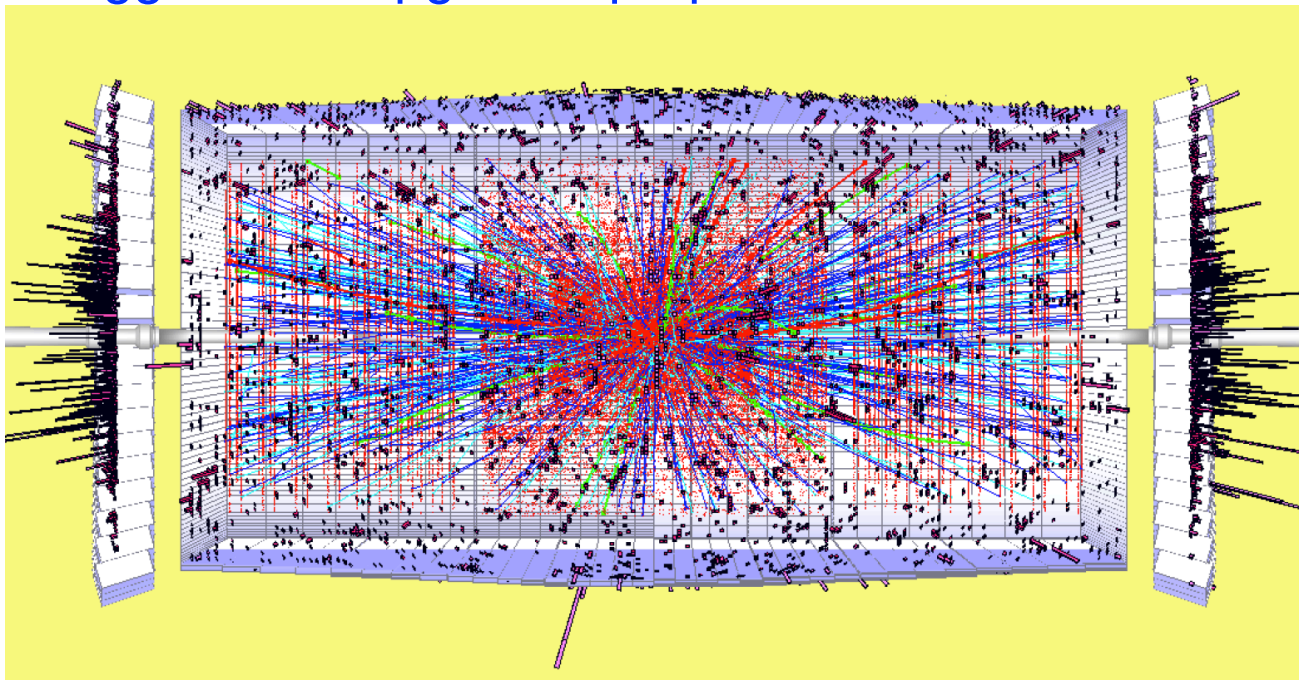
HL-LHC

- High-Luminosity LHC Running ~2026
  - ➡ Luminosity: ~5-8 x 10^{34} cm^2s^{-1}
  - ➡ "Pileup" (multiple interactions/crossing): 140 - 200
  - ➡ Integrated Luminosity: ~3000 fb^{-1} (10 years)
- Upgrades to LHC Detectors
  - ➡ Need to handle challenging environment
  - ➡ Wide range of detector/trigger/DAQ upgrades proposed.
- CMS:
  - ➡ ***Central Tracker***
  - ➡ End-cap Calorimetry
  - ➡ Muon Systems
  - ➡ ***Trigger***/DAQ
- CMS Technical Proposal (2015)



Trigger Challenges

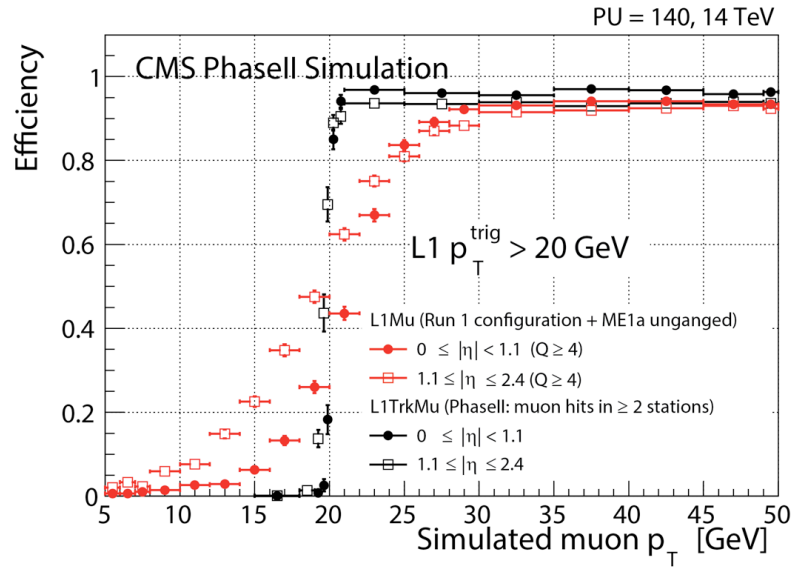
- Current Level-1 Trigger
  - ➡ No central tracking information
  - ➡ Electrons/Gammas (EG), Taus, Jets based solely on calorimeter deposits.
  - ➡ Muons reconstructed from tracks in muon chambers.
  - ➡ **Maximum Bandwidth: 100 kHz**
- HL-LHC:
  - ➡ Current Trigger System:
    - ▸ EG rate @25 GeV > 100 kHz
    - ▸ Muon rate plateaus
    - ▸ Overall Trigger Rate > 1000 kHz for ~2012 thresholds.
  - ➡ Upgraded System
    - ▸ Must increase total bandwidth
    - ▸ Must increase trigger capabilities
      - ◉ **Level-1 Tracking is a completely NEW handle.**

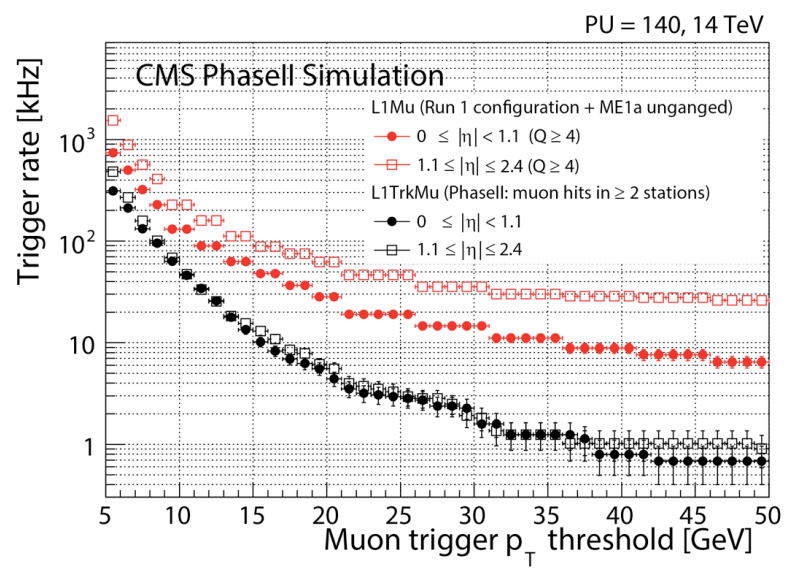
$L = 5.6 \times 10^{34}$ cm^{-2}s^{-1} $\langle PU \rangle = 140$	Level-1 Trigger with Level-1 Tracks	
Trigger Algorithm	Rate [kHz]	Offline Threshold(s) [GeV]
Single Mu (tk)	14	18
Double Mu (tk)	1.1	14 10
ele (iso tk) + Mu (tk)	0.7	19 10.5
Single Ele (tk)	16	31
Single iso Ele (tk)	13	27
Single γ (tk-iso)	31	31
ele (iso tk) + e/γ	11	22 16
Double γ (tk-iso)	17	22 16
Single Tau (tk)	13	88
Tau (tk) + Tau	32	56 56
ele (iso tk) + Tau	7.4	19 50
Tau (tk) + Mu (tk)	5.4	45 14
Single Jet	42	173
Double Jet (tk)	26	2@136
Quad Jet (tk)	12	4@72
Single ele (tk) + Jet	15	23 66
Single Mu (tk) + Jet	8.8	16 66
Single ele (tk) + H_T^{miss} (tk)	10	23 95
Single Mu (tk) + H_T^{miss} (tk)	2.7	16 95
H_T (tk)	13	350
Rate for above Triggers	180	
Est. Total Level-1 Menu Rate	**260**	

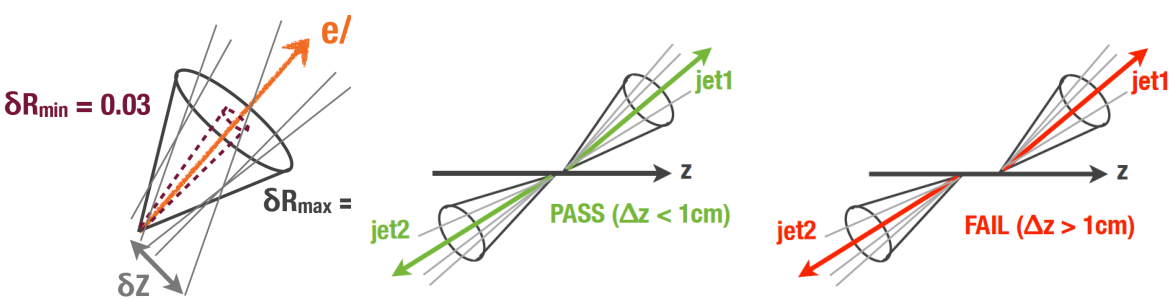
Benefits of L1 Tracking

- Electrons/Photons
  - ➡ Extra measurement - Rate Reduction
  - ➡ Isolation
- Muons
  - ➡ Excellent P_T Resolution
    - ▸ Rate Reduction
  - ➡ Isolation
- Tau Triggers
  - ➡ Multi-pronged
- Separation of Interactions
  - ➡ Hadronic/Multi-object Triggers

Improved Reconstruction
↓
Lower Rates
↓
Lower Thresholds
↓
Improved Physics Sensitivity



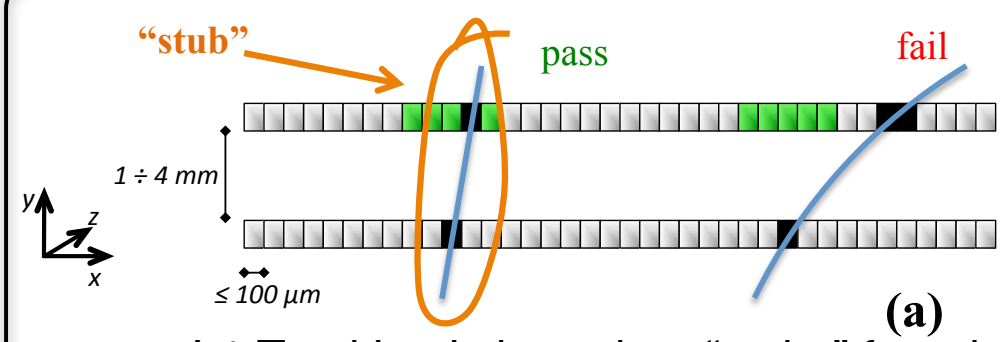




CMS Tracker

- Silicon pixel/strip Tracker
  - ➡ Inner Pixel Detector
  - ➡ Outer Pixel/Strip Detector
- Outer Tracker Geometry:
  - ➡ Barrel: 6 layers
  - ➡ Endcaps: 5 disks

} Used for L1 Tracking



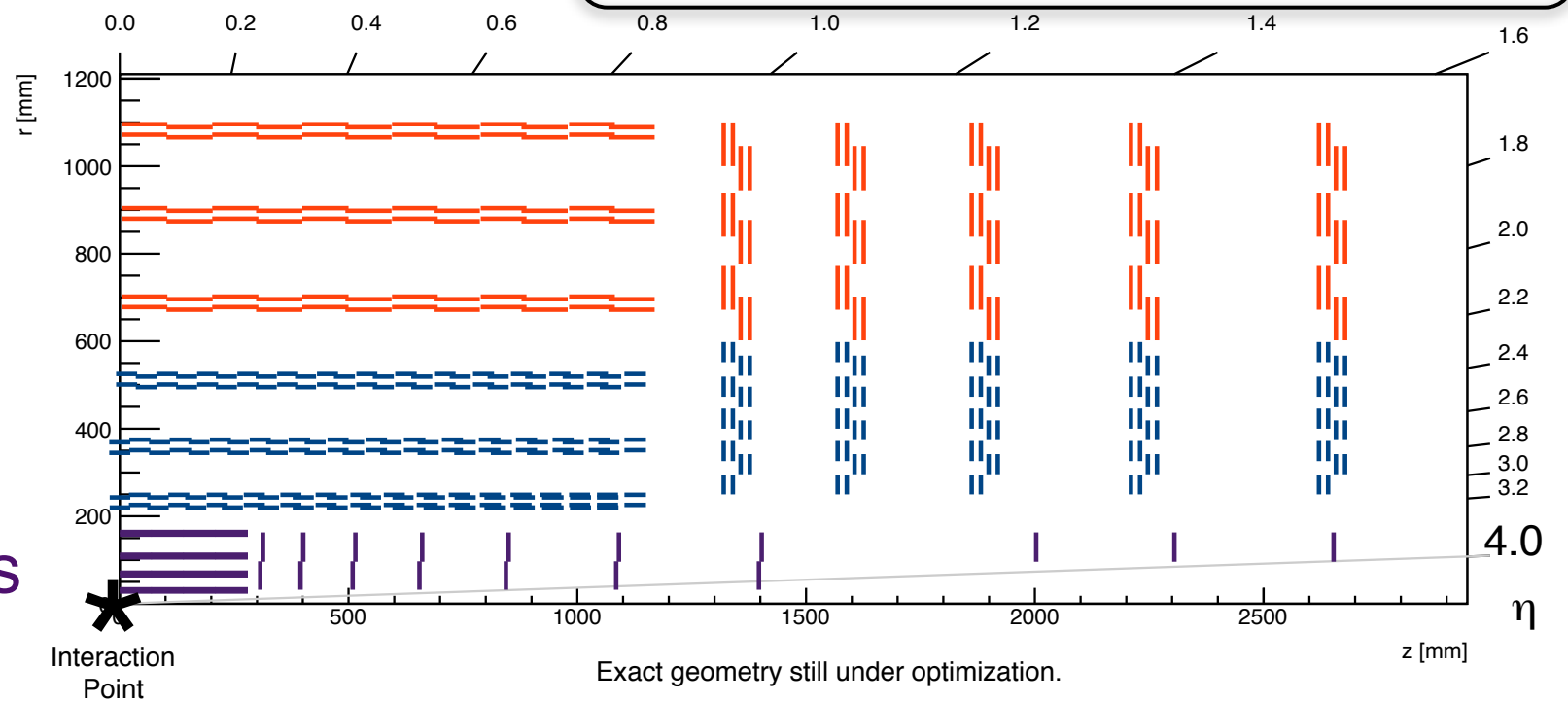
L1 Tracking is based on "stubs" found in the FE. Stub consists of pairs of hits on closely spaced layers.

Strip/Strip (2S)

Pixel/Strip (PS)

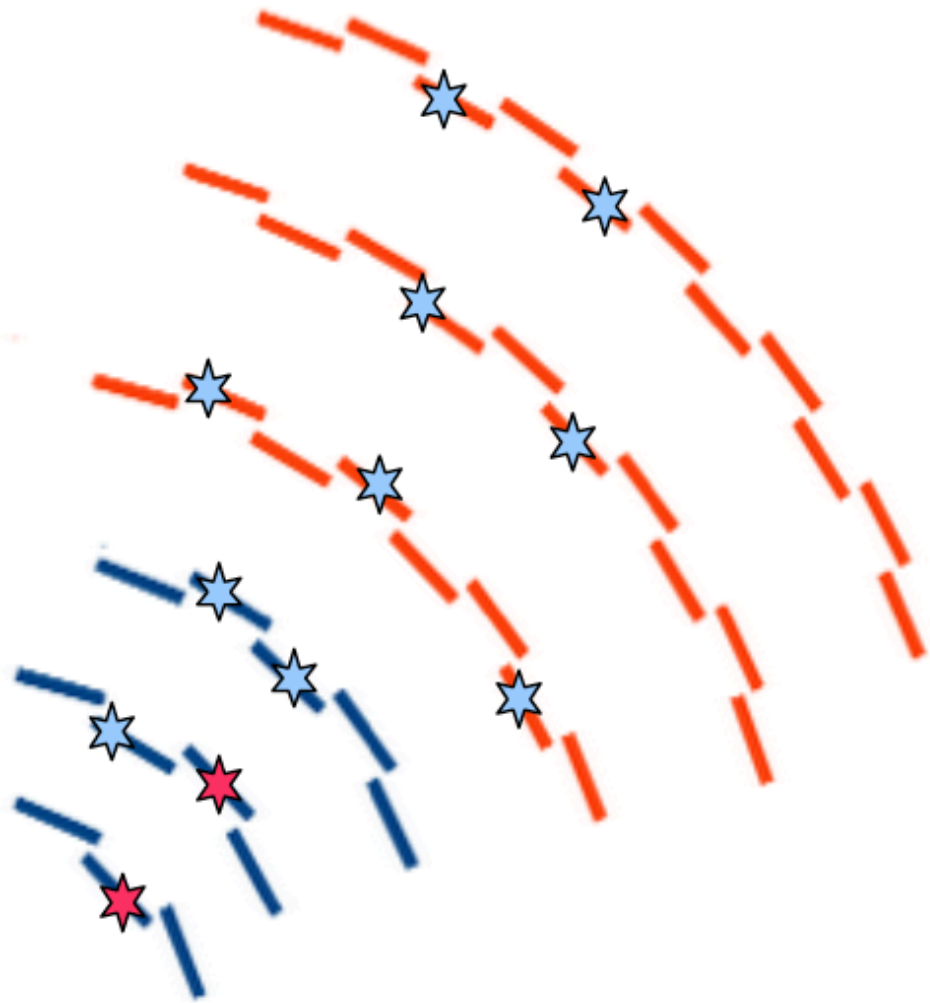
Pixels

Pixels not included in L1 Tracking described here.



Exact geometry still under optimization.

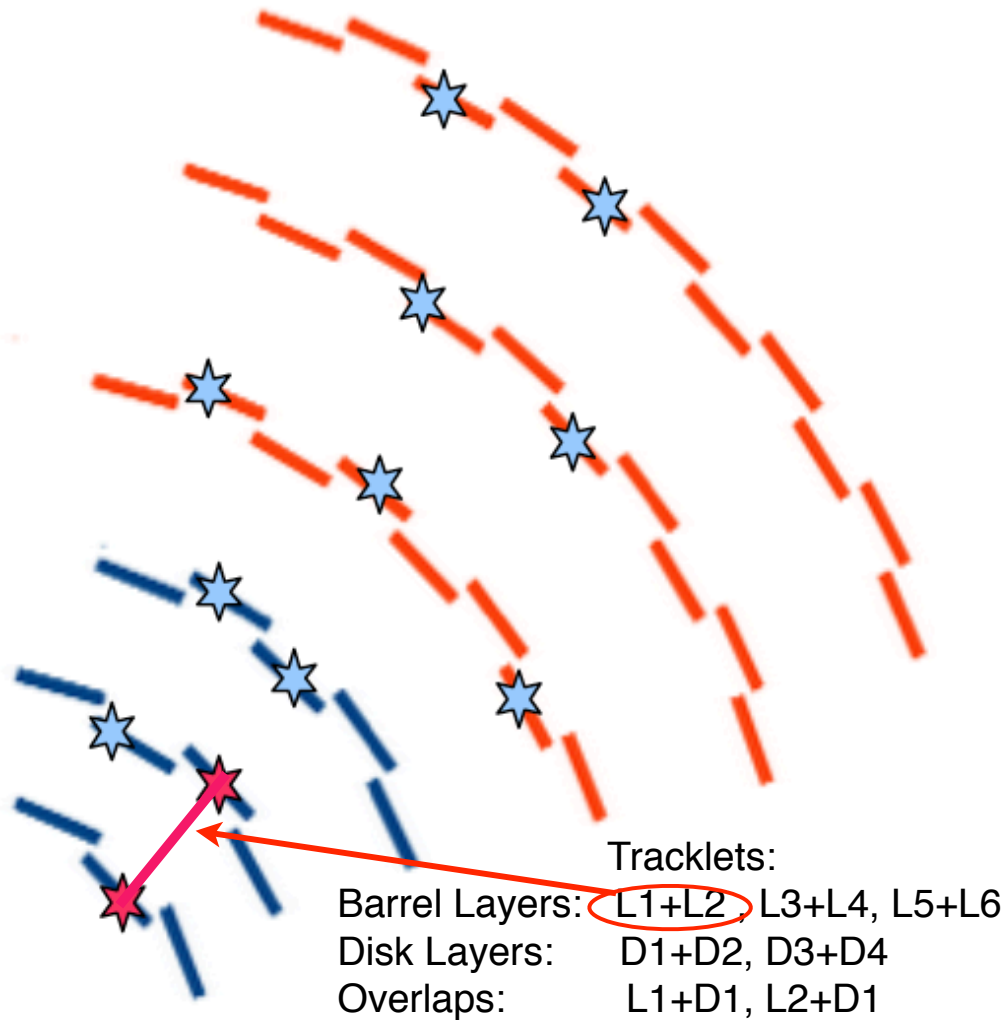
Basic Approach



Note: This is one of several approaches being explored by CMS. The remainder of the talk describes this “Tracklet” approach.

Basic Approach

- Form "Tracklets"
  - ➡ Stubs from adjacent layers
  - ➡ Find initial track parameters using beam constraint.



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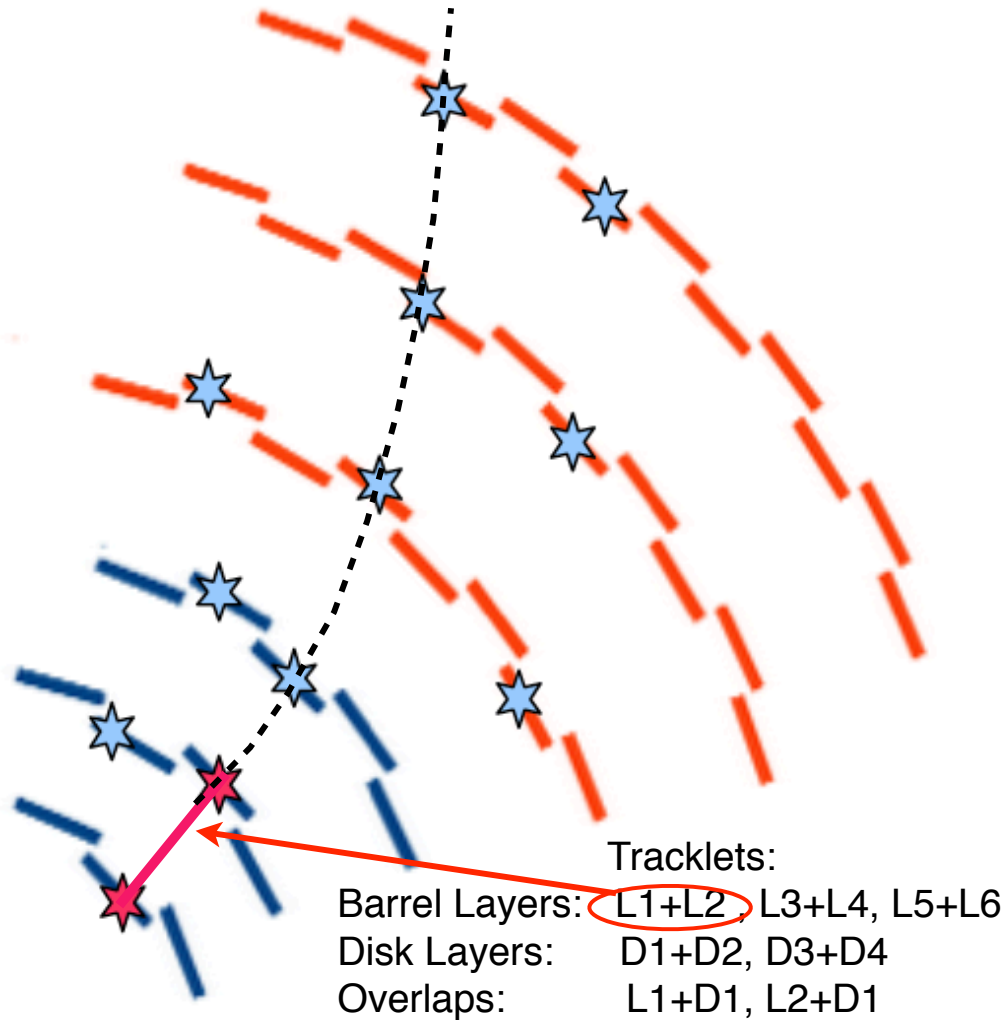
- Project into other layers
  - ➡ Locate additional stubs



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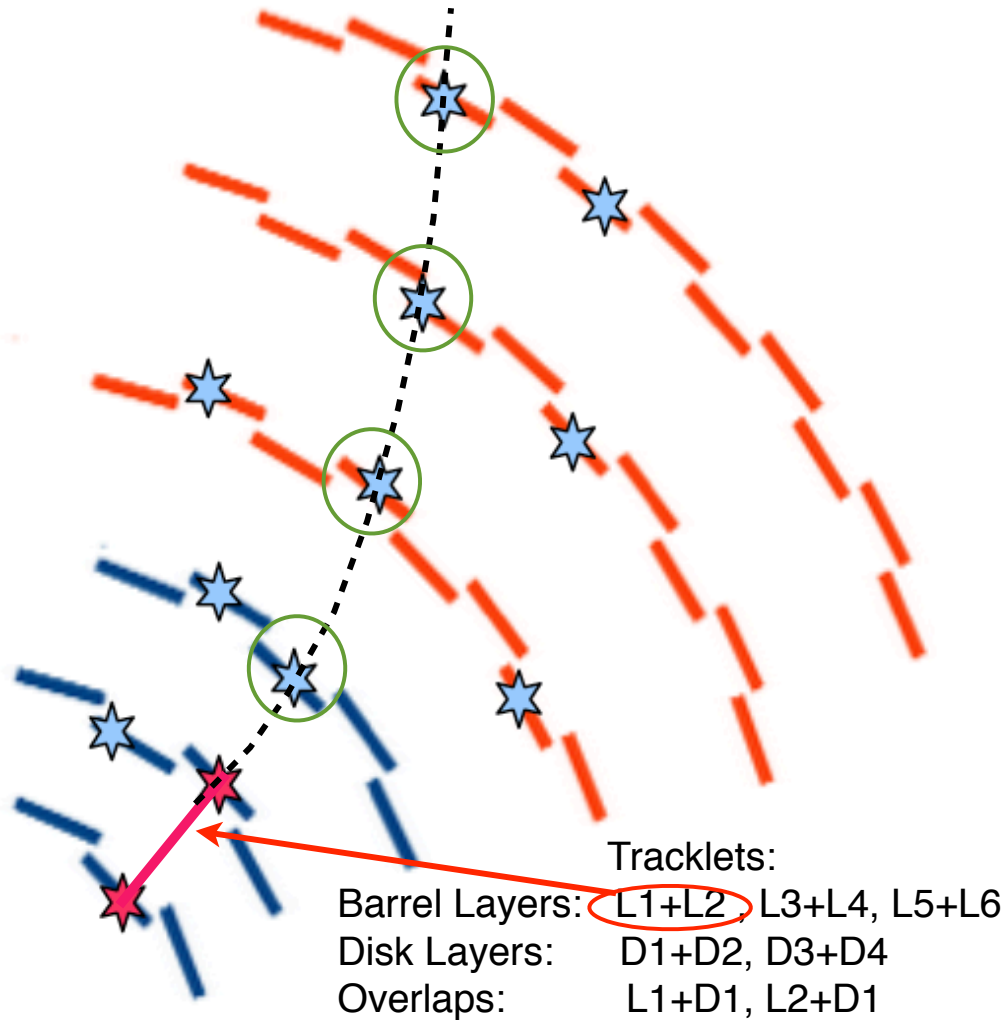

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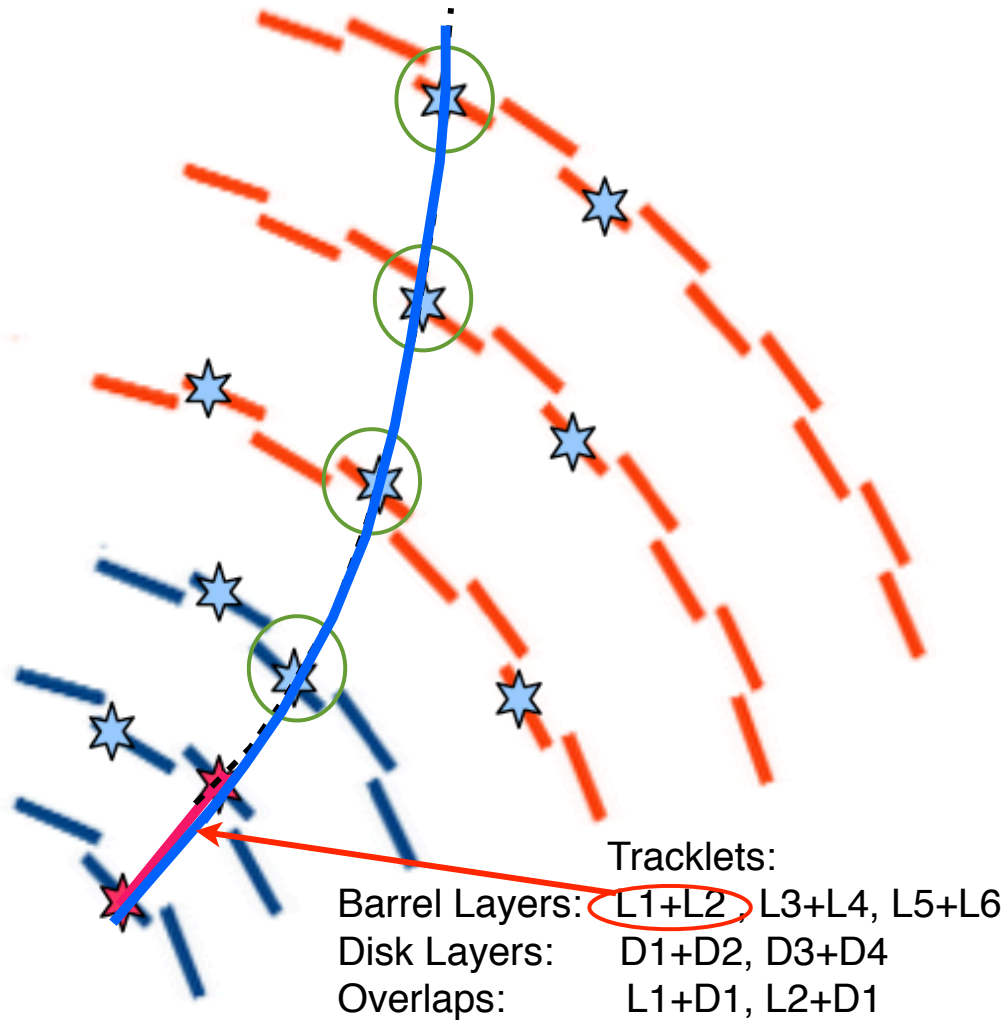
  - ➡ Locate additional stubs
- Perform a fit to all stubs
  - ➡ Linearized chi-squared
  - ➡ Determine final track parameters



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- Project into other layers
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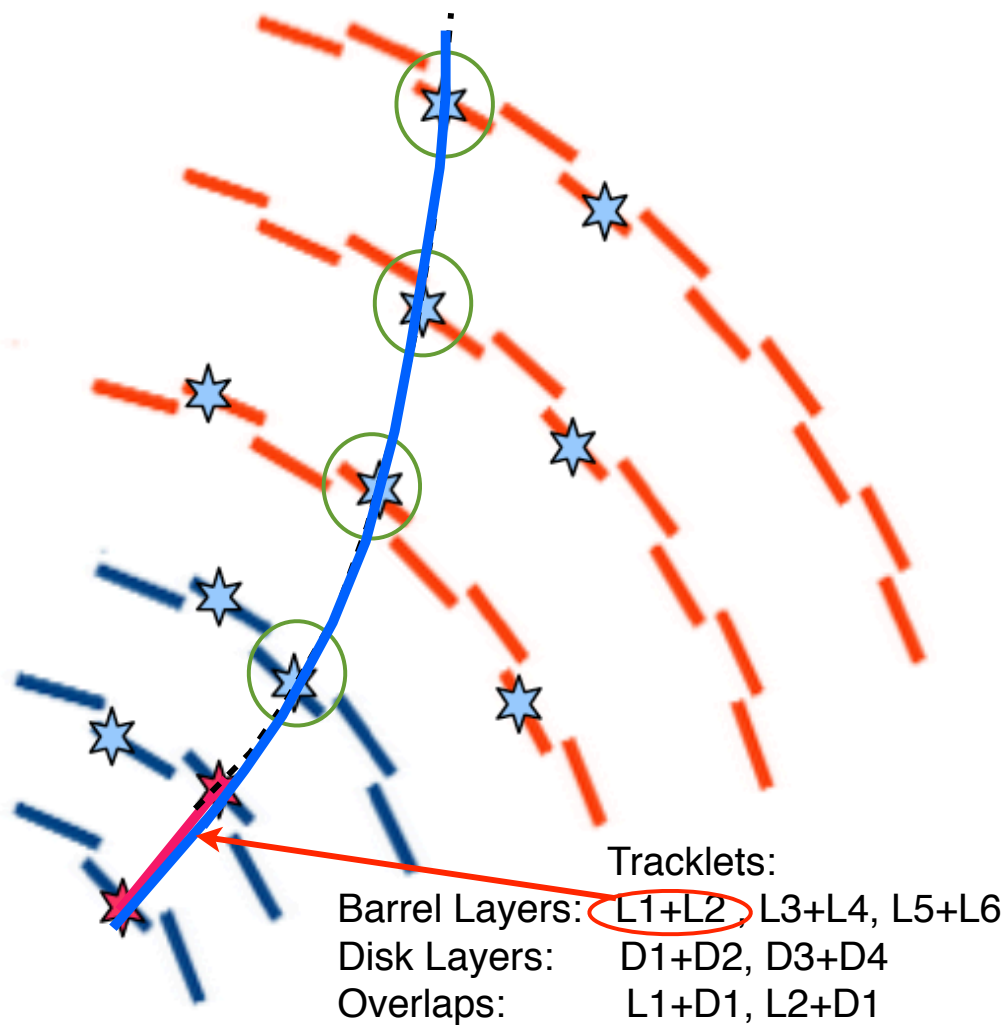
- Perform a fit to all stubs
  - ➡ Linearized chi-squared
  - ➡ Determine final track parameters
- Remove duplicate tracks
  - ➡ Seeding tracks on multiple layers leads to the same particle being found multiple times.



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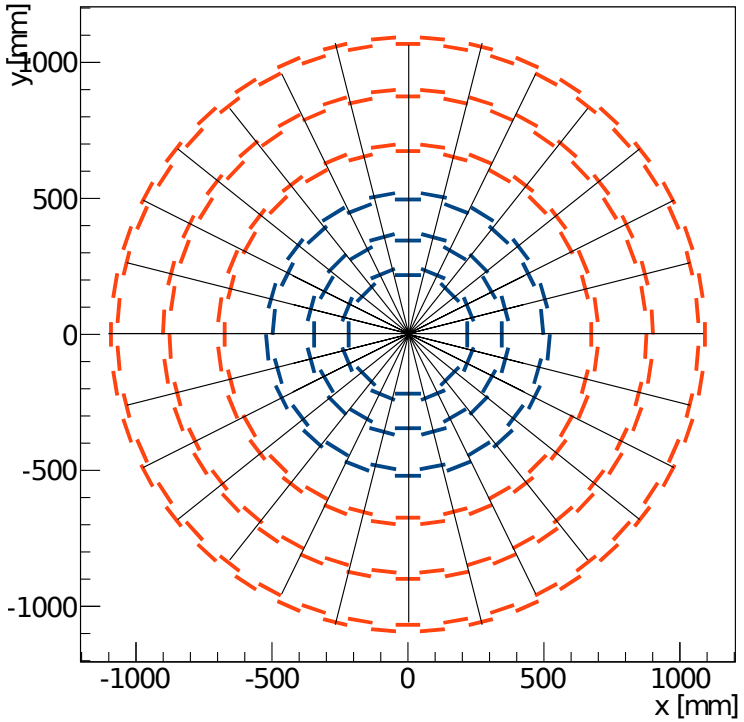
Hardware Configuration

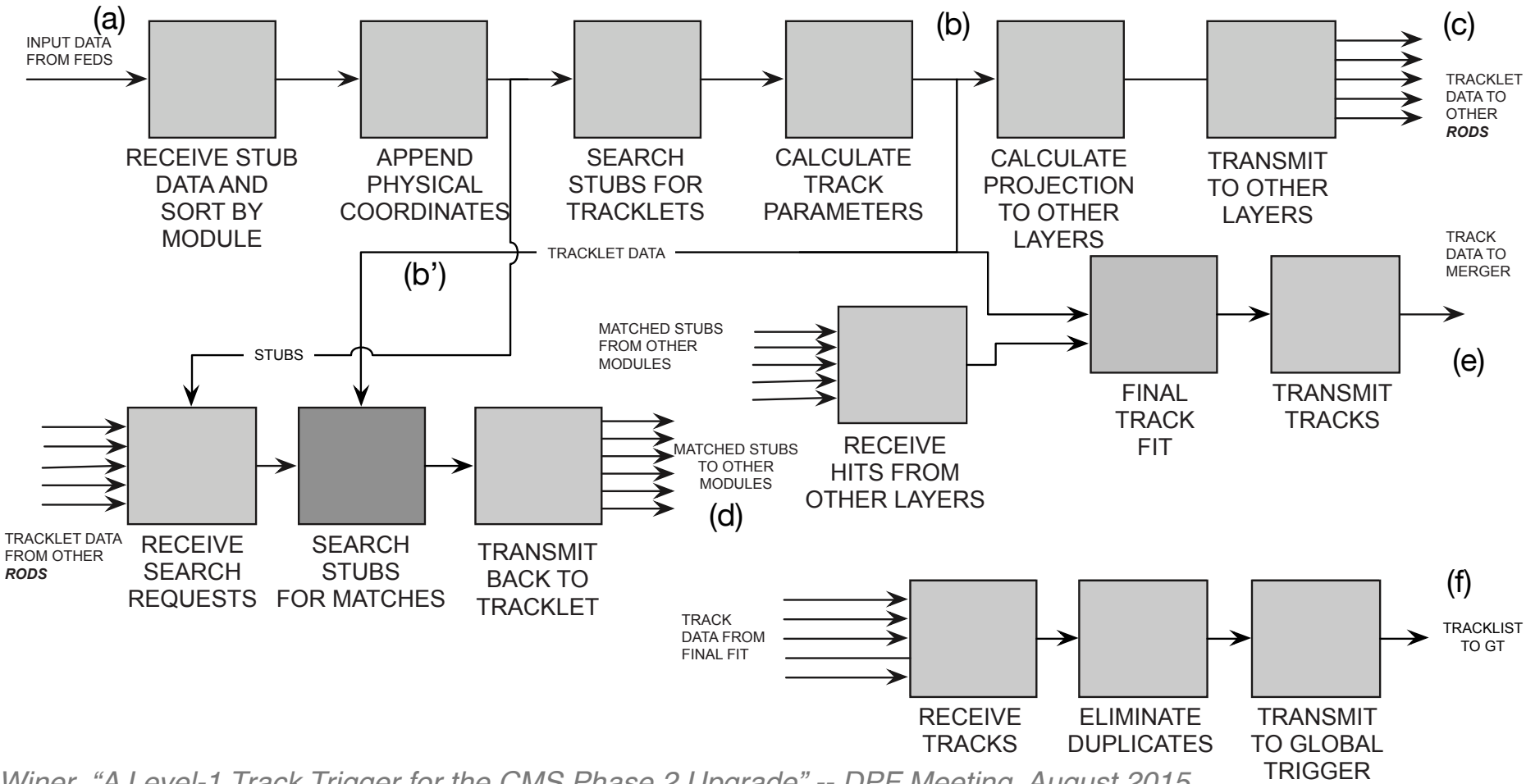
- Parallel Processing
  - ➡ Divide tracking system into 28 sectors in ϕ.
    - Min P_T 2 GeV
    - Tracks contained within a sector and nearest neighbor, which simplifies communications.
  - ➡ Each sector has a dedicated processor board.
  - ➡ 4-8x time multiplexing
    - @ 4x TM: each sector receives new event every 100 ns.
    - Current spec: Latency < 4 μs.
- Sector Processors:
  - ➡ Target large commercial FPGAs
  - ➡ I/O:
    - Stub Input: ~200 Gbits/s
    - Neighbor Boards: 2 x 80 Gbits/s
    - Track list: ~20 max trk/sec/event = ~20 Gbits/s



Downstream trigger systems will associate tracks with calorimeter and muon system objects to form L1 trigger objects.

Firmware Structure

- Firmware:
  - ➡ Pipelined: 13 steps each ~100 ns
  - ➡ Verilog Implementation (R&D target: Xilinx Vertex-7 chip)
  - ➡ Currently achieved a 1/4 barrel design with 320 MHz clocking.



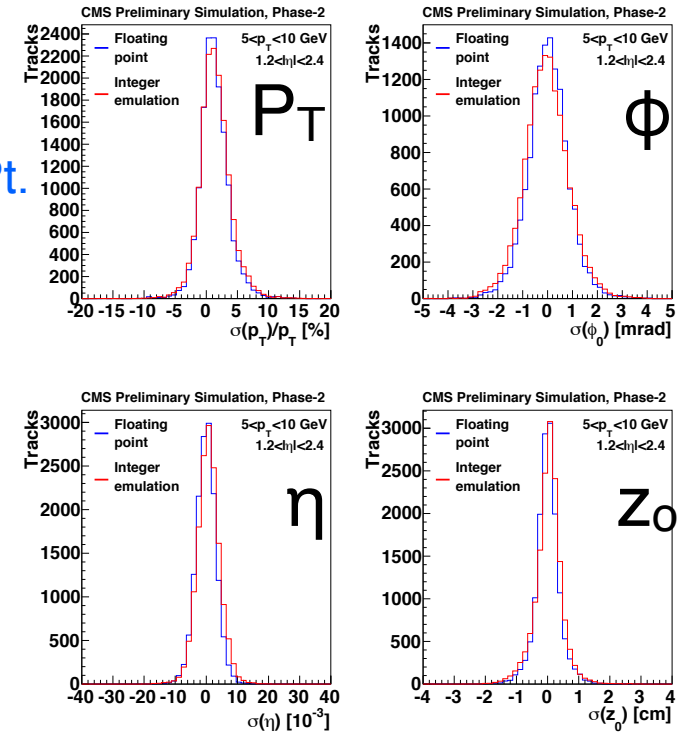
Firmware Performance

- C++ Firmware Emulation
  - ➡ Evaluate firmware performance
  - ➡ Evaluate choices
- Comparisons:
  - ➡ Integer vs floating point calculations
  - ➡ Coverage based on tracklet seed
  - ➡ duplicate track removal.
- Single particle MC w/o pileup
  - ▸ High pileup performance (next page)

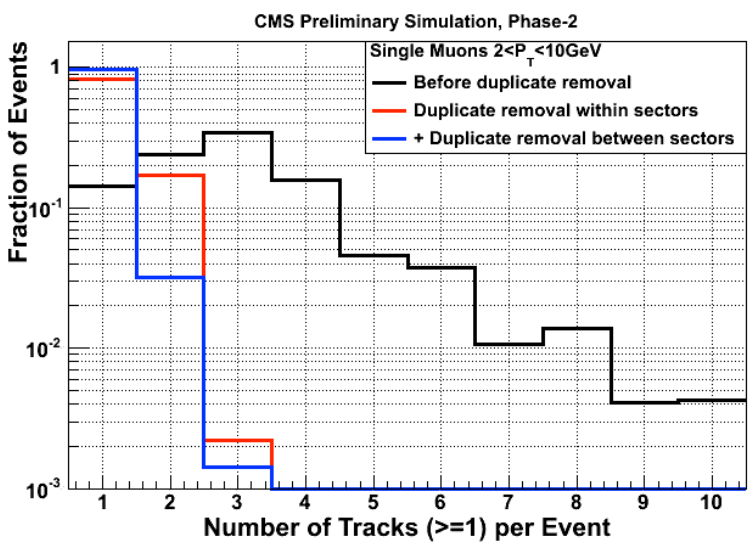
Tracks in Disks

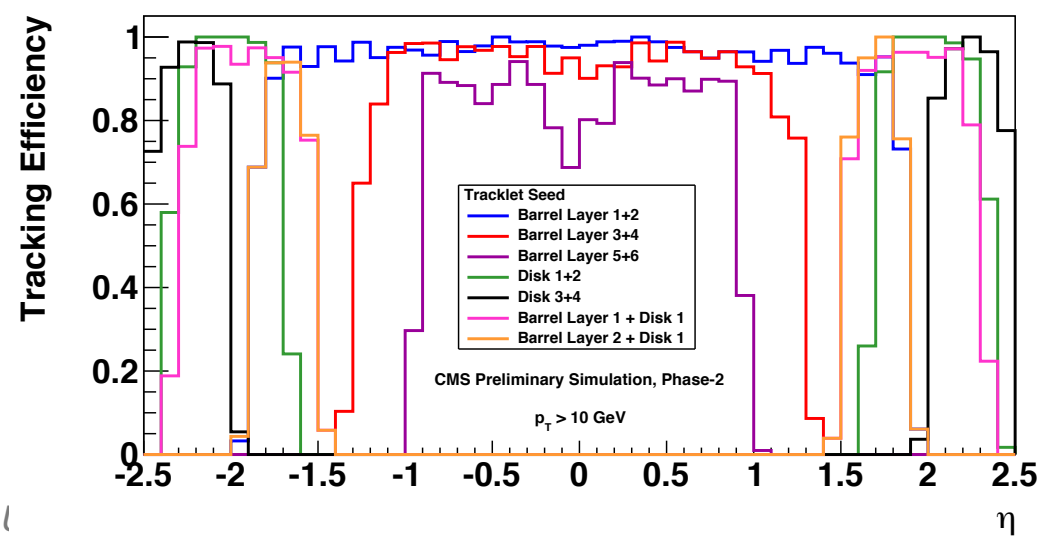
Floating Pt.

Integer



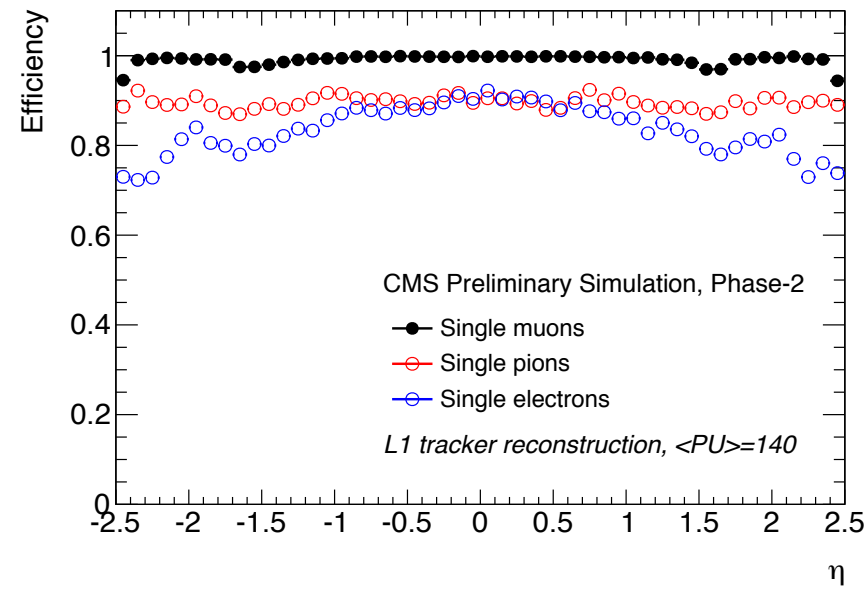
Muon Track Finding

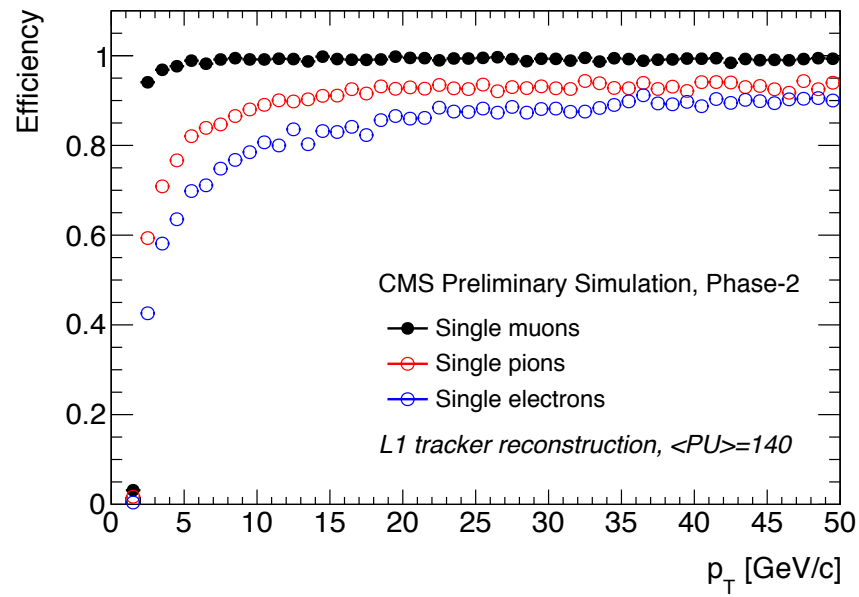


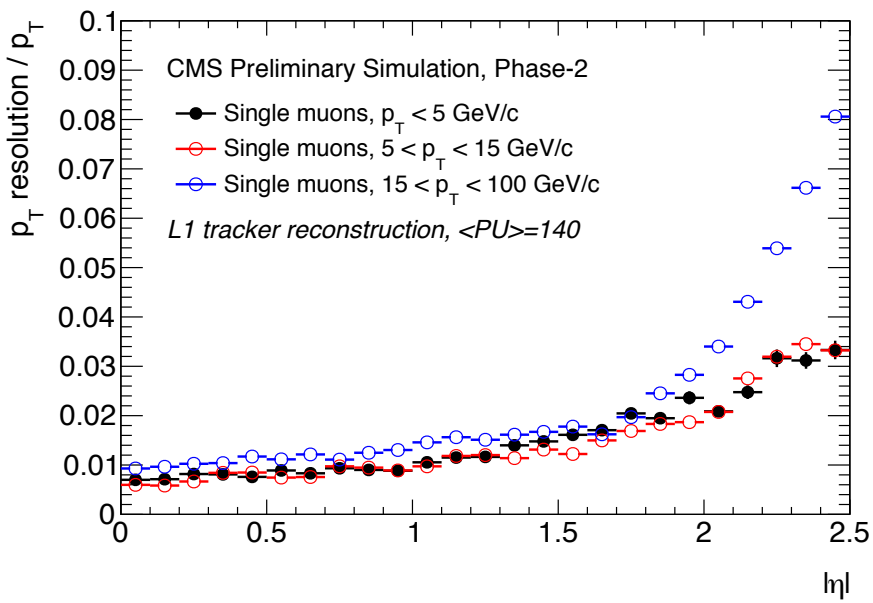


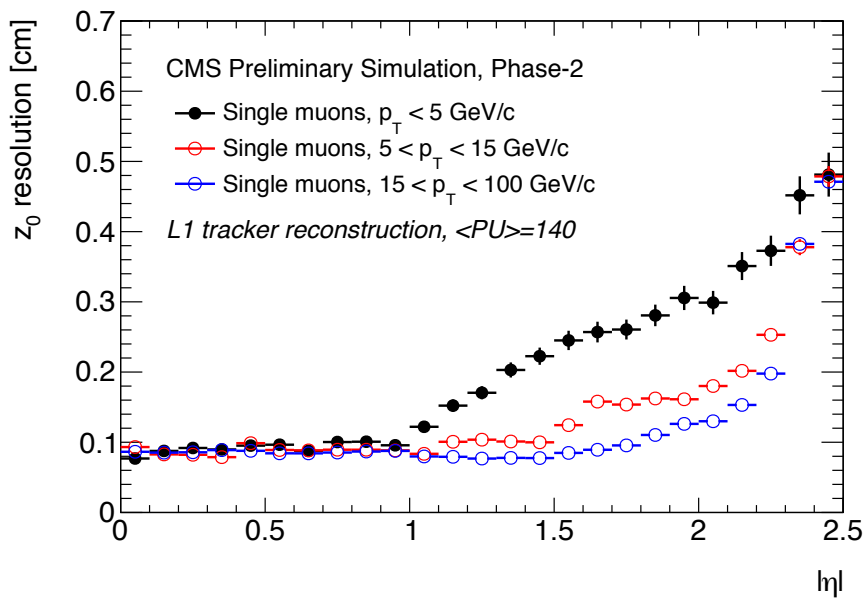
Algorithm Performance

Based on simulations with <PU>=140.





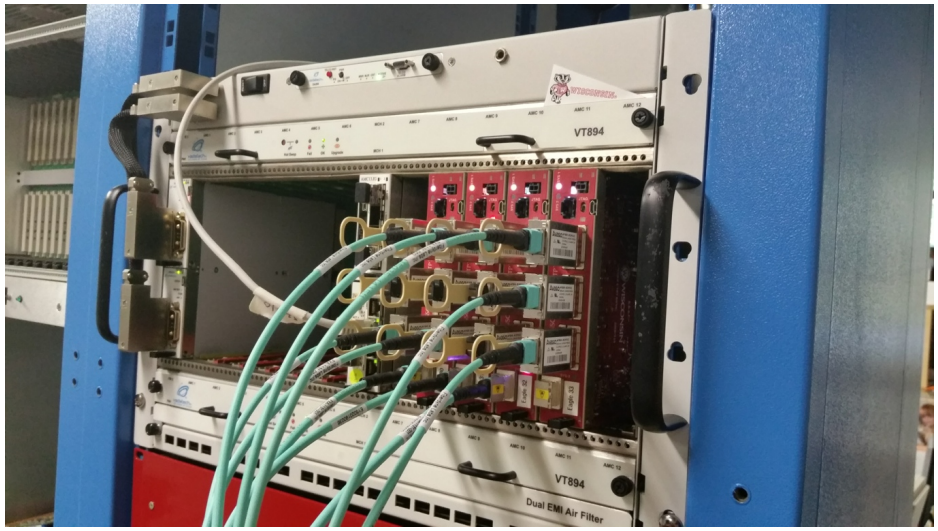




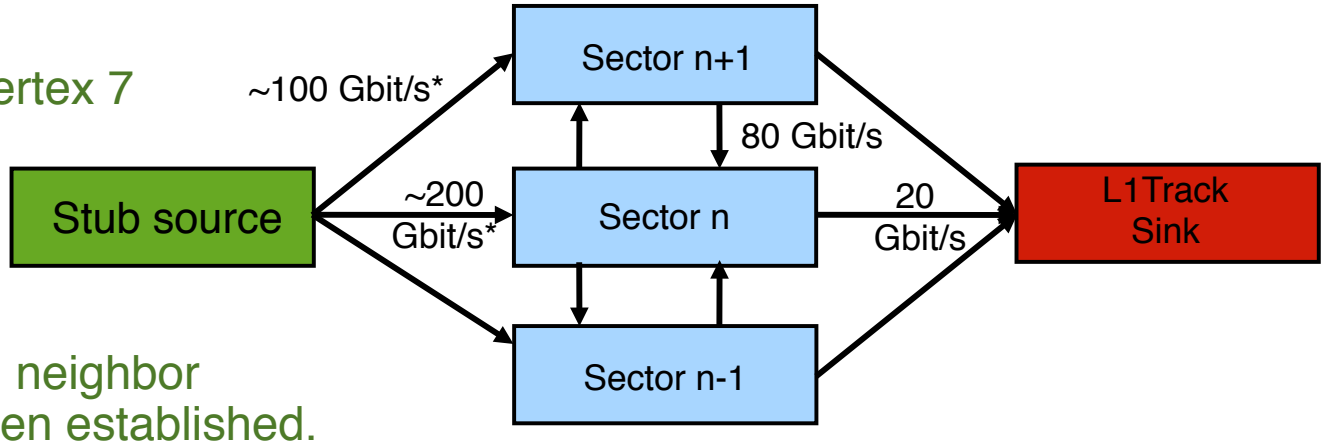
Sector Demonstration

- Goal: Establish overall viability of tracklet approach.
  - ➡ Firmware/Algorithm
  - ➡ I/O Tests (input, neighbor, output)
  - ➡ Latency
  - ➡ Stress tests with data volumes
- Setup:
  - ➡ Four µTCA cards
    - ▸ Core sector board + 2 neighbors
    - ▸ 4th acting as data source/sink.
  - ➡ Firmware
    - ▸ Developed for Xilinx Vertex 7
    - ▸ 1/4 barrel
  - ➡ Status:
    - ▸ Test stand functional
    - ▸ Basic track finding and neighbor communication has been established.

Test crate at CERN



Used µTCA boards developed by University of Wisconsin for the current 2016 Level-1 Trigger upgrade.



Summary

- High Luminosity Running of the the LHC
  - ➡ Outstanding physics potential
  - ➡ Enormous challenges
- The CMS trigger system will require substantial upgrades
  - ➡ More bandwidth
  - ➡ New and improved object reconstruction
- Tracking at the Level-1 Trigger
  - ➡ Added capability with substantial impact on trigger rates
  - ➡ Complex pattern recognition problem with large data volumes
- R&D on a Track Trigger System
  - ➡ Algorithms developed show excellent performance
  - ➡ FPGA based system shows promise
  - ➡ Efforts are ongoing to demonstrate full viability of design, identify and mitigate vulnerabilities

Backup Slides

Resolutions in Barrel