New powering methods for SLHC trackers

Marc Weber, RAL

- **Why needed ?**
- **How does it work ?**
- **R&D results**
- **Next steps**

Executive Summary

Have a big challenge to meet

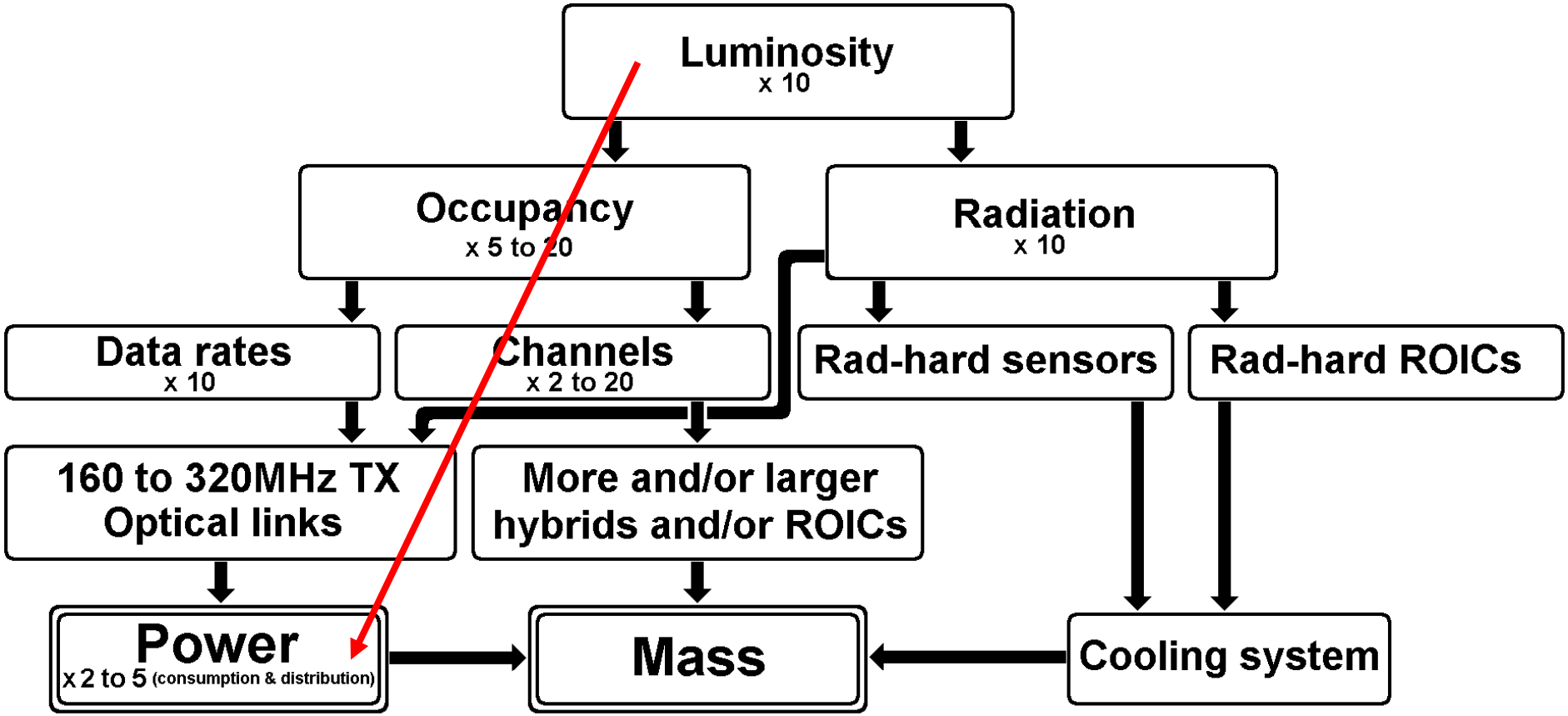
Field gets the attention it needs: ~20 groups working actively on this as of today. There is a wealth of first results. You will see a few only.

Communication between ATLAS and CMS is good; good collaboration between power WP8 of EU FP7 SLHC-PP. I expect collaboration between experiments to increase to everyone's benefit

Several solutions are investigated in parallel, which is fine at this stage. The arrival of first working custom devices (this year) will bring us a major step forward. Then need to consolidate somewhat.

Work on system aspects has started (redundancy, protection, slow-control; integration; grounding and shielding)

Power consumption and power distribution is major challenge for SLHC trackers



Generic problem for both ATLAS and CMS, strip and pixels,
independent of detector details

Cable pollution is observed everywhere

ATLAS tracker end view

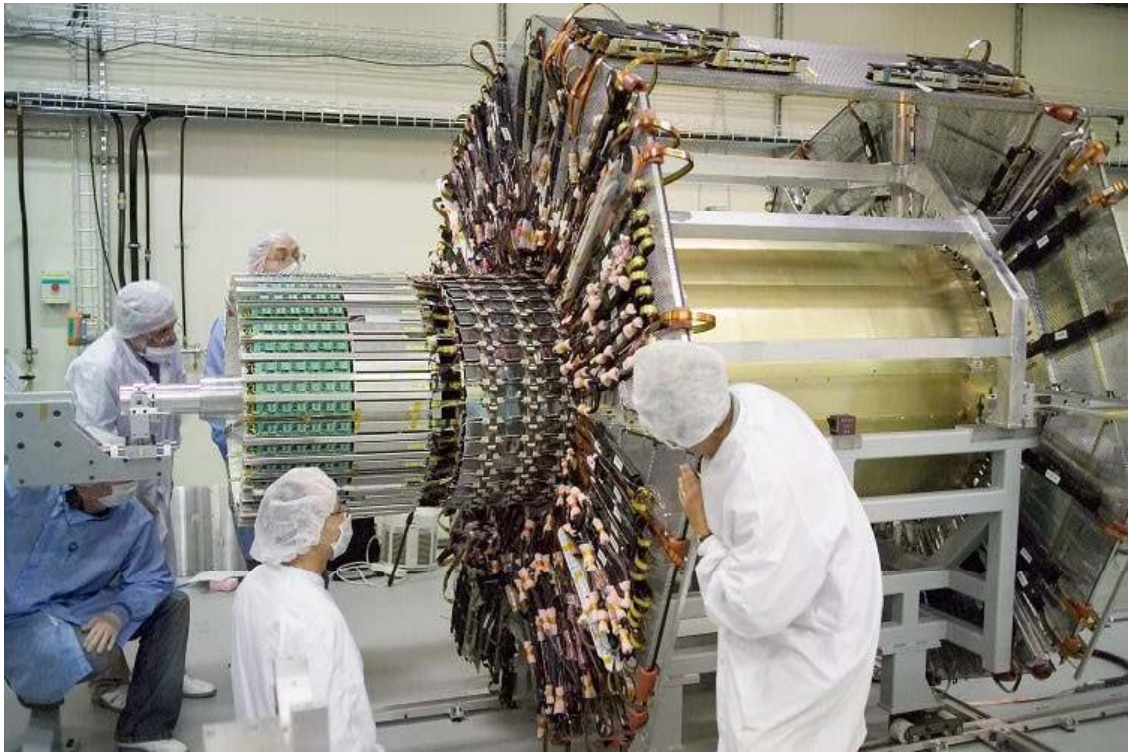
ATLAS pixels side view

Cannot afford this at SLHC and don't need to. New systems will be much better. (Less cables; less copper; better performance; higher power efficiency)

Why independent powering fails at SLHC ?

Need many more channels, but current/channel ~ constant,

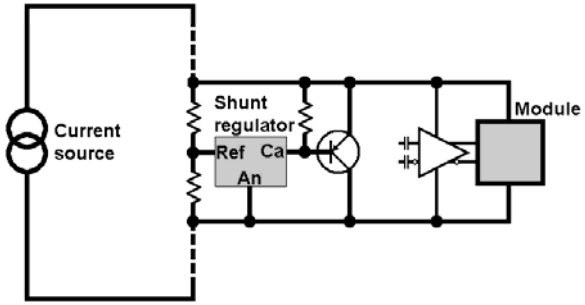
1. Don’t get 5 or 10 times more cables in
2. Power efficiency is too low (50% ATLAS SCT ⇔ ~15% SLHC)
3. Cable material budget: 0.2% of R.L. per layer (barrel normal incidence) ⇔ 1% or 2% SLHC
4. Packaging constraints on detector



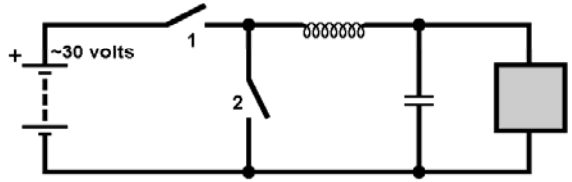
Each reason by itself is probably sufficient for a No-No

How do new powering schemes work?

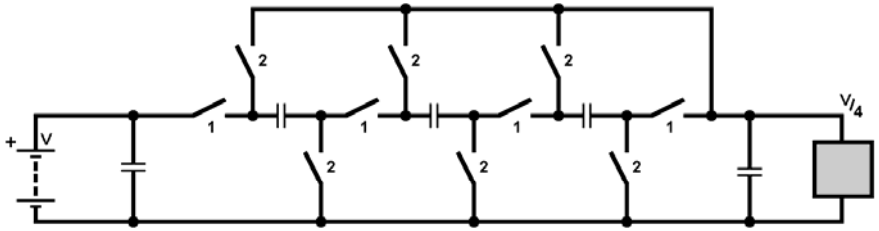
Minimize current through cables by
a) "recycling" current (SP) or b) "high-voltage" power lines (DC-DC)



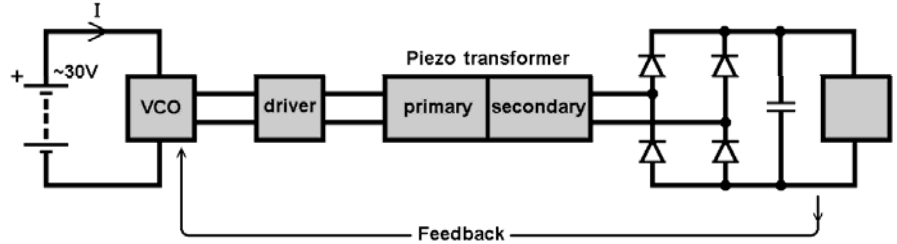
Serial powering



DC-DC buck converter



DC-DC charge pump



Piezo transformer

Why is it difficult ?

Power distribution is an old problem. Standard approaches don't work for extreme boundary conditions of SLHC trackers

radiation levels

magnetic field (no ferrites)

minimum size and mass ("no" shielding)

high currents

extreme reliability

silicon strips sensitive to "pick-up"

Limited experience with power supply design in HEP IC design

R&D Results

1) Tests with commercial electronics and LHC silicon modules

2) Design of custom electronics

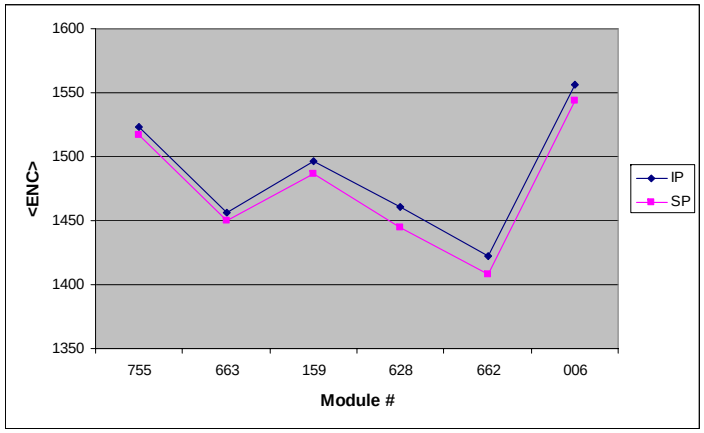
(Shunt regulators, DC-DC converters, piezo transformers)

3) Design redundancy and protection schemes

(mostly commercial at this stage)

4) System considerations

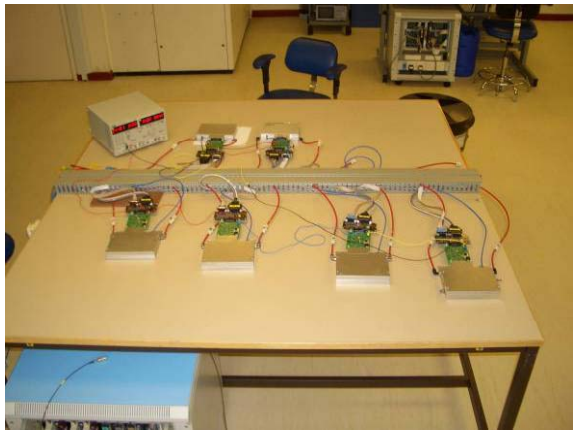
(cable budget; overall efficiency; grounding and shielding; slow-control; power supplies; etc.)



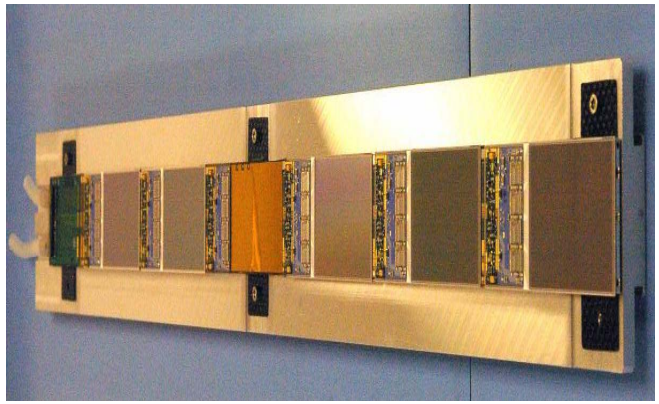
SP Results

1. SP with commercial components and 6 SCT modules (RAL)

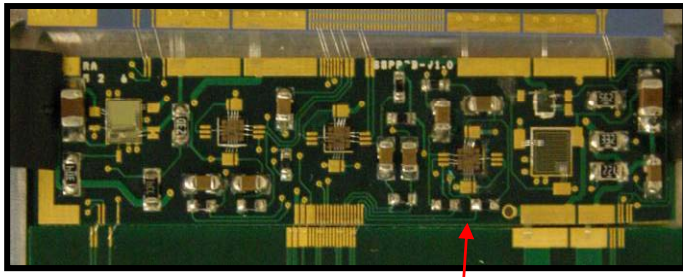
Many results, looking good.



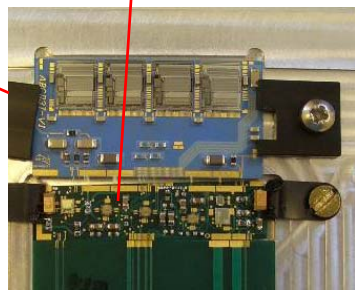
2. Six-module stave (at LBNL and RAL)



Miniature SP PCB; bare die

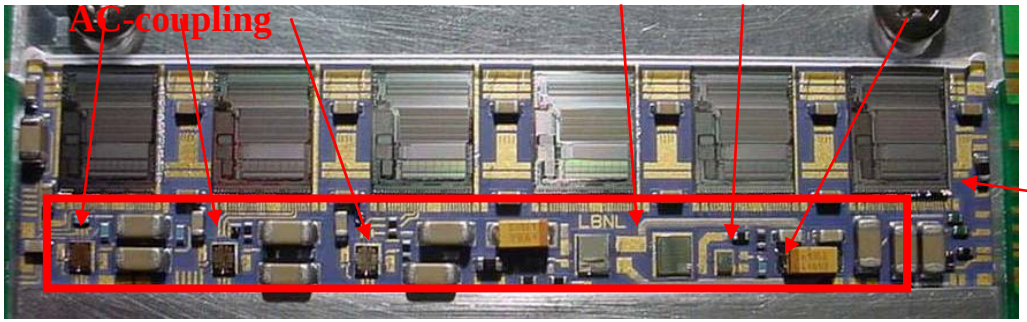


38 mm x 9 mm



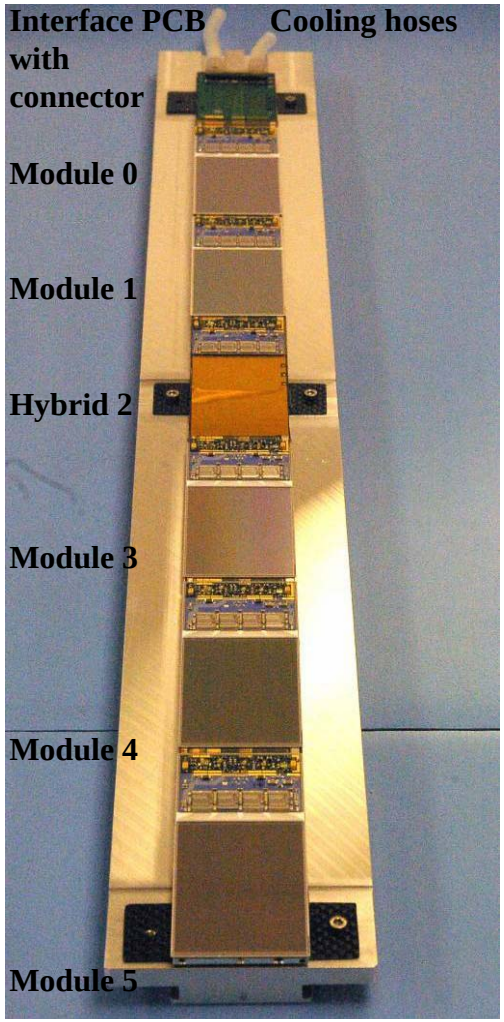
Data/clock/command AC-coupling

Linear regulator ST SR



3. Six-ABCD hybrid with integrated SP for 30 module stave (LBNL)

Six-module stave (finished; LBNL/RAL)

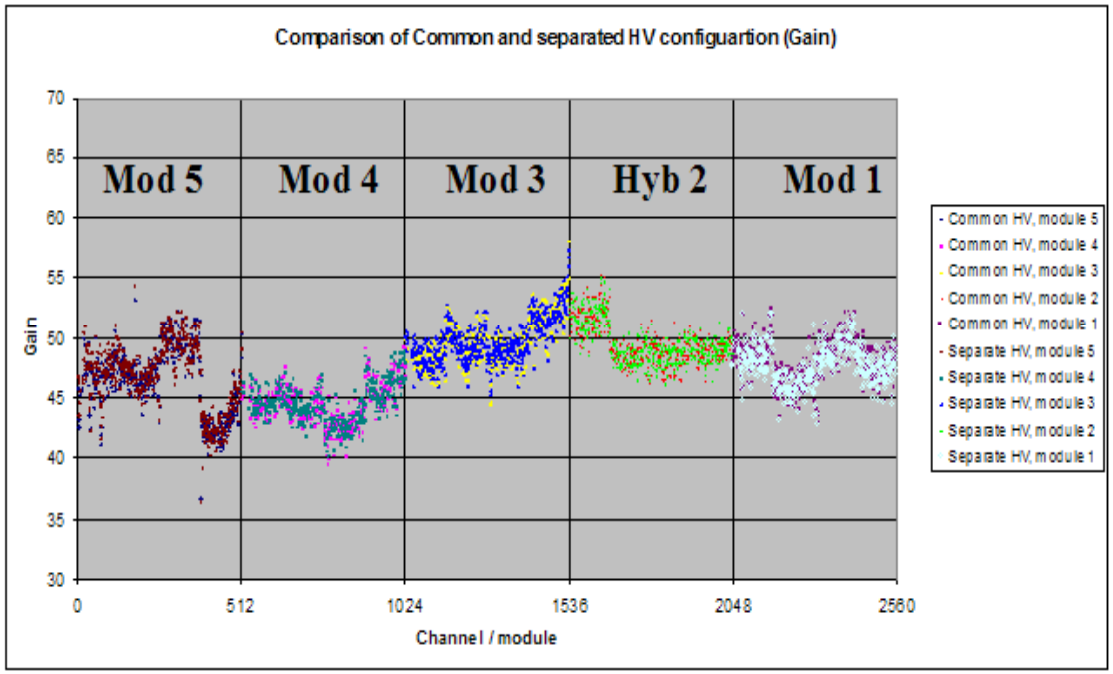


-operating reliably with multi-drop control/command cables

-Low noise despite some compromises

-Can run from a single HV line

-**Major milestone**

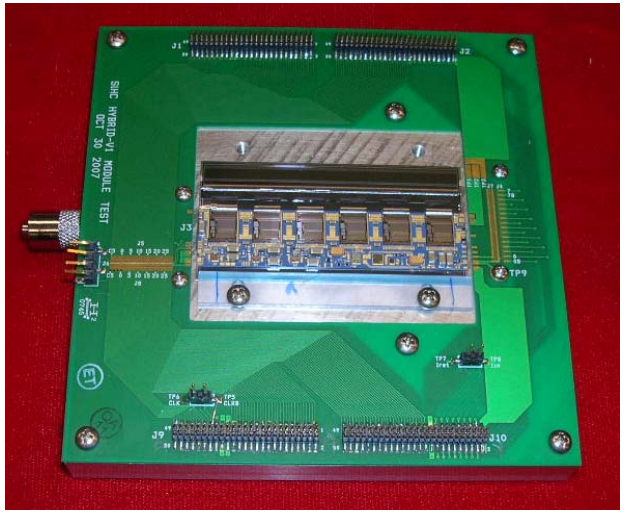


30-module stave (LBNL)

-might become the largest serial powering stave ever built

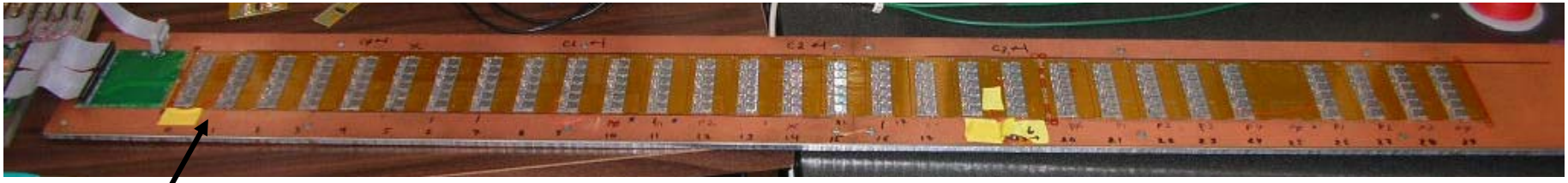
-so far looking very good in terms of SP

6-chip hybrid with SP on 3 cm long silicon sensors



4 V x 30 hybrids = 120 V (0.8 A)

In future systems: 1.5 V x 20 hybrids = 30 V



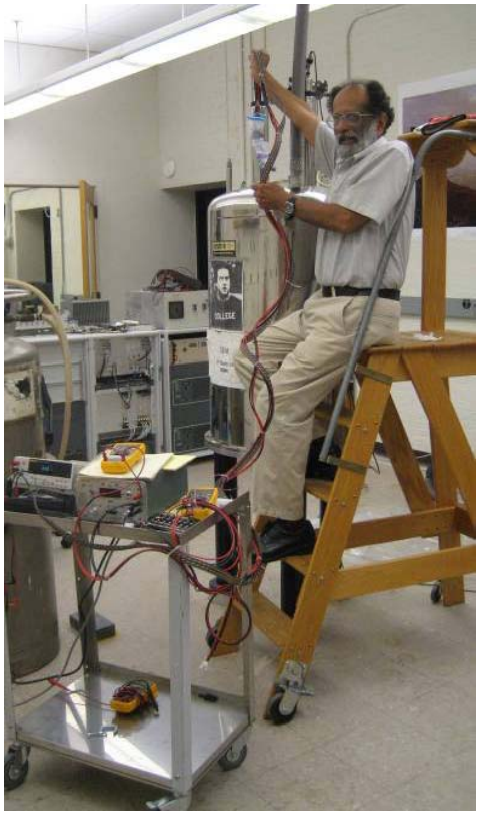
Chain of 30 hybrids is working fine

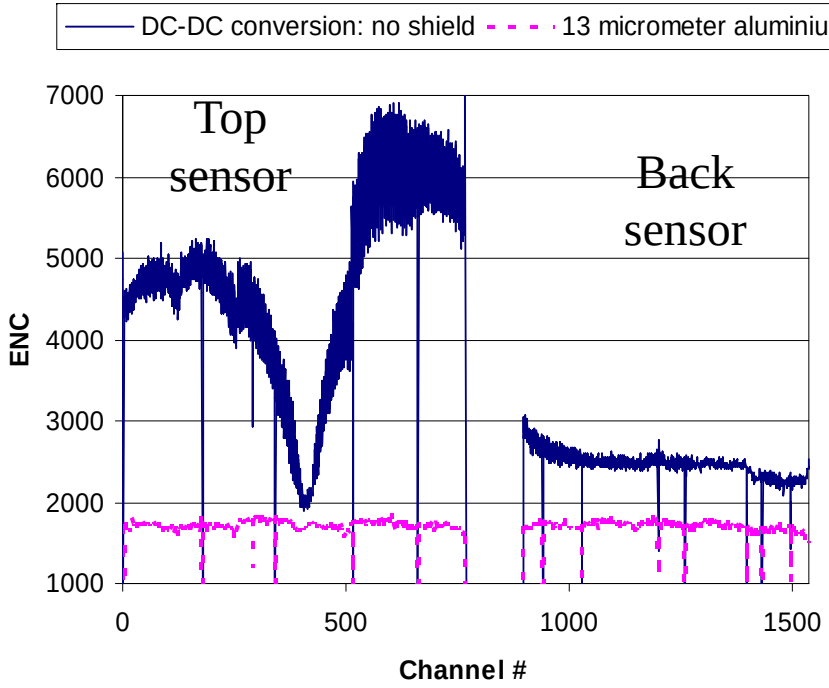
Module stave is being built up

DC-DC Results

1. Tests with commercial buck converters

Operation in 7 T is fine; Co-60 irradiation to 100 MRad looking good; noise tests with converter placed on SCT modules (Satish Dhawan, Yale)



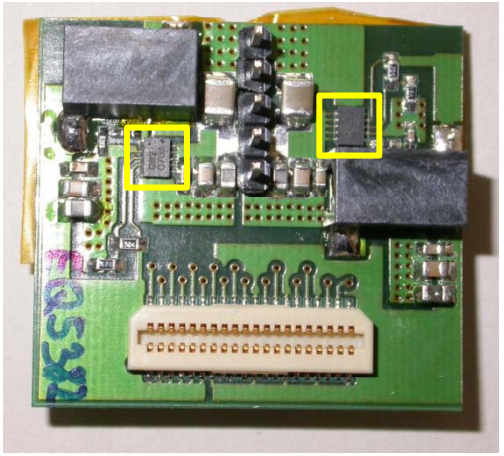


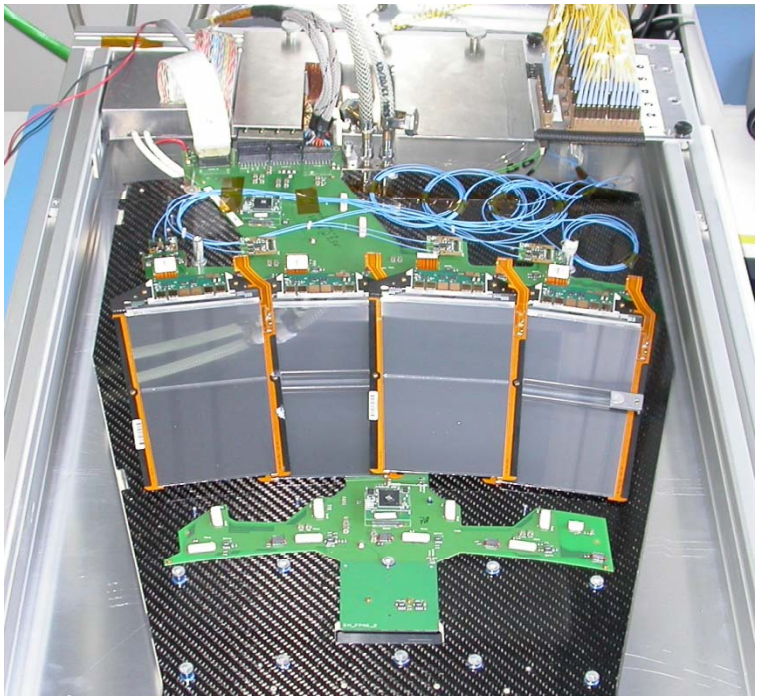
2. More EMI Tests with commercial buck converter silicon module

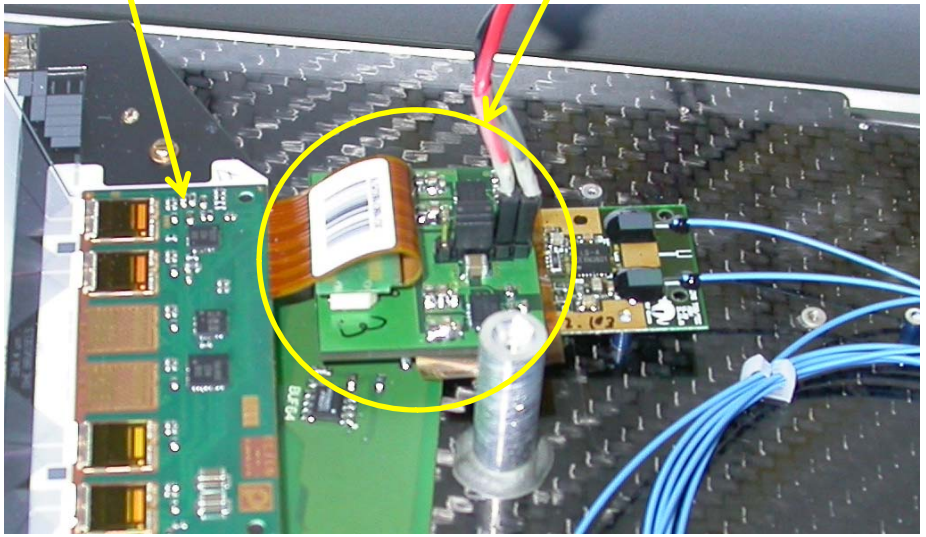
(BNL, Yale)

System Test with commercial buck converters at Aachen

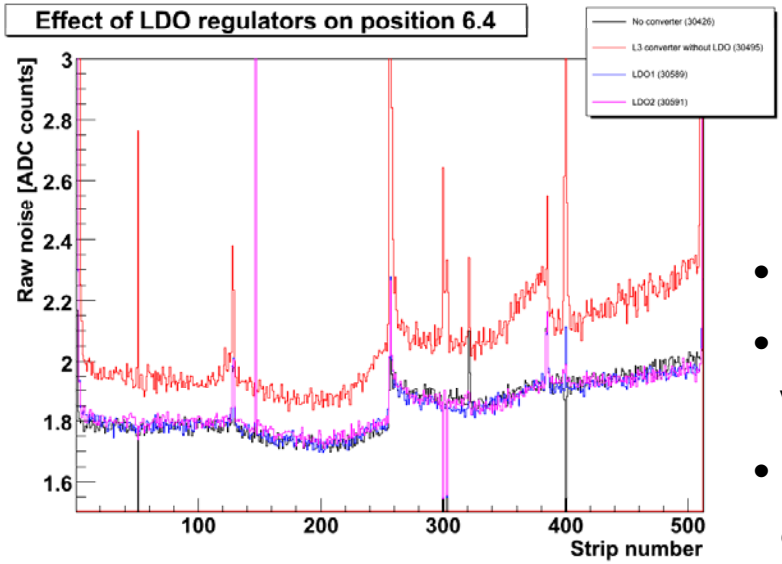
- Selected device**: Enpirion EN5312QI**
  - Small footprint: 5mm x 4mm x 1.1mm
  - $f_s \approx 4$ MHz
  - V_{in} = 2.4V – 5.5V (rec.) / 7.0V (max.)
  - I_{out} = 1A
  - Integrated ferrite inductor or external air-core coil
- Two chips integrated on PCB provide APV supply voltages
- System test set-up: end cap substructure with 4 strip modules







System Test with commercial buck converters at Aachen



---- No converter

---- L type without LDO

---- L type with LDO, dropout = 50mV

---- L type with LDO, dropout = 100mV

- With **internal inductor** noise increases by 10%
- Filters or low drop-out regulator (LDO) reduce voltage ripple and thus noise significantly
- Indicates that noise is mainly conductive and differential mode

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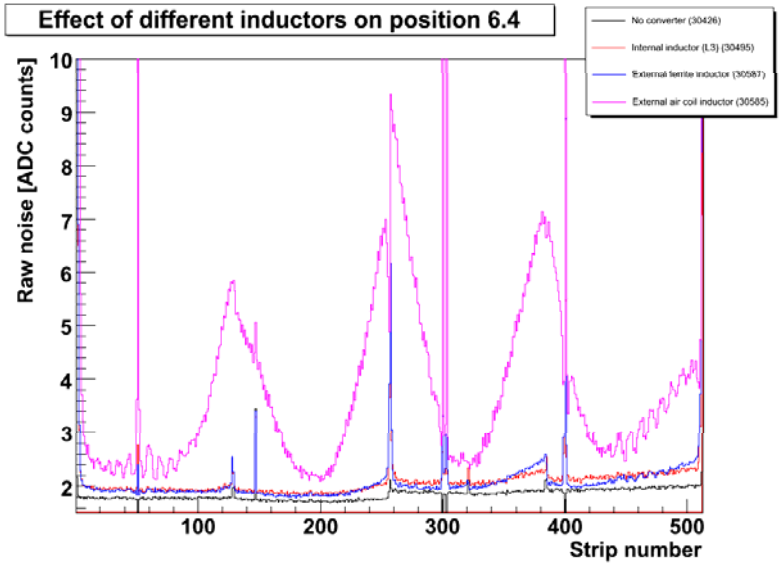
- External air-core coil radiates noise
- Air-core coil leads to cross-talk
- More investigations are needed: can radiated noise be avoided by clever coil design or at least be shielded?



---- No converter

---- Internal inductor

---- External ferrite inductor

---- External air-core inductor

Custom IC for Serial powering

1) ABC_Next shunt regulator and transistors (Cracow; ATLAS strips)
2) SPi (generic serial powering interface) (FNAL, Penn, RAL)

These two chips will enable us to test 3 SP architectures. SPi will also be useful for multi-drop transmission line studies. Both SPi and ABC_Next will be submitted in July 2008

3) FE-I4 shunt regulator and transistors (Bonn, ATLAS strips)
FE-I3 custom circuitry provided proof of principle of serial powering for pixels *(Nucl. Instr. Meth. A557 (2006) 445-459)*

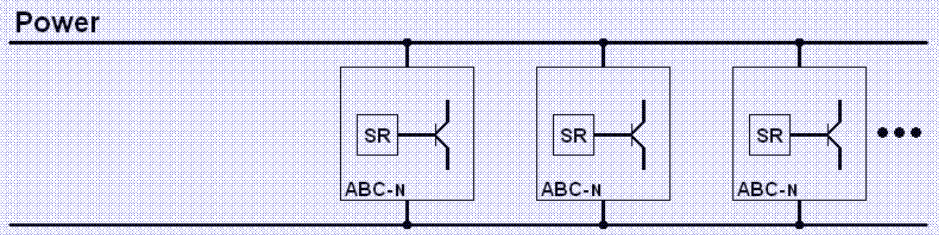
Q&A:

Why not take commercial devices? There are none
What are the three SP architectures? See appendix slides.
Why investigate all three architectures ? It just happened, exploits synergy between SLHC and ILC and requires only two ICs. Can not discriminate "on paper"

ABC-N serial powering options

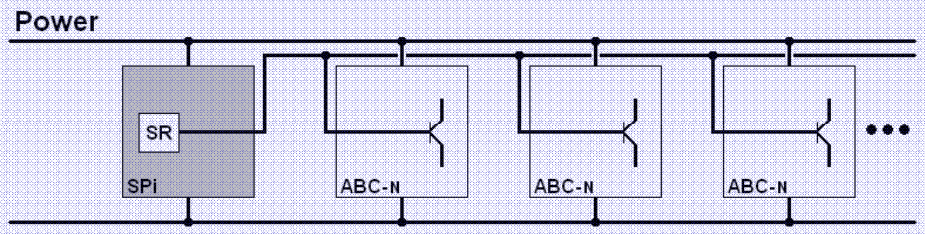
Wladek Dabrowski scheme

Each ABC-N has its own shunt regulator & transistor(s)



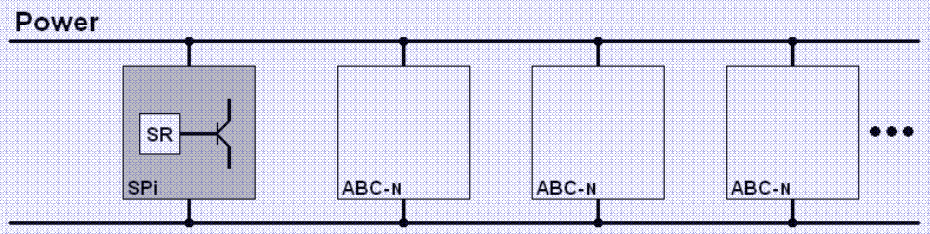
Mitch Newcomer scheme

Just one shunt regulator – Use each ABC-N transistor(s)



SPi-type scheme

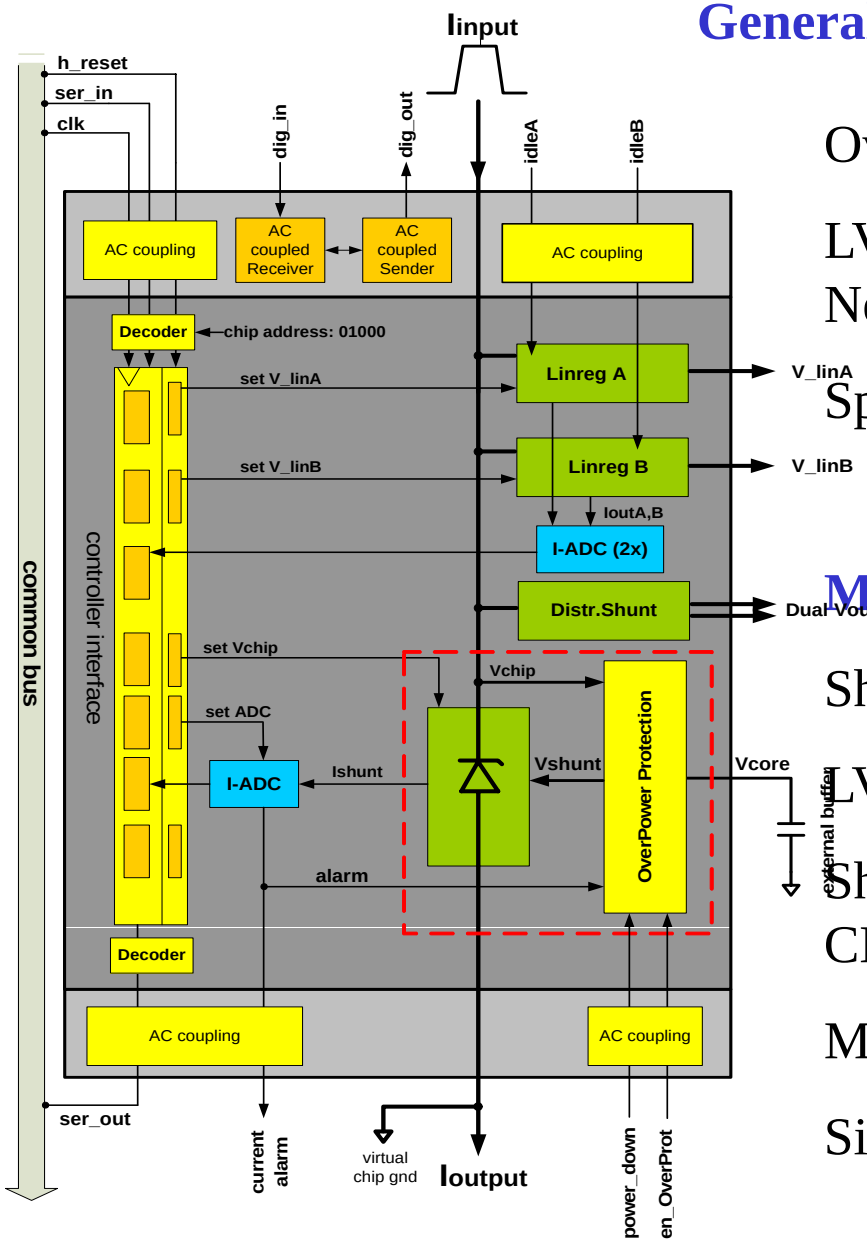
Just one shunt regulator and transistor



SR = Shunt regulator
Linear regulators and other connections omitted

Interlude: SPi chip

General purpose SP interface



Overall layout and design: Marcel Trimpl, FNAL

LVDS comports and stand-alone SR: Mitch Newcomer and Nandor Dressnandt, Penn

Specification and KE: Giulio Villani, RAL

Main blocks and features:

Shunt regulator(s) and shunt transistors;

LVDS buffers; over current protection;

Shunt current sensing ADC; TSMC 0.25µm CMOS with almost rad-hard layout;

Max. shunt current: 1 A design, “expected” >3 A;

Size: ~ 14 mm^2; flip-chip

Custom IC for DC-DC

1) DC-DC buck converter with gain (Vin/Vout) of ~10 (CERN)
2) DC-DC switched capapacitors with gain 4 (LBNL)
3) DC-DC switched cap for integration into ROIC with gain 2 (LBNL PSI, for now aimed at pixels)

4) DC-DC buck converter for integration into ROIC with gain 2 (CERN)

Integrated converters use standard CMOS processes which limits gain; higher gain devices exploit more specialized rad-hard processes; many encouraging irradiation results by CERN and LBNL

Q&A:

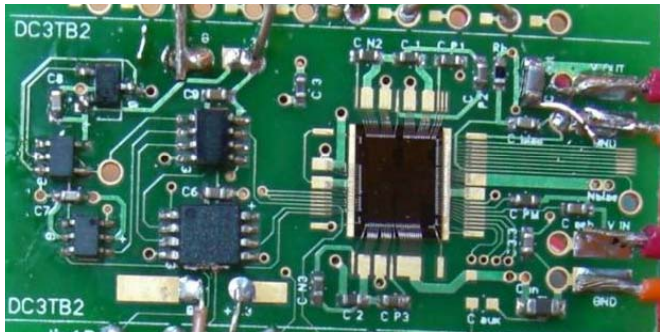
Do we need custom devices at all? Yes, due to magnetic field and radiation. Yale is following market developments and exploring commercial devices, but it would be far too risky to rely on those.

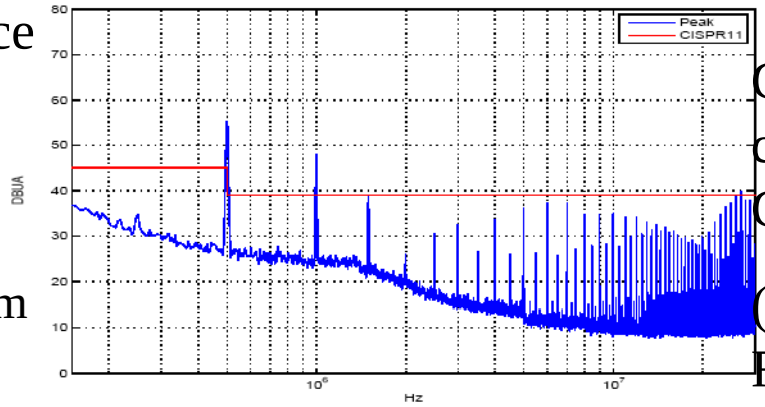
Why do we develop integrated and stand-alone devices? Integrated devices with high efficiency allow for 2-stage conversion (e.g. gain 4 x gain 2 = gain 8) and boost total gain. Integration is a good trend followed by all participants. It has enlarged the scope of the R&D, however.

Why develop both switched caps and buck? Approaches are complementary in terms of current capability, size, EMI.

Custom ICs for DC-DC

1. Custom, gain 4, DC-DC switching capacitors chip (Maurice Garcia-Sciveres, P. Denes, R. Ely)

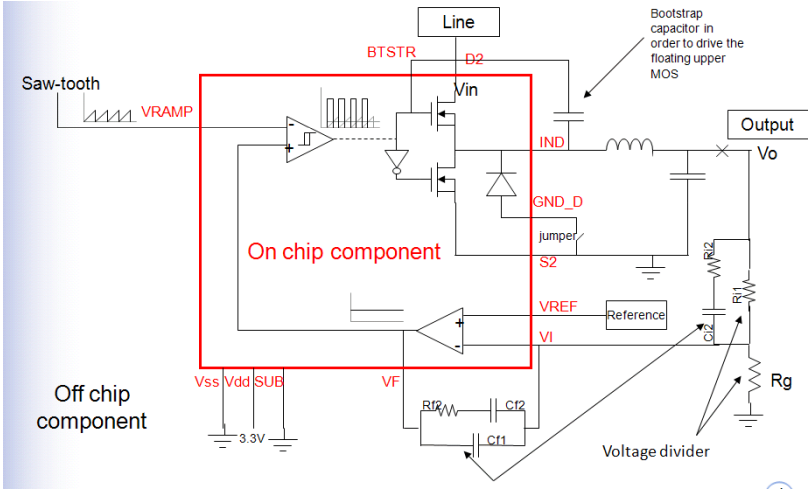




Common-model characterization in CERN test stand

(by Cristian Fuentes-Rojas)

2. Received custom gain 10 buck converter in June. AMIS 0.35 um (CERN)



3. Submit on- chip converters

(switched-cap LBNL, PSI, buck CERN)

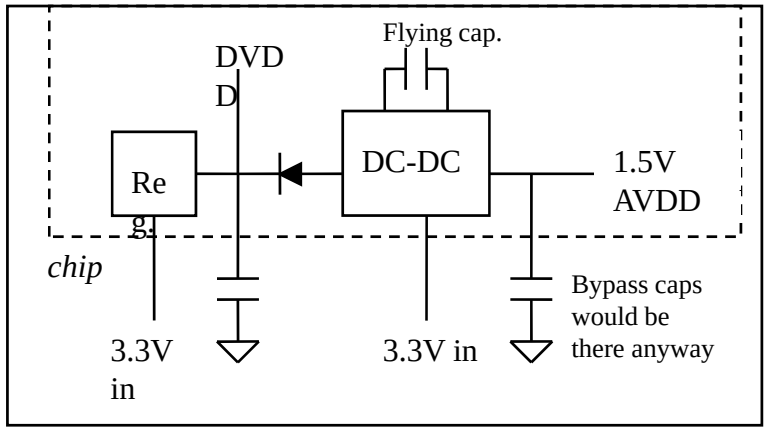
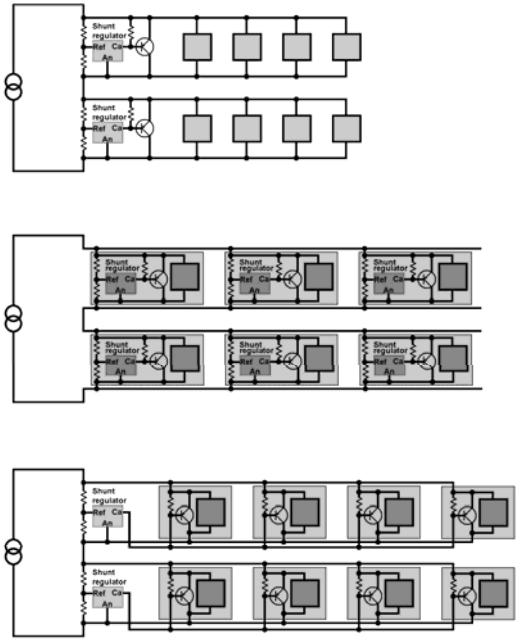


Figure 1: Block diagram of DC-DC converter and power-up/ loss of clock linear regulator

SP Plans

1. Finish tests with existing set-ups and 30 module stave (previous slides)



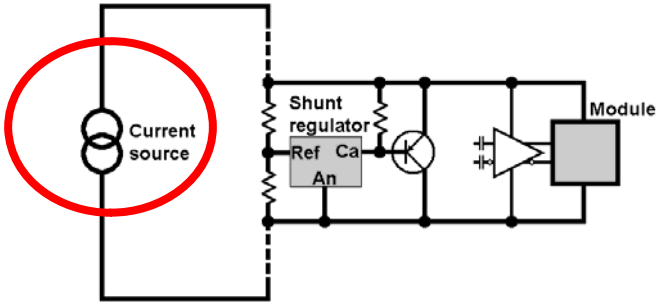
2. Get custom circuitry out

3 architectures; 4 chips:

ABC_Next, SPi,

FE-I4, Pixel LVDS chip

(Bonn, CERN, Cracow, LBL, Penn, FNAL)



3. Constant current source

(Prague: J. Stastny, RAL)

4. Characterize custom circuitry (RAL/strips; Bonn/pixel)

5. Build and test power plug-ins

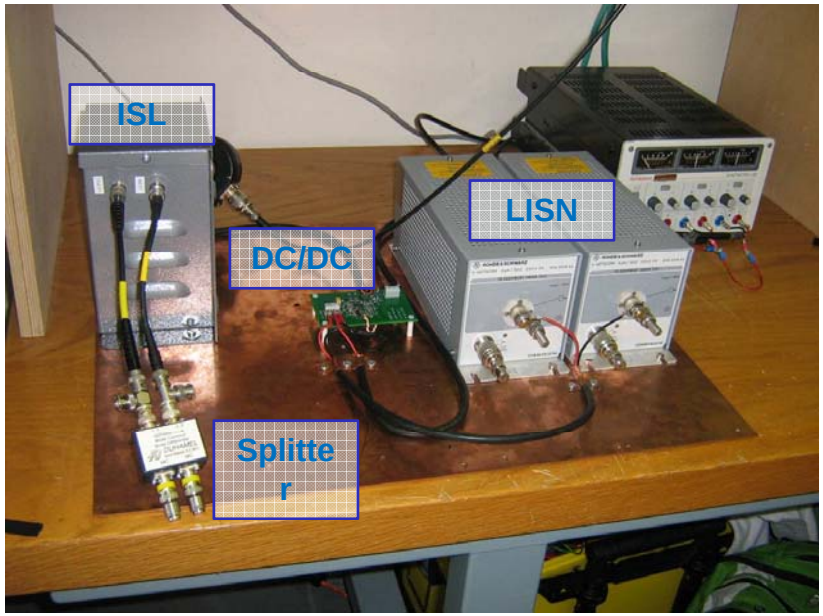
6. Develop commercial SP protection schemes

7. Use all this for next stave

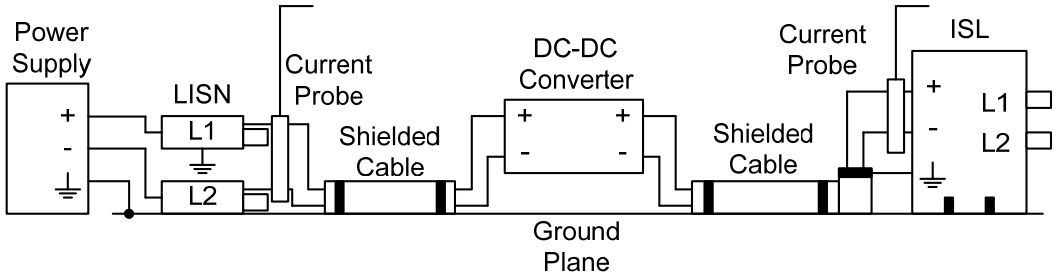
DC-DC Plans

1. **Understand EMI with commercial devices**
2. **Continuous market study and irradiation tests of commercial devices**
3. **Design, submit and characterize custom circuitry; use CERN test stand**
4. **Develop DC-DC system architecture**

   (e.g. 1 gain 10 converter vs. gain 2 times gain 4 converter stages
5. **Build and test power plug-ins for SLHC modules and staves**



CERN reference test stand



Powering activities within ATLAS

- Bonn pioneered work on serial powering for pixels many several years ago
- Power distribution working group started ~2 years ago. R&D was formally endorsed by ATLAS management. First review in February 2008

- Formal participants or interested parties:
  Bonn, BNL, CERN, Cracow, KEK, LBNL, NYU, ASCR Prague, RAL, SLAC, Wuppertal, Yale. Good collaboration with FNAL, good communication with CMS
- Some of us participate in the EU FP7 SLHC-PP power distribution work package (current members: Bonn, CERN, Cracow, PSI, RAL)

- ATLAS aims to cover all aspects of power distribution: SP and DC-DC; strips and pixels; commercial devices; custom designs and system aspects. We will discriminate between approaches, but –based on the ATLAS review recommendations- not at this stage.

Powering activities within CMS

- Powering is a big challenge for the CMS tracker upgrade
- Ramp-up of activities since 2007
- Tracker Power Working Group established in 2008 (contact: Katja Klein)
- Activities are currently focused on DC-DC conversion:
  - RWTH Aachen University (Lutz Feld):
    - Contribution to development and test of custom inductor-based DC-DC converter in coll. with CERN-PH-ESE (F. Faccio), e.g. development of converter PCB
    - System-test measurements with commercial and custom DC-DC converters
  - University of Bristol (Christopher Hill):
    - Focus on air-core magnetic components (e.g. air-core toroid) for DC-DC converters
  - PSI (Roland Horisberger):
    - On-chip CMOS step-down converter with switched capacitors
  - IEKP Karlsruhe (Wim de Boer):
    - Focus on powering-related aspects of cooling system and module layout
- CMS tracker is currently in the process of moving towards a realistic straw man → implications for powering activities are likely

HV distribution

There is also an HV distribution challenge since existing HV cable budget is too low if cables have to be reused

It is worse: HV cables would have to re-qualified for higher voltage (~800 V) and current ratings; before and after irradiation

There are only two options:

a) Reduced HV granularity with option to by-pass/short faulty sensors

b) local HV generation e.g. with step-up piezo transformer

I lack the time to discuss details. Work has just started

Summary

Have a big challenge to meet

Field gets the attention it needs: ~20 groups working actively on this as of today. There is a wealth of first results. You saw a few only.

Communication between ATLAS and CMS is good; good collaboration between power WP8 of EU FP7 SLHC-PP. I expect collaboration between experiments to increase to everyone's benefit

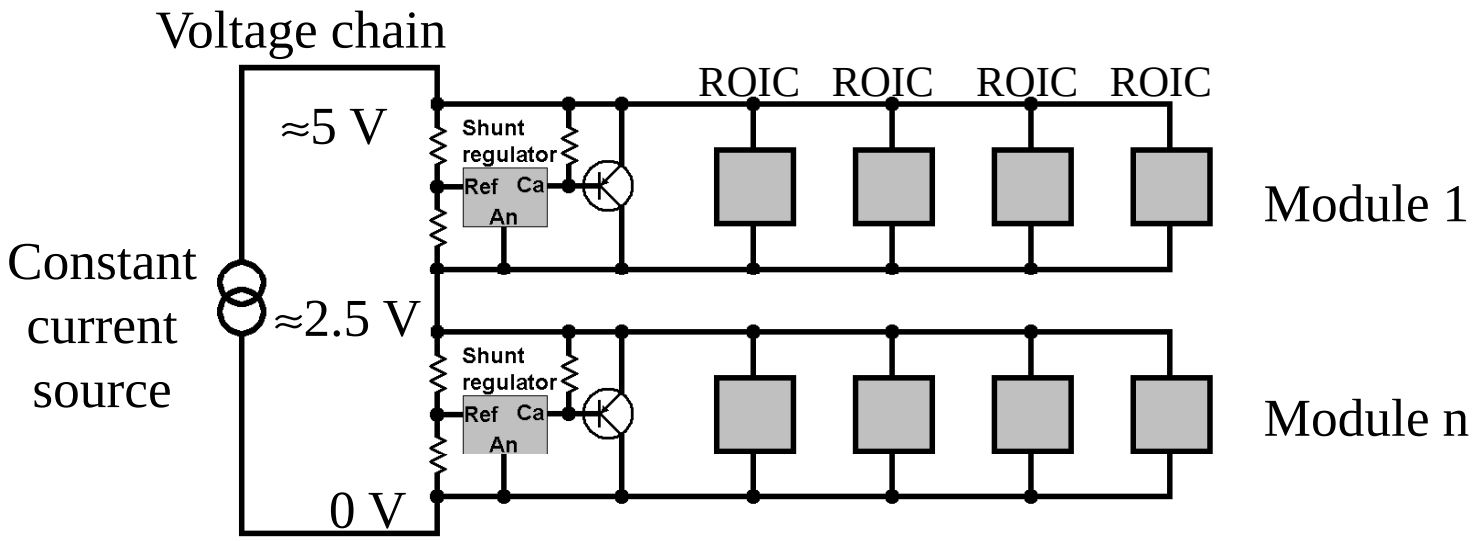
Several solutions are investigated in parallel, which is fine at this stage. The arrival of first working custom devices (this year) will bring us a major step forward. Then need to consolidate somewhat.

Work on system aspects has started (redundancy, protection, slow-control; integration; grounding and shielding)

Appendix

SP architecture choices

a) External shunt regulator + external power transistor



External commercial SR+ ST, used for RAL studies with SCT modules.

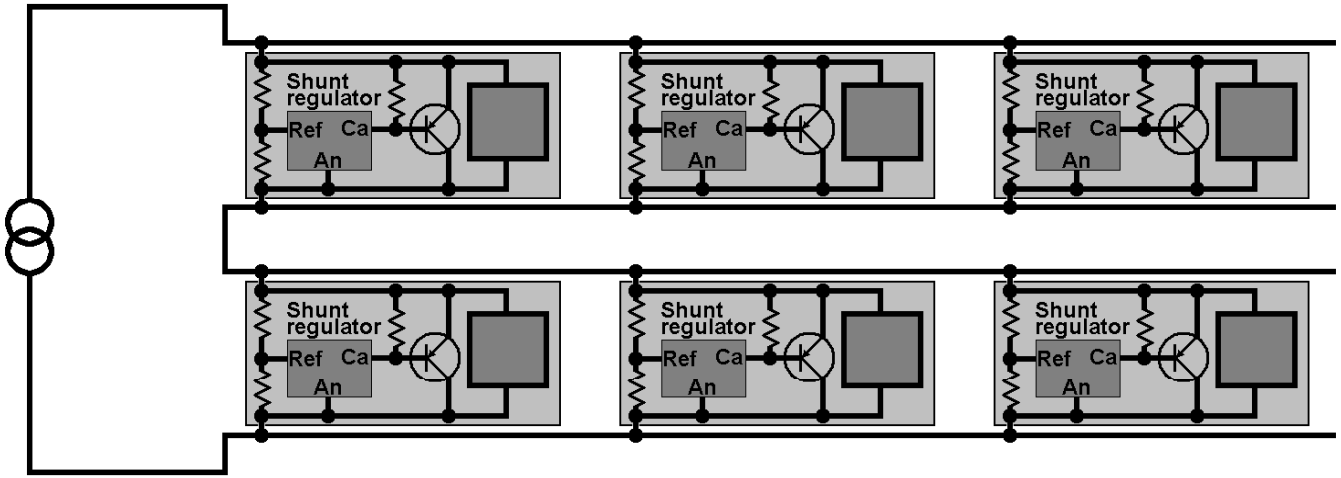
With custom electronics could be part of one chip.

This is good engineering, but implies a high-current device; limited expertise in HEP IC community.

We will test this with "SPi" stand-alone

SP architecture choices

b) Shunt regulator + transistor in each ROIC



Integrated (custom) SR and transistor designed by Bonn worked well for pixels.

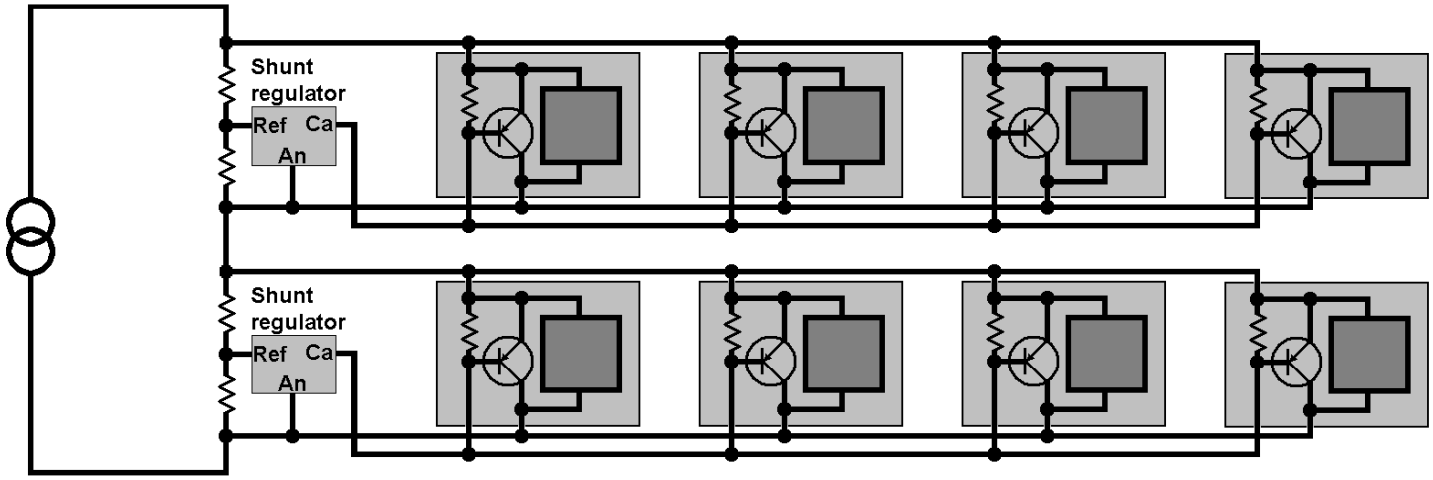
Many power supplies in parallel; Addresses high-current limitation and provides protection. Difficulty is matching and switch-on behaviour of shunt transistors. Must avoid hot spots that kill one shunt transistor after the other.

Wladek Dabrowski found an ingenious implementation for the ABC_Next

We will test this with ABC_Next (and SPi LVDS buffers)

SP architecture choices

c) External shunt regulator + integrated parallel power transistors



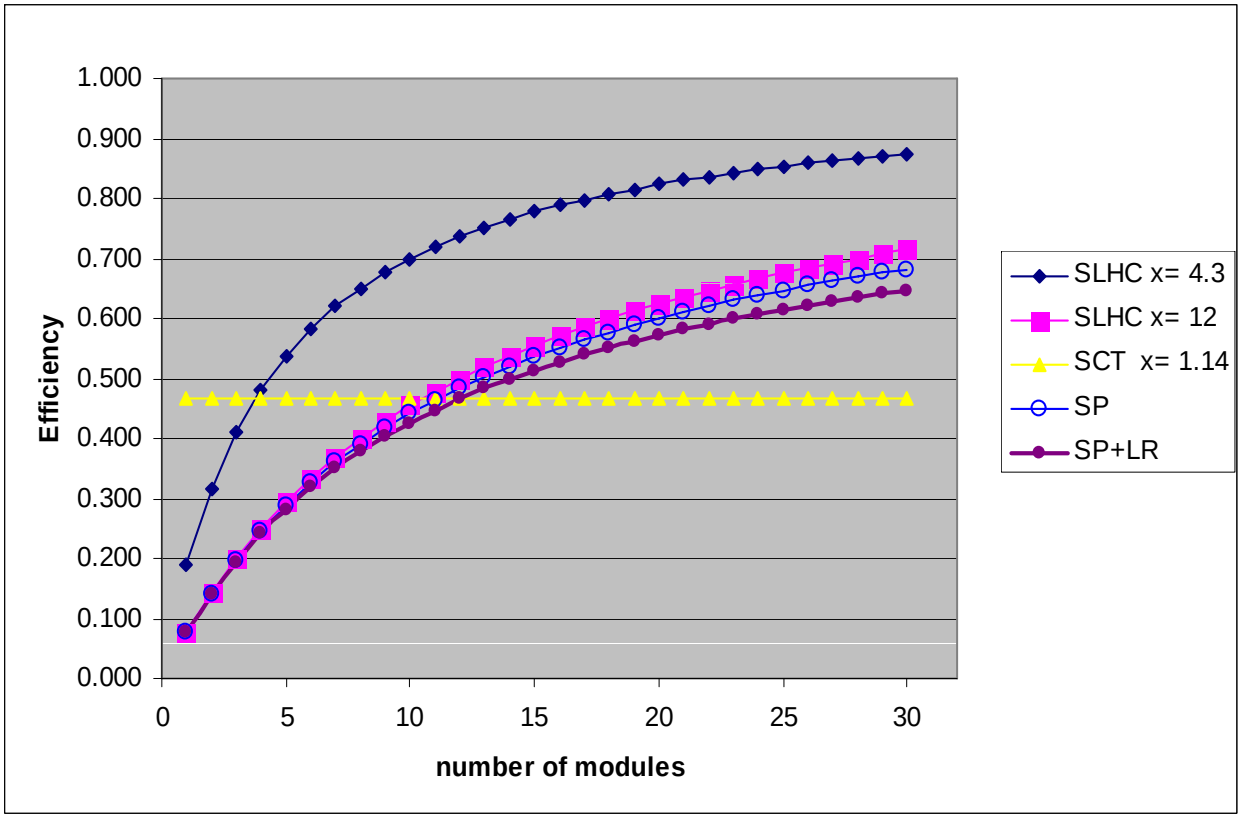
New attractive idea. Addresses high-current limitation. Conceptually simple. Need to understand how well distributed feed-back works. Design by Mitch Newcomer

Will test this with SPi (for SR and buffers) and ABC_Next (for ST)

Power efficiency for SP at LHC and SLHC

Illustration of various cases:

SCT ⇔ 4V, 1.5 A, R= 4.5 Ω ⇔ x=1.14; IP
SLHC ⇔ 2.5V, 2.4 A, R= 4.5 Ω ⇔ x=4.3; SP (only cable losses)
SLHC ⇔ 1.5V, 4 A, R= 4.5 Ω ⇔ x=12; SP (only cable losses)
same but including SR power and LR power (extrapolated from ATLAS SCT measurements)



Keep hybrid current low!

SR inefficiency ~7% for 10% digital current variation

LR for analog has similar losses

SR inefficiency is reduced for 0.13 μm CMOS

Features of IP and alternative schemes

	IP	SP	DC-DC	Comment
Power efficiency	10-20%	60-80%	60-80%	Varies with I, **n** (SP); gain (DC-DC)
Local regulator inefficiency	0%	~10%	<20%	This is without linear regulator for analog
number of power cables	4 per hybrid	Reduction by factor 2n	Reduction by factor 2n	**n** = number of hybrids
Voltage control over ind. hybrids	Yes On/Off; fine-adjustment	Stand-by mode: 2.5V/1.5V -> 0.7 V; Limited fine-adjustment	Yes On/Off; limited fine-adjustment	New schemes have regulators; no fine adjustment needed
Hybrid current info	Yes	Yes (sensing current through power device)	Yes	Some power penalty for DC-DC
Hybrid voltage info	Yes (need sense wires)	Yes	Yes	Not strictly needed, since regulators
Floating hybrid power supplies	Yes	No, voltage chain	No	
Protection features	Separate set of cables for each hybrid	Local over-current protection; redundant regulators	Don't know yet	Protect against open (SP) and short (DC-DC)

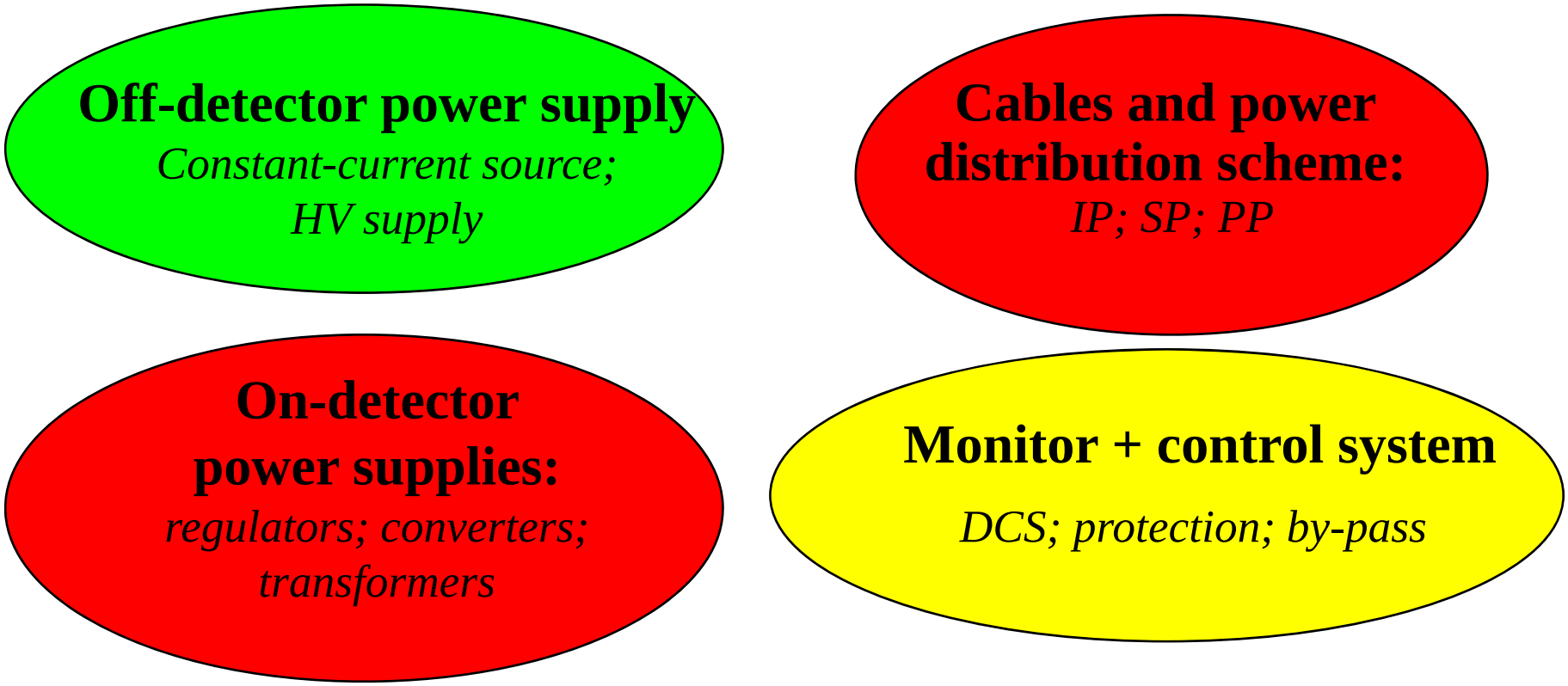
Let's preserve the good features of IP ⇔ **have voltage control, current monitoring, and protection features**

Hybrid power consumption

Short strips barrel	Typ.	Min.	Max.	**Pixels barrel**	Typ.	Min.	Max.
# of hybrids per barrel stave (top side)	**20**	10	20	# modules per barrel stave	**~12 ?**		
# of ABC_Nexts/hybrid	**20**	20	40	# of FE/module	**4**	1	10
Hybrid voltage	**1.5 V**	1.5 V	2.5 V	Module voltage	**1.6 V**	1.5 V	1.8 V
Channels/hybrid	**2560**	2560	5120	Channels/ 4 chips module	**82000**	75000	90000
Hybrid power	**~4 W**	~4 W	~14 W	Hybrid power	**7 W**	6 W	9 W
Hybrid current	**2.8 A**	2.8 A	5.6 A	Hybrid current	**4 A**	3 A	5.5 A
Voltage across SM for SP	**30 V**	15 V	50 V	Voltage across stave for SP	**20 V**	18 V	30 V
Total power per SM (both sides)	**160 W**	160 W	280 W	Total power per barrel stave	**~84 W?**		

- Pixel and strips target same technology (at least at this stage)
- **Pixel and strip module power consumption are similar**
- Currents are still rather high, in particular for pixels

Elements of power systems



IP: independent powering; *SP: Serial powering;* *PP: parallel powering*

Developing on-detector supplies and understanding cable budget is most urgent, but we need all elements eventually

Need to understand how elements come together in a system

Latching Switch (Transistor Shown) for SP

- Shown is representation of serial shunt regulator power with protection.
- The alternate current path provides protection against an OPEN circuit and over-voltage on module. Typical response time is < 1 msec
- Addressable Switches would allow external turn-on of the alternate current path isolating the module. Signal would be isolated from module
- This arrangement has been tested with some success. The transistors latch in either an over-voltage condition or when activated with the addressable switch.
- Parts for testing are readily available.
- Failure of protection components might disable the module but would not threaten other modules.