Advanced Semiconductor Technologies for SLHC

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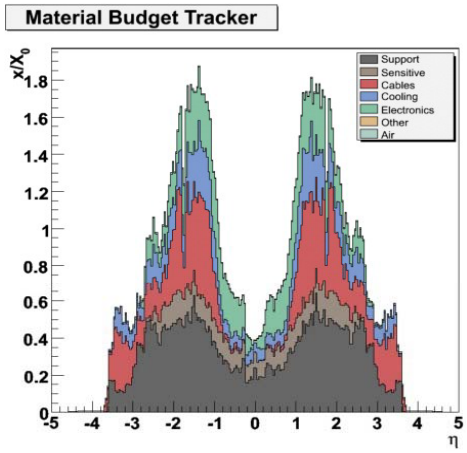
Motivations

- SLHC needs more advanced technologies because:
  - Power dissipation must be reduced to build better physics detectors
    - Ultimately, material budget is limited by the power to be carried to and removed from the front-end channel
  - New improved functionality can only be achieved with higher integration. Examples:
    - CMS trigger with tracker info
    - Higher bandwidth data links (to achieve lower cost/bit at high rate)
  - Demand for Radiation Hardness will increase and newer technologies are expected to work better
  - Obsolescence of older micron

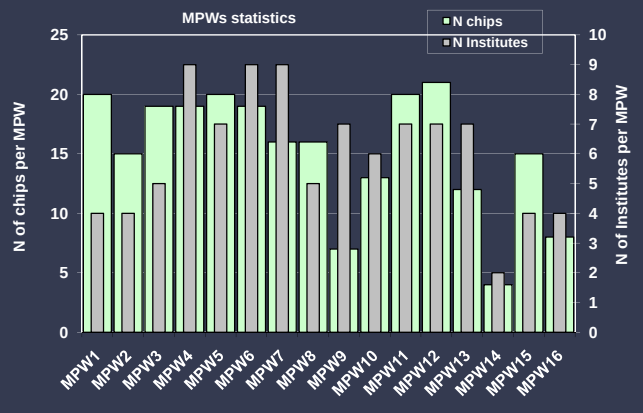
Power and material budget



Why central support?

- Development cost for products in new technologies (not production cost!) is increasing exponentially
- Common projects are mandatory to share:
  - High development cost
  - Difficult engineering challenges (HEP has many small design groups)

Multi-Project-Wafer (MPW) activities



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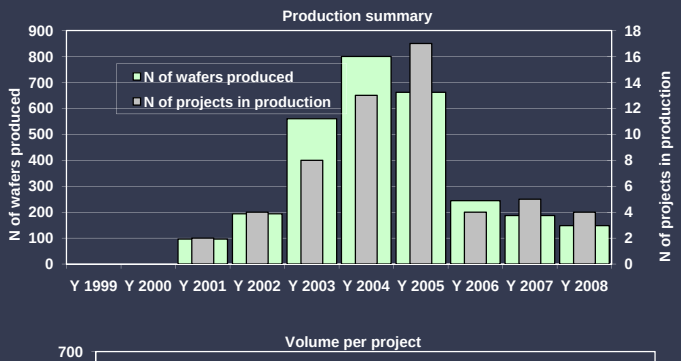
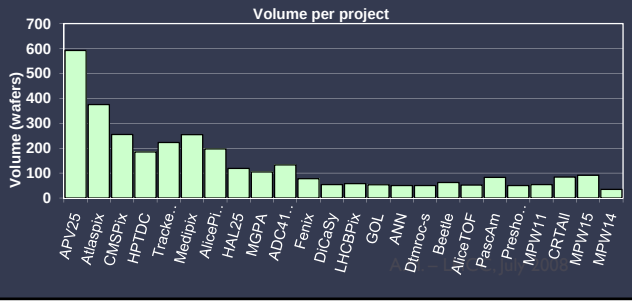
Support Activities: Submissions





Which technology does HEP need for SLHC?

… and where are the others?

Technologies used in state of the art industrial application

Which technology and when

- Scenario A): SLHC in one single big upgrade after2017
  - Assuming final designs done around 2010-2011, 90 nm and beyond are very advantageous
  - 130 nm to be used as learning tool for designers
    - It is NOT easy to migrate directly from ¼ micron to 90 nm in one step!
- Scenario B): SLHC in a series of intermediate evolutionary steps
  - First demonstrators and prototypes or intermediate solutions can profit from the 130 nm generation
  - Final upgrade solutions can be further optimized using 90 nm and beyond

If 130 nm is good, why is 65 nm better?

- ADCs are good indicators of circuit and technology progress in mixed-signal chips
- Standard metric to characterize them is the:
  FOM=Power/($2^{Neff} * f_{sample}$)
  which is constantly progressing:

	.25 um (FOM=@ 1 pJ/conv)	65 nm (FOM=@50fJ/conv)	Saving in PS Units(@5 CHF/W)
Atlas Calo 200K ch, 16 b, 40 MHz	262 KW	13 KW	>1 MCHF
ILC Calo 15M ch, 14 b, 50 MHz	6.4 MW	.34 MW	Very Big !!!

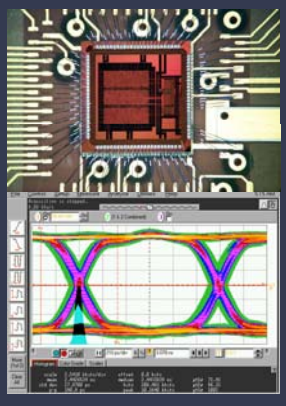
Summary

- μ–electronics is a key enabling technology for modern detectors
- The reference environment in this technology is industry and (unfortunately) not the HEP physics labs
  - We need to have well trained people capable of speaking industry's language, to maintain respectability in their world, to translate their technologies into the HEP world
- HEP must maintain a few strong labs with enough critical mass to
  - Provide tools and technologies for the community
  - Serve as catalyzer for common projects
  - Be accepted as reliable (and commercially non-negligible) partners by industry
- Continuous investment is necessary at CERN to seed others

Export of advanced Technology from US

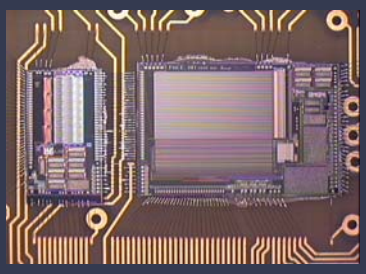
- The export of advanced CMOS technology and related designs will be severely restricted under US law if the ASICs designed with them are proved to be potentially useful for military purposes
  - Even moving to a non-US based foundry, the problem remains a serious one because the US component of HEP is a very important one and they would be excluded anyway
- A delicate negotiation is undergoing between the US State Department and the users (= CERN, foundry, DoE and the US Labs and Institutes)
- Various solutions are being explored (involving some compromises on performance and/or functionality)
- CERN DG recommends that a solution is found by end of '08 as not to delay new R&D work for SLHC

Microelectronics Projects @ CERN

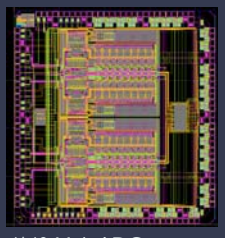


GOL: 1.6Gb/s serializer

K-Chip



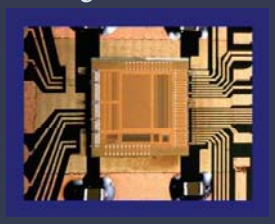
PACE: Pre-shower readout



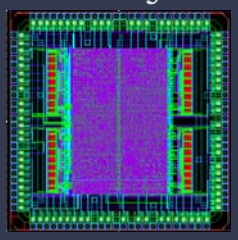
4*40 Ms/s ADC

TTCrx

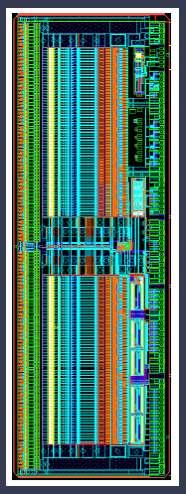
Projects from HEP community



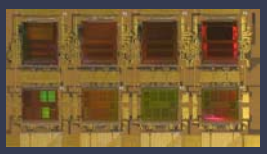
APV25: RAL & IC



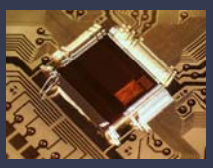
Carlos: INFN Bologna



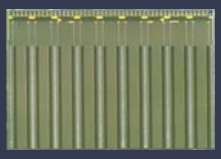
HAL25: Strasbourg



Pascal &Ambra: INFN To



Beetle: Heidelberg



Atlas Pixel: LBL

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Current Projects

- Technology Support
  - Technology Validation for 130 nm and 90 nm
  - MPW organization
  - Design methodology support
- IP Blocks in 130 nm
  - General purpose analog and digital blocks for complex ASICs
- Fast Optical Links
  - Bidirectional, all purposes optical link
    - GBT13: 4.8 Gb/sec in 130 nm
    - GBT90: 10 Gb/sec in 90 nm
- Powering
  - Design of rad-tolerant, high efficiency DC-DC converter for future tracker
- Gigatracker
  - Very Fast, high rate pixel detector with integrated TDC
- S-Altro
  - Compact readout for TPC and Gas detectors with enhanced digital processing
- Medipix
  - Medipix3, TimepixII, DosePix

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Technology Support

- SLHC FE electronics will be based at least on 130 nm technology and beyond
  - To ameliorate detectors, substantial improvements are necessary in the power/channel characteristic of FE ASICs
  - New detectors become conceivable when better technologies become available.
    For example, new ADCs with very low power consumption (100 times better than current) can allow radically new detectors
- Current CERN responsibilities
  - Interface with foundry Supplier
    - Contract for entire community
  - Organization of common and dedicated submissions
    - Share mask costs whenever possible
  - Technical support
    - Training and Design assistance
    - Design kit for full design flow: analog and digital
    - Library
    - Tools