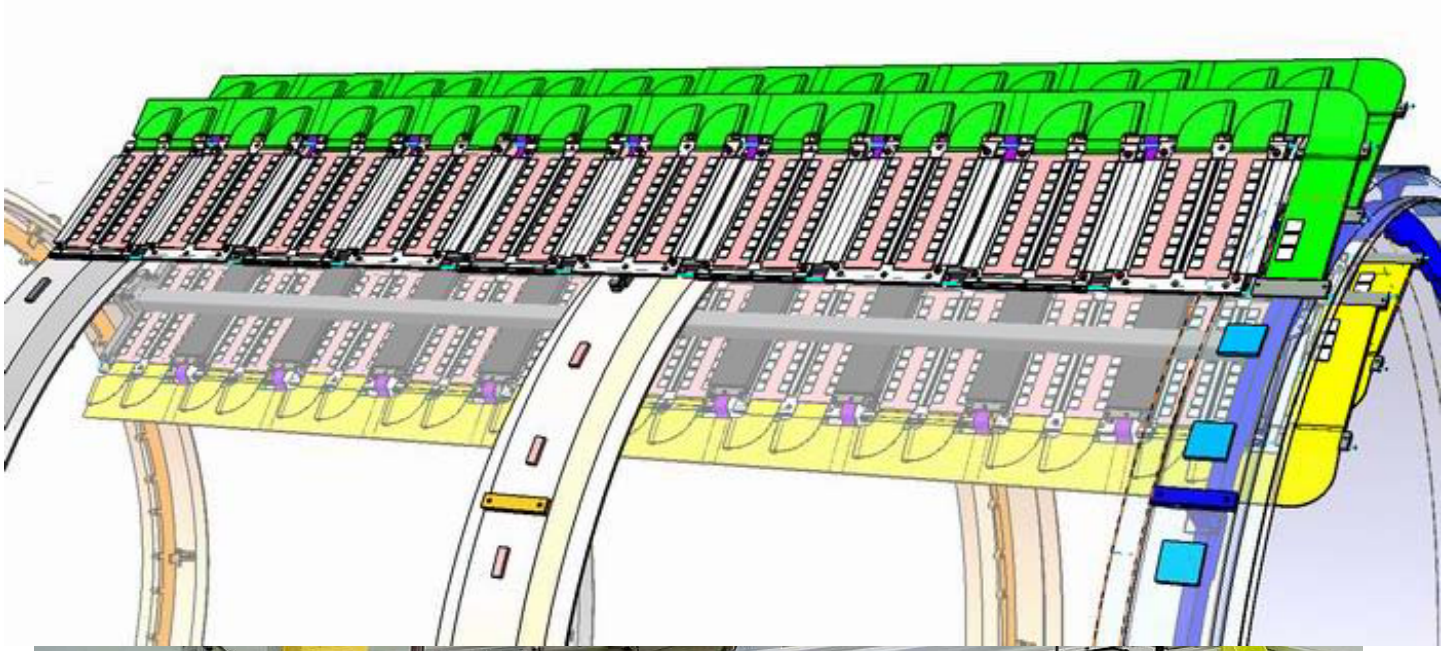
ATLAS Silicon Strip Tracker Upgrade

LHCC Upgrade Session

CERN, July 1st 2008

D. Ferrère, University of Geneva

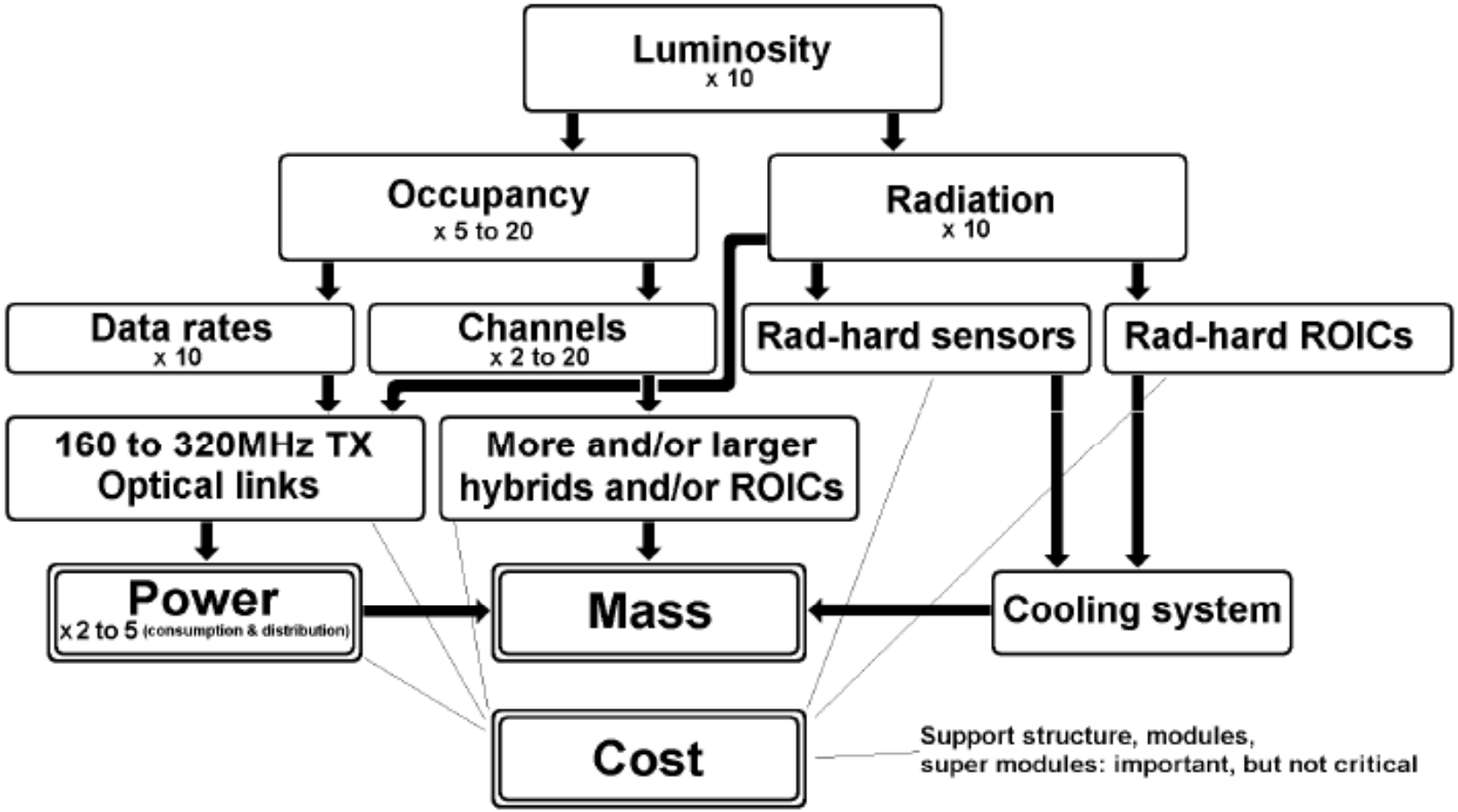


What are we considering for the ID Upgrade

- **New ID layout:** Only silicon pixel and strip detectors
- **New detector technology:** n-in-p
- **New ASICs technologies:** 250 nm →130nm or 90 nm
- **Cooling with more headroom:** Silicon temperature below -20°C
- **New biasing scheme:** Serial powering or DC-DC for parallel powering
- **Faster readout:** FE asics and data transmission link (5Gb/s)
- **Module integration will be grouped** on a stave or a super-module structure → performances
- **DCS is proposed to be integrated into the readout architecture**
- Main engineering requirement: **Assemble and commission the complete ID in a surface building**. B-layer could be inserted separately together with the beam pipe.

All the working group has to keep in mind the detector challenges at SLHC…

The ID challenges at SHLC



From M. Weber

ID Upgrade - Layout

The goal for b-layer replacement is fall 2012

Actual b-layer is expected to survive 3 years at LHC design luminosity (~300fb^{-1})

The Upgrade of the entire tracker should take place in 2016

Strawman 06 → 07 → Fixed length barrel

Including disks this leads to:

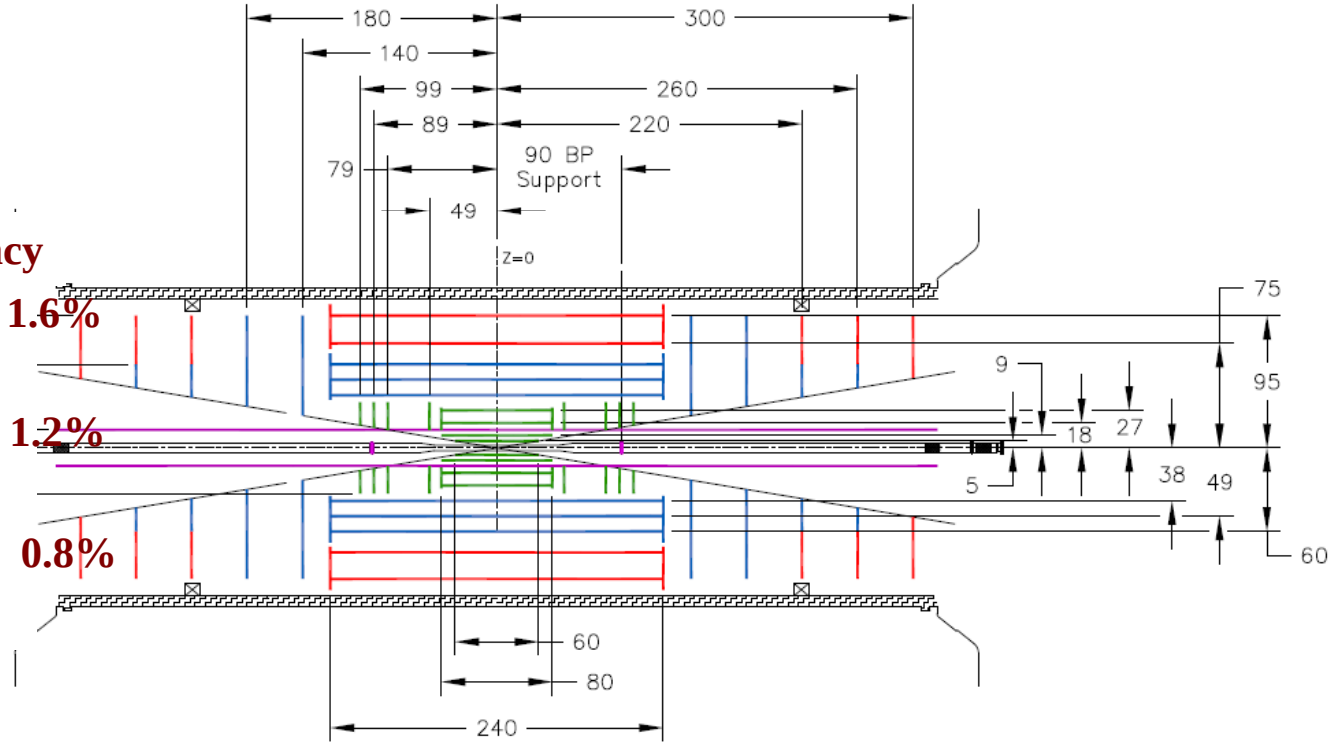
Pixels: 5 m^2, ~300,000,000 channels

Short strips: 60 m^2, ~30,000,000 channels

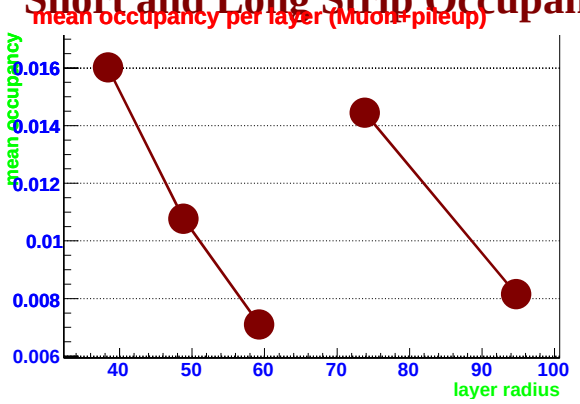
Long strips: 100 m^2, ~15,000,000 channels

long strips (~10 cm x 80 µm)
short strips (~2,5/5 cm x 80 µm)
pixels

V13–Fixed Length (Proposed)



Short and Long Strip Occupancy

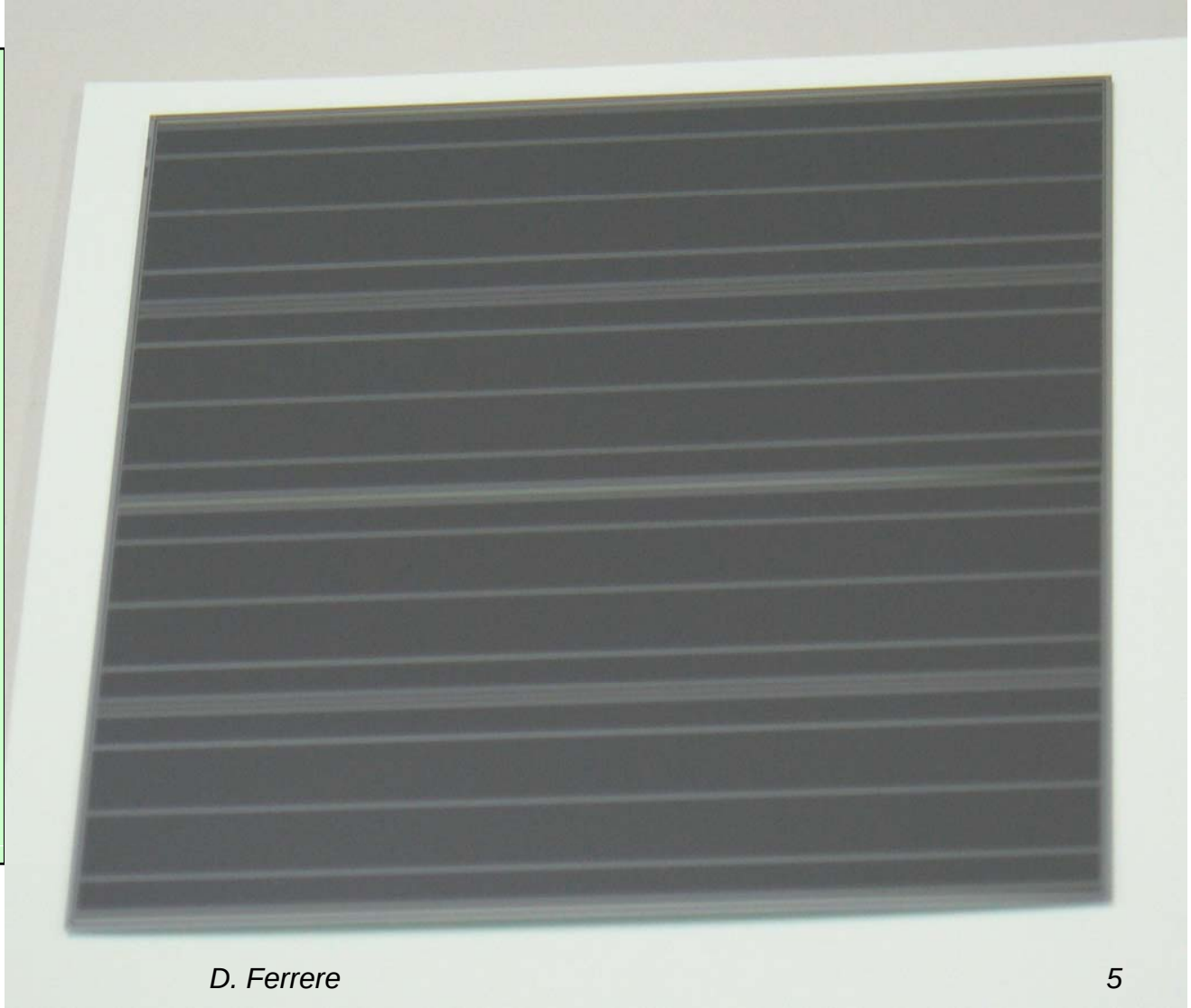


Short Strip Sensors - HPK

- Strip segments
  - **4 rows of 2.38 cm strips (each row 1280 channels)**

130 detectors ordered end of last year (~360 kCHF)

- **Dimension**
  - **Full square**
- **Wafer**
  - **150 mm p-type FZ(100)**
  - **138 mm dia. usable**
  - **320 µm thick**
- **Axial strips**
  - **74.5 µm pitch**
- **Stereo strips**
  - **40 mrad**
  - **71.5 µm pitch**
- **Bond pads location**
  - **accommodating 24-40 mm distances**
- **n-strip isolation**
  - **P-stop**
  - **Spray on miniatures**



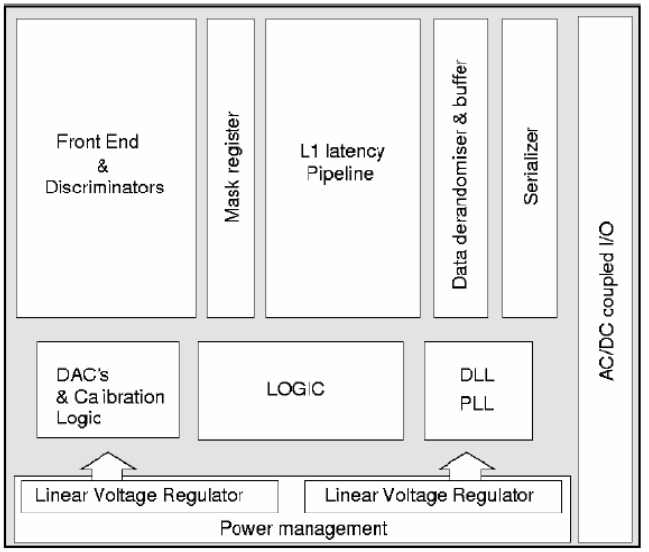
FE Readout for Strip Upgrade

Goal: Prepare a design of the FE ASIC in deep submicron radiation tolerant. Design and evaluation with 250 nm towards 130 or 90 nm technology

Minimum requirements:

- Implementation of an on-chip shunt regulation to allow any powering scheme (Serial or DC-DC)
- Increased data bandwidth up to 160 Mb/s → 80 Mb/s
- Compatibility with existing ATLAS SCT DAQ ROD hardware
- Front-end for two signal polarities, 3 to 12 cm long silicon strips
- Minimum power circuit techniques
- Delay adjustment for control and data signals
- Similar "core" functionality as for the present silicon strip tracker: signal amplification, discriminator, binary data storage for L1 latency, readout buffer with compression logic, and data serializer.

ABC-N Readout architecture

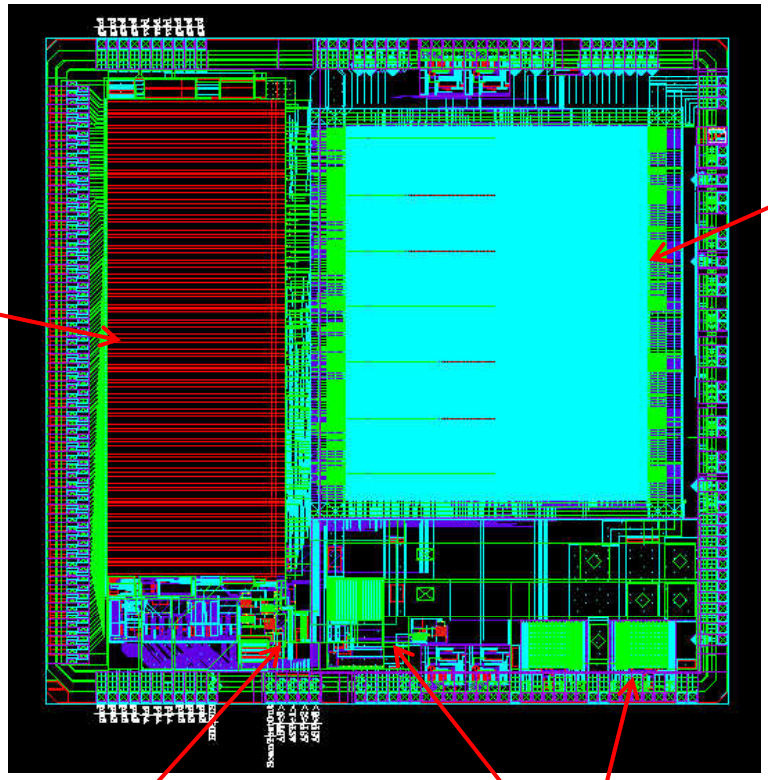


Submission is imminent: Engineering run should be delivered in less than 13 weeks
Order for ~140k$: 2-6 wafers of an engineering run + 24 production wafers (400 chips/wafer)

FE Readout for Strip Upgrade

ABCN : FRONTEND Development in 250nm technology

128 Channels Front-End opt. for Short Strips 0.7mW/channel



Digital part : reuse of existing SCT protocols, SEU protections, 80Mbits/sec output rate, power control , 2mW/channel @2.5V

ABCN 250nm is an intermediate version of the FE chip for modules prototypes developments

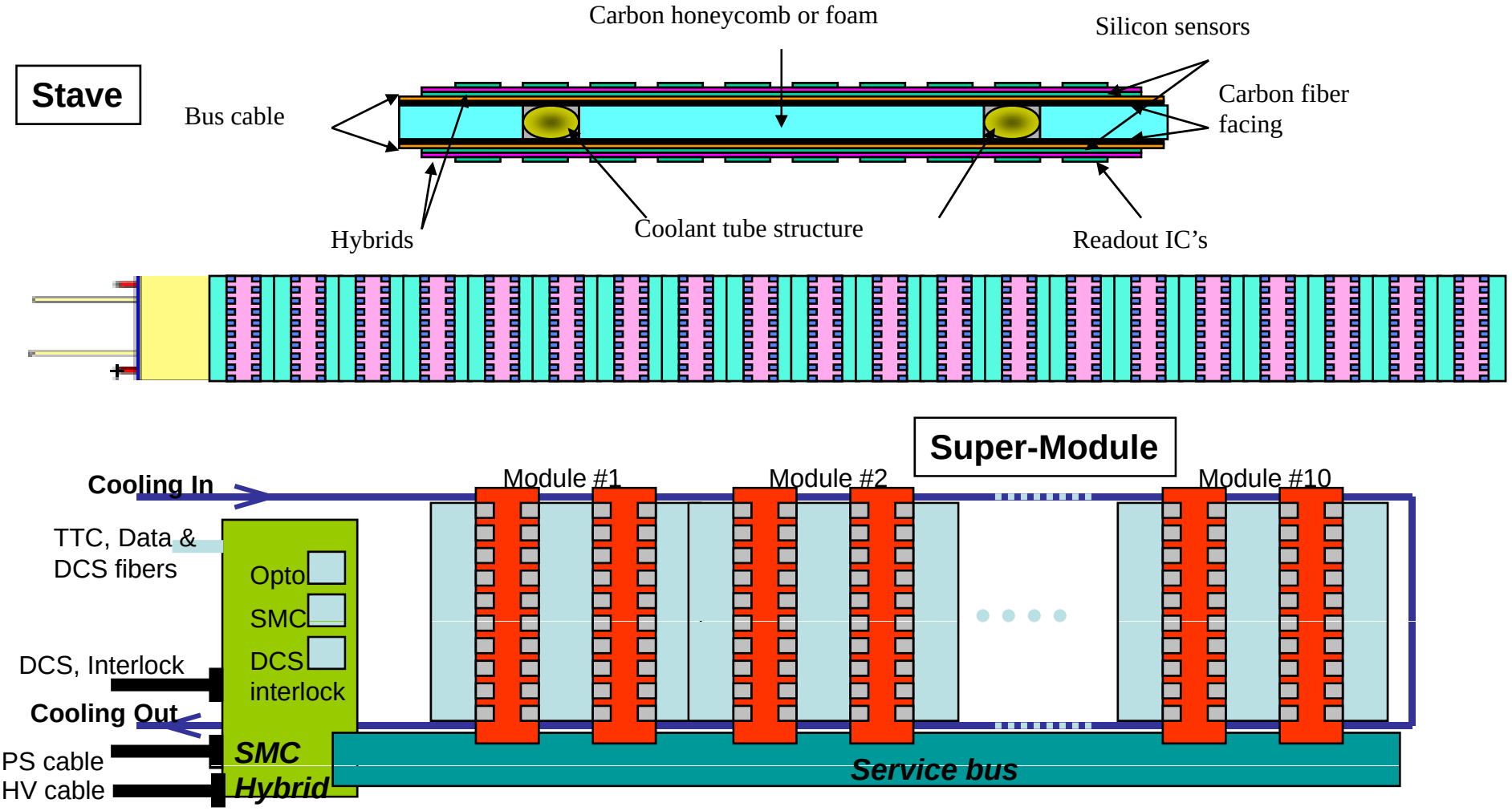
From F. Anghinolfi

Serial regulator to provide analogue from a unique digital+ analogue power source

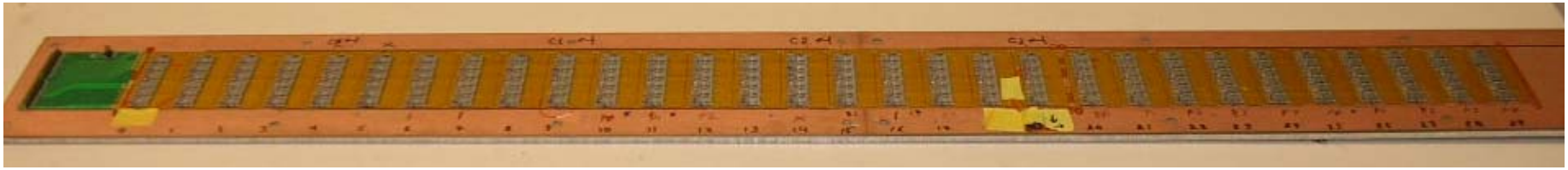
Shunt regulators (2 options) to exercise 2 different serial powering systems

Module Integration

Powering and readout are grouped for several modules and a pre-integration is considered on a ~1m long stave (or Super-Module).

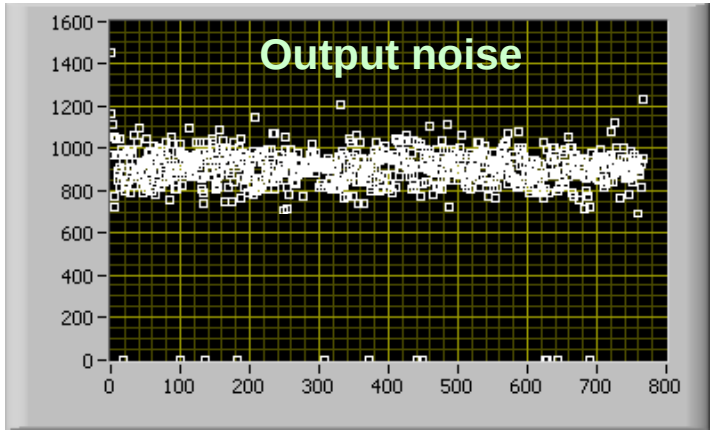


Electrical Prototypes



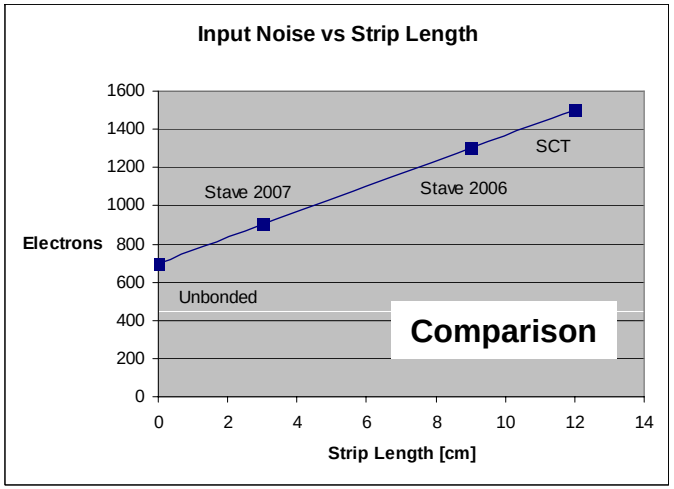
30 modules with ABCD & serial power
(ABCnext will be 30 V)

From C. Haber (LBNL)

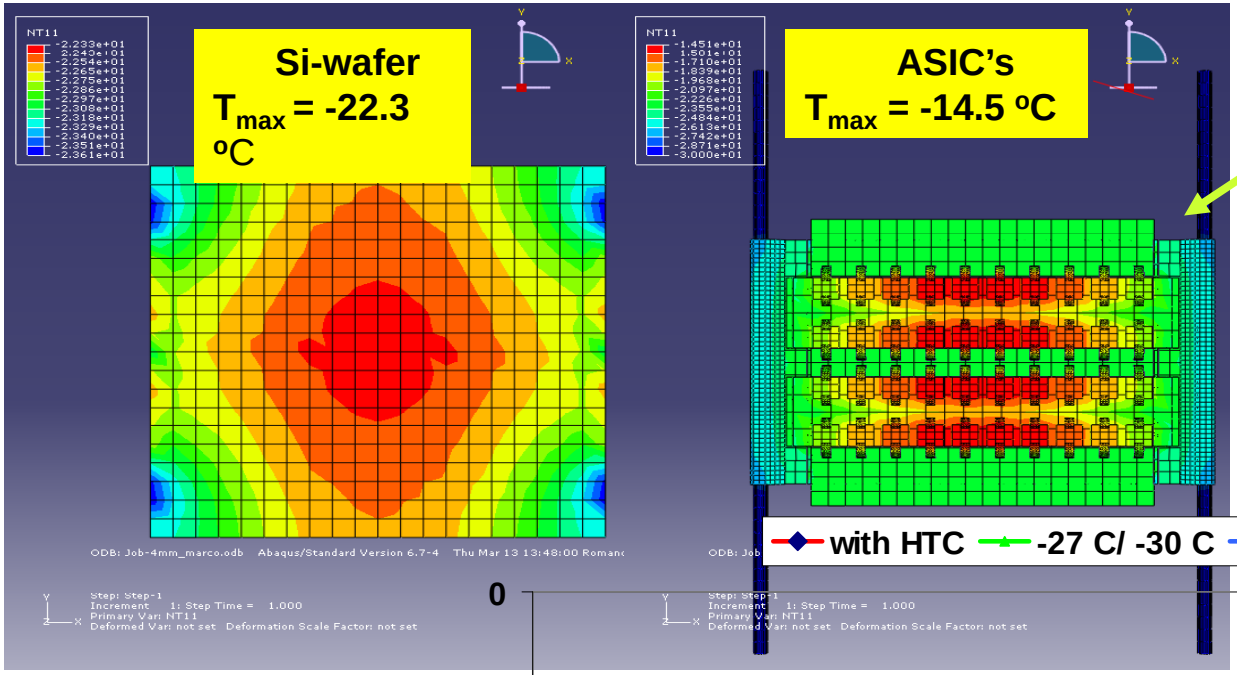


Ceramic hybrid directly glued onto Silicon

2 adjacent modules glued on a stave



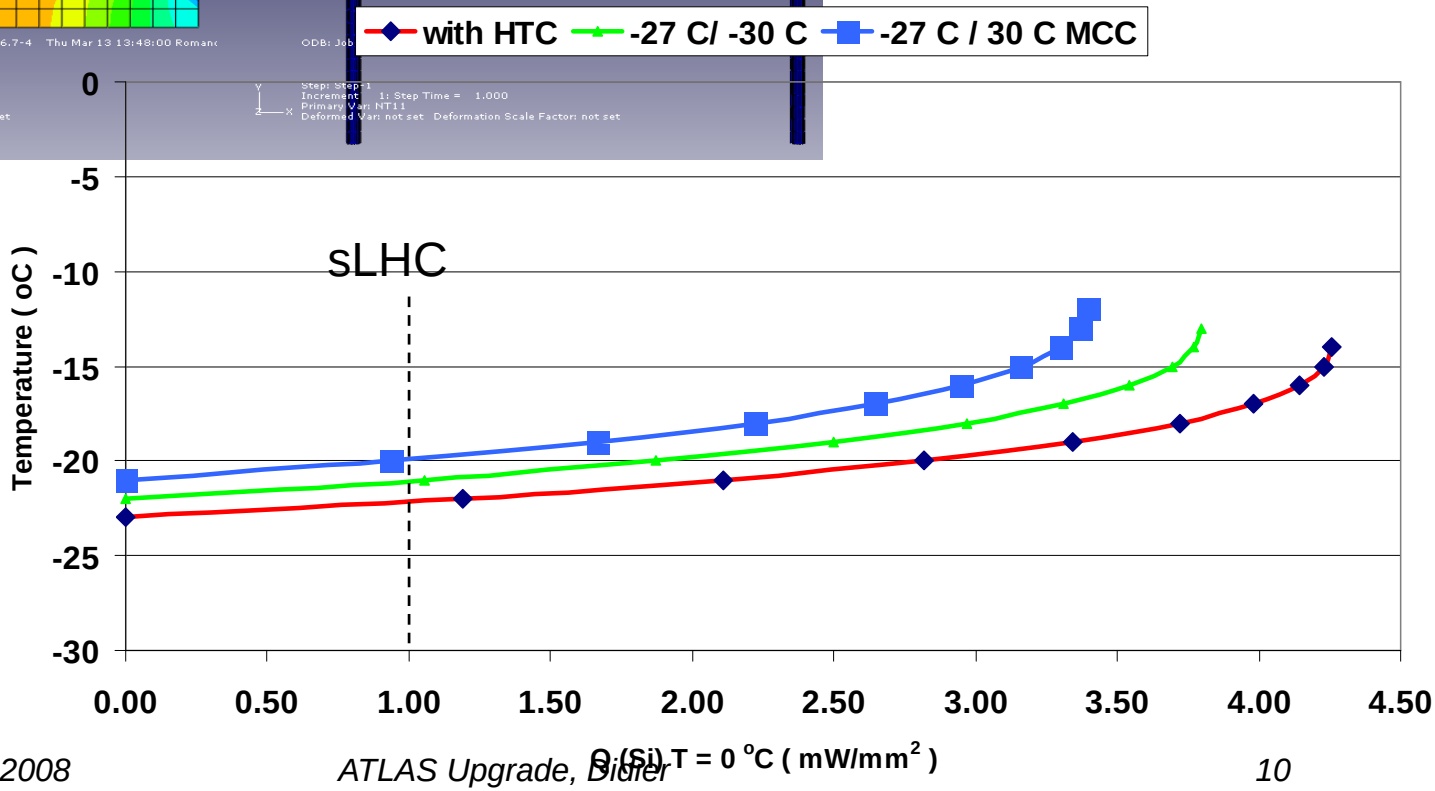
Module Integration – Thermal FEA



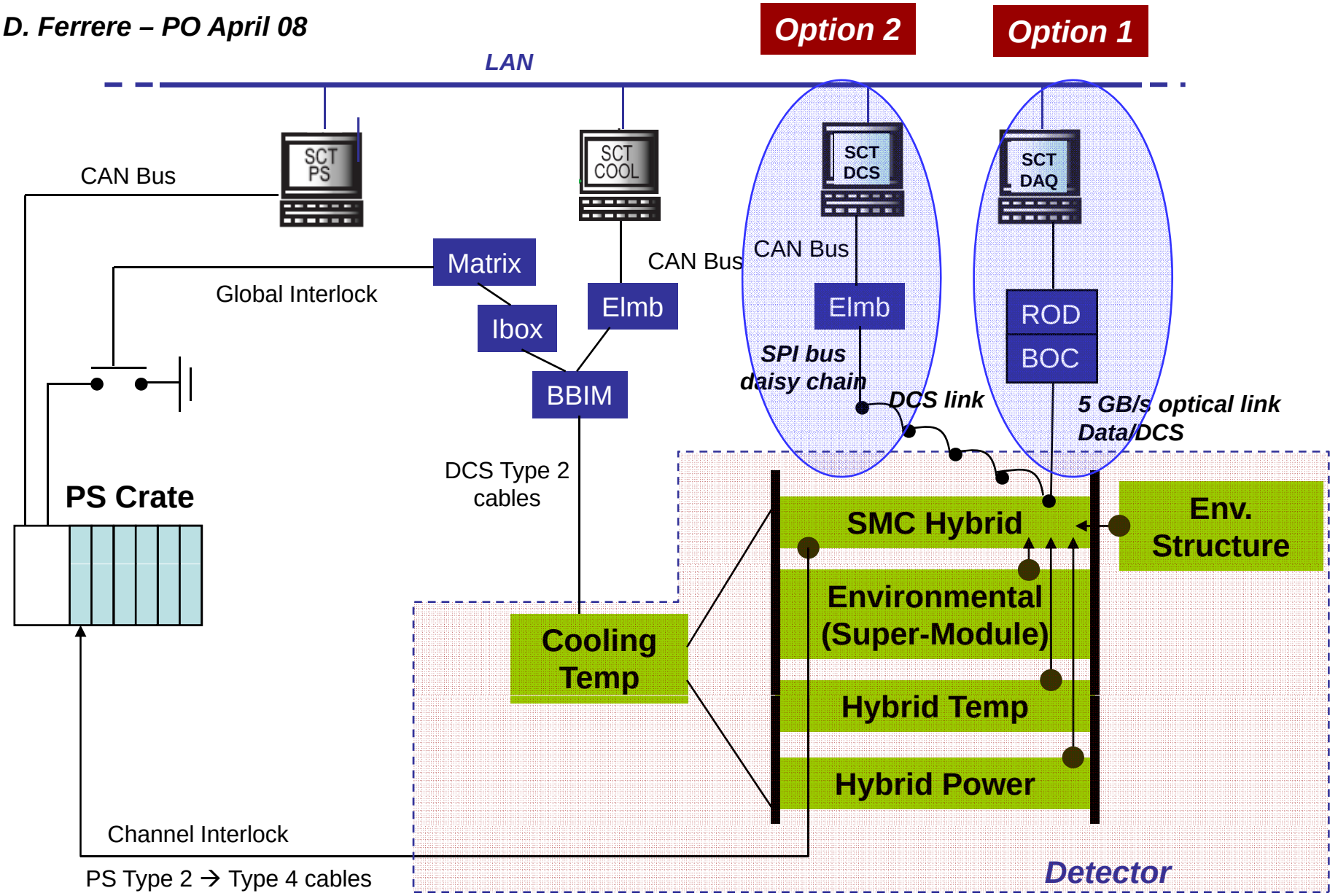
K.P. Streit Preview 05.06.2008

Double-sided Module: 24W

Excellent performance with respect to the thermal runaway



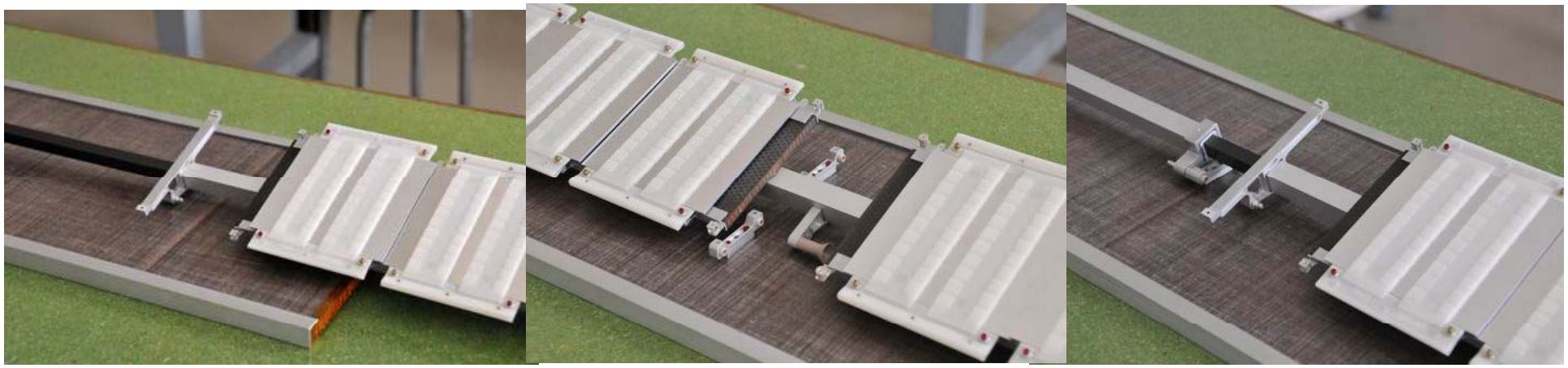
Proposed DCS Architecture



End-insertion Stave/SM

- ***Flexibility:*** Barrel structures can be assembled before the SMs are integrated → Flexibility of the assembly procedure
- ***Time saving:*** No need to test a fully populated barrel after another and then integrate the 5 barrel layers → Time saving about ~1 year (2-3 months per layer)
- ***Parallel work:*** Assembly of the structure can be done in parallel with the SM/Stave production. Time saving can be considered!
- ***Rework:*** The rework or replacement of a SM could occur even late (even after the commissioning). But when final services installed access is difficult!
- ***SM/Stave replacement*** could happen in any working area (few light jigs).

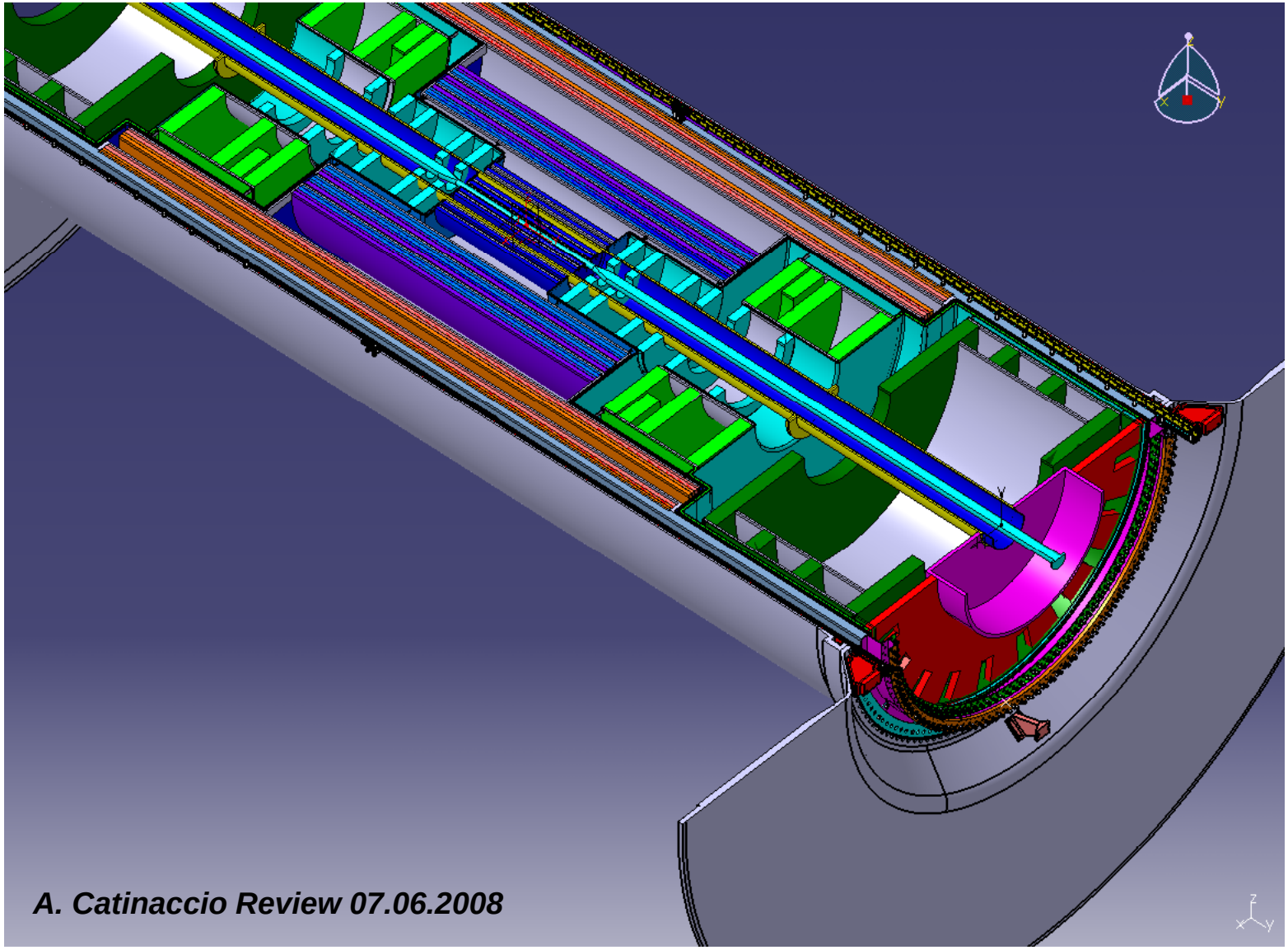
End-insertion concept presented to work fine with a mockup demonstrator (June 4th 2008)



D. Ferrere – Preview 05 Jun 08

Module Integration – Engineering

1 single ID element Integrated and commissioned at the surface building



Conclusions

- ***ATLAS is considering to be ready with an Upgrade detector from 2016***
- ***The ATLAS ID will be completely renewed and is in a design and specification phase***
- ***The major challenges are: Service and material reductions, Cooling, Powering scheme, schedule, …***
- ***Significant efforts in working groups started to tackle all the new challenges***
- ***Frequent working meeting organized and review sessions processed***
- ***The evaluation of the new sensors technology, the FE Asics and the module electrical functionalities will be a major step in the near future***
- ***Next event:***
  - ***ID Upgrade Workshop Nov 2008 at Nikhef***