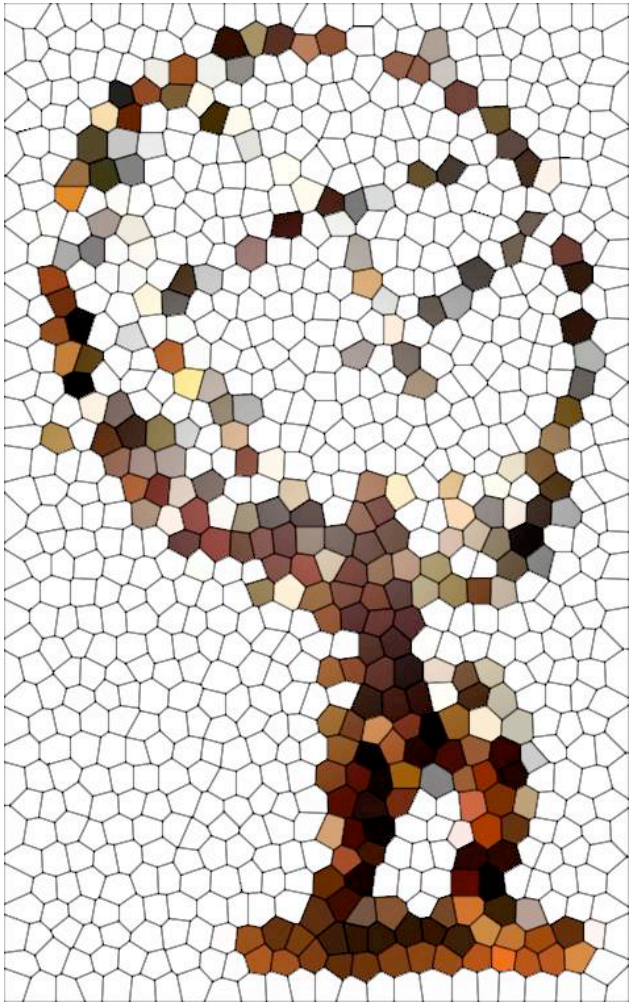
Pixel/B-layer Developments

LHCC Upgrade Session

CERN, 1 / 7 / 2008

G. Darbo - INFN / Genova



Agenda Page:

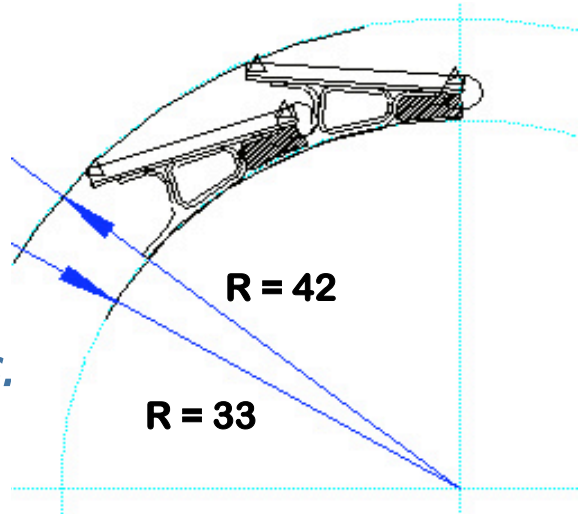
http://indico.cern.ch/conferenceDisplay.py?confId=36149

B-Layer Replacement

- B-layer replacement in 2012 shutdown:
  - *Detector designed for 300 fb^{-1}, could probably withstand to 400fb^{-1} or a bit higher with reduced efficiency;*
  - *integrated dose acceptable even with margin of error until 2013, but not until 2016*
  - *Details are very dependent on operating conditions (temperature, warm-ups)*
  - *Hard detector failures requires to have a replacement*
- Replacement scenarios (B-layer task force):
  - *B-layer cannot be replaced in a long shut down (8 months) – requires extraction of the pixel package, opening the whole detector (also beam pipe cannot be extracted without opening of pixel package -> special tooling and procedure to make in situ)*
  - *Other options as a simpler 2 hit system with present technology (case of disaster) not realizable (collaboration to make, spares not available)*
  - *Study the insertion of a smaller b-layer and a smaller beam pipe inside the existing detector*

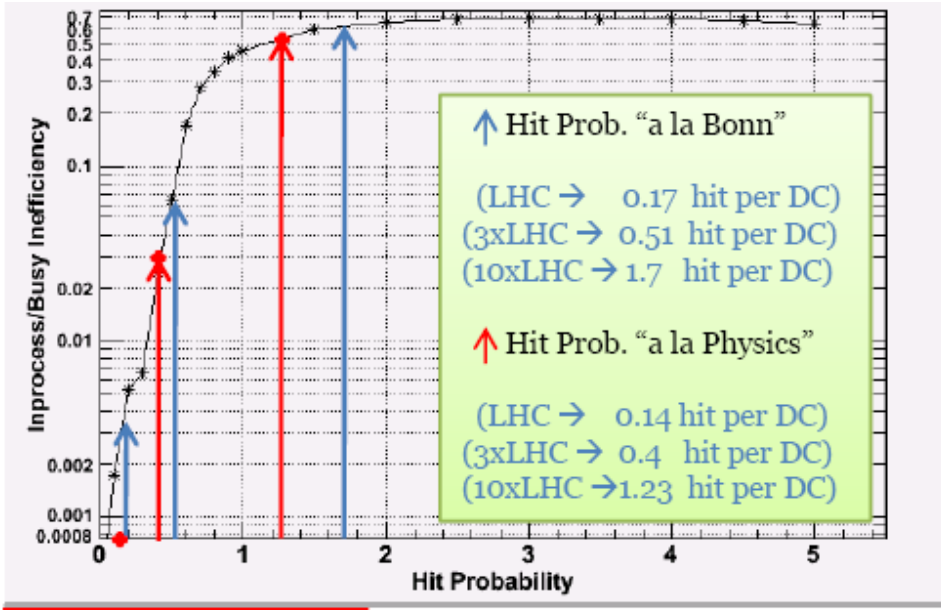
B-Layer Replacement - Insertion

- Study a smaller radius B-layer to insert in the existing Pixel
  - *It seems feasible (or not unfeasible) but not demonstrated yet;*
  - *16-staves (present module "active" footprint gives hermetic coverage in phi) not shingled b-layer. Requires new smaller beam-pipe (long procurement time, dimensions will be known after LHC operation - 2009);*
  - *Module technology: tracking hermetic requires new module design – increase live area of the footprint:*
    - *New chip design (FE-I4) – live fraction, I/O bandwidth;*
    - *Sensor – increase radiation hard (smaller radius and ramping up LHC luminosity).*
  - *R&D and prototyping in 2009 – construction 2010-2012;*
  - *Services need feasibility studies and solutions.*



Limit of FE-I3 Architecture

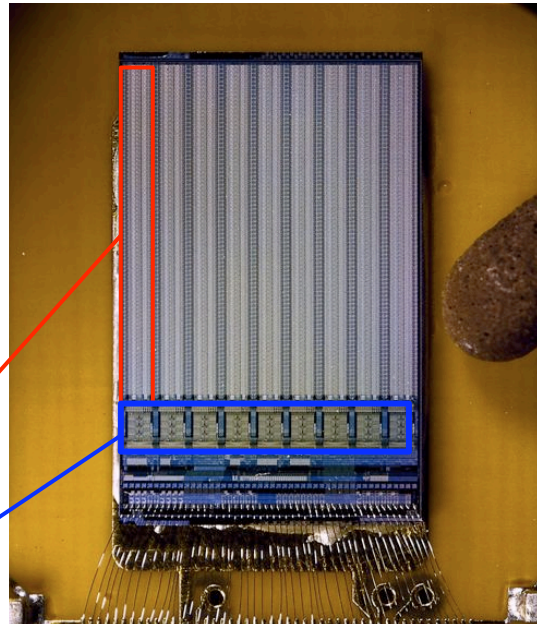
- Inefficiency is a very steep function of hit rate:
  - *Inefficiency is small for B-layer at nominal luminosity;*
  - *Very much at the limit for LHC "Ultimate Luminosity"*
  - *Unacceptable for B-layer @ 3.6 cm in 2016 and SLHC*



In proc./Busy:
LHC → 0.08%
3xLHC → 3%
10xLHC→52.5 %

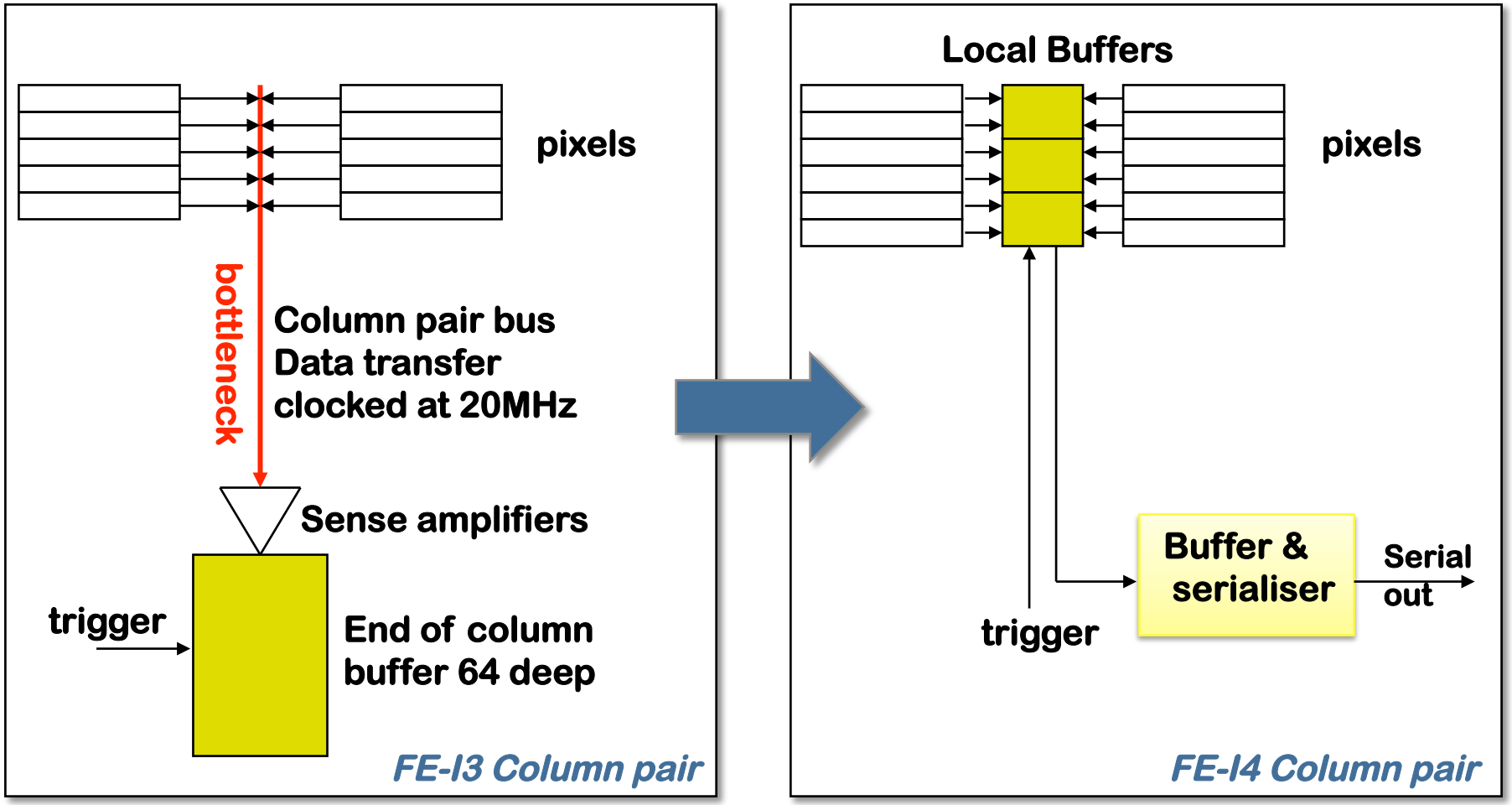
- Bottleneck is congestion in the double columns:
  - *All hits has to be transferred to the EoC buffers;*
  - *What are the architecture changes…*

Simulated events: "LHC @ 5cm" : WH(120) + 23 MB



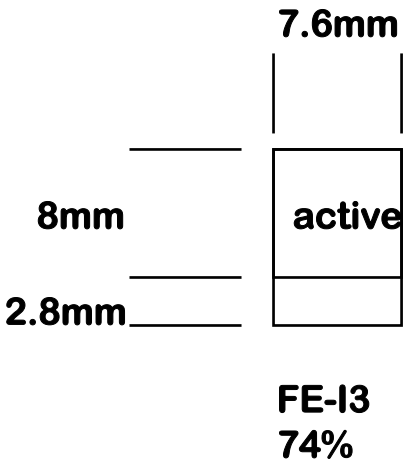
Obvious Solution to Bottleneck

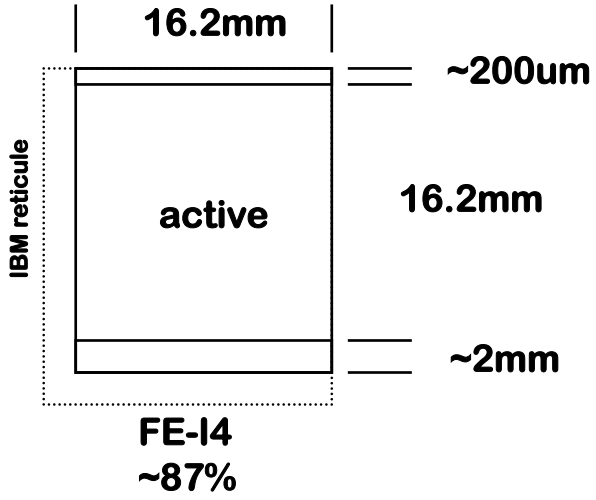
- >99% or hits will not leave the chip (not triggered)
  - *So don't move them around inside the chip! (this will also save digital power!)*
- This requires local storage and processing in the pixel array
  - *Possible with smaller feature size technology (130nm)*



FE-I4 Chip Size

- Larger live fraction of FE-I4 will make possible to meet the tight mechanical constraints of the B-layer replacement
- Larger chip will reduce bump-bonding costs mainly driven by chip placement.



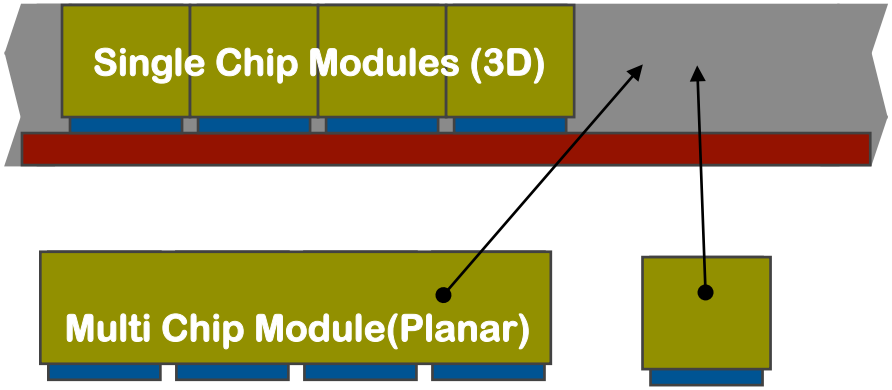


	FE-I3	FE-I4 goals	
Analog A/cm^2 (active)	130mA	80mA	~same voltage as now
Digital A/cm^2 (active)	85mA	80mA?	Lower voltage
Total power/cm^2 (active)	**385mW**	240mW	Nominal (not worst case)
WORST CASE for MODULE (footprint!)	500mW/cm^2 (used for mech. design)	?*	Take FE-I3 absolute, scale factor, or do "*stand alone*" estimate?

B-Layer & SLHC Communalities

- The FE-I4 will not be enough for B-Layer at SLHC.
- FE-I4 hit rate target fits well the SLHC environment in the range R=12÷30cm.
- B-layer @ SLHC will need new front-end design: FE-I5.

Pre-tested stave structure with integrated bus and cooling, SMD and burned-in power adapters

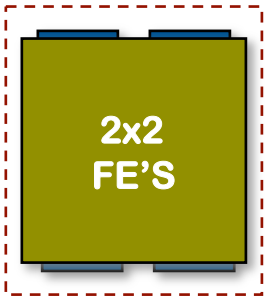


Robotically placed, fully tested 1-chip or multi-chip modules. Wire bond to stave after placement.

Radius (cm)	# Events	Hits/FE-I3 Module	FE-I3 Module (Mb/s)	FE-I4 (Mb/s)
5.05	23	18.7	48.6	3.0
5.05	230	156.9	407.9	25.5
5.05	230	156.9	407.9	102.0
5.05	400	*320.0*	*832.0*	*208.0*
12.25	400	*40.0*	*104.0*	*26.0*
3.5	230	*320.2*	*832.5*	*208.1*
3.5	400	*556.9*	*1447.9*	*362.0*
	z	x		
Module Size	60.8	16.4		

SLHC

2x2 chip modules for external layers @ SLHC.

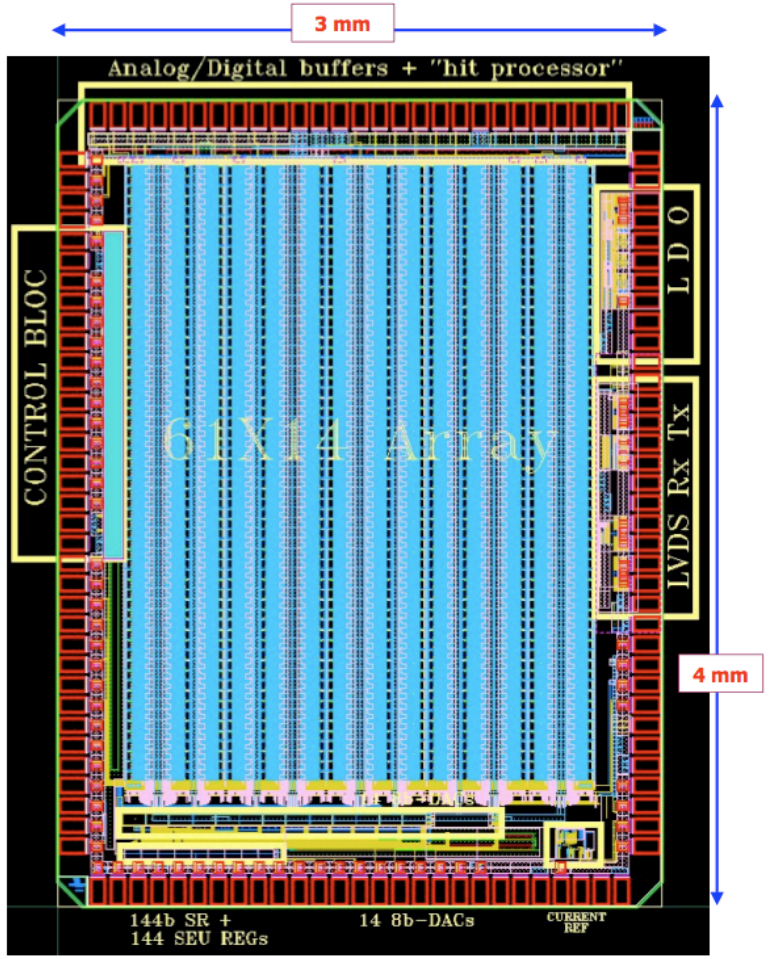


Prototyping - Pixel Collaboration Chips

- Pixel (FE-I4p) and Opto chips submitted 24/3/08:
  - *Prototypes for new FE-I4 in 0.13 µm CMOS*
  - *Designing labs: Bonn, Genova, LBNL, Marseille, Nikhef,*
- FE-I4 Main Design Parameters.

Pixel size	**50 x 250**	μm^2
DC leakage current tolerance	100	nA
Pixel array size	**≥ 64 x 320**	Col x Row
Normal pixel input capacitance range	300-500	fF
Long pixel input capacitance range	450-700	fF
In-time threshold with 20ns gate (400pF)*	4000	e
Hit-trigger association resolution	25	ns
Same pixel two-hit discrimination (time)	400	ns
Single channel ENC sigma (400fF)	300	e
Tuned threshold dispersion (max)	100	e
Charge resolution	4	bits
ADC method	TOT	
Operating voltage range	1.2 – 1.5	V
Total analog supply current @400fF	10	µA / pixel
Radiation tolerance (specs met at this dose)	200	MRad
Average hit rate	200	MHz/cm^2
Trigger latency (max)	3.2	µs
Single chip data output rate	160	Mb/s
Maximum trigger rate	200	KHz
Total digital supply current @ 100KHz	10	µA / pixel

"Pixel Collaboration Chip"



Pixel Oriented R&Ds

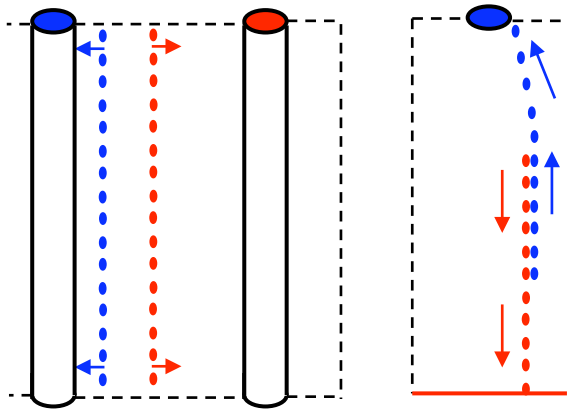
10 R&Ds where Pixels are involved have been (or will be) submitted

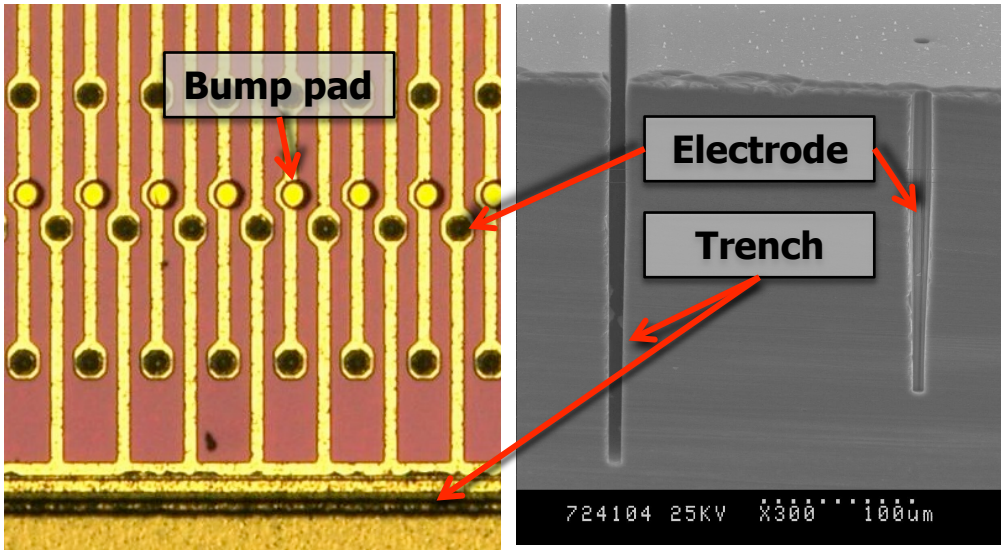
Doc no.	Short name	Title	Institutes	Status at 30/6/2008
ATL-PA-MN-0001	Opto	Radiation Test Programme for the ATLAS Opto-Electronic Readout System for the SLHC for ATLAS upgrades	*Taiwan, Ljubljana, Ohio, Oklahoma, Oxford, SMU*	Approved EB
ATL-PA-MN-0007	3D Sensors	Development, Testing and Industrialization of Full-3D Active-Edge and Modified-3D Silicon Radiation Pixel Sensors	*CNM Barcellona, Bonn, Freiburg, Genova (Milano), Glasgow, Hawaii, LBNL, Manchester, Oslo, SINTEF Oslo, Prague, MBC/Stanford, IRST Trento, Valencia*	Approved by EB
ATL-P-MN-0012	R/O Architectures	Read-out Electronics for the ATLAS upgraded tracker		
ATL-P-MN-0016	Gossip	R&D proposal to develop the gaseous pixel detector Gossip for the ATLAS Inner Tracker at the Super LHC (SLHC)	*NIKHEF, SACLAY, Twente*	EoI Received
ATL-P-MN-0035	Versatile Link	The Versatile Link Common Project	*CERN, Strasbourg, Oxford, SMU Dallas.*	Sent to CB for comments
ATU-RD-MN-0008	Powering	Research and Development of Power Distribution Schemes for the ATLAS Silicon Tracker Upgrade	*BNL, Bonn, CERN, Krakow, LBNL, RAL, Wuppertal, Yale*	Approved by EB
ATU-RD-MN-0010	Thin Pixels	R&D on thin pixel sensors and a novel interconnection technology for 3D integration of sensors and electronics	*MPI Munich*	Approved by EB
ATU-RD-MN-0012	Diamond	Diamond Pixel Modules for the High Luminosity ATLAS Inner Detector Upgrade	*Bonn, Carleton, CERN, Jožef Stefan Institute, Ohio State, Toronto*	Approved by EB
ATU-RD-MN-XXXX	Planar Pixel	R&D on Planar Pixel Sensor Technology for the ATLAS Inner Detector Upgrade	*Prague, LAL Orsay, Bonn, HU Berlin, TU Dortmund, MPP Munich, MPI Munich, Udine, Liverpool, UNM Albuquerque, UCSC Santa Cruz.*	EoI to Submit
ATL-RD-MN-XXXX	Pixel Local Supports	Research and Development Local Supports for Pixel Detector Upgrades		EoI to Submit

3D Sensors Basics

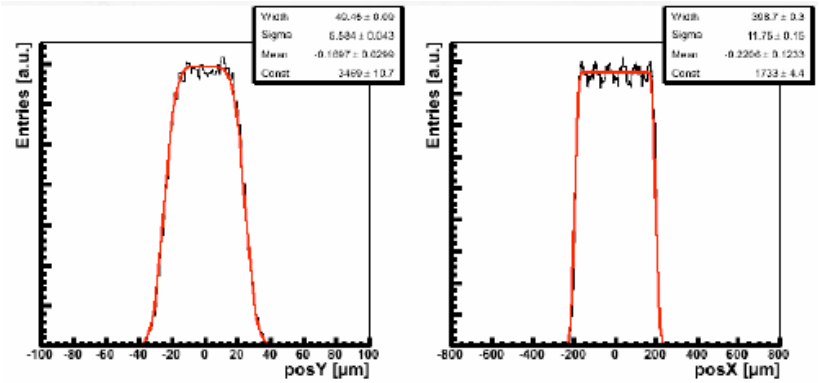
- Decoupled directions: track traversal versus drift field.
  - *Shorter traveling distance, more charged collected.*
- Active edge: Deep Reactive Ion Etching (DRIE) trench can replace saw dicing.
  - *Edge itself is an electrode*
  - *2-way butt-able, edge sensitive tile, will be tested in module construction*

Planar and 3D Charge Collection Principle





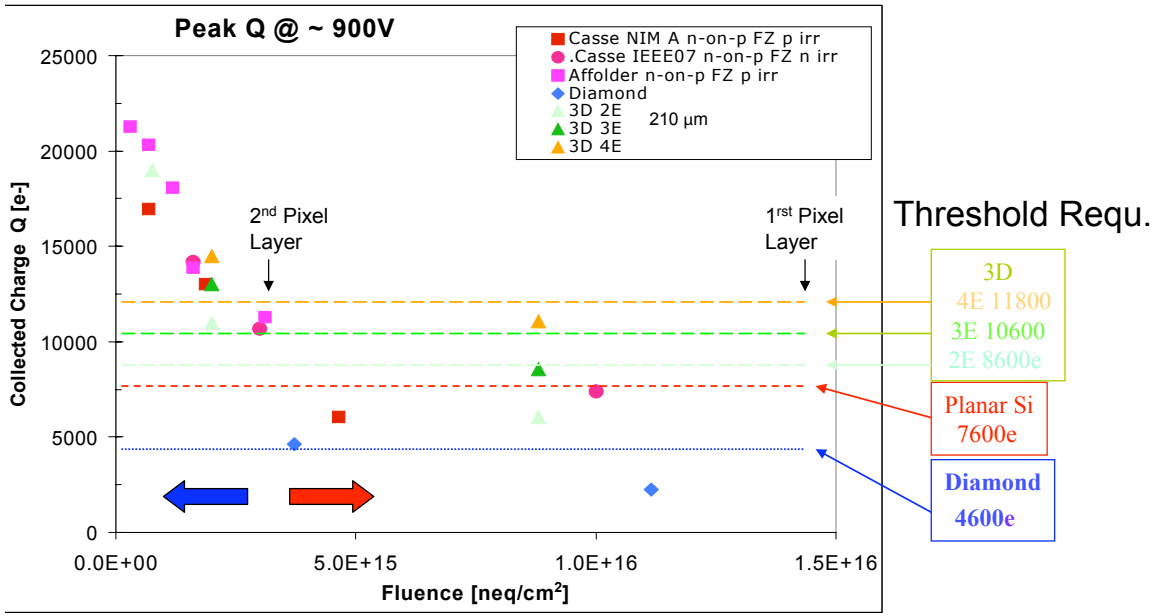
3D Space Resolution – ATLAS FE-I3 R/O



- Pure digital hit reconstruction, center position of pixel with highest signal
- Track density normalized
- Fluctuations indicate inefficiencies

Planar Sensors

- R&D on planar silicon technologies mainly to reduce cost, increase radiation tolerance and reduce inactive area:
  - *Bulk material: n-type (n-on-n current pixel sensor) or p-type (single side cost effective)*
  - *Thin sensors (50÷75μm thickness): reduce volume leakage current (noise, power)*
  - *Active edge: no need of shingling or double face stave for hermetic coverage*
  - *Slim edge: guard rings from 1100μm to ~100μm*
- Diamonds
  - *No cooling;*
  - *No leakage current;*
  - *Small capacitance -> small noise;*
  - *High radiation hard -> B-layer*



Hartmut F.-W. Sadrozinski, LBL Pixel Upgrade, May 22, 2008