Firmware Design

ALIREZA KOKABI

MOHSEN KHAKZAD

INSTITUTE FOR RESEARCH IN FUNDAMENTAL SCIENCES

Outline

FPGA selection and availability

Schematic design

FPGA Selection

- Microsemi **M2GL025T** Package **FG484**
  - We have inquired for the *market availability* last week but no response till now
  - We asked for the foot-print of FPGA and HPTDC last week
    Documents to be added to Twiki
- Future check (Based on yesterday email):
  - Compatibility with SAMPIC
    - Number of I/O required
    - Data rate frequency compatibility
    - Cell requirement

Table 1 • IGLOO2 FPGA Product Family

	Features	M2GL005	M2GL010(T)	M2GL025(T)	M2GL050(T)	M2GL090(T)	M2GL100(T)	M2GL150(T)
Logic/DSP	Maximum Logic Elements (4LUT + DFF)*	6,060	12,084	27,696	56,340	86,316	99,512	146,124
	Mathblocks (18x18)	11	22	34	72	84	160	240
	PLLs and CCCs		2			6		8
	SPI/HPDMA/PDMA				1 each			
	Fabric Interface Controllers (FIC)		1		2	1		2
Memory	eNVM (kbytes)	128		256			512	
	LSRAM 18K Blocks	10	21	31	69	109	160	236
	uSRAM 1K Blocks	11	22	34	72	112	160	240
	eSRAM (kbytes)				64			
	Total RAM (kbits)	703	912	1104	1826	2586	3552	5000
High Speed	DDR Controllers		1x18		2x36	1x18		2x36
	SERDES Lanes (T)	0		4	8	4	8	16
	PCIe Endpoints	0		1		2		4
User I/O	MSIO (3.3 V)	115	123	157	139	309	292	292
	MSIOD (2.5 V)	28	40	40	62	40	106	106
	DDRIO (2.5 V)	66	70	70	176	76	176	176
	Total User I/Os	209	233	267	377	425	574	574
Grades	Commercial (C), Industrial (I), Military (M)	C,I			C,I,M			

Notes: *Total Logic may vary based on utilization of DSP and memories in your design. Refer to the IGLOO2 FPGA Fabric UG for details.

*Feature availability is package dependent, refer to Table 3.

Schematic Design

- Design of the schematic needs some consideration
  - Power Supplies: Required DC voltages (Almost done)
  - Achieving Two Rail Design: Two rail of Power distribution
  - Power Supply Decoupling: Noise and ripple decoupling (Done)
  - Clocks (Almost done)
  - Reset Circuit
  - JTAG
  - Special Pins: Unused I/Os and …
  - Configuring Pins in Open Drain: Pullup resistor and…
  - SERDES (Done)

Power Supply Decoupling

Pin Name	Number of Pins	Ceramic Capacitors			Titanium Capacitors				
		10nF	100nF	10µF	4.7µF	22µF	47µF	100µF	330µF
VDD	21	11	11			2	1	1	1
VDDI0	14	7	7				2		
VDDI1	4	2	2	1					
VDDI2	4	2	2	1					
VDDI3	1	1		1					
VDDI4	6	3	3	1					
VDDI5	1	1		1					
VDDI6	4	2	2	1					
VDDI7	4	2	2	1					
VPP	5	2	3	1					
VREF0	3	2	1	1					
VPPNVM	1	1		1					
SERDES_0_VDD	2	1	1	1					
SERDES_0_L01_VDDAIO	1	1	1	1					
SERDES_0_L23_VDDAIO	1	1	1						
SERDES_0_PLL_VDDA	1		1			1			
CCC_NE0_PLL_VDDA	1		1			1			
CCC_NE1_PLL_VDDA	1		1			1			
CCC_NW0_PLL_VDDA	1		1			1			
CCC_NW1_PLL_VDDA	1		1			1			
CCC_SW0_PLL_VDDA	1		1			1			
CCC_SW1_PLL_VDDA	1		1			1			
SERDES_0_L01_VDDAPLL	1		1		1				
SERDES_0_L23_VDDAPLL	1		1		1				

Designed Schematic
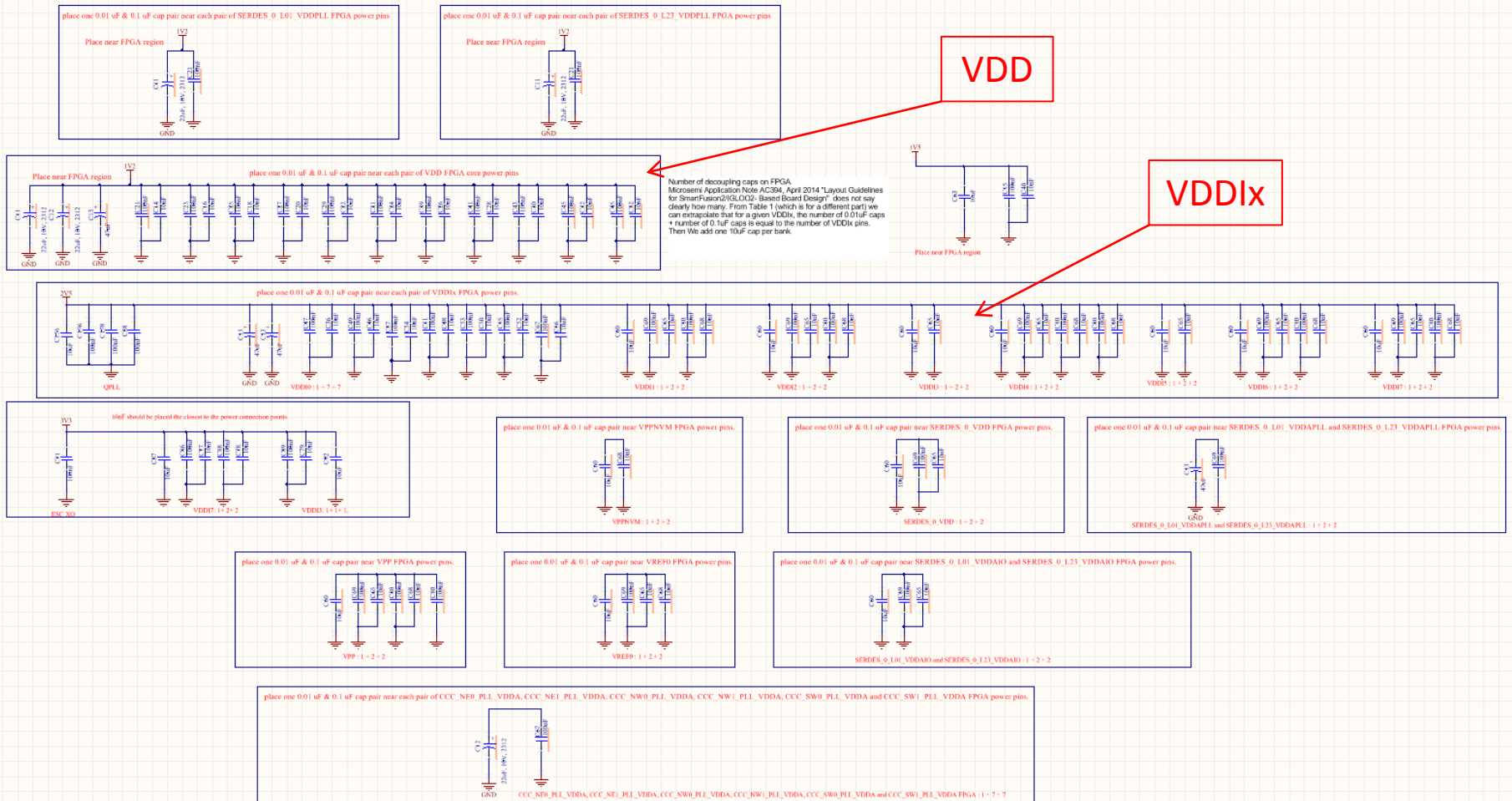
Future Works

HPTDC footprint and needed passive and active devices should be added