VMM ASIC Status Report

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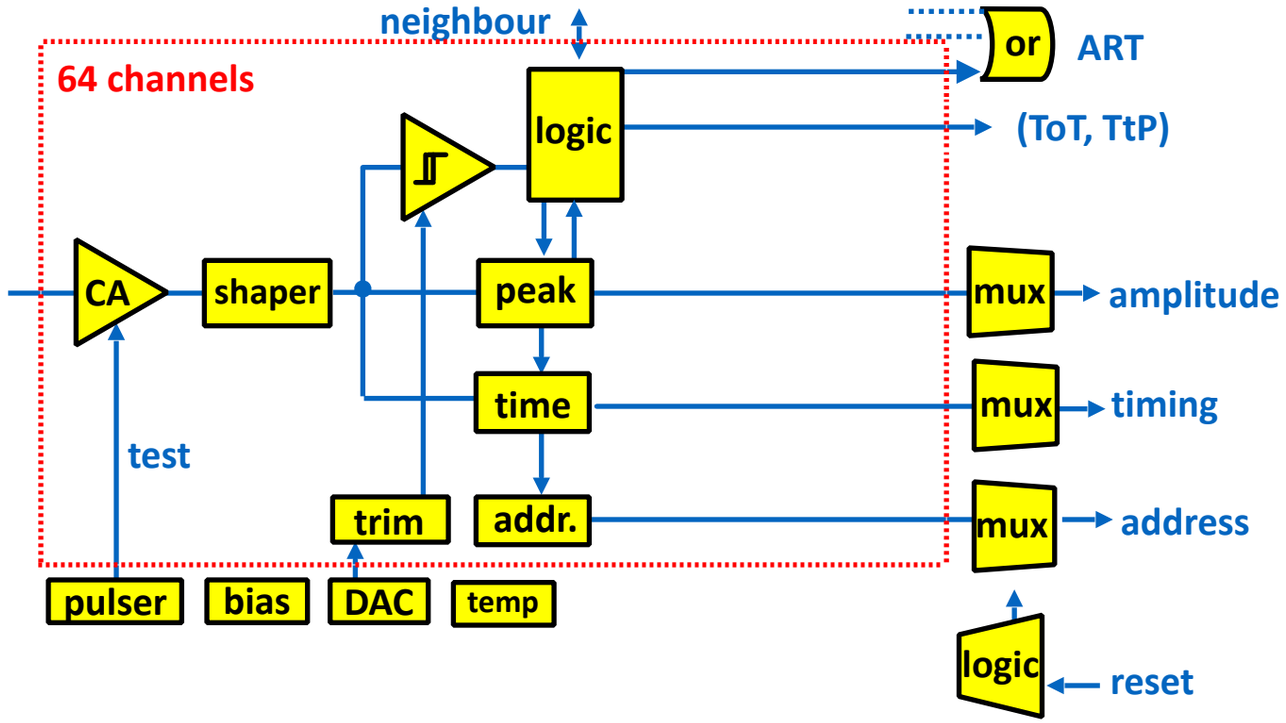
Outline

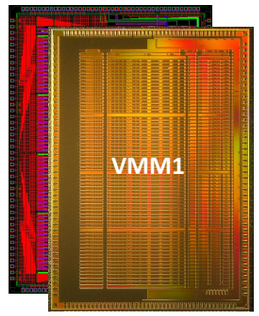
- VMM1 as the first prototype of the VMM ASIC.
  - Design, architecture and specs
  - Testing, noise
  - Test beam results
- VMM ASIC evolution
- VMM2 - Design and new features
  - Timeline and delays in packaging
  - Board prototype and integration to the SRS
  - Issues until now and timeline for VMM3
- Conclusions

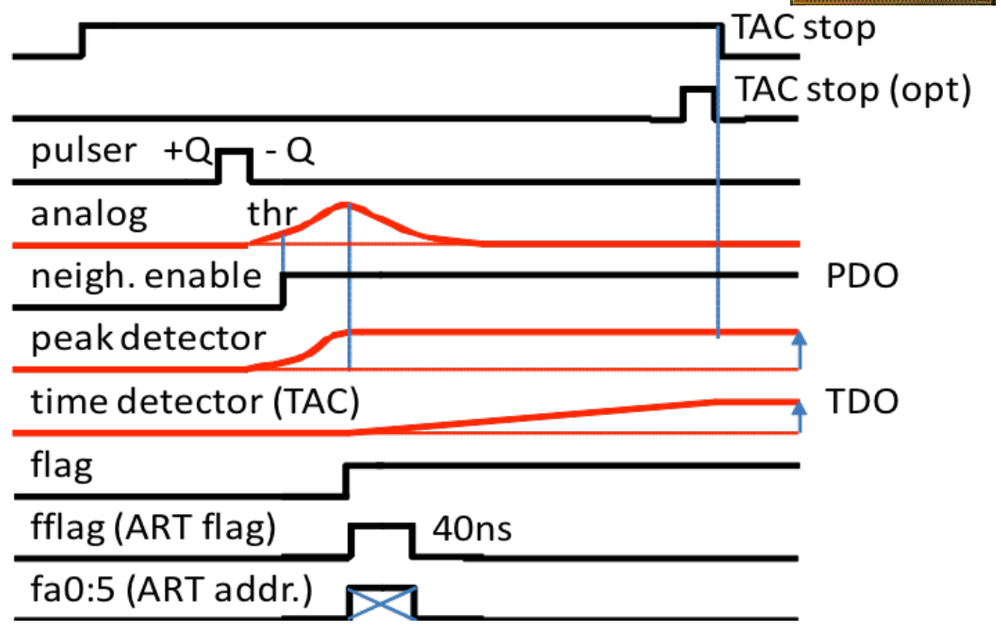
VMM1 - First ASIC prototype in 2012 (1/2)

- VMM: ASIC family for ATLAS Muon Spectrometer upgrade (Micromegas and small Thin Gap Chamber)
- Charge-interpolating trackers



- VMM1 (2012) 6 x 8.4 mm²
- 500k MOSFETs - (8k/ch.)
- mixed-signal, 2-phase readout
- IBM CMOS 130nm 1.2V



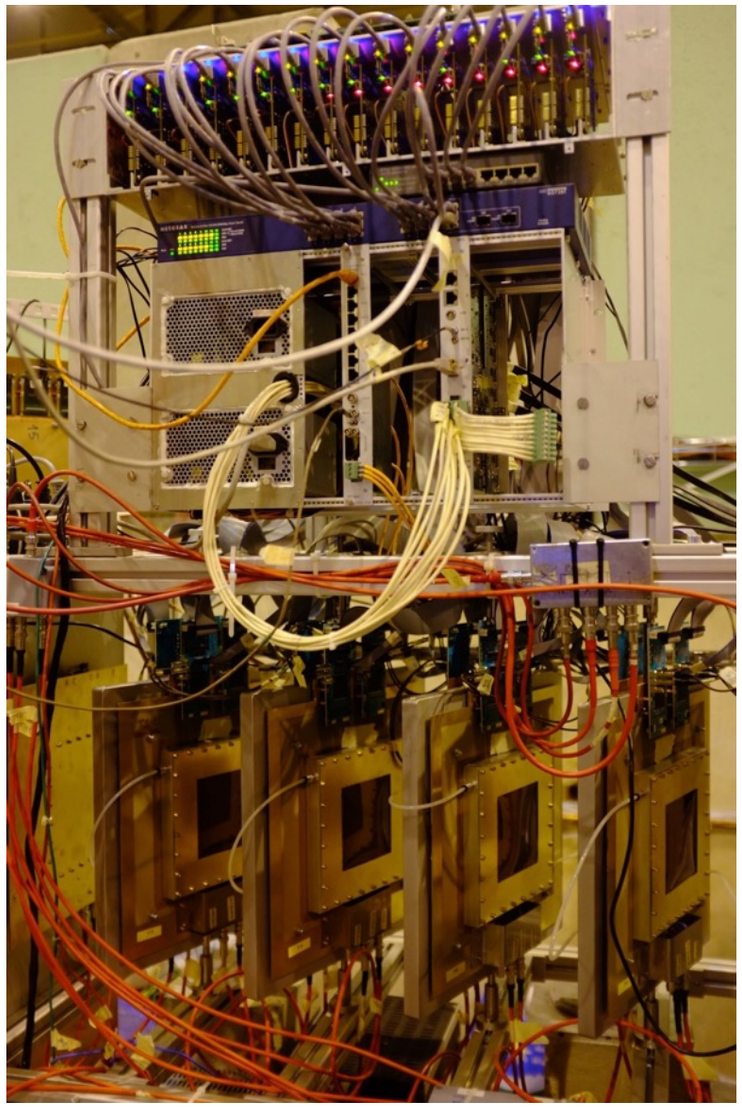


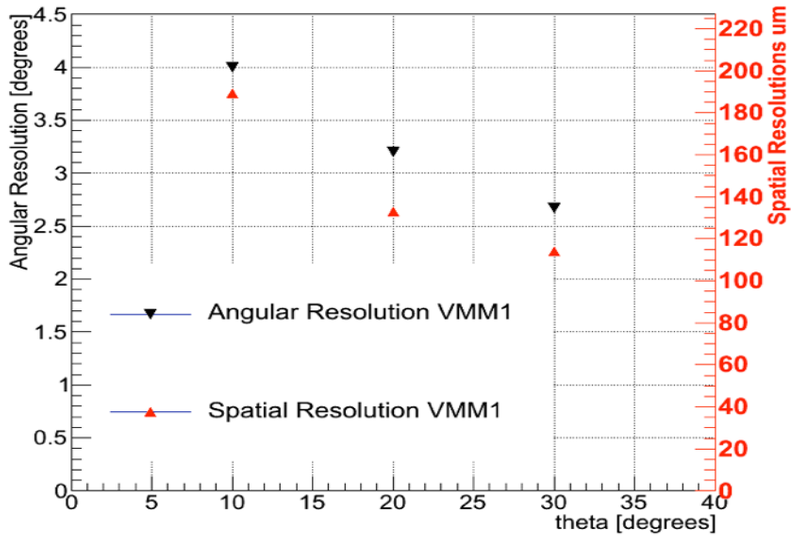
- dual polarity, adj. gain (0.5, 1, 3, 9 mV/fC) (0.11 to 2 pC), adj. peak-time (25-200 ns)
- discriminator with sub-hysteresis and neighbouring (channel and chip)
- address of first event in real time at dedicated output (ART)
- direct timing outputs: time-over-threshold or time-to-peak
- peak detector, time detector <1 ns
- multiplexing with sparse readout and smart token passing (channel and chip)
- threshold and pulse generators, analog monitors, channel mask, temperature sensor, 600mV BGR, 600mV LVDS

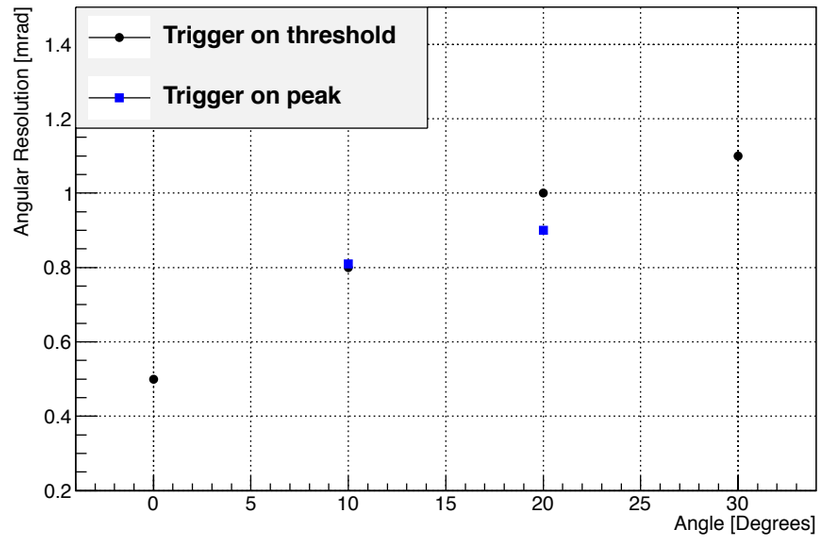
G. De Geronimo et al. ‘‘VMM1 - An ASIC for Micro-pattern Detectors’’. Nuclear Science, IEEE Transactions on 60 (June 2013), p. 2314.
doi: 10.1109/TNS. 2013.2258683.

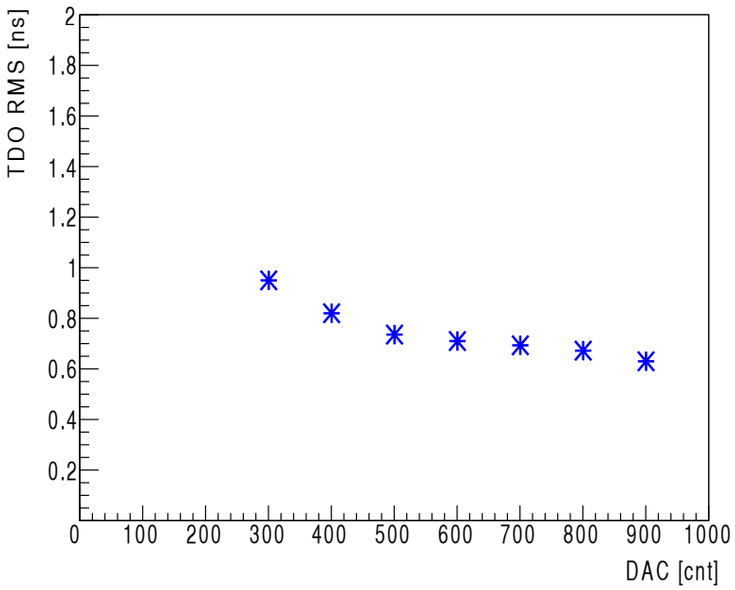
VMM1 - First ASIC prototype in 2012 (2/2)

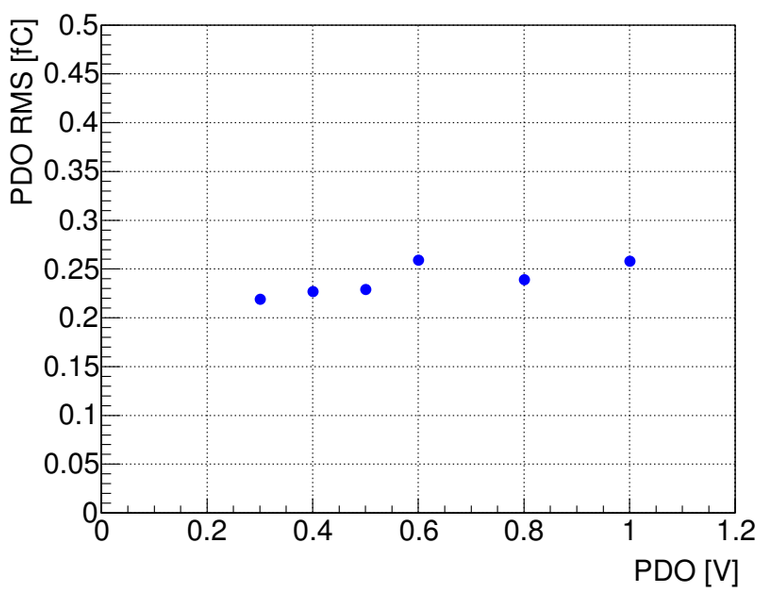
- First prototypes (x16) tested in 2012 test beam successfully with custom made readout system.
- First time testing the Resistive Micromegas as trigger system.
- Couple of bugs found in the design and fixes implemented in the next version(s)





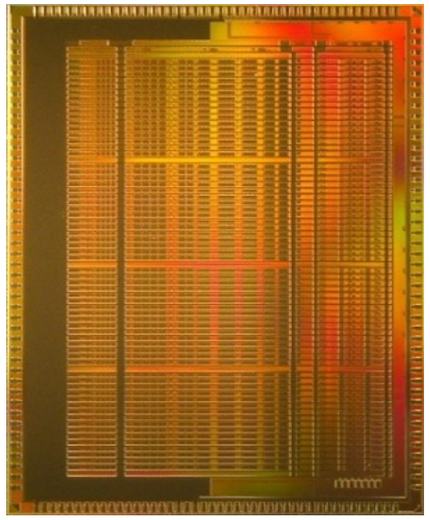




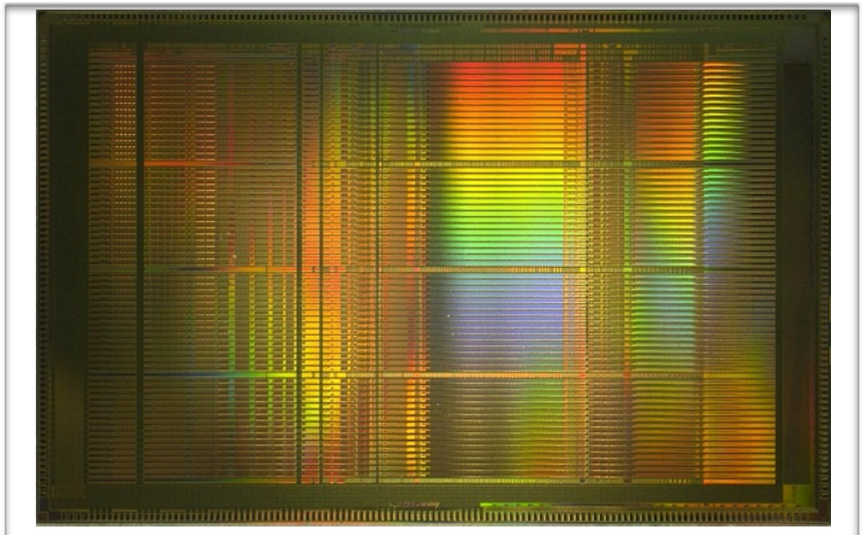


T. Alexopoulos *et al*. - Performance of the First Version of VMM Front-End ASIC with Resistive Micromegas Detectors, ATL-UPGRADE-PUB-2014-001, https://cds.cern.ch/record/1753328?ln=en

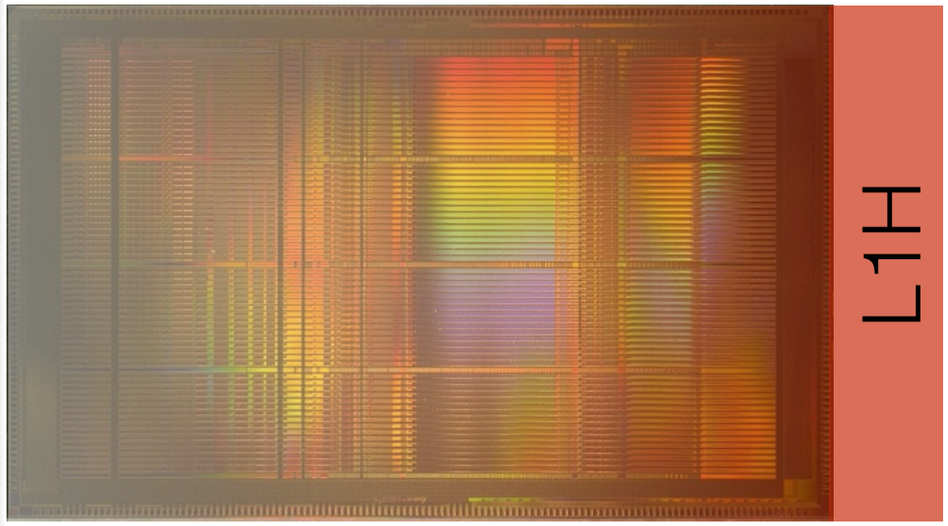
VMM - ASIC evolution



- VMM1 (2012)
- 50 mm²
- 500k MOSFETs
- (8k/ch.)
- mixed-signal
- 2-phase readout



- VMM2 (2014)
- 115 mm²
- > 5M MOSFETs (>80k/ch.)
- planned deep re-design of VMM1
- higher functionality and complexity
- continuous fully-digital readout

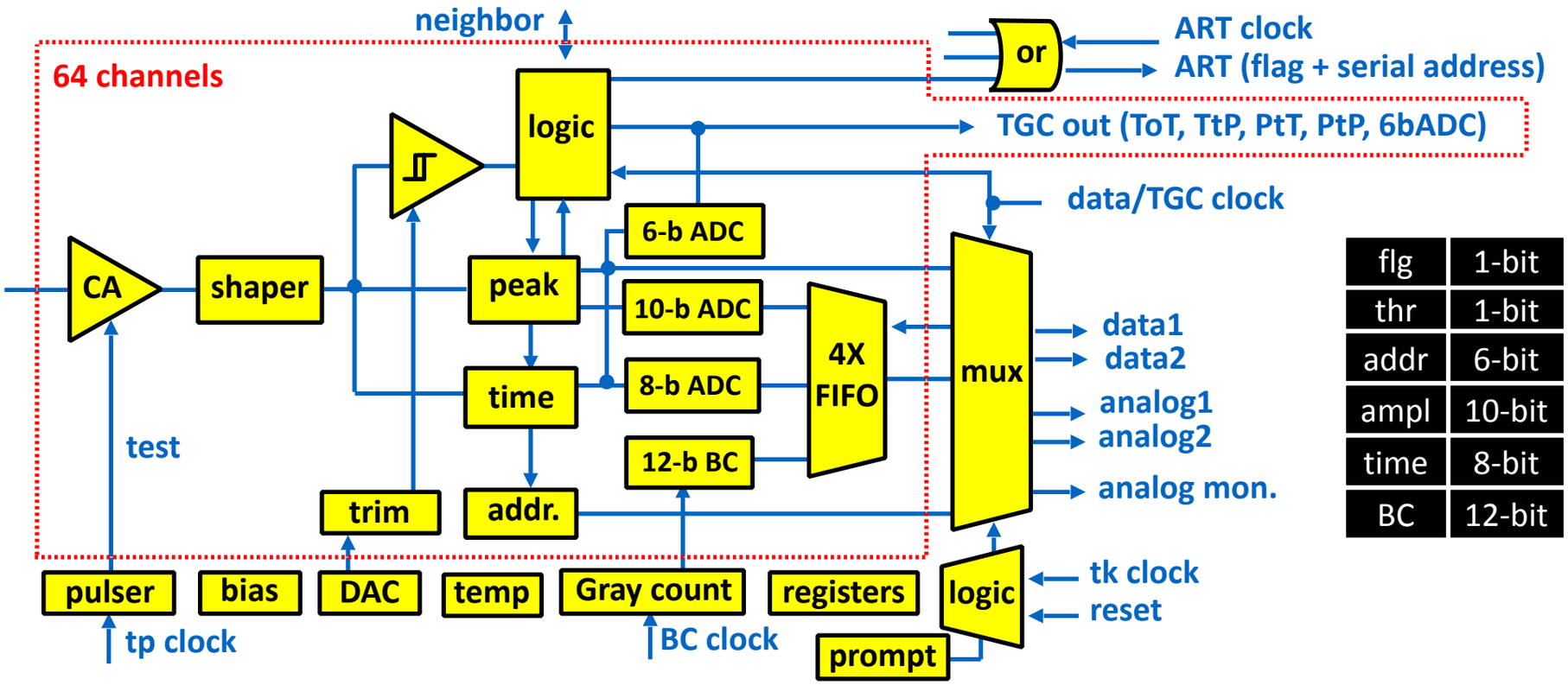


- VMM3 (2015-16)
- 130 mm²
- > 6M MOSFETs
- includes L1 handling and SEU-tolerant logic

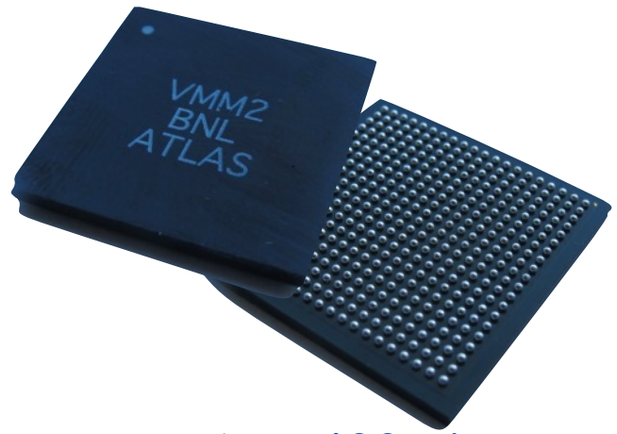
G. De Geronimo - ''VMM2 - An ASIC for the New Small Wheel''.TWEPP 2014 - Topical Workshop on Electronics for Particle Physics.

https://indico.cern.ch/event/299180/session/4/contribution/45

VMM2 - Second ASIC prototype in 2014



flg	1-bit
thr	1-bit
addr	6-bit
ampl	10-bit
time	8-bit
BC	12-bit



custom 400-pin

21 x 21 mm² BGA

- adjustable discrimination threshold per channel
- trimming range: 15 mV in 1m increments
- sub-hysteresis mode: effective discrimination ~ 2 mV
- neighbour logic: sub-threshold neighbor channels
- polarity: adjustable positive or negative
- gain: adjustable 0.5, 1, 3, 4.5, 6, 9, 12, 16 mV/fC (max charge 2 to 0.06 pC)
- peaking time: adjustable 25, 50, 100, 200 ns
- clock frequency: up to 200 MHz to the 6bit ADC
- 12-bit timestamp: 12-b Gray-code counter on BC provides timing TAC stop (20-b, ~100 μs, sub-ns resolution)
- 4-deep FIFO
- 10-bit, 200 ns , 1.5 mW, for peak amplitude
- 8-bit, 100 ns , 1.5 mW for peak timing (relative to BC)
- 38-bit event data at digital outputs

VMM2 - Manufacturing and packaging

- Wafers processed at IBM, die received at BNL May 18
- BGA substrate design was completed by that time
- Expected packaged devices in 6-8 weeks
- In late August i2a (packaging company) informed us that their moulding equipment had broken down and would take 2 weeks to fix it
- Subsequently they decided that they need to replace it and that would take months
- They proposed using a workaround and packaged 26 chips which we received in September and were not flat even to the naked eye.
- In addition the size of the chips was wrong 22.7x22.7 mm^2 instead of 21x21mm^2
- Nevertheless we used them to hand assemble a few mini-one and SRS128 boards with mixed results (occasional shorts at the corners)
- On 27/10 we received another batch of 11 devices. (Still wrong size)

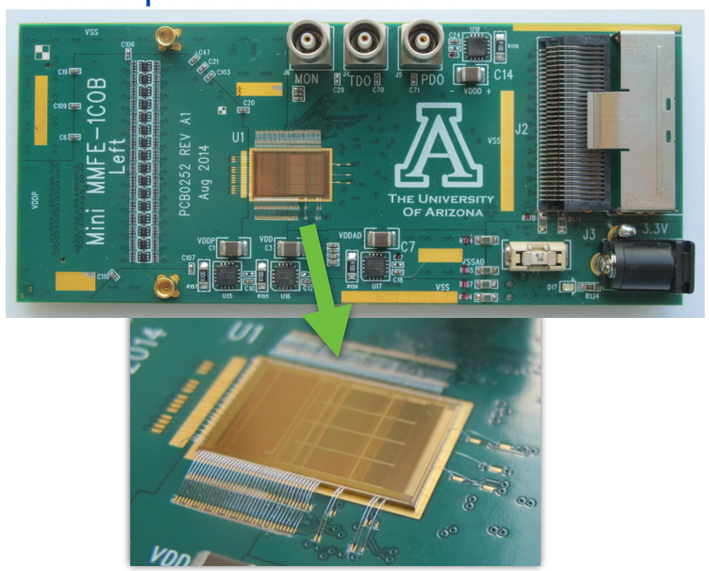
VMM2 - Present Status

- NASA guidelines for selection and use of BGA: <5% of BGA size – In our case < 100 microns
- First batch non-coplanarity 150-200 um (6-8 mils)
- Second batch ~ 100-150um (4-6 mils)
- After the first batch all were trimmed to correct size (21x21 mm^2)
- Received the remaining 163 devices from the original 200-die lot
- Measured 8 randomly:
  - Results excellent, even meet NASA's strict guidelines
- Laser probe of a CMM Machine
- Scans were made with a 1 mm sampling period in x and y in the regions between the solder bumps.

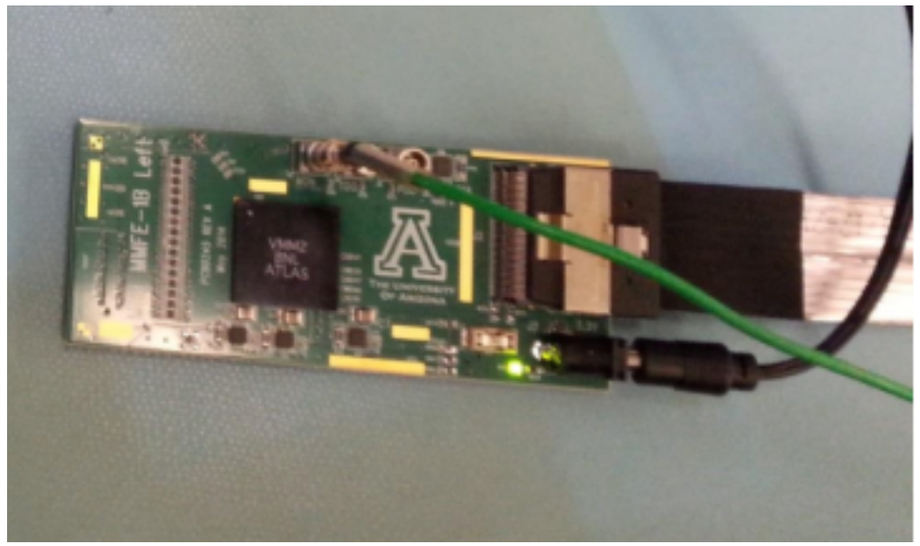
PV [microns]	PV [mils]
32.7	1.28
37.9	1.49
78.5	3.09
87.4	3.44
34.1	1.34
49.2	1.94
70.3	2.76
34.5	1.36

VMM2 - Frontend boards and readouts

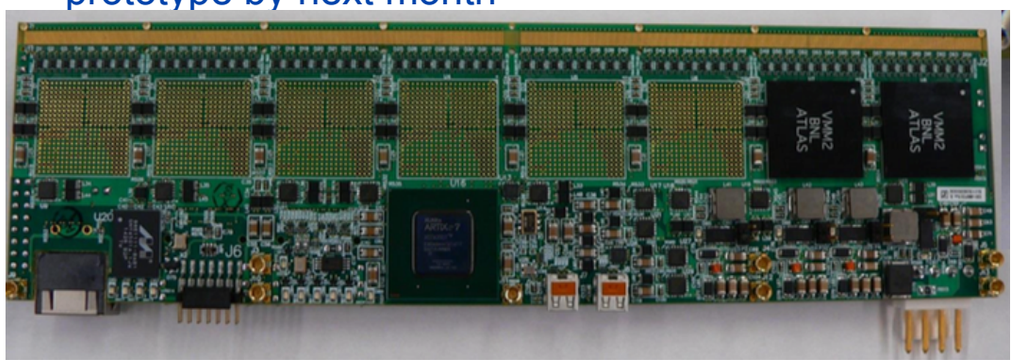
First wire bonded front end for testing purposes
Four Mini-1 cards were assembled with the first batch of non-planar VMM2 ASICs



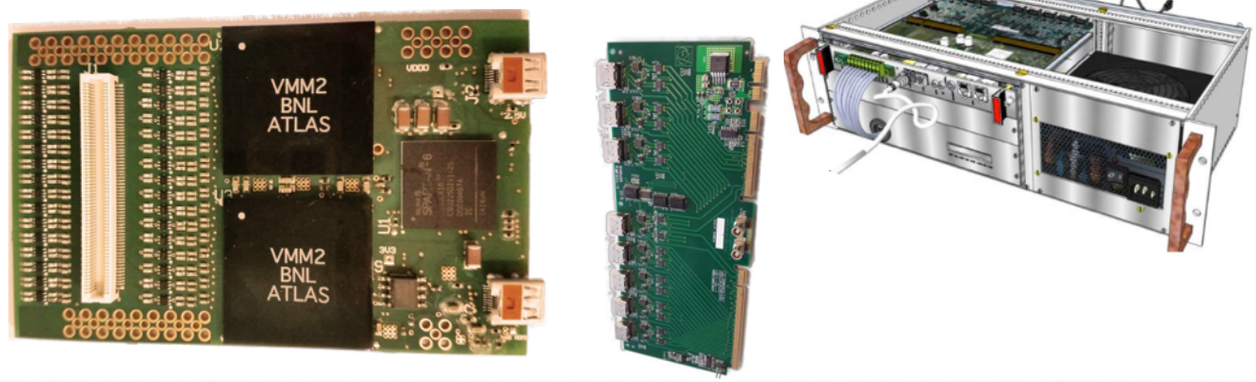
Same board with packaged chip



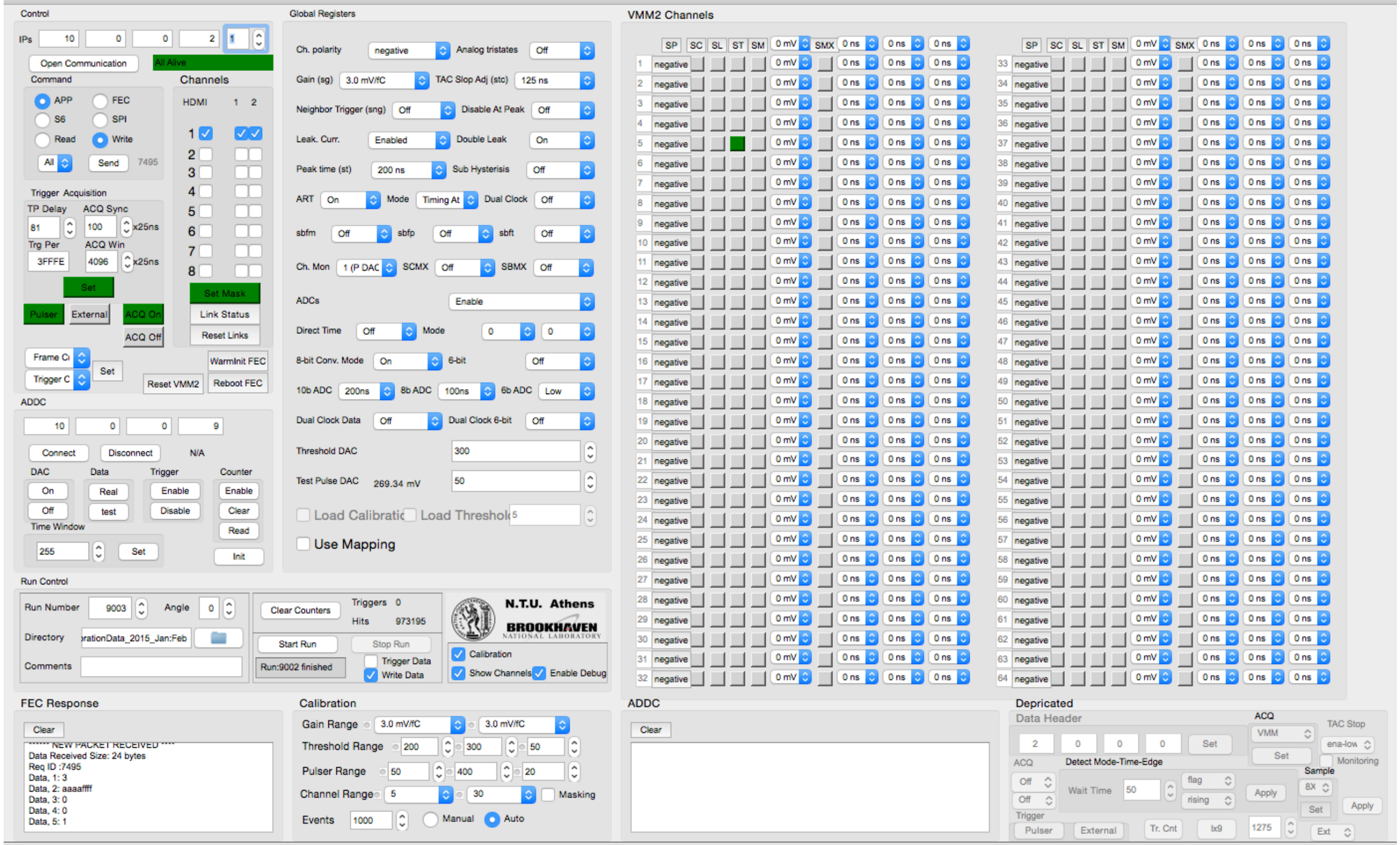
MMFE8- frontend board with 8xVMM2 - final board prototype by next month



Mini-2 - frontend board with 2xVMM2 for the SRS
2xHDMI one for the readout and the other for the trigger signals (ART)
DCARD instead of the ADC card
Same FEC classic card with another firmware
Readout UDP based SRS protocol

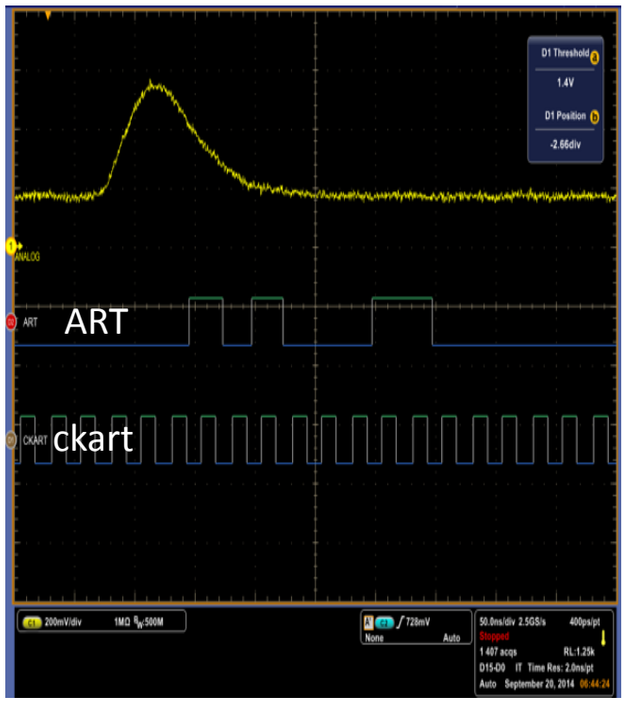


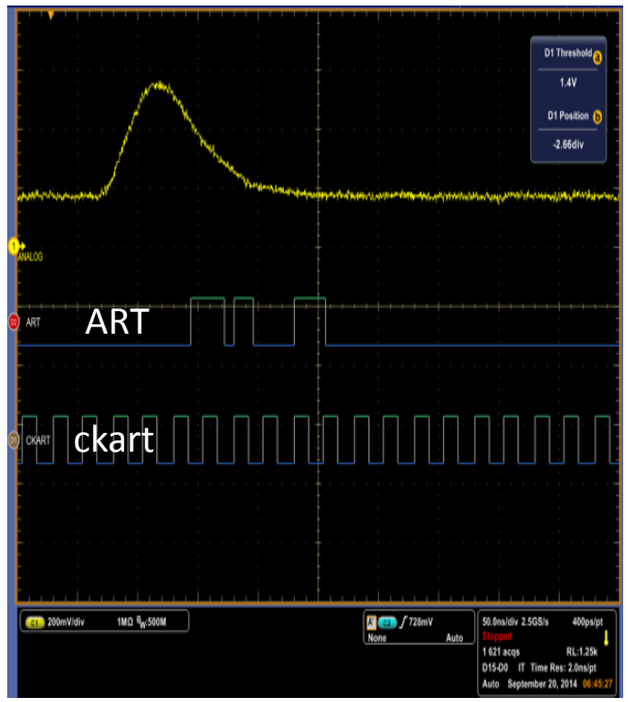
VMM2 - SRS - Software developed



VMM2 - Preliminary tests from designer

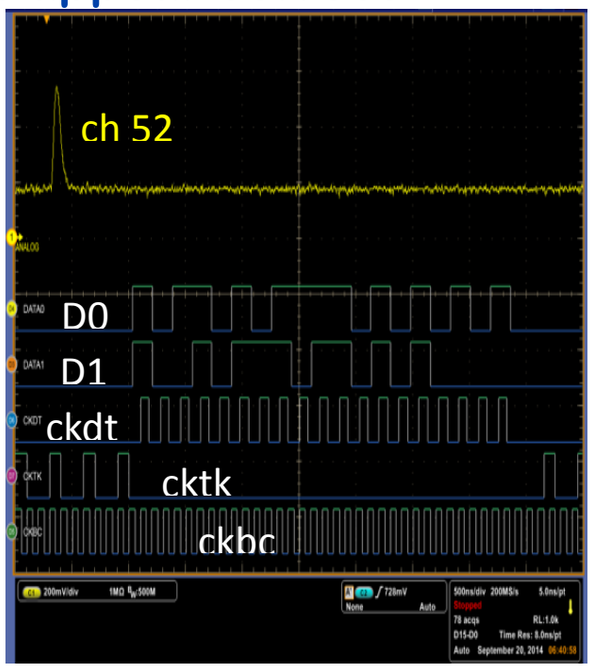
- ART output in single and dual data / clock



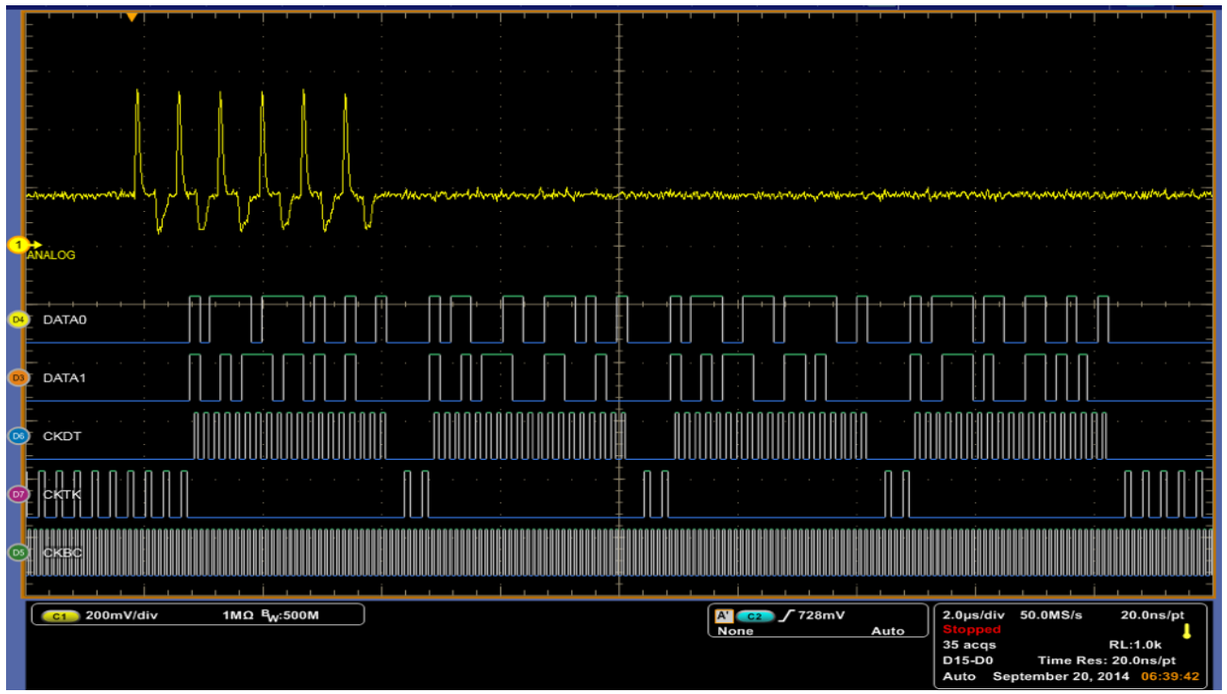


- ART auto-reset at end of serialisation works fine

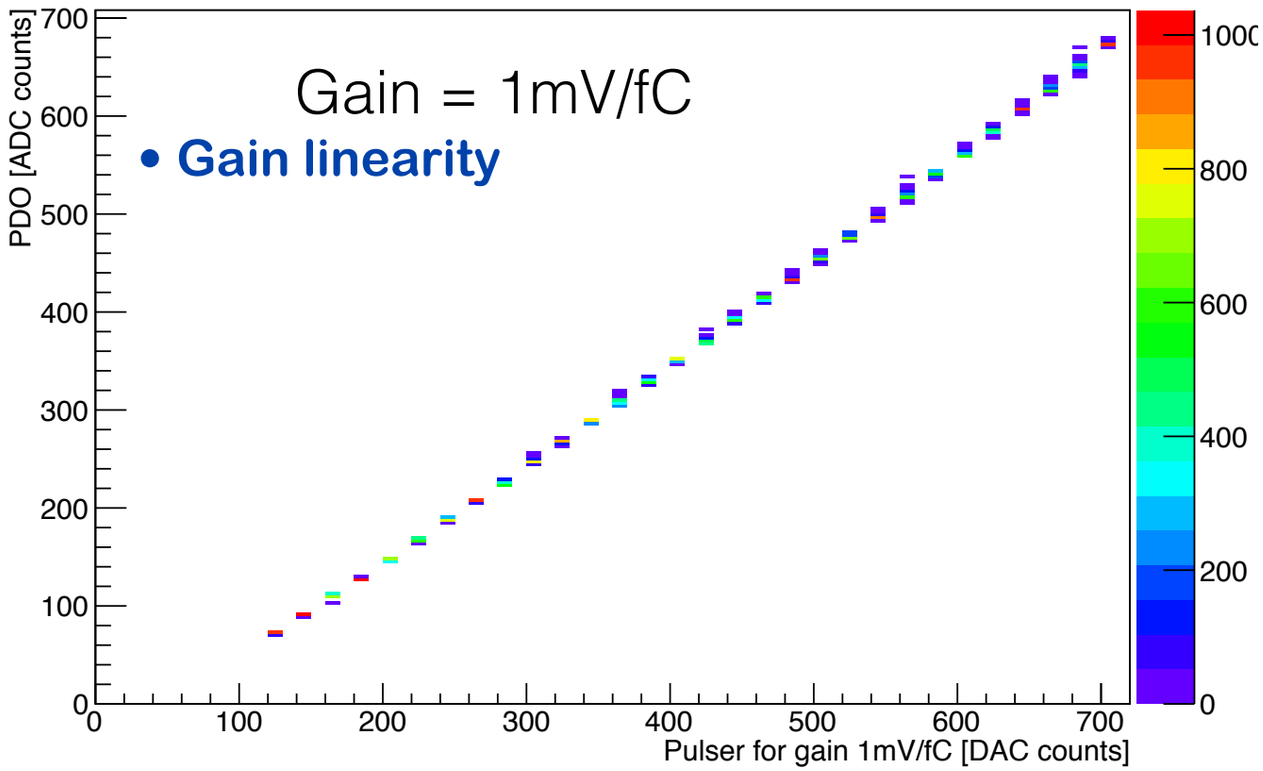
- Flag, threshold, address, amplitude, timing, timestamp appear correct



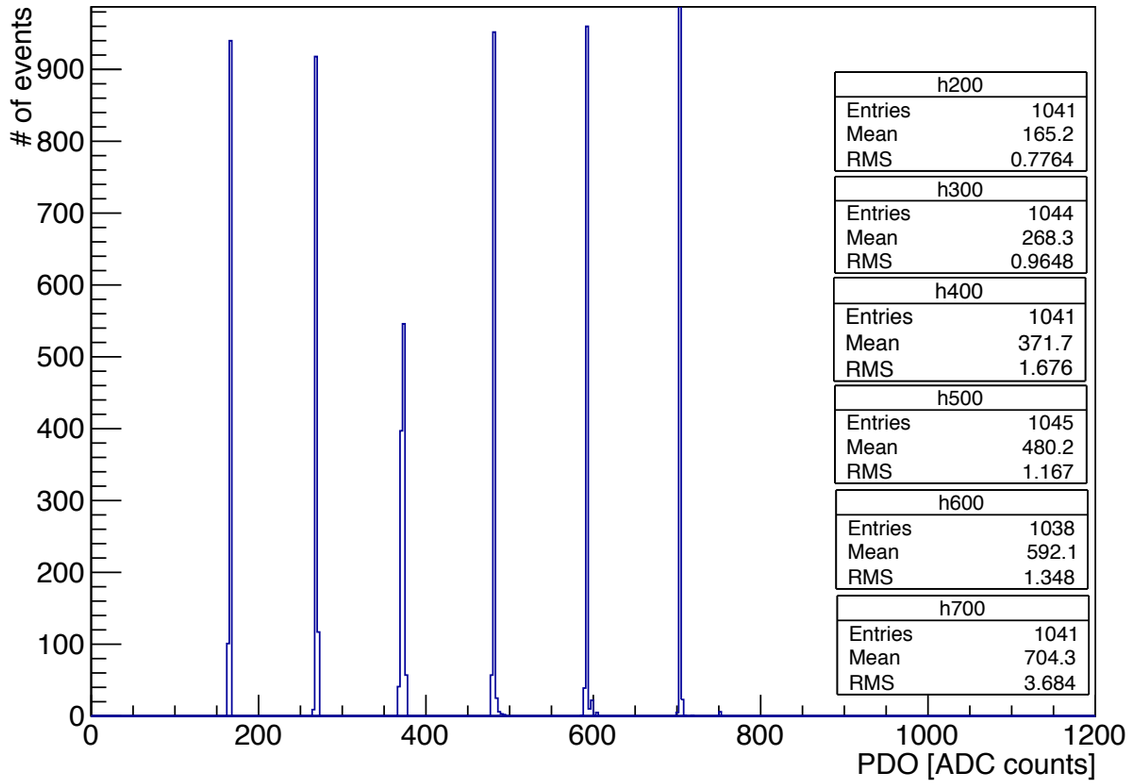
- Digital readout with FIFO for 6-event burst

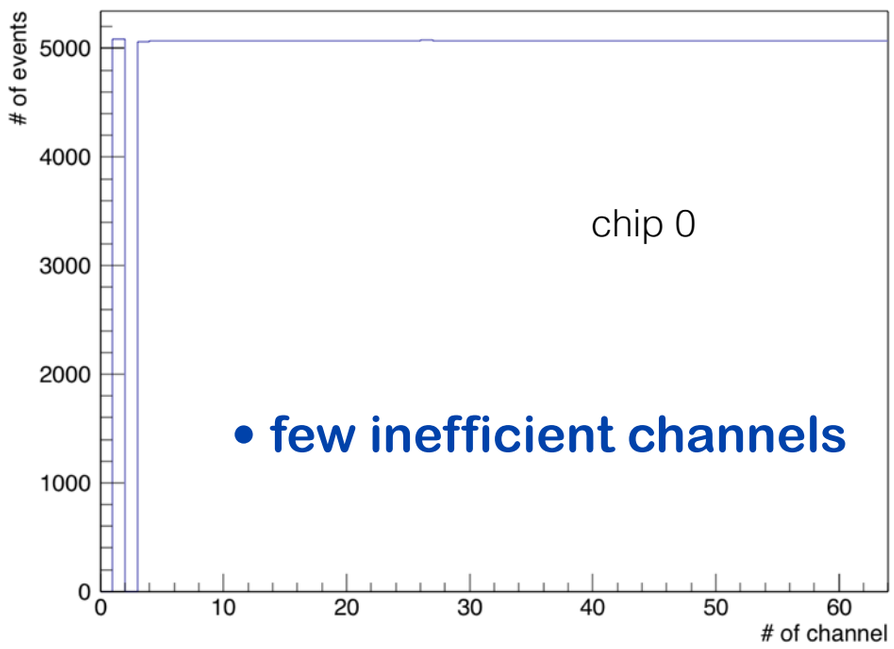


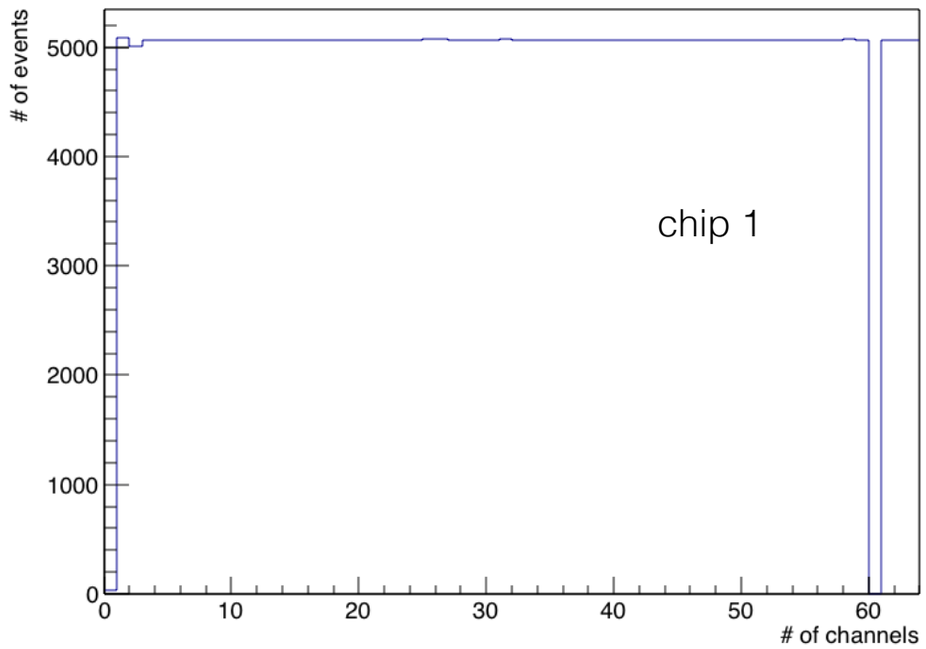
Tests with internal pulser - SRS



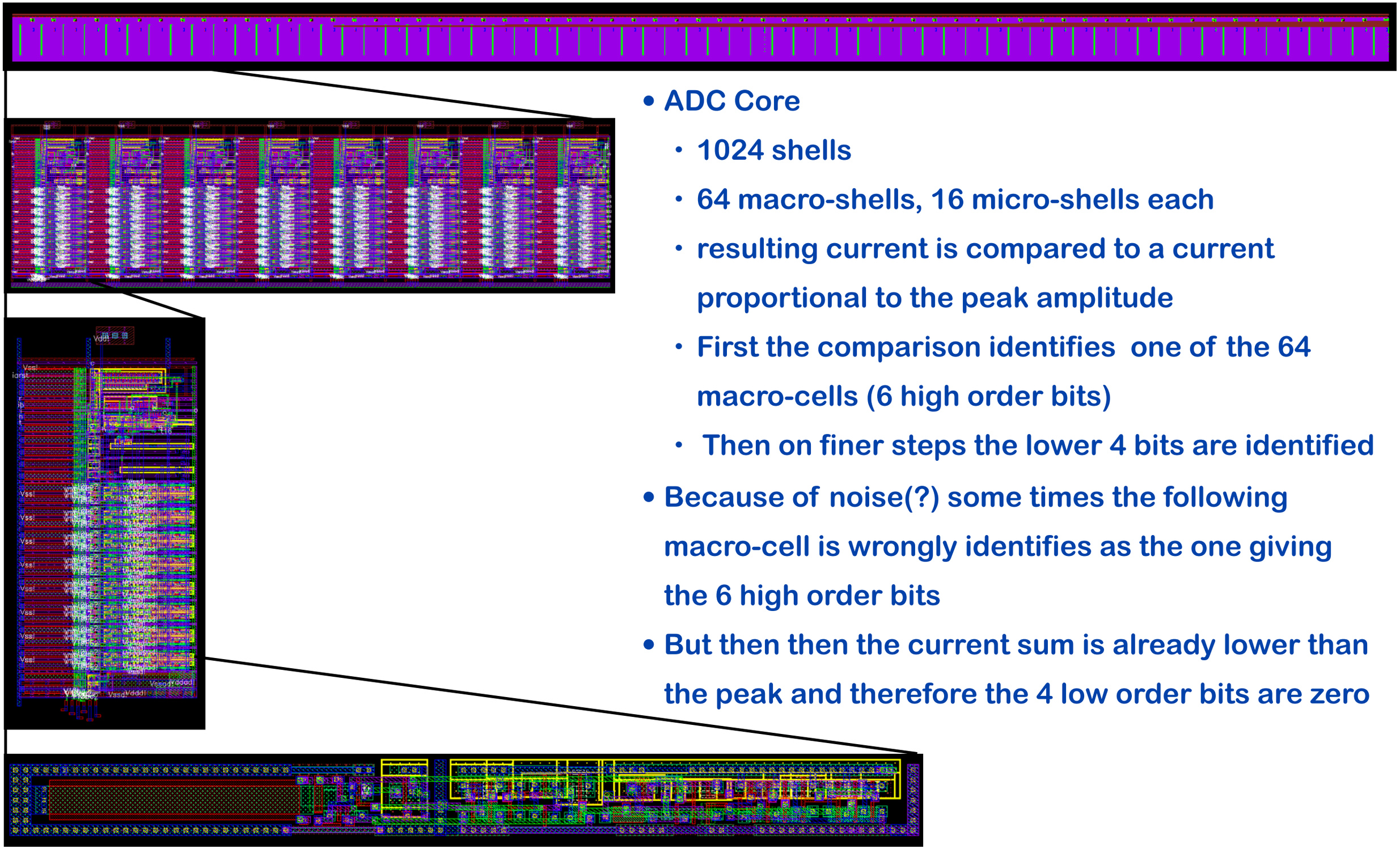
• Noise at good level







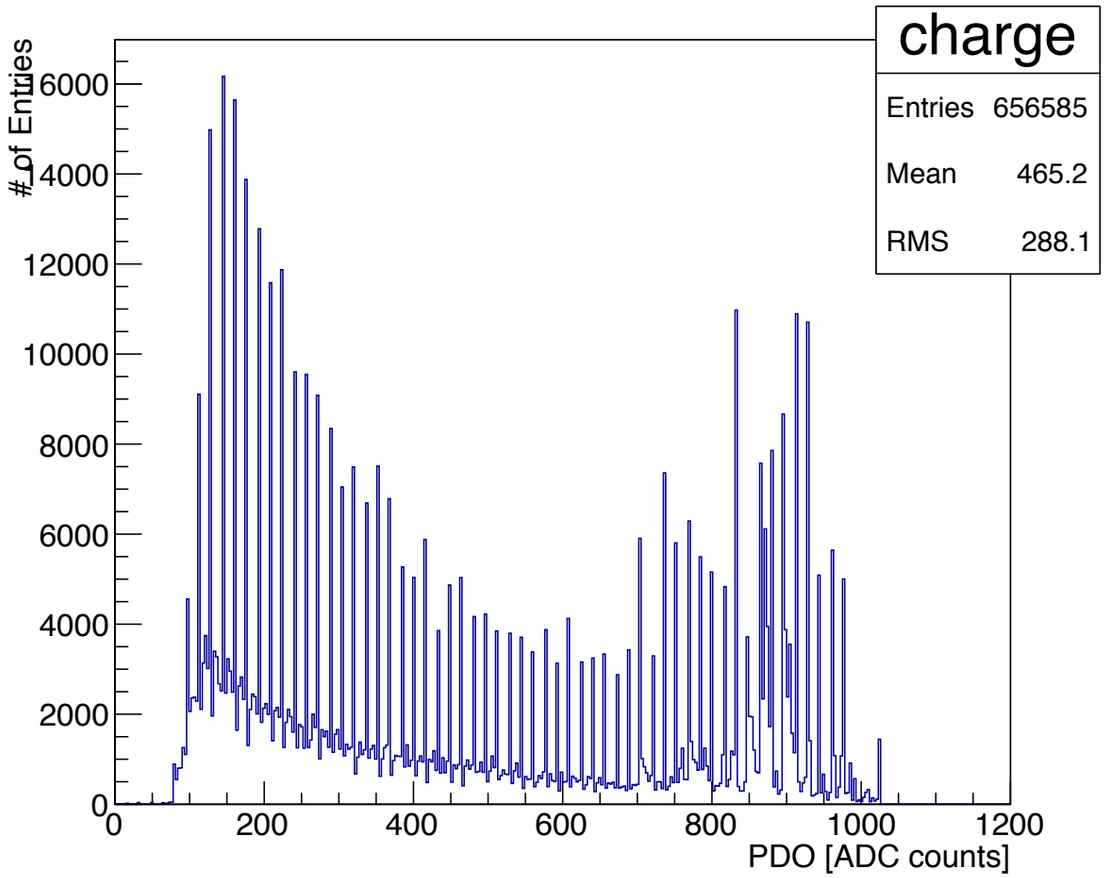
10-bit Current-Mode Domino ADC

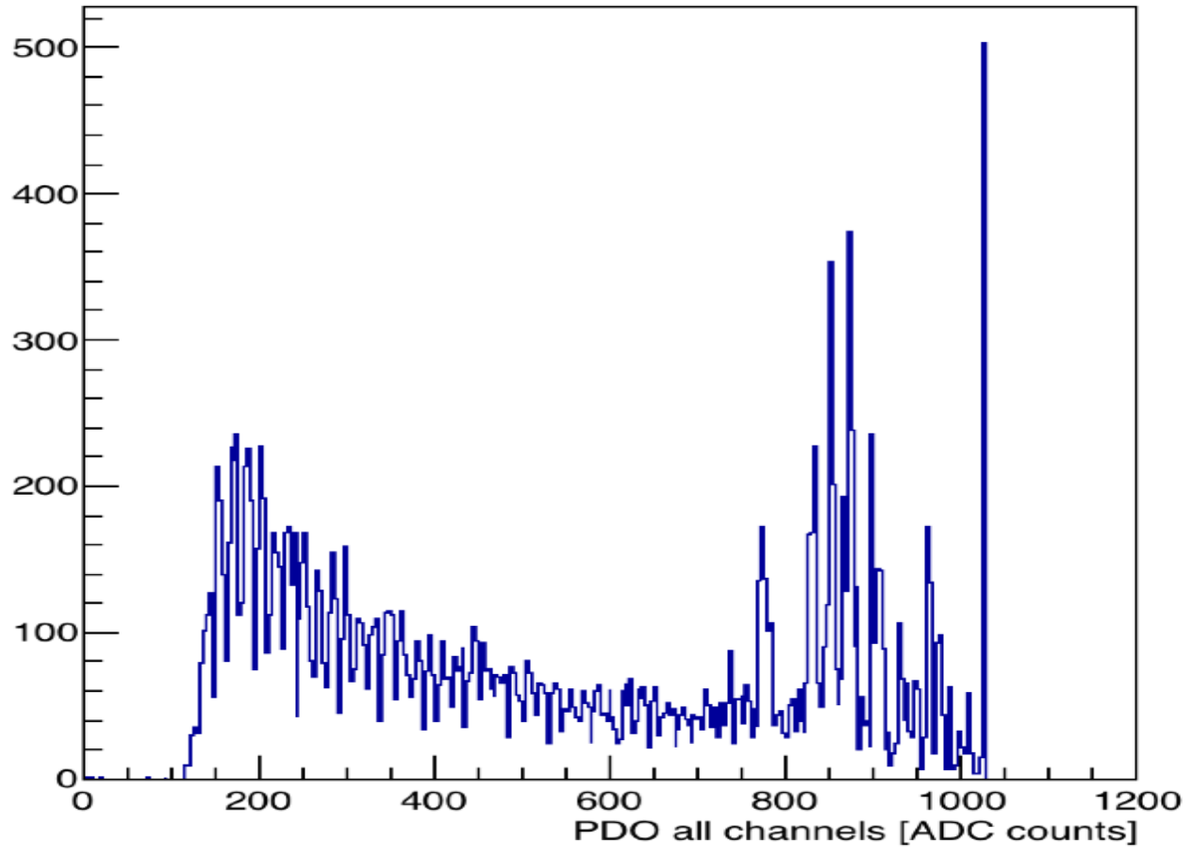


- ADC Core
  - 1024 shells
  - 64 macro-shells, 16 micro-shells each
  - resulting current is compared to a current proportional to the peak amplitude
  - First the comparison identifies one of the 64 macro-cells (6 high order bits)
    - Then on finer steps the lower 4 bits are identified
- Because of noise(?) some times the following macro-cell is wrongly identifies as the one giving the 6 high order bits
- But then then the current sum is already lower than the peak and therefore the 4 low order bits are zero

Domino ADC - Issue & Workaround

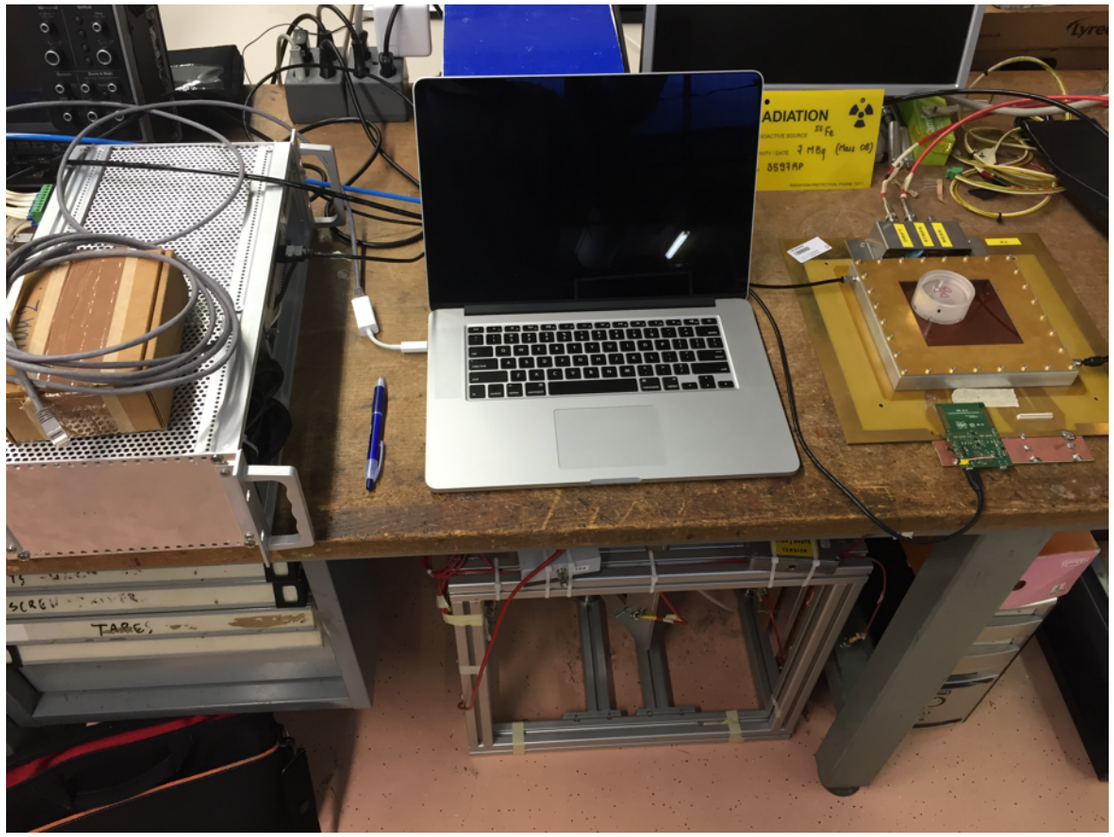
- **Resulting 000000xxxx repeated values**
- **Sophisticated clustering helps to filter out these values**

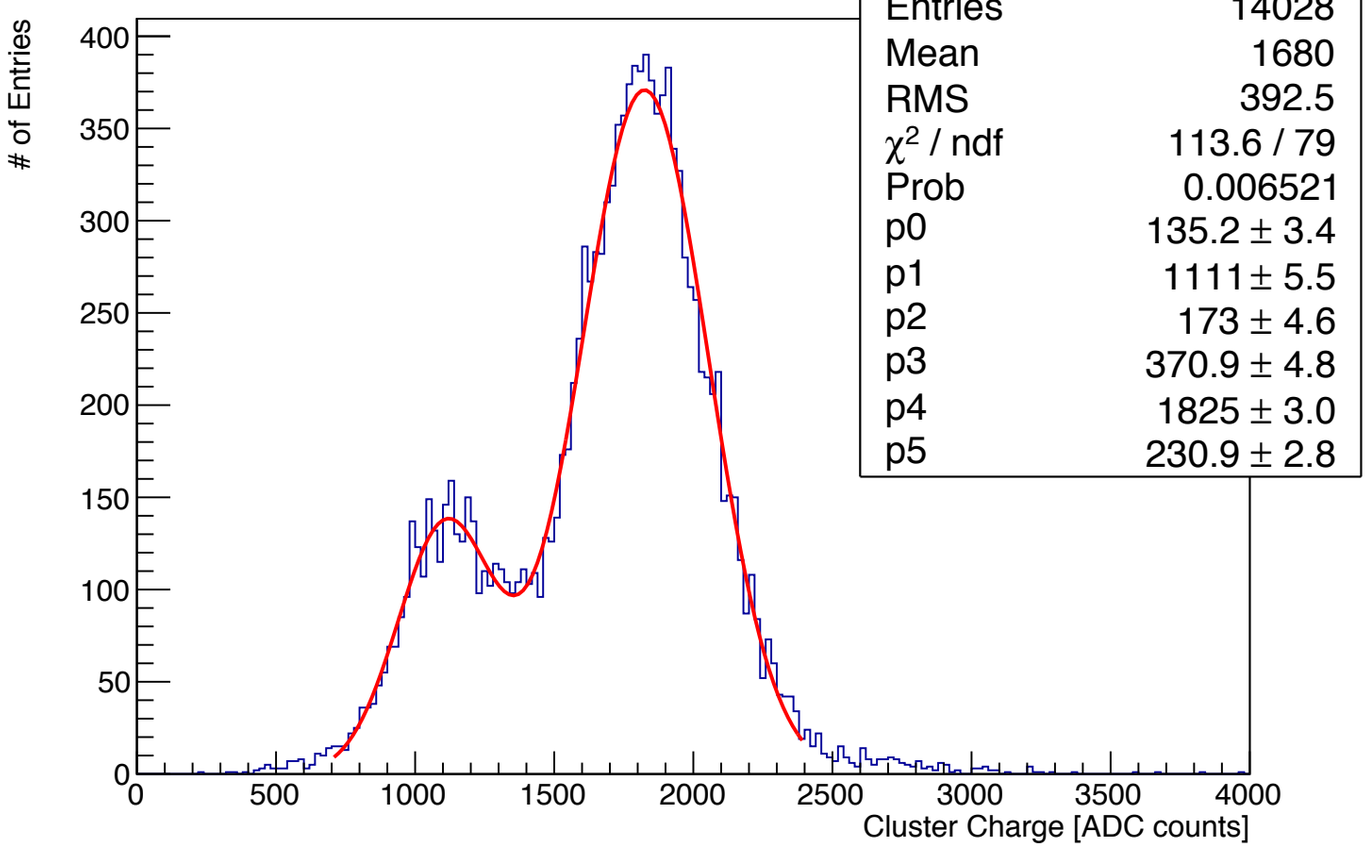




^{55}FE Spectrum

- Setup consists of 1xMicromegas “T” chamber operated at V_D=-300V and V_S=540V. Gas mixture is Ar+7%CO_2.
- The data are readout with random trigger at 152Hz.
- Gain 3mV/fC, threshold 250 DAC counts, neighbouring off
- No calibration, not optimised conditions, thresholds since there was no analog output on the current Mini2 board.
- Very preliminary result
- The VMM2 were not calibrated at all
- Low electronics gain (for the MM we typically need more than 9mV/fC)





VMM2 - Issues so far

Issue	Circuit	Solution	Simulated	Design status
Direct timing enable	Control logic	Logic inversion	yes	complete
Event loss from ADC reset	Channel logic	Logic fix and routing	yes	complete
Threshold bit error	Channel logic	Logic fix	yes	complete
DAC compression at baseline	MOSFET compression in DAC analog	MOSFET size and biasing	yes	complete
Internal pulser rise-time and noise	Channel injection switch	Optimize switch size	yes	complete
Gray-code counter turnaround	Counter cells	Re-routing	yes	complete
Floating node in output buffer at bypass	Buffer input stage	Switch addition	yes	complete
Recovery from saturating charge, ion current, and high rate	Front-end charge amplifier	Reduction of feedback time constant	Yes	in progress
Threshold crossing efficiency at high rate	Shaping amplifier	Implement bipolar response (SLF bypass)	Yes	in progress
MSB accumulations in 10-bit and 8-bit ADCs	ADC decision nodes	TBD	no	queued
Front-end disabled in negative mode with SFM low	Front-end charge amplifier	TBD		queued
Decay time in peak detector in analog readout mode	Leakage in hold node of peak detector	Dual front-end for voltage and current-mode	no	queued

Improvements in VMM3 and schedule

Function	Circuit	Status
L0 handling logic	Readout	in progress
SLVS IOs	Digital interface	in progress
Latency reduction in analog and digital paths (incl. ck to data)	Shaping amplifier and passive filter	queued
Operation at 2nF input capacitance	Front-end charge amplifier	queued
Simultaneous high-resolution and direct-output operation	Channel and control logic	queued
SEU-tolerant logic	Register, control and reset	queued
Direct input for ADC characterization	ADC or peak detector input node	queued
Configuration	Slow interface	being discussed

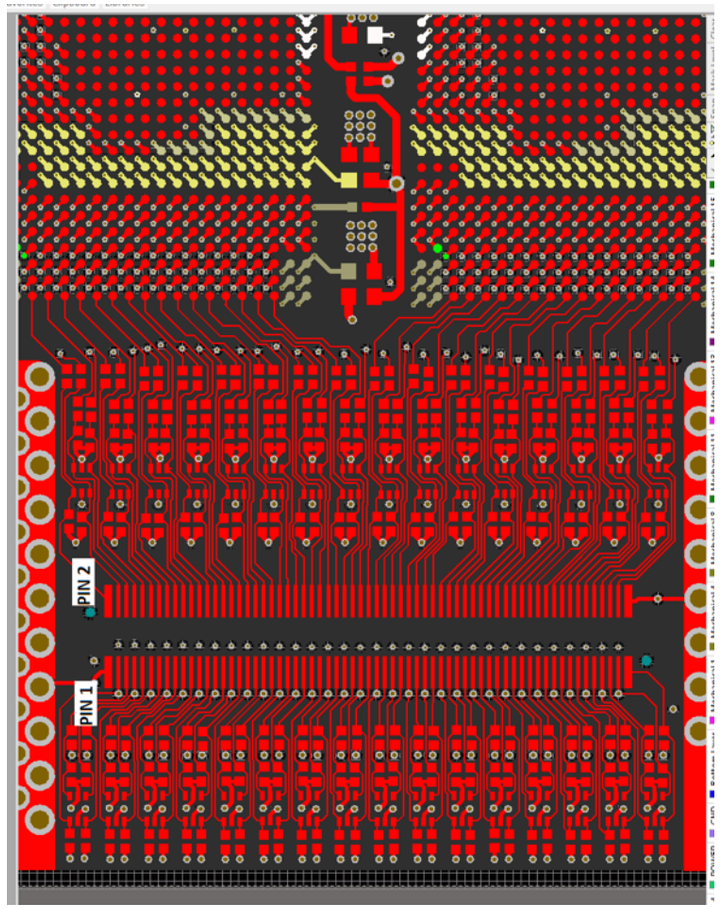
task	status
VMM2 design / fabrication	*complete*
BGA package	*complete*
PCB (AZ)	*complete*
VMM2 tests	*in progress*
VMM SEU & L1H circuits	*in progress*
VMM3 design	*in progress*

Conclusions

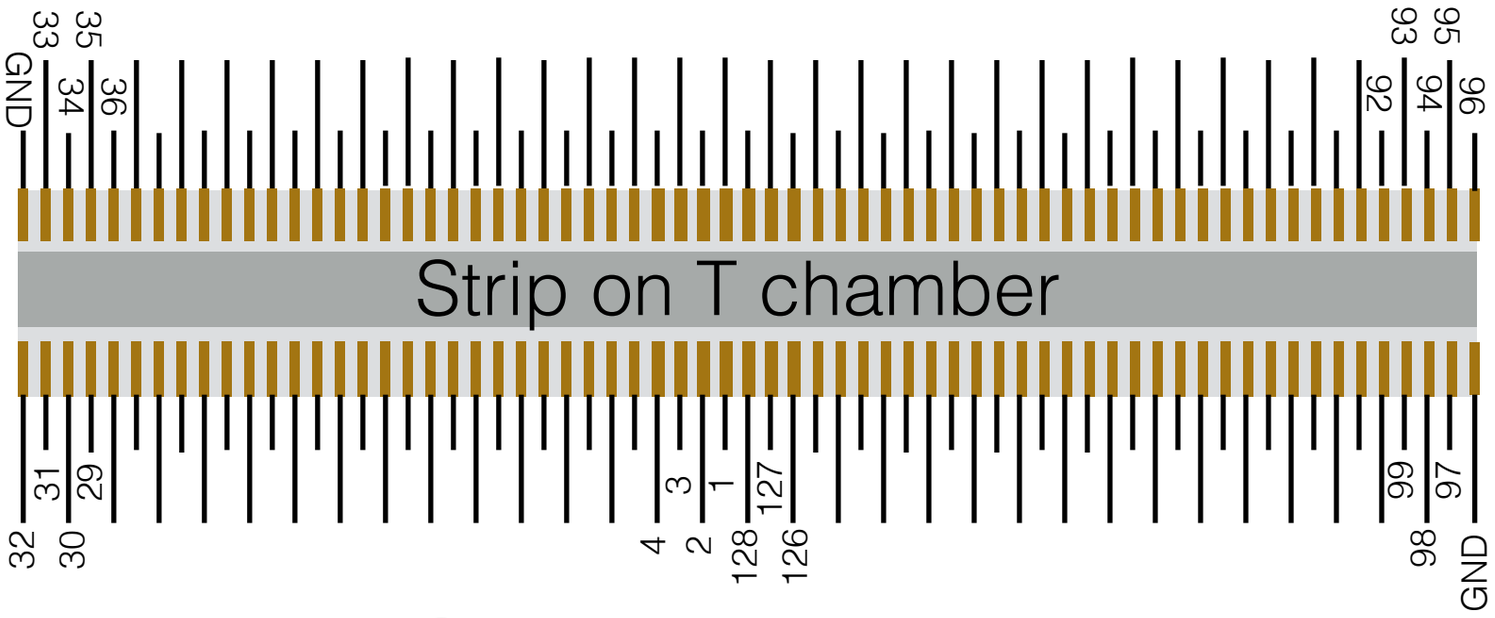
- VMM2 was realised finally within NASA guidelines for selection and use of BGA
- Mini2 (SRS) hybrid worked fine - We look forward for the new one with the analog output
- DCARD needs to be revised due to high power consumption of the 2xVMM2 board
- The readout and configuration of the VMM2 was understood
- Overall good functionality
- ADCs need revision
- Most of the issues identified - still ongoing work
- Design and fixes will be implemented in VMM3 with additional functionality (expected in fall 2015)

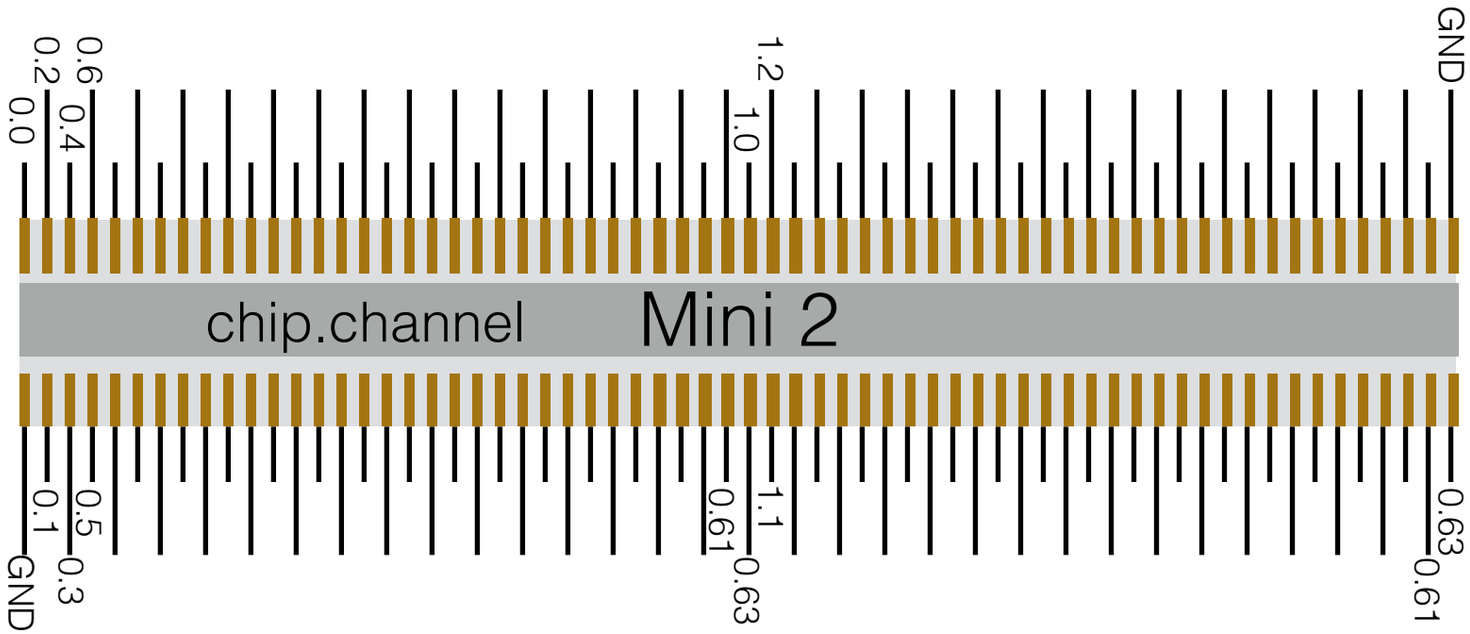
Backup

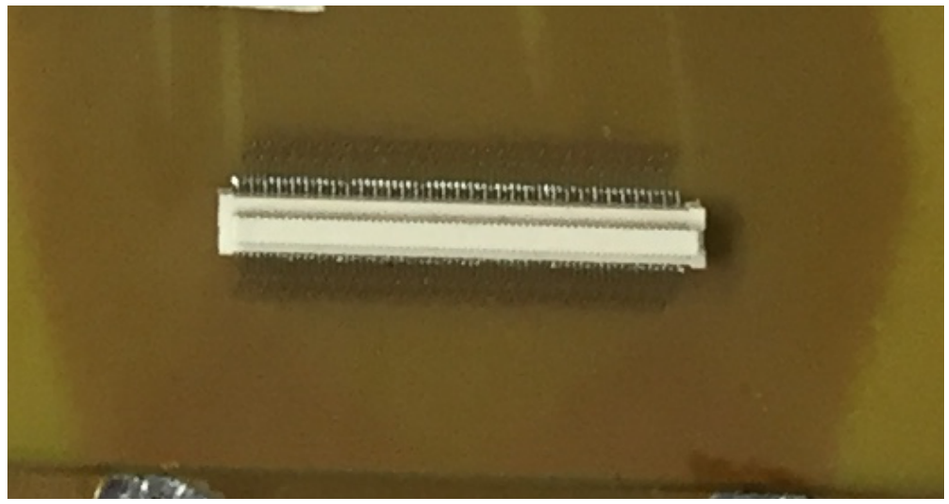
Strip-Electronics mapping (1/2)



- The mapping was done to translate the T chamber strips to electronic channels.
- In the way the Mini-2 card is designed the VMM **neighbour logic cannot be tested** unless there is an adapter board. (valid for T, Tmm chambers, probably ok for large modules).







Readout issues…

Problematic Pattern with stuck values - Crosstalk on mini2 ??

- Cluster: 8
  - Channel: 66 (VMM 1.3), chip: 1, pdo: 192, tdo: 60, bcid: 2011
- charge of the cluster: 192
- Cluster: 9
  - Channel: 127 (VMM 1.2), chip: 1, pdo: 192, tdo: 60, bcid: 2011
- charge of the cluster: 192
- Cluster: 10
  - Channel: 68 (VMM 1.7), chip: 1, pdo: 610, tdo: 75, bcid: 2011
  - Channel: 69 (VMM 1.9), chip: 1, **pdo: 147, tdo: 72**, bcid: 2011
- charge of the cluster: 757
- Cluster: 11
  - **Channel: 124 (VMM 1.8), chip: 1, pdo: 147, tdo: 72, bcid: 2011**
  - **Channel: 124 (VMM 1.8), chip: 1, pdo: 147, tdo: 72, bcid: 2011**
  - **Channel: 124 (VMM 1.8), chip: 1, pdo: 147, tdo: 72, bcid: 2011**
  - **Channel: 124 (VMM 1.8), chip: 1, pdo: 147, tdo: 72, bcid: 2011**
- charge of the cluster: 735
- Cluster: 12
  - Channel: 68 (VMM 1.7), chip: 1, **pdo: 323, tdo: 75,** bcid: 2011
- charge of the cluster: 323
- Cluster: 13
  - **Channel: 125 (VMM 1.6), chip: 1, pdo: 323, tdo: 75, bcid: 2011**
  - **Channel: 125 (VMM 1.6), chip: 1, pdo: 323, tdo: 75, bcid: 2011**
  - **Channel: 125 (VMM 1.6), chip: 1, pdo: 323, tdo: 75, bcid: 2011**
  - **Channel: 125 (VMM 1.6), chip: 1, pdo: 323, tdo: 75, bcid: 2011**
  - **Channel: 125 (VMM 1.6), chip: 1, pdo: 323, tdo: 75, bcid: 2011**

- Cluster: 0 (neighbouring channels in VMM give same results and one stuck with PDO=xxxxxx0000)
  - Channel: 67, chip: 1, pdo: **1025**, tdo: 78, bcid: 1488
  - **Channel: 68 (VMM 1.7), chip: 1, pdo: 619, tdo: 64, bcid: 1488**
  - **Channel: 125, (VMM 1.6) chip: 1, pdo: 619, tdo: 64, bcid: 1488**

- Cluster: 0 (same channel fires twice with same numbers)
  - **Channel: 117, chip: 1, pdo: 1025, tdo: 67, bcid: 991**
  - **Channel: 117, chip: 1, pdo: 1025, tdo: 67, bcid: 991**

- Event: (PDO & TDO = 0 !)
  - **Event: 13986, UDP: 143, chip: 0, channel: 2, pdo: 0, tdo: 0, bcid: 1, gray (decoded): 1**
  - **Event: 13986, UDP: 144, chip: 0, channel: 2, pdo: 0, tdo: 0, bcid: 1, gray (decoded): 1**
  - **Event: 13986, UDP: 145, chip: 0, channel: 2, pdo: 0, tdo: 0, bcid: 1, gray (decoded): 1**
  - **Event: 13986, UDP: 57, chip: 0, channel: 0, pdo: 0, tdo: 40, bcid: 528, gray (decoded): 992**
  - **Event: 13986, UDP: 58, chip: 0, channel: 0, pdo: 0, tdo: 40, bcid: 528, gray (decoded): 992**
  - **Event: 13986, UDP: 59, chip: 0, channel: 0, pdo: 0, tdo: 32, bcid: 528, gray (decoded): 992**
  - **Event: 13986, UDP: 60, chip: 0, channel: 0, pdo: 0, tdo: 32, bcid: 528, gray (decoded): 992**