

VMM ASIC Status Report

<u>George Iakovidis</u> Vinnie Polychronakos Gianluigi De Geronimo

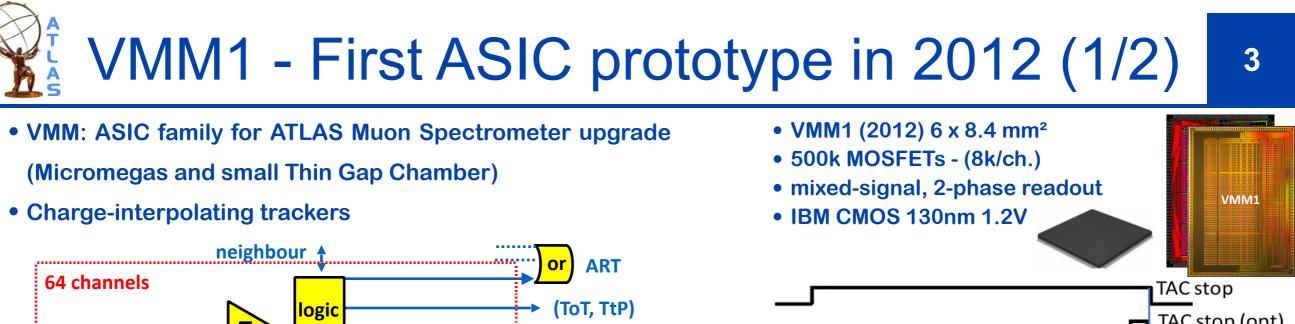


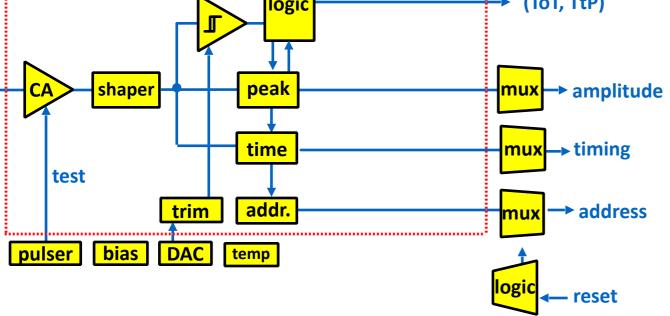
RD51 - Collaboration meeting

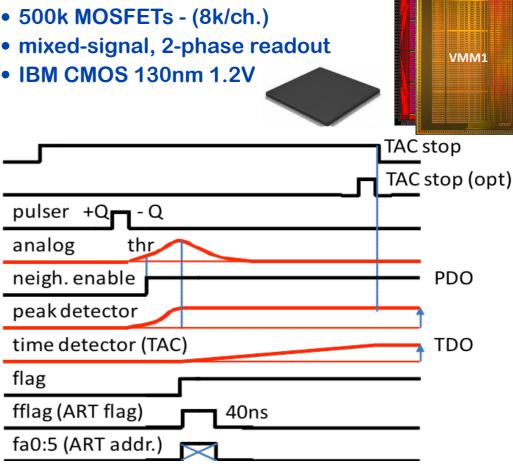


- VMM1 as the first prototype of the VMM ASIC.
 - Design, architecture and specs
 - Testing, noise
 - Test beam results
- VMM ASIC evolution
- VMM2 Design and new features
 - Timeline and delays in packaging
 - Board prototype and integration to the SRS
 - Issues until now and timeline for VMM3
- Conclusions









- dual polarity, adj. gain (0.5, 1, 3, 9 mV/fC) (0.11 to 2 pC), adj. peak-time (25-200 ns)
- discriminator with sub-hysteresis and neighbouring (channel and chip)
- address of first event in real time at dedicated output (ART)
- direct timing outputs: time-over-threshold or time-to-peak
- peak detector, time detector <1 ns
- multiplexing with sparse readout and smart token passing (channel and chip)
- threshold and pulse generators, analog monitors, channel mask, temperature sensor, 600mV BGR, 600mV LVDS
- G. De Geronimo et al. "VMM1 An ASIC for Micro-pattern Detectors". Nuclear Science, IEEE Transactions on 60 (June 2013), p. 2314.

doi: 10.1109/TNS. 2013.2258683.

George lakovidis - RD51 Collaboration meeting

VMM1 - First ASIC prototype in 2012 (2/2)

- First prototypes (x16) tested in 2012 test beam successfully with custom made readout system.
- First time testing the Resistive Micromegas as trigger system.
- 4 [degrees] Angular Resolution [mrad **Trigger on threshold** <u>200 호</u> Trigger on peak Angular Resolution [C C C C 180 🚊 patial Re 740 Tel 740 120 0.8 100 Angular Resolution VMM1 80 1.5 0.6 60 Spatial Resolution VMM1 0.4 0.5 0 02 25 30 35 10 15 20 25 30 theta [dearees] Angle [Degrees] TDO RMS [ns] [O] 0.5 SWB 0.45 WB 0.4 .8F .6F 0.35 0.3 0.25 Ж Ж 0.2 0.15 0.1 0.4 0.05 0 0.2 0.4 0.6 0.8 1.2 400 500 600 200 300 700 PDO [V] DAC [cnt]
- Couple of bugs found in the design and fixes implemented in the next version(s)

T. Alexopoulos et al. - Performance of the First Version of VMM Front-End ASIC with Resistive Micromegas Detectors,

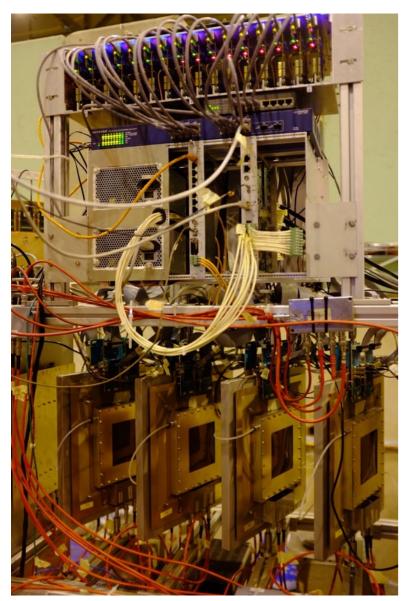
ATL-UPGRADE-PUB-2014-001, https://cds.cern.ch/record/1753328?In=en



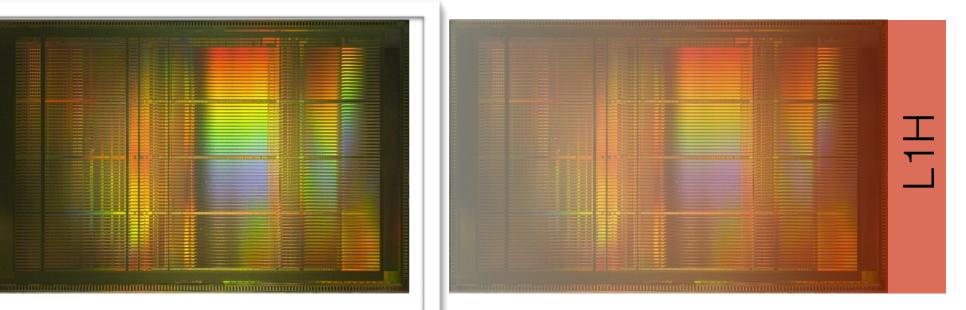
George lakovidis - RD51 Collaboration meeting

19/03/2015

Δ







- VMM1 (2012)
- 50 mm²
- 500k MOSFETs
- (8k/ch.)
- mixed-signal
- 2-phase readout

- VMM2 (2014)
- 115 mm²
- > 5M MOSFETs (>80k/ch.)
- planned deep re-design of VMM1
- higher functionality and complexity
- continuous fully-digital readout

- VMM3 (2015-16)
- 130 mm²
- > 6M MOSFETs
- includes L1 handling and SEUtolerant logic

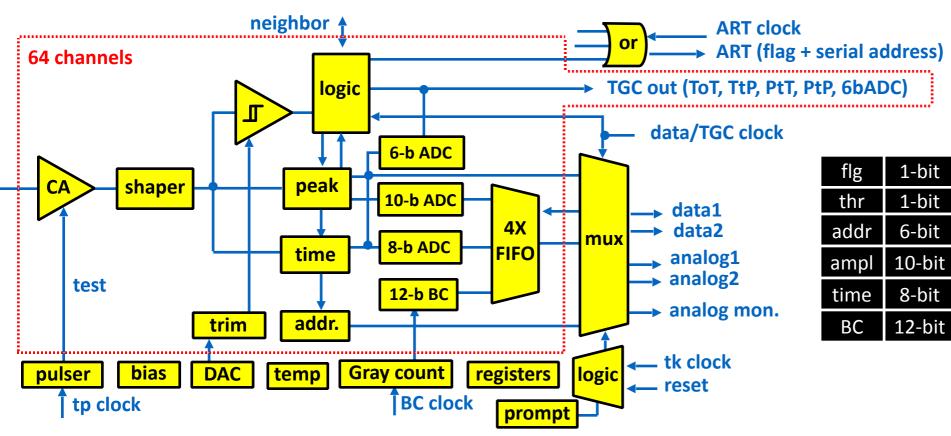
G. De Geronimo - "VMM2 - An ASIC for the New Small Wheel". TWEPP 2014 - Topical Workshop on Electronics for Particle Physics.

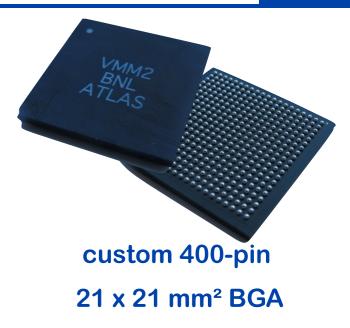
https://indico.cern.ch/event/299180/session/4/contribution/45



George Iakovidis - RD51 Collaboration meeting

VMM2 - Second ASIC prototype in 2014





6

- adjustable discrimination threshold per channel
- trimming range: 15 mV in 1m increments
- sub-hysteresis mode: effective discrimination ~ 2 mV
- neighbour logic: sub-threshold neighbor channels
- polarity: adjustable positive or negative
- gain: adjustable 0.5, 1, 3, 4.5, 6, 9, 12, 16 mV/fC (max charge 2 to 0.06 pC)
- peaking time: adjustable 25, 50, 100, 200 ns

- clock frequency: up to 200 MHz to the 6bit ADC
- 12-bit timestamp: 12-b Gray-code counter on BC provides timing TAC stop (20-b, ~100 μs, sub-ns resolution)
- 4-deep FIFO
- 10-bit, 200 ns , 1.5 mW, for peak amplitude
- 8-bit, 100 ns , 1.5 mW for peak timing (relative to BC)
- 38-bit event data at digital outputs

BROOKHAVEN

George lakovidis - RD51 Collaboration meeting

VMM2 - Manufacturing and packaging

- Wafers processed at IBM, die received at BNL May 18
- BGA substrate design was completed by that time
- Expected packaged devices in 6-8 weeks
- In late August i2a (packaging company) informed us that their moulding equipment had broken down and would take 2 weeks to fix it
- Subsequently they decided that they need to replace it and that would take months
- They proposed using a workaround and packaged 26 chips which we received in September and were not flat even to the naked eye.
- In addition the size of the chips was wrong 22.7x22.7 mm² instead of 21x21mm²
- Nevertheless we used them to hand assemble a few mini-one and SRS128 boards with mixed results (occasional shorts at the corners)
- On 27/10 we received another batch of 11 devices. (Still wrong size)

VMM2 - Present Status

- NASA guidelines for selection and use of BGA: <5% of BGA size In our case < 100 microns
- First batch non-coplanarity 150-200 um (6-8 mils)
- Second batch ~ 100-150um (4-6 mils)
- After the first batch all were trimmed to correct size (21x21 mm²)
- Received the remaining 163 devices from the original 200-die lot

Measured 8 randomly:	PV [microns]	PV [mils]
 Results excellent, even meet NASA's strict guidelines 	32.7	1.28
	37.9	1.49
	78.5	3.09
 Laser probe of a CMM Machine 	87.4	3.44
 Scans were made with a 1 mm sampling period in x 	34.1	1.34
and y in the regions between the solder bumps.	49.2	1.94
	70.3	2.76
	34.5	1.36



VMM2 - Frontend boards and readouts

First wire bonded front end for testing purposes Four Mini-1 cards were assembled with the first batch of non-planar VMM2 ASICs



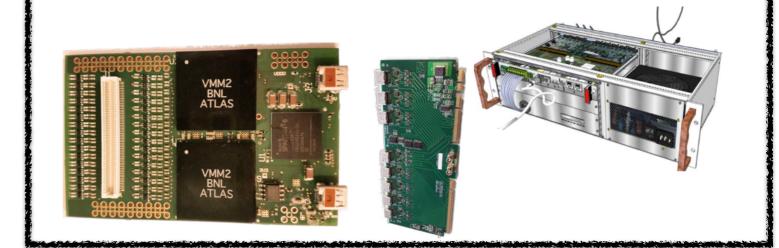
MMFE8- frontend board with 8xVMM2 - final board prototype by next month

2		Contraction of the local division of the		Contraction of Contra
······································		(and a start of a	NH PHH PH. PH	
				auguran in a second a
Diat Jawa Jawa				Ams in Ams
				LAS
	UIS UIS SA			
	ARTX-7			
	Little Contraction			once manna a M
				1997 - 2096 - 2096 - 2
	(11-1-1-1-1-7-7-Q	CONTRACTOR OF CONTRACTOR
				10111

Same board with packaged chip



Mini-2 - frontend board with 2xVMM2 for the SRS 2xHDMI one for the readout and the other for the trigger signals (ART) DCARD instead of the ADC card Same FEC classic card with another firmware Readout UDP based SRS protocol



BROOKHAVEN

George Iakovidis - RD51 Collaboration meeting



VMM2 - SRS - Software developed

Calibration

Gain Range

Pulser Range

Events

Threshold Range

Channel Range

1000

🖊 Write Data

3.0 mV/fC

50

5

\$

0 200

Analog tristates Off

TAC Slop Adj (stc) 125 ns

Mode Timing At 📀 Dual Clock Off

300

30

Manual 💽 Auto

400

Disable At Peak Off

SBMX Off

On

Off

Off

0

Off

Off

N.T.U. Athens

BROOKHAVEN

 \odot

0

0

Masking

Show Channels 🗸 Enable Debu

3.0 mV/fC

0

0

50

20

6b ADC Low

0

\$

SMX 0 ns 🗘 0 ns 🗘 0 ns 🗘

0 ns

0 ns 😒

Ons 🗘 Ons 🗘 Ons 🗘

0 ns 🗘 0 ns 🗘

0 ns 📫

0 ns 💲

0 ns 😂

0 ns 💲

0 ns \Rightarrow

0 ns 📫

0 ns 💲

0 ns 😂

0 ns 🗘

🛾 0 ns 📘 😂

0 ns

0 ns 😂

0 ns 0 ns 📫

0 ns 💲

0 ns 😂

0 ns 💲

0 ns 😂

0 ns 😂

0 ns 💲

0 ns 😳

0 ns 💲

0 ns 🖸

🗧 🛛 🔿 🕄

0 ns 🗘 0 ns 🗘

0 ns 🜔 0 ns 😂

0 ns 🖸 0 ns 🕄

0 ns 🗘 0 ns 🗘

0 ns 0

0 ns 0

0 ns 🔅

0 ns

0 ns

0 ns 😂

0 ns 🔅

0 ns

0 ns

0 ns

0 ns 🚺 0 ns 🔒

0 ns \Rightarrow

0 ns 🔅

0 ns

0 ns

0 ns

0 ns

0 ns

0 ns 🔅 0 ns 🔅

0 ns

0 ns 😒

0 ns 💲

0 ns

0 ns

0 ns

0 ns

0 ns \Rightarrow

0 ns 🔅

0 ns 🔅 0 ns

0 ns 🔛

Control		Global Registers	
	2 1 🗘	Ch. polarity negative	Analog tristates
Open Communication All A	Channels	Gain (sg) 3.0 mV/fC	TAC Slop Adj (stc)
APP FEC	HDMI 1 2	Neighbor Trigger (sng) Off	Disable At Peak
Read O Write	1 🗹 🗹 🗸	Leak. Curr. Enabled	Oouble Leak
All Send 7495	2	Peak time (st) 200 ns	Sub Hysterisis
Trigger Acquisition TP Delay ACQ Sync	4	ART On ᅌ Mode 1	Timing At ᅌ Dual Cloc
81 0 x25ns Trg Per ACQ Win	6	sbfm Off ᅌ sbfp	Off ᅌ sbft
3FFFE 4096 \$x25ns	8	Ch. Mon 1 (P DAC 📀 SCM)	COFF SBMD
Set Pulser External ACQ On	Set Mask Link Status	ADCs	Enable
ACQ Off	Reset Links	Direct Time Off 📀 M	Node 0
Frame Ci 🗘 Set	WarmInit FEC	8-bit Conv. Mode On	ᅌ 6-bit
ADDC	VMM2 Reboot FEC	10b ADC 200ns ᅌ 8b AD	C 100ns ᅌ 6b AE
10 0 0	9	Dual Clock Data Off	Dual Clock 6-bit
Connect Disconnect	N/A	Threshold DAC	300
DAC Data Trigg	er Counter	Test Pulse DAC 269.34 mV	50
Off test Dis	sable Clear	Load Calibratic	oad Threshok
Time Window	Read	Use Mapping	
255 🗘 Set	Init	- Ose Mapping	
Run Control			
Run Number 9003 C A	ngle 0 🗘 CI	ear Counters 0 Hits 973195	
Directory prationData_2015_Jan	Feb	Start Run Stop Run	NATE NATE
Comments	Run:	9002 finished Trigger Date	a Calibration

VMM2 Channels

	SP	SC	SL	ST	SM	0 mV	SM	x) ns	0	0 ns	0	0 ns	0			SP	SC	SL	ST	SM	0 п
1	negative					0 mV) ns	0	0 ns	0	0 ns	٢	33	n	egative	•				0 n
2	negative					0 mV] _]) ns		0 ns	0	0 ns	٥	34	n	egative					0 r
3	negative					0 mV		10) ns	0	0 ns	0	0 ns	٥	35	n	egative					0 r
4	negative					0 mV) ns	0	0 ns	0	0 ns	\$	36	n	egative					0 r
5	negative	1				0 mV) ns		0 ns	0	0 ns	0	37	n	egative					0
6	negative	1				0 mV		0) ns		0 ns	0	0 ns	0	38	n	egative					0
7	negative					0 mV		10) ns	0	0 ns	0	0 ns	0	39	n	egative					0
8	negative					0 mV) ns	0	0 ns	0	0 ns	0	40	n	egative					0
9	negative	1				0 mV) ns		0 ns	0	0 ns	0	41	n	egative					0
10	negative					0 mV		10) ns	0	0 ns	0	0 ns	٥	42	n	egative	5				0
11	negative					0 mV) [) ns	0	0 ns	0	0 ns	٥	43	n	egative					0
12	negative					0 mV) ns	0	0 ns	0	0 ns	٥	44	n	egative	•				0
13	negative					0 mV) ns	0	0 ns	0	0 ns	0	45	n	egative					0
14	negative					0 mV) ns	0	0 ns	0	0 ns	0	46	n	egative					0
15	negative	1				0 mV) ns		0 ns	0	0 ns	0	47	n	egative					0
16	negative	1				0 mV		10) ns	0	0 ns	0	0 ns	٢	48	n	egative	,				0
17	negative	1				0 mV		10) ns	0	0 ns	0	0 ns	٢	49	n	egative	,				0
18	negative	1				0 mV		10) ns	0	0 ns	0	0 ns	0	50	n	egative	,				0
19	negative	1				0 mV		10) ns	0	0 ns	0	0 ns	٥	51	n	egative	,				0
20	negative	1				0 mV		10) ns	0	0 ns	0	0 ns	٢	52	n	egative	,				0
21	negative	5				0 mV		10) ns	0	0 ns	0	0 ns	0	53	n	egative					0
22	negative					0 mV]	0) ns	0	0 ns	0	0 ns	0	54	n	egative					0
23	negative					0 mV) ns	0	0 ns	0	0 ns	٥	55	n	egative					0
24	negative					0 mV) ns	0	0 ns	0	0 ns	0	56	n	egative					0
25	negative	1				0 mV) ns		0 ns	0	0 ns	0	57	n	egative					0
26	negative	1				0 mV		10) ns	0	0 ns	0	0 ns	٢	58	n	egative	,				0
27	negative					0 mV) ns	0	0 ns	0	0 ns	0	59	n	egative					0
28	negative	1				0 mV		10) ns	0	0 ns	0	0 ns	0	60	n	egative					0
29	negative	1				0 mV		10) ns	0	0 ns	0	0 ns	٢	61	n	egative	,				0
30	negative	1				0 mV		10) ns	0	0 ns	0	0 ns	٢	62	n	egative	,				0
31	negative					0 mV		10) ns	0	0 ns	0	0 ns	٥	63	n	egative	,				0
_	negative	-				0 mV]] [) ns	0	0 ns	0	0 ns	0		-	egative	_				0
	C															C	Deprio	cate	d			
	ear																Data I					
Ck	ear																2		0	T	0	
																	CQ		Data	t Mov	de-Tin	20.6





FEC Response

Reg ID :7495

Data, 2: aaaafff

Data, 1: 3

Data, 3:0

Data, 4:0

Data, 5: 1

NEW PACKET RECEIVED

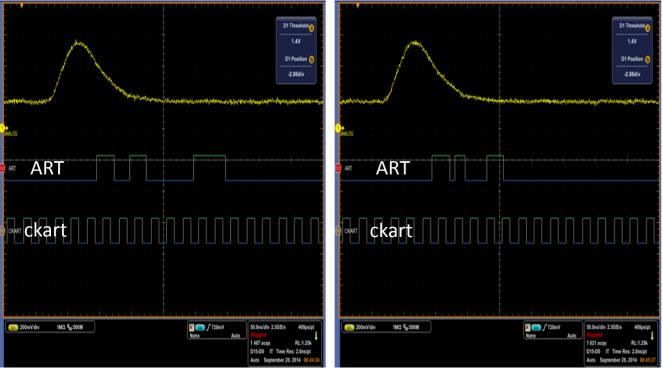
Data Received Size: 24 bytes

Clear

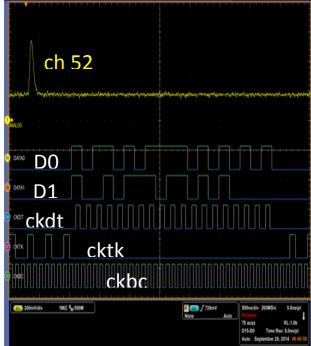
George lakovidis - RD51 Collaboration meeting

VMM2 - Preliminary tests from designer

• ART output in single and dual data / clock

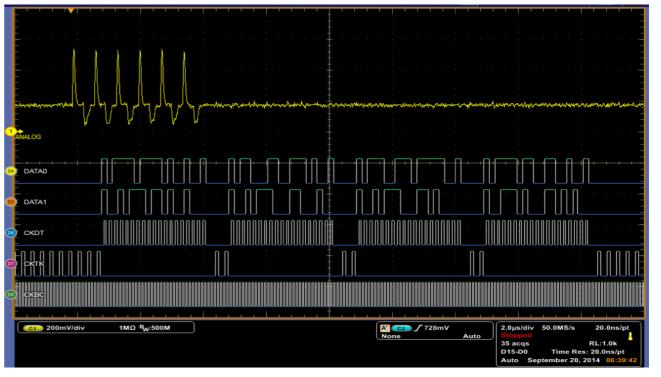


• Flag, threshold, address, amplitude, timing, timestamp appear correct





Digital readout with FIFO for 6-event burst





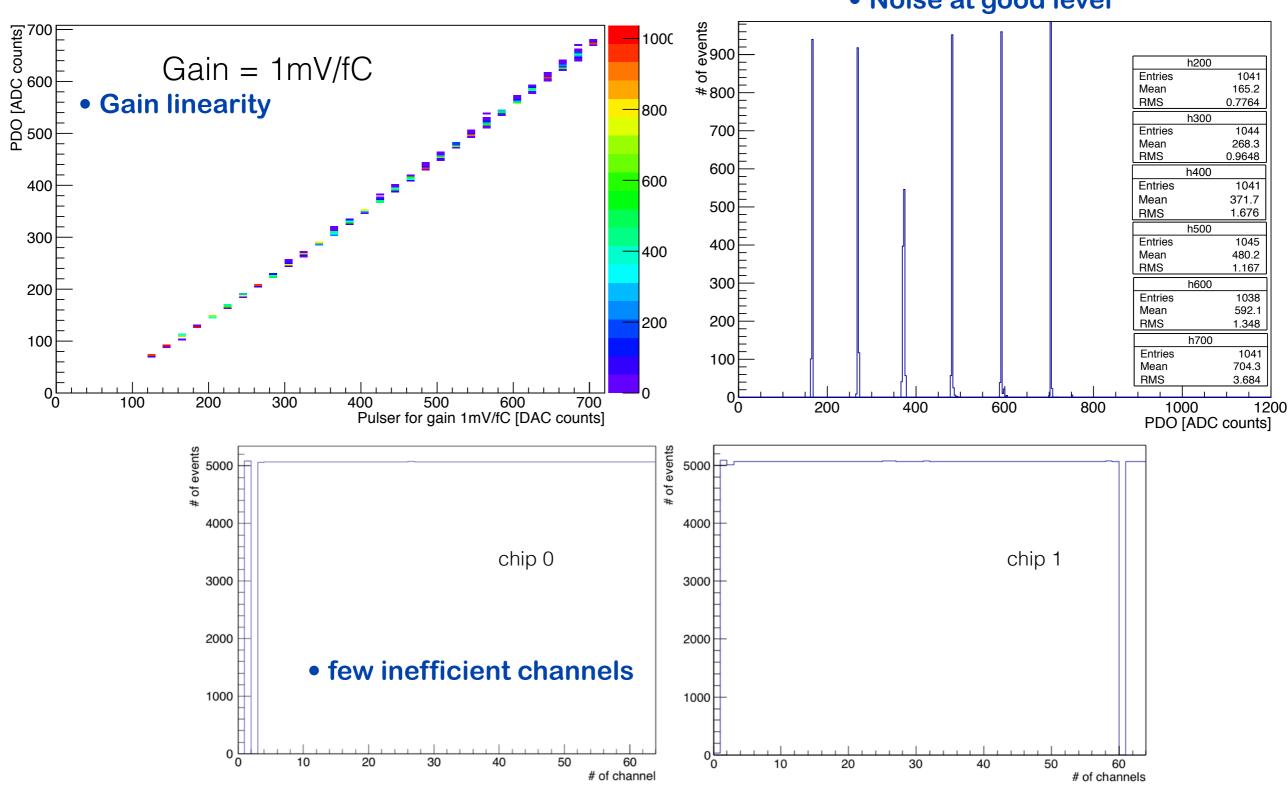
George lakovidis - RD51 Collaboration meeting

19/03/2015

11

ART auto-reset at end of serialisation works fine

Tests with internal pulser - SRS AS



• Noise at good level

19/03/2015

George lakovidis - RD51 Collaboration meeting

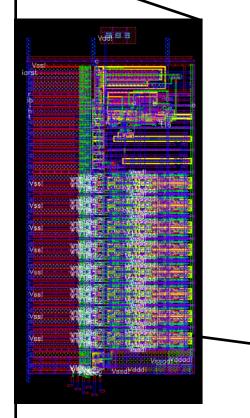
ΤEΝ

BRO

ATIONAL LABORATORY

10-bit Current-Mode Domino ADC

Via				100
	1.0 La		a diamana ang barangan baranga	
				Read
				122



• ADC Core

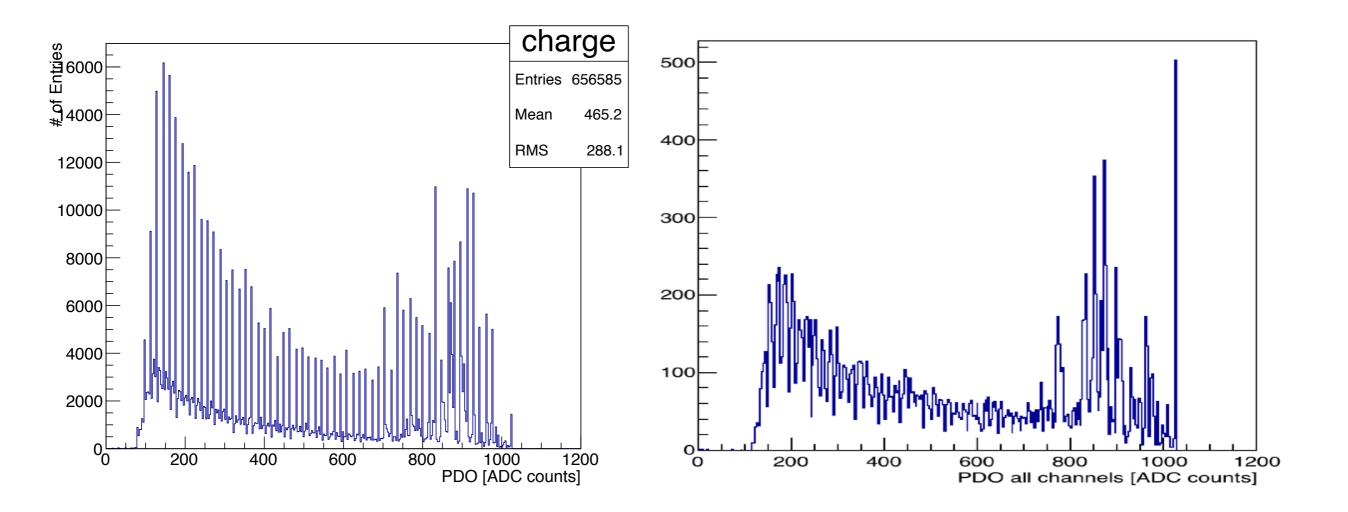
- 1024 shells
- 64 macro-shells, 16 micro-shells each
- resulting current is compared to a current proportional to the peak amplitude
- First the comparison identifies one of the 64 macro-cells (6 high order bits)
- Then on finer steps the lower 4 bits are identified
- Because of noise(?) some times the following macro-cell is wrongly identifies as the one giving the 6 high order bits
- But then then the current sum is already lower than the peak and therefore the 4 low order bits are zero

BROOKHAVEN

George Iakovidis - RD51 Collaboration meeting



- Resulting 000000xxxx repeated values
- Sophisticated clustering helps to filter out these values



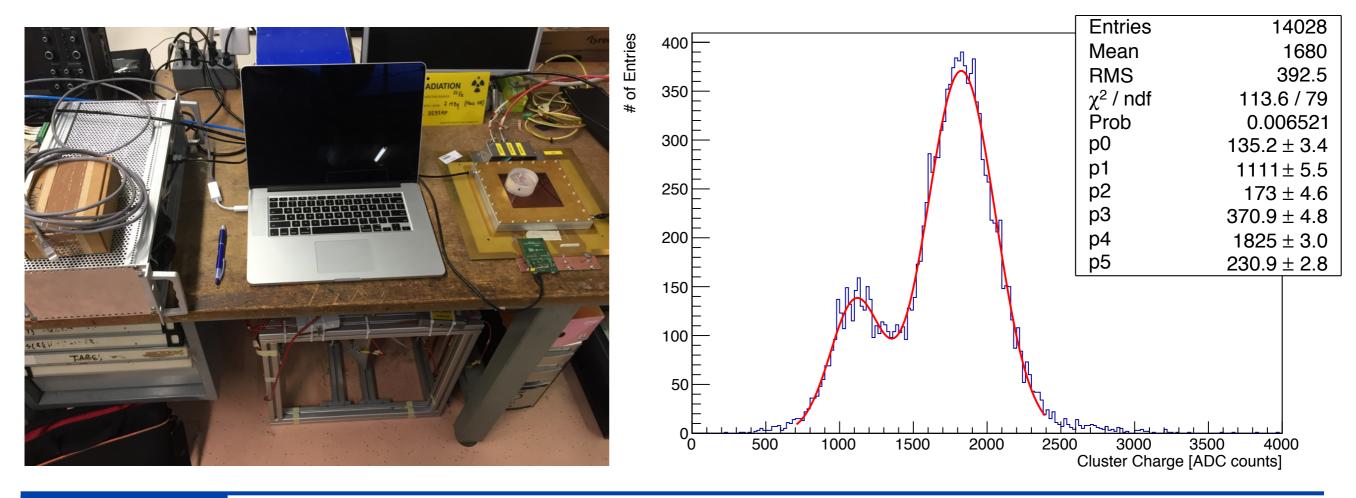
BROOKHAVEN George lakovidis - RD51 Collaboration meeting

19/03/2015

14

55FE Spectrum

- Setup consists of 1xMicromegas "T" chamber operated at V_D =-300V and V_S =540V. Gas mixture is Ar+7%CO₂.
- The data are readout with random trigger at 152Hz.
- Gain 3mV/fC, threshold 250 DAC counts, neighbouring off
- No calibration, not optimised conditions, thresholds since there was no analog output on the current Mini2 board.
- Very preliminary result
- The VMM2 were not calibrated at all
- Low electronics gain (for the MM we typically need more than 9mV/fC)





George Iakovidis - RD51 Collaboration meeting



Issue	Circuit	Solution	Simulated	Design status
Direct timing enable	Control logic	Logic inversion	yes	complete
Event loss from ADC reset	Channel logic	Logic fix and routing	yes	complete
Threshold bit error	Channel logic	Logic fix	yes	complete
DAC compression at baseline	MOSFET compression in DAC analog	MOSFET size and biasing	yes	complete
Internal pulser rise-time and noise	Channel injection switch	Optimize switch size	yes	complete
Gray-code counter turnaround	Counter cells	Re-routing	yes	complete
Floating node in output buffer at bypass	Buffer input stage	Switch addition	yes	complete
Recovery from saturating charge, ion current, and high rate	Front-end charge amplifier	Reduction of feedback time constant	Yes	in progress
Threshold crossing efficiency at high rate	Shaping amplifier	Implement bipolar response (SLF bypass)	Yes	in progress
MSB accumulations in 10-bit and 8-bit ADCs	ADC decision nodes	TBD	no	queued
Front-end disabled in negative mode with SFM low	Front-end charge amplifier	TBD		queued
Decay time in peak detector in analog readout mode	Leakage in hold node of peak detector	Dual front-end for voltage and current-mode	no	queued



George lakovidis - RD51 Collaboration meeting

Improvements in VMM3 and schedule

Function	Circuit	Status
L0 handling logic	Readout	in progress
SLVS IOs	Digital interface	in progress
Latency reduction in analog and digital paths (incl. ck to data)	Shaping amplifier and passive filter	queued
Operation at 2nF input capacitance	Front-end charge amplifier	queued
Simultaneous high-resolution and direct-output operation	Channel and control logic	queued
SEU-tolerant logic	Register, control and reset	queued
Direct input for ADC characterization	ADC or peak detector input node	queued
Configuration	Slow interface	being discussed

task	status
VMM2 design / fabrication	complete
BGA package	complete
PCB (AZ)	complete
VMM2 tests	in progress
VMM SEU & L1H circuits	in progress
VMM3 design	in progress



George Iakovidis - RD51 Collaboration meeting



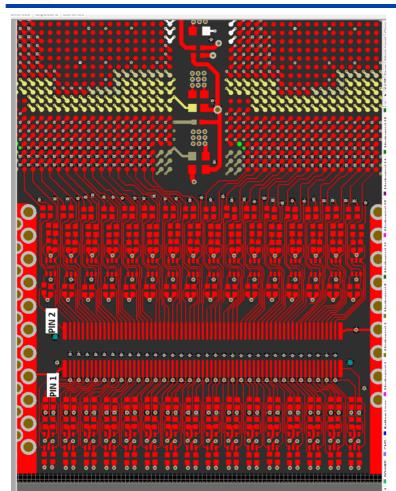
- VMM2 was realised finally within NASA guidelines for selection and use of BGA
- Mini2 (SRS) hybrid worked fine We look forward for the new one with the analog output
- DCARD needs to be revised due to high power consumption of the 2xVMM2 board
- The readout and configuration of the VMM2 was understood
- Overall good functionality
- ADCs need revision
- Most of the issues identified still ongoing work
- Design and fixes will be implemented in VMM3 with additional functionality (expected in fall 2015)



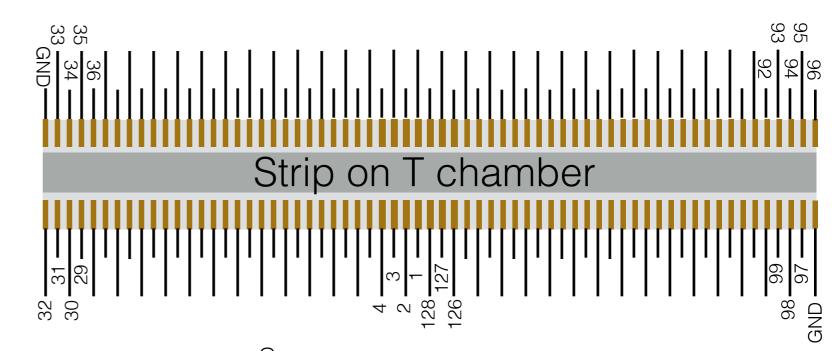


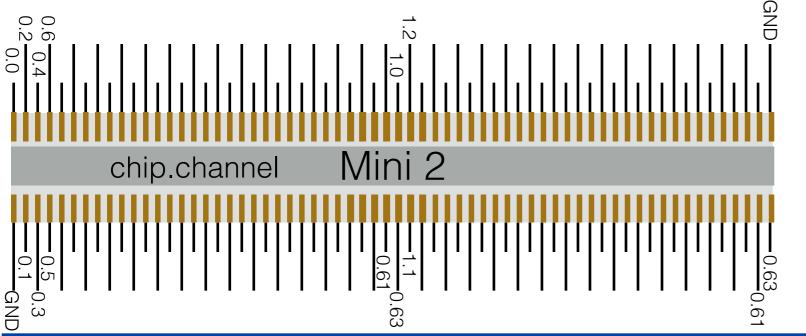


Strip-Electronics mapping (1/2)



- The mapping was done to translate the T chamber strips to electronic channels.
- In the way the Mini-2 card is designed the VMM neighbour logic cannot be tested unless there is an adapter board. (valid for T, Tmm chambers, probably ok for large modules).







George lakovidis - RD51 Collaboration meeting



- Problematic Pattern with stuck values Crosstalk on mini2 ??
- Cluster: 8
 - Channel: 66 (VMM 1.3), chip: 1, pdo: 192, tdo: 60, bcid: 2011
- charge of the cluster: 192
- Cluster: 9
 - Channel: 127 (VMM 1.2), chip: 1, pdo: 192, tdo: 60, bcid: 2011
- charge of the cluster: 192
- Cluster: 10
 - Channel: 68 (VMM 1.7), chip: 1, pdo: 610, tdo: 75, bcid: 2011
 - Channel: 69 (VMM 1.9), chip: 1, pdo: 147, tdo: 72, bcid: 2011
- charge of the cluster: 757
- Cluster: 11
 - Channel: 124 (VMM 1.8), chip: 1, pdo: 147, tdo: 72, bcid: 2011
 - Channel: 124 (VMM 1.8), chip: 1, pdo: 147, tdo: 72, bcid: 2011
 - Channel: 124 (VMM 1.8), chip: 1, pdo: 147, tdo: 72, bcid: 2011
 - Channel: 124 (VMM 1.8), chip: 1, pdo: 147, tdo: 72, bcid: 2011
 - Channel: 124 (VMM 1.8), chip: 1, pdo: 147, tdo: 72, bcid: 2011
- charge of the cluster: 735
- Cluster: 12
 - Channel: 68 (VMM 1.7), chip: 1, pdo: 323, tdo: 75, bcid: 2011
- charge of the cluster: 323
- Cluster: 13
 - Channel: 125 (VMM 1.6), chip: 1, pdo: 323, tdo: 75, bcid: 2011
 - Channel: 125 (VMM 1.6), chip: 1, pdo: 323, tdo: 75, bcid: 2011
 - Channel: 125 (VMM 1.6), chip: 1, pdo: 323, tdo: 75, bcid: 2011
 - Channel: 125 (VMM 1.6), chip: 1, pdo: 323, tdo: 75, bcid: 2011
 - Channel: 125 (VMM 1.6), chip: 1, pdo: 323, tdo: 75, bcid: 2011

- Cluster: 0 (neighbouring channels in VMM give same results and one stuck with PDO=xxxxx0000)
 - Channel: 67, chip: 1, pdo: 1025, tdo: 78, bcid: 1488
 - Channel: 68 (VMM 1.7), chip: 1, pdo: 619, tdo: 64, bcid: 1488
 - Channel: 125, (VMM 1.6) chip: 1, pdo: 619, tdo: 64, bcid: 1488
- Cluster: 0 (same channel fires twice with same numbers)
 - Channel: 117, chip: 1, pdo: 1025, tdo: 67, bcid: 991
 - Channel: 117, chip: 1, pdo: 1025, tdo: 67, bcid: 991
- Event: (PDO & TDO = 0 !)
 - Event: 13986, UDP: 143, chip: 0, channel: 2, pdo: 0, tdo: 0, bcid: 1, gray (decoded): 1
 - Event: 13986, UDP: 144, chip: 0, channel: 2, pdo: 0, tdo: 0, bcid: 1, gray (decoded): 1
 - Event: 13986, UDP: 145, chip: 0, channel: 2, pdo: 0, tdo: 0, bcid: 1, gray (decoded): 1
 - Event: 13986, UDP: 57, chip: 0, channel: 0, pdo: 0, tdo: 40, bcid: 528, gray (decoded): 992
 - Event: 13986, UDP: 58, chip: 0, channel: 0, pdo: 0, tdo: 40, bcid: 528, gray (decoded): 992
 - Event: 13986, UDP: 59, chip: 0, channel: 0, pdo: 0, tdo: 32, bcid: 528, gray (decoded): 992
 - Event: 13986, UDP: 60, chip: 0, channel: 0, pdo: 0, tdo: 32, bcid: 528, gray (decoded): 992

