SRS Activities at IFIN-HH:

VMM2 Hybrid, FECv6 Firmware, High-Density Optical ATCA-SRS Mezzanine

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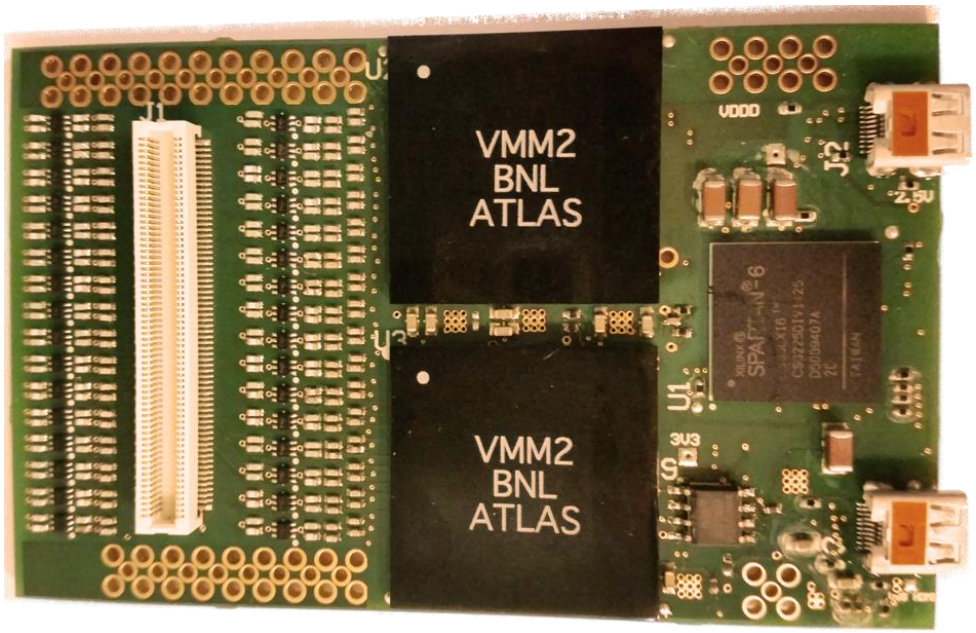
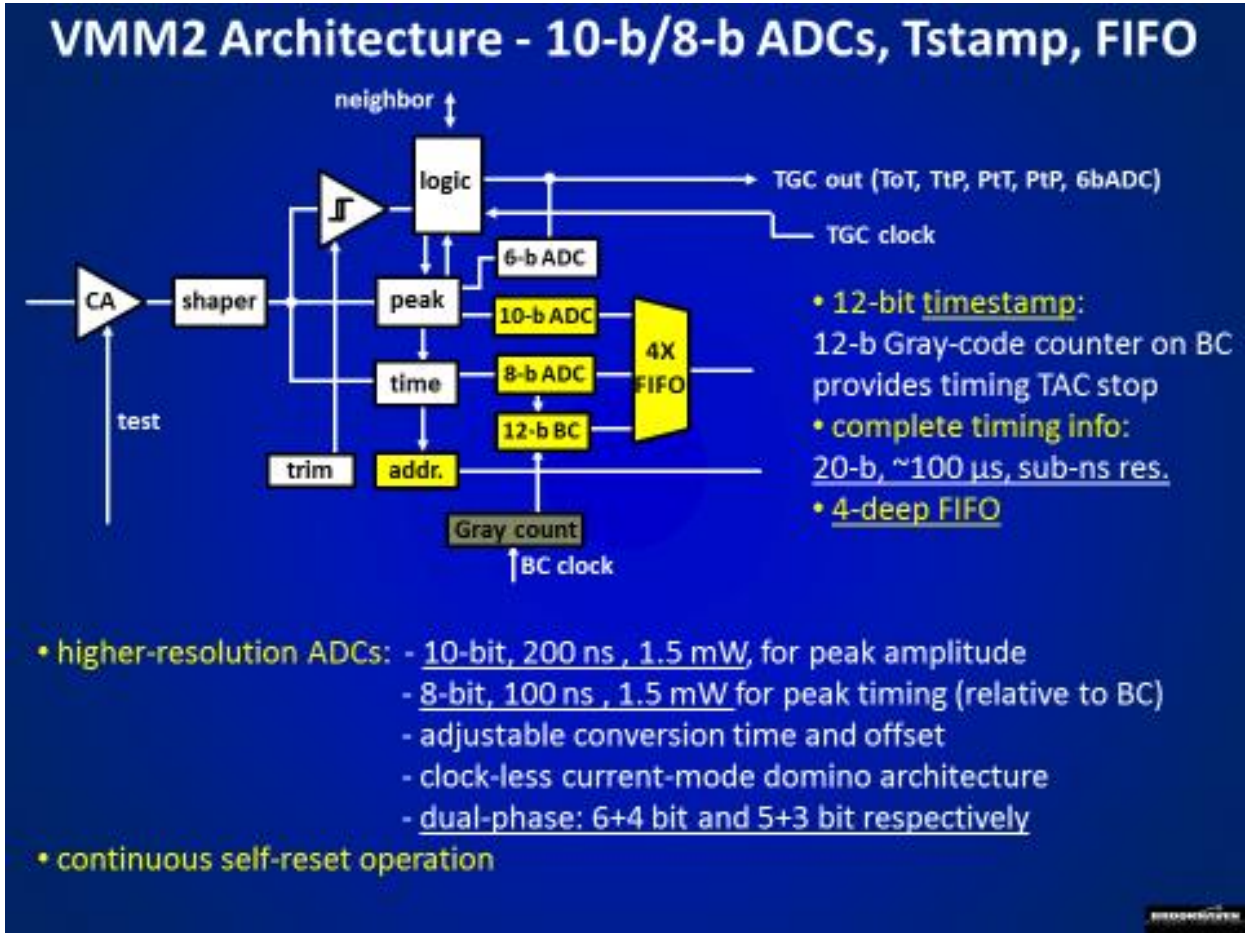
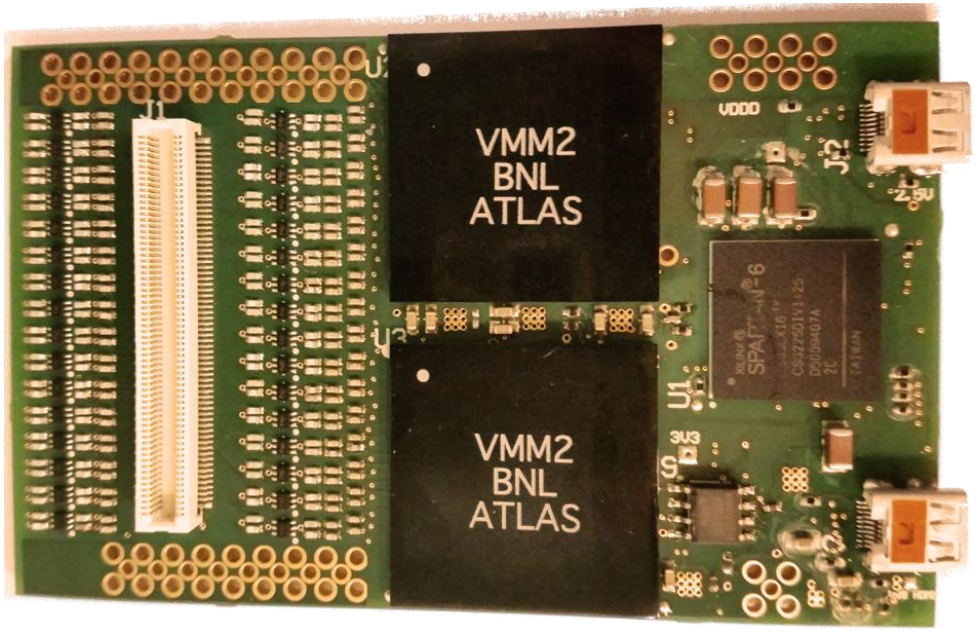
VMM2 SRS Hybrid - Overview



G. De Geronimo, et al., VMM2 - An ASIC for the New Small Wheel, TWEPP 2014

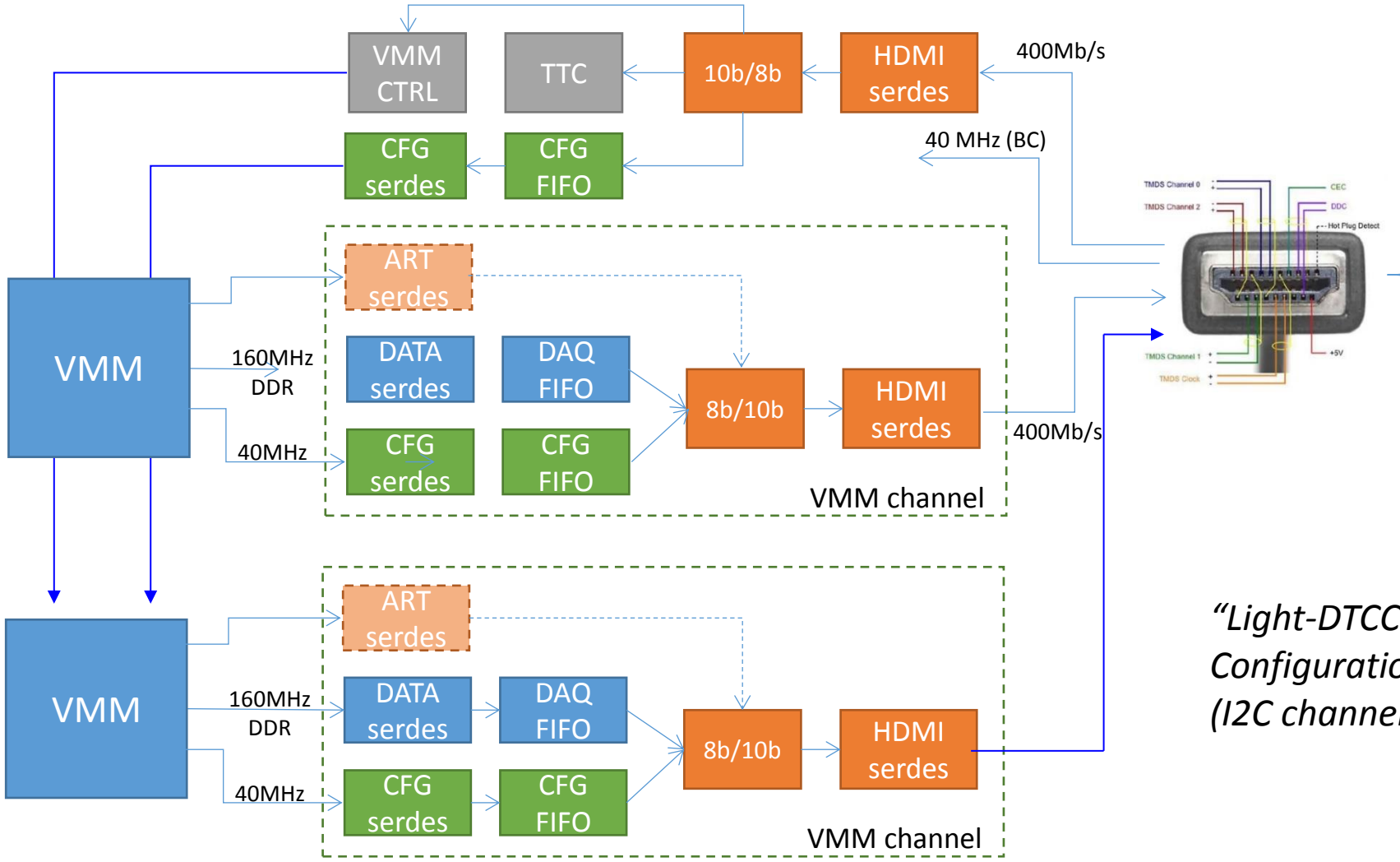


VMM2 SRS Hybrid - Specifications



- Spartan6 LX9/16 FPGA for VMM control/data acquisition
- 1 x Micro HDMI for DAQ
  - Clk (40MHz)
  - TTC and configuration (400Mbps – 10b8b)
  - 2x data lines (400Mbps – 10b8b)
  - (opt.) ART info over data lines
- 1 x Micro HDMI for ART
  - Buffered ART signals (trigger signals)
  - (opt.) clk, ttc
- Power in via HDMI (> 2.7 V)
- On-board LDOs
  - 4 x 1.2V (analog, a/d, digital, fpga)
  - 1x 2.5V (fpga)

VMM2 SRS Hybrid - Firmware



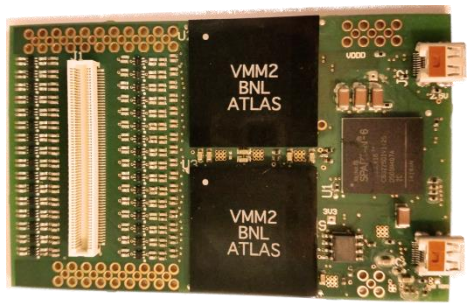
→ DAQ Data (Uplink)
→ ART Data (Uplink)
- "Fast-Or" with address

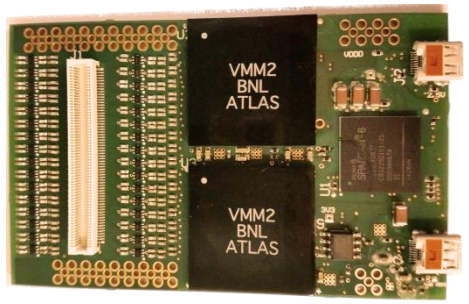
↔Configuration (Up/Downlink)
← TTC (Downlink)

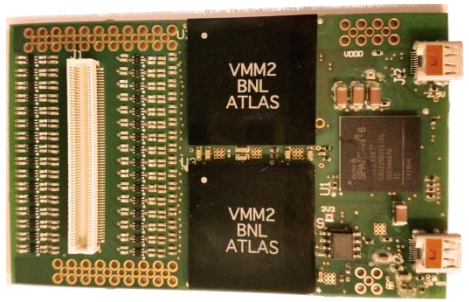
← Power

"Light-DTCC" protocol with one particularity: Configuration and DAQ are mutually exclusive. (I2C channel is not used)

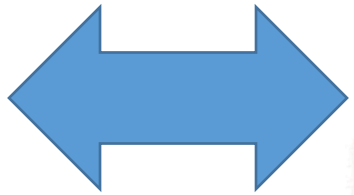
VMM2 SRS Hybrid – Connectivity with SRS

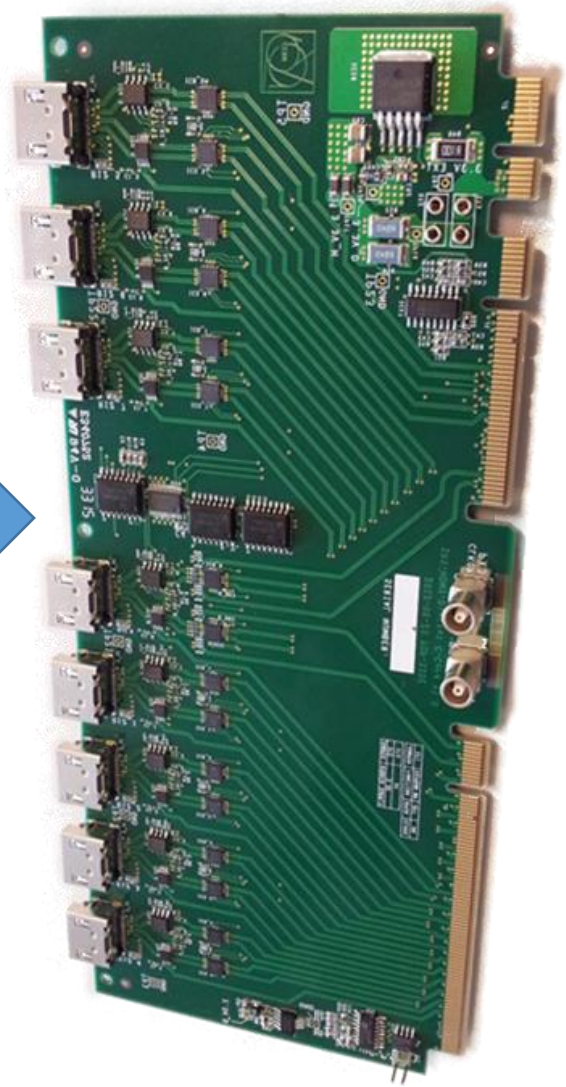






8 Hybrids
16 VMM2 Chips

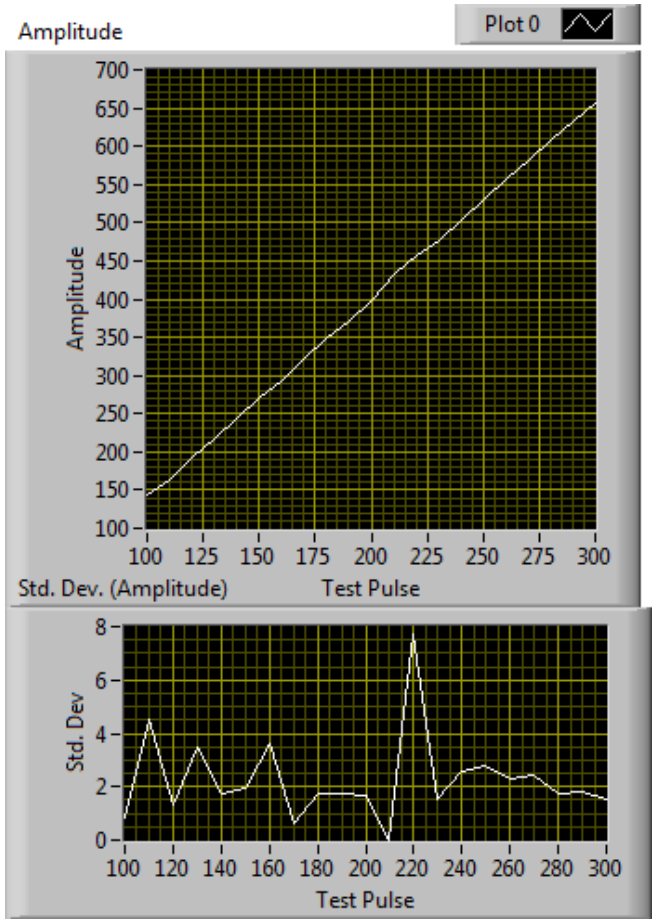




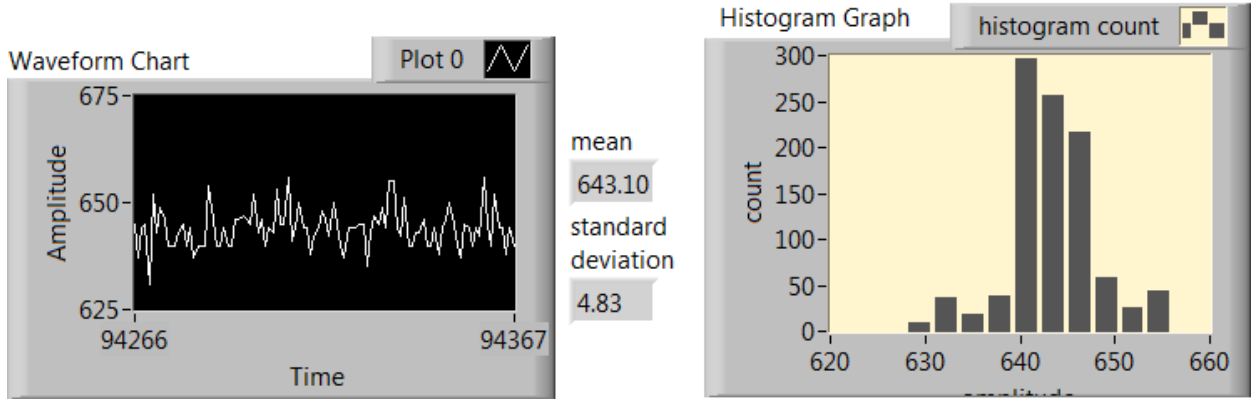
Digital adapter
(16 digital channels)
for digital ASICs
like VMM

VMM2 SRS Hybrid - Testing

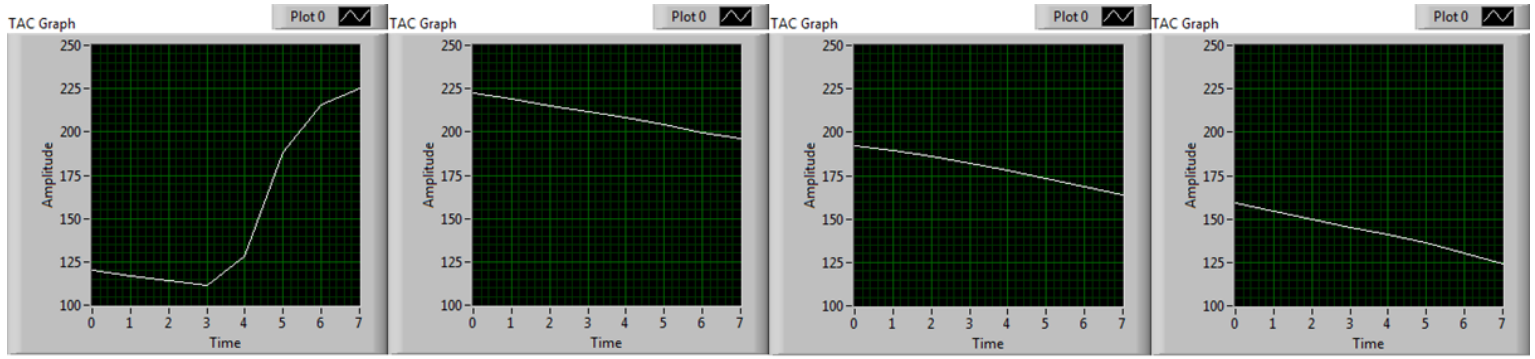
Amplitude (TestPulse) Scan



Pulse Amplitude Histogram



Timing Scan



100 ns

VMM2 SRS Hybrid – Status

A few modifications under way:

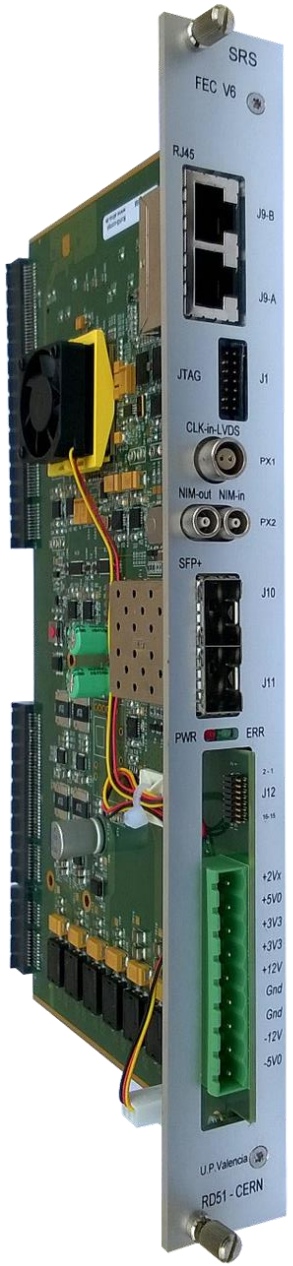
- Access to analog monitor outputs for calibration and debug
- Layout changes to improve power distribution and decoupling
- Separate power option

- Also, digital DCARD is being modified to provide the needed power to the VMM Hybrid (1.5A/hybrid)

FECv6

- Upgrade of the FEC board with Virtex-6 FPGA

- Production batch ordered by CERN Store at Samway Electronics, Bucharest
- First samples arrived at IFIN-HH for initial testing
- So far no problems detected
- Full verification procedure is now being defined

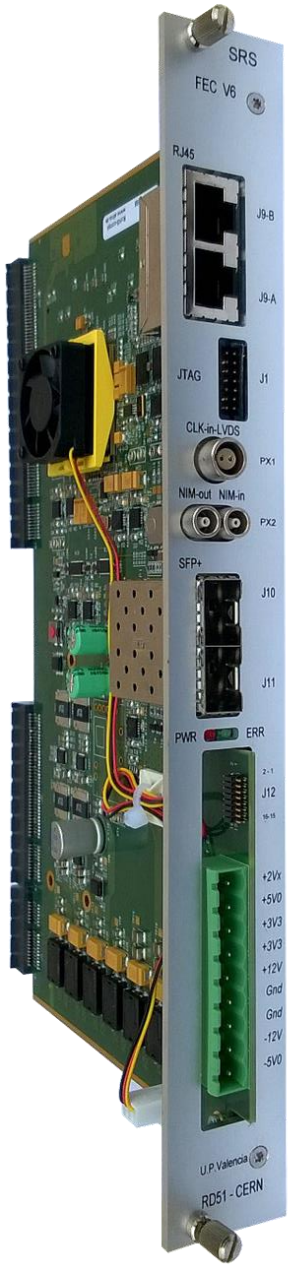


FECv6 - Firmware

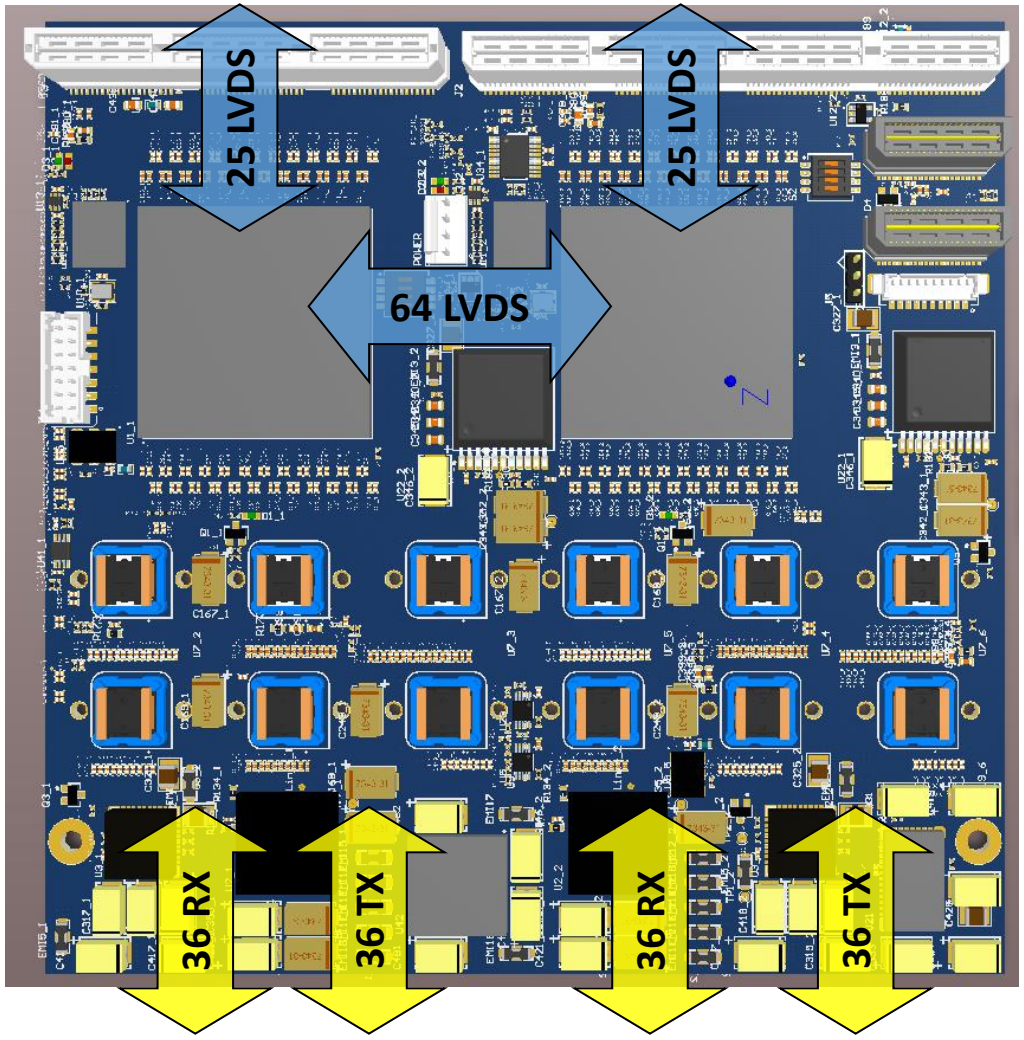
- Beta firmware port (raw APV data over Ethernet) tested successfully by Eraldo with APV

Feature integration pending:

- DTCC link to SRU
  - A lot of input from Andre (Munich) and Raul (Valencia)
  - Ethernet and DTTC versions may be merged into a single FW variant
- APV Zero suppression
- VMM2 logic



High Density Optical Mezzanine for ATCA-SRS

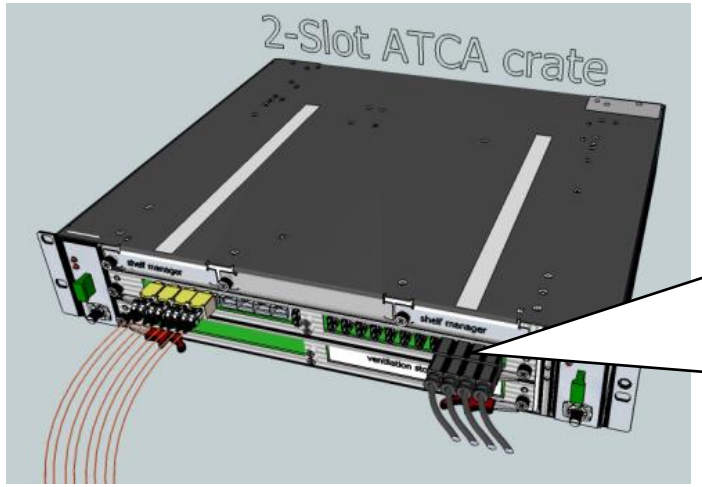


- Build under specification for ATLAS NSW Trigger Processor
- 2 x Virtex-7 FPGA (356K – 477K logic cells)
- 72 RX + 72 RX Optical (36/36 each FPGA)
  - Avago Micropods
- > 900 Gbps integrated front-end bandwidth

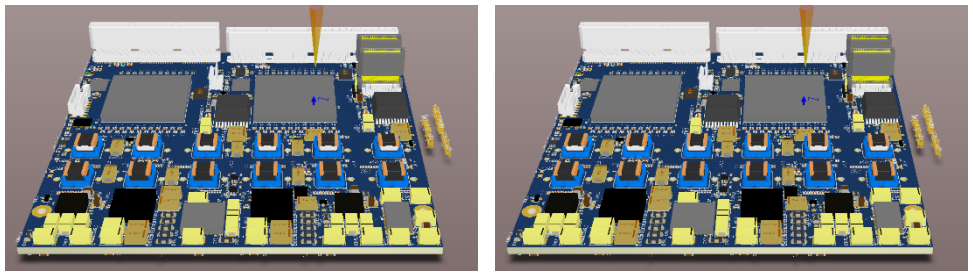
- Possibility to have light/low-cost version
  (1 x FPGA / 36 optical connections)

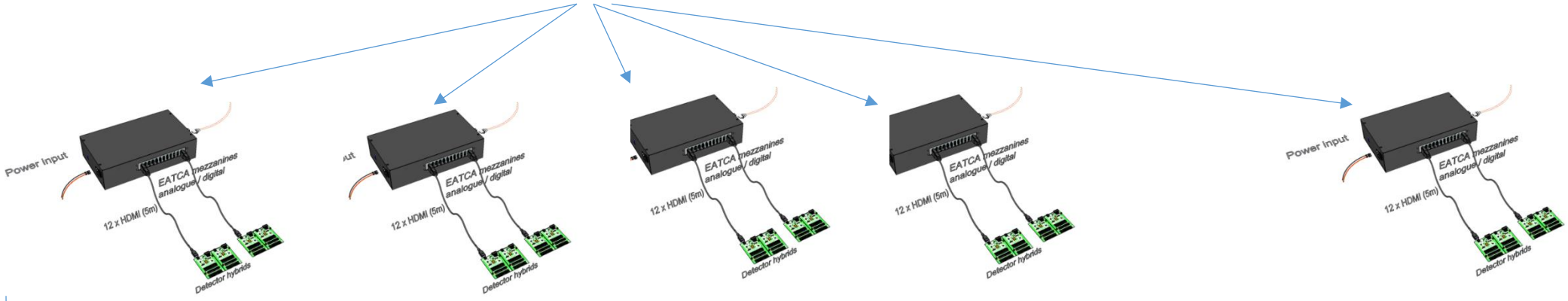
- Prototype board is in our hands
- First tests pending

HD-ORX Integration into ATCA-SRS



2 x HD-ORX / ATCA-SRS





144OCX boxes / 1.7K VMM Hybrids / 220K channels
144OCX boxes / 3.4K APV Hybrids / 440K channels

Thank You