Floating multi-channel picoAmmeter

University of Zagreb

A. Utrobičić

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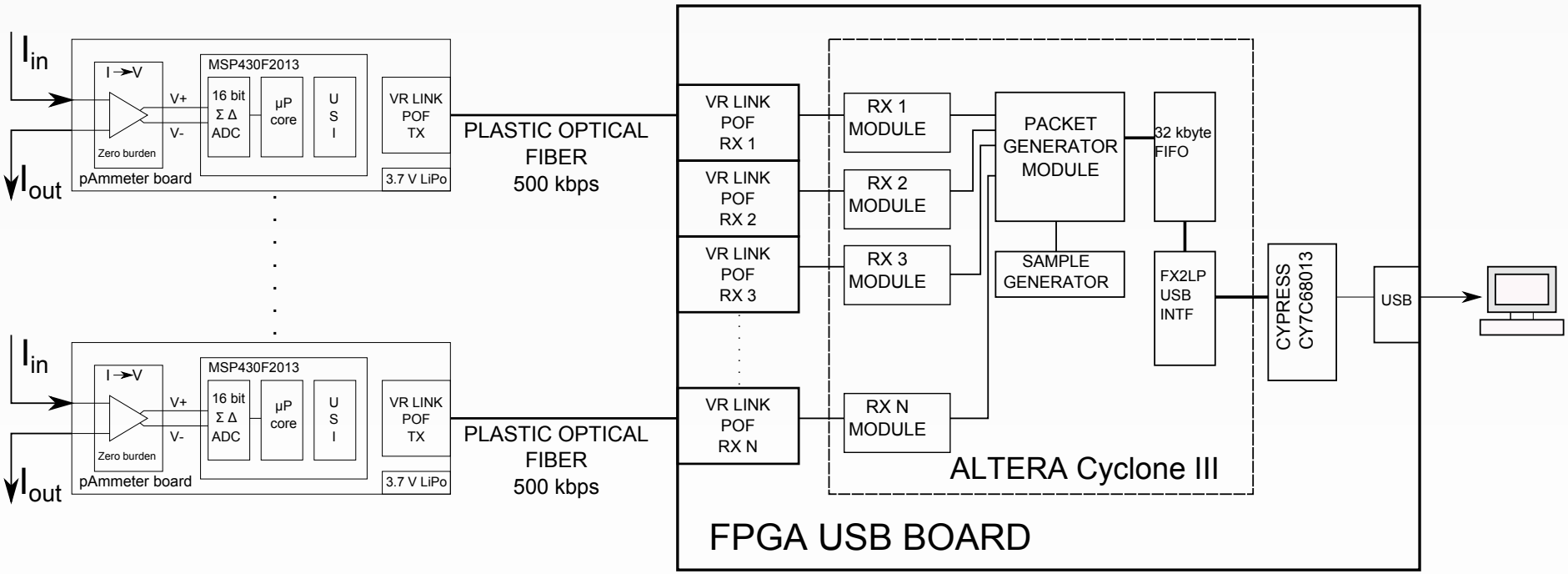
Current measurements requirements

- floating current measurement at high potential > 5kV
- current resolution < 100 pA
- small dimensions for easier fitting to chamber
- low leakage current to ground
- ultra low power requirements for longer time measurement, when used on the battery source
- single side supply
- digital readout
- 10 channels (one current measurement for each GEM electrode + drift cathode)
- simultaneous high speed, real time readout for all channels

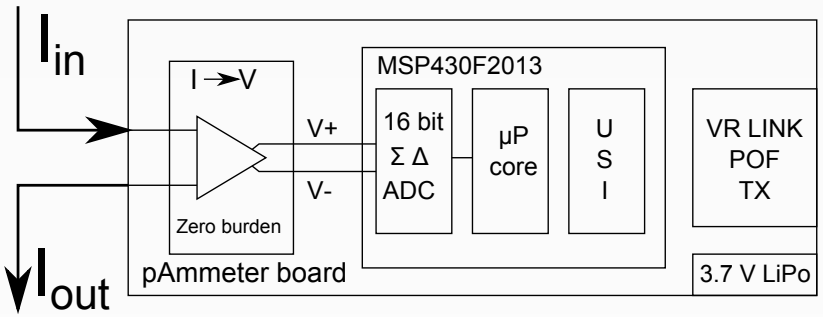
Choice of the concept

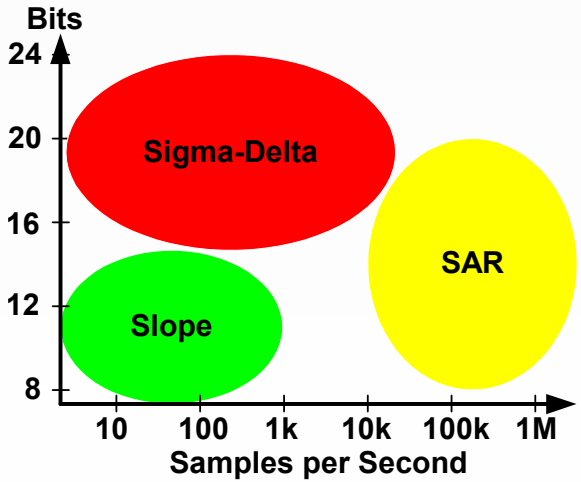
Multiple current measurement nodes send current data to the central FPGA board which is used as a data router to the PC by USB.



Choice of the low power components for the current measurement node

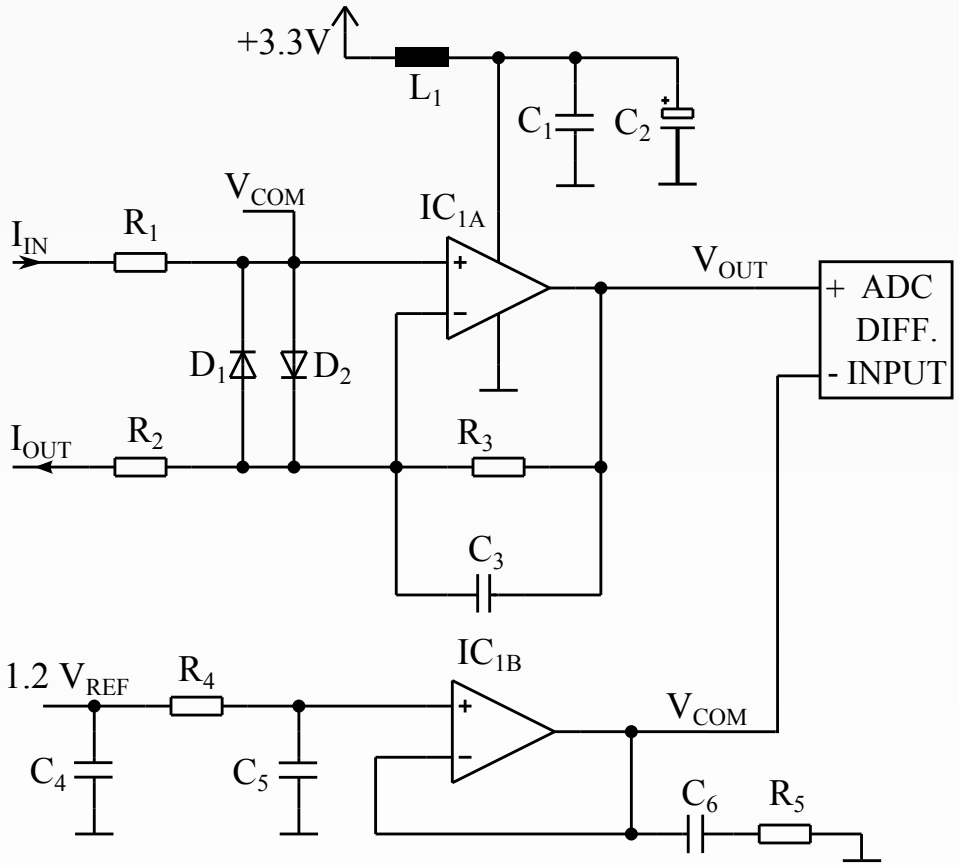
- ΣΔ-ADC was chosen to fulfil resolution requirements.
- LMC6442 (4 μW, I_b=5 fA typ.) was used for current signal conditioning.
- MSP430F2013 with integrated 16-bit ΣΔ-ADC and advanced low-power modes capabilities was used as a heart of the measurement node.
- Avago Versatile-Link 5 Mbps optical fibre transmitter is employed to output digitized data.
- Entire module is supplied from a single 3.7 V battery cell (Li-ion or LiPo).



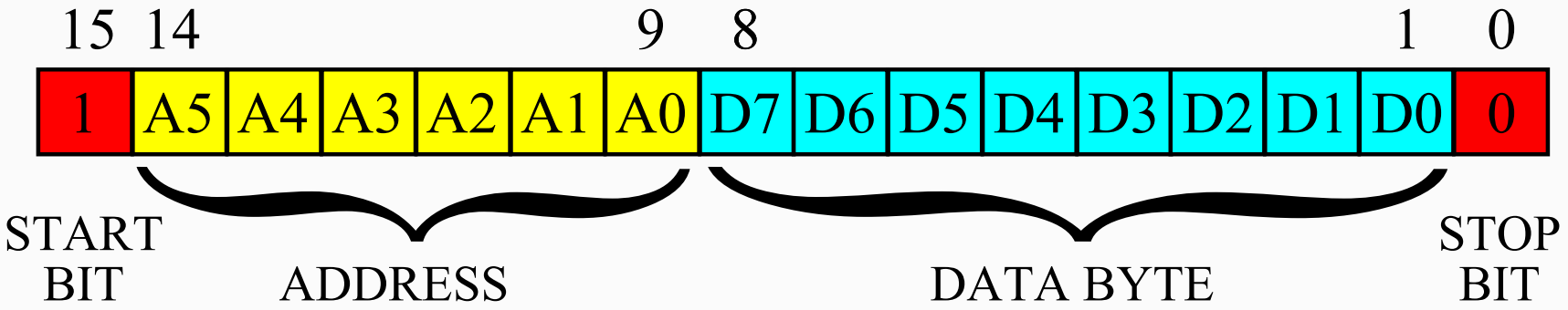


Analog signal conditioning section

- Zero voltage burden OP-amp circuit was chosen to convert current to voltage.
- Due to the zero voltage on the protection devices (D_1 and D_2), excellent linearity can be achieved when compared to the shunt measurement.
- Common mode voltage is set to 1.2 V, which enables bidirectional current measurement using differential ADC input.

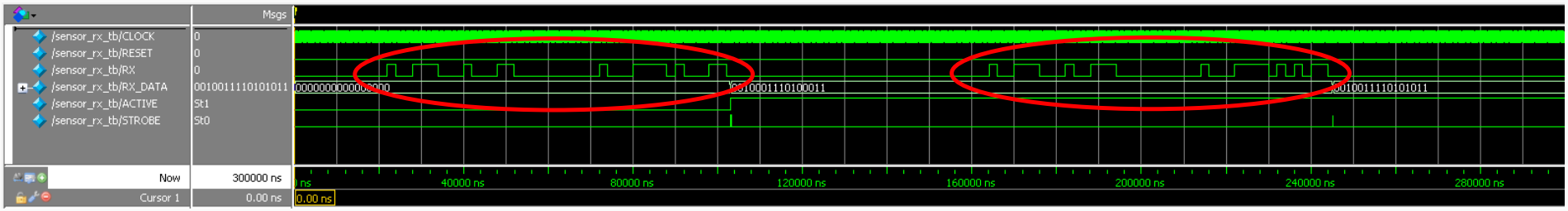


Serial data communication trough optical link



- Data from the nodes is sent trough an optical fibre using USI port which is available on MSP430F2013 μC.
- 14-bit asynchronous serial communication was emulated by a 16-bit serial stream, start and stop bit were added.
- By dividing the 14-bit of useful data to 6-bit address and 8-bit data part it is possible to send multiple data from the node.
- Only the current measurement is implemented for now and it is using 2 addresses.
- Temperature and μC supply voltage can be measured and sent over the optical link if required.

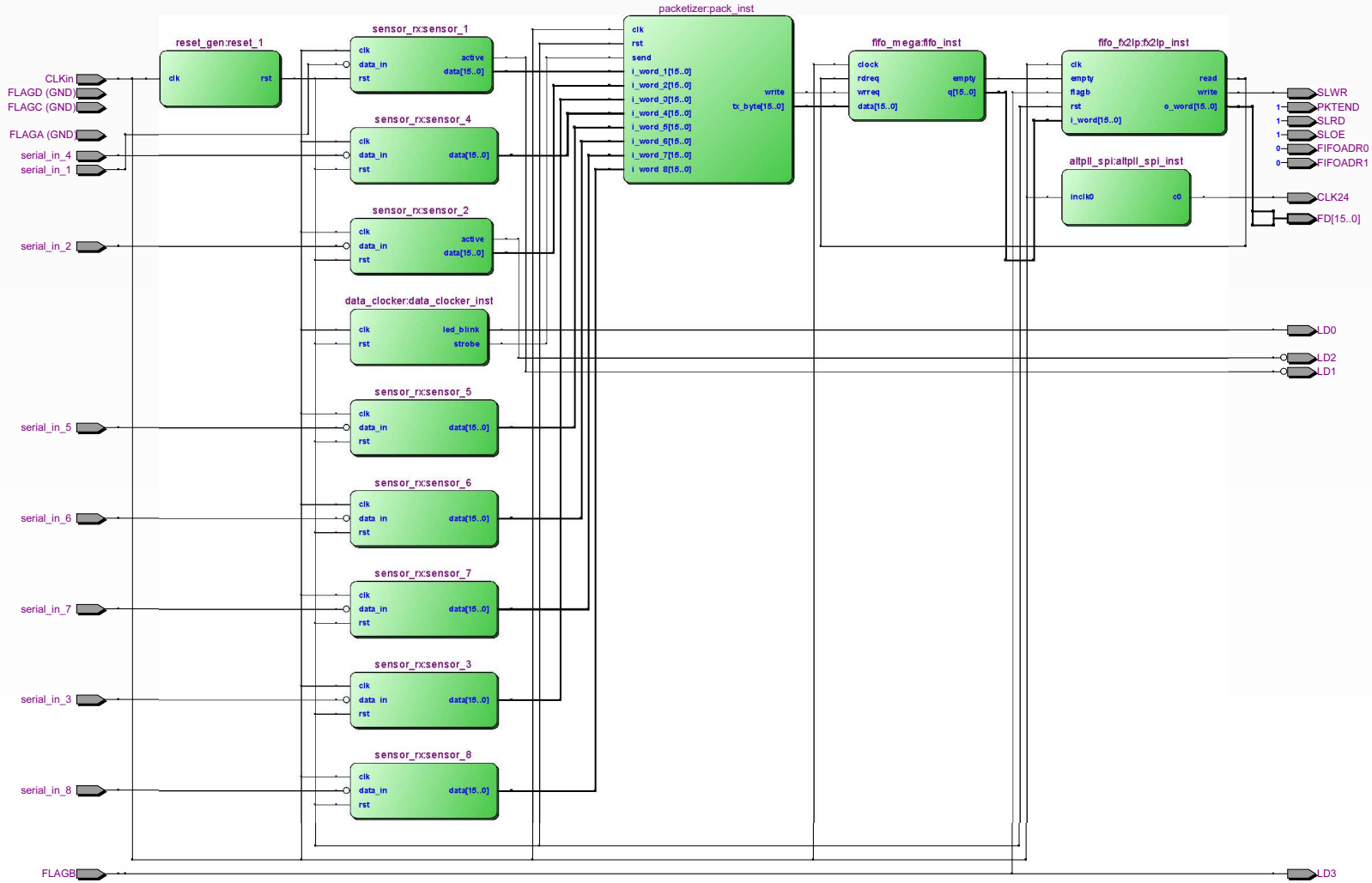
Packet #1 Packet #2



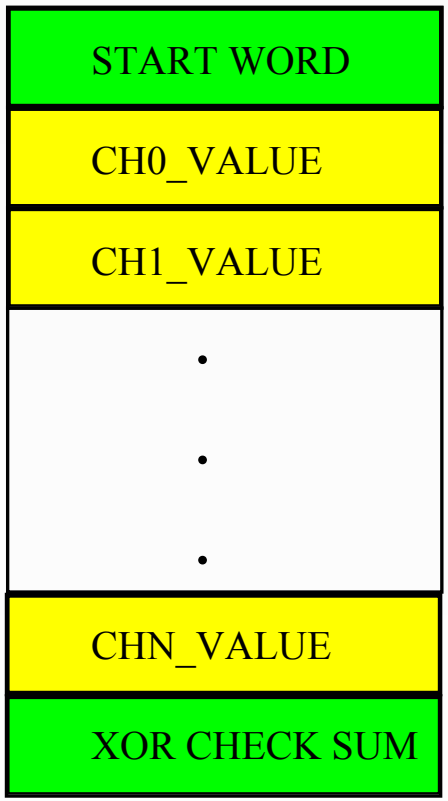
- For the purpose of the current measurement 2 words are sent out from the measurement node to create one 16-bit current value.
- Data rate is set to 500 kbps.
- Sampling frequency is set to approx. 1 kHz.
- The sampling time is crucial for the power consumption as it dictates the TX LED duty-cycle.
- Maximum LED duty cycle for this settings (2-words, 500 kbps and 1 kHz sampling time) is 6.4 %.
- Hardware is capable to work with higher current sampling rate (5 kHz max) if required. However this would imply higher power consumption.

FPGA code block diagram

The entire FPGA code is written in Verilog HDL, schematics shown:



Packetization of data from multiple channels



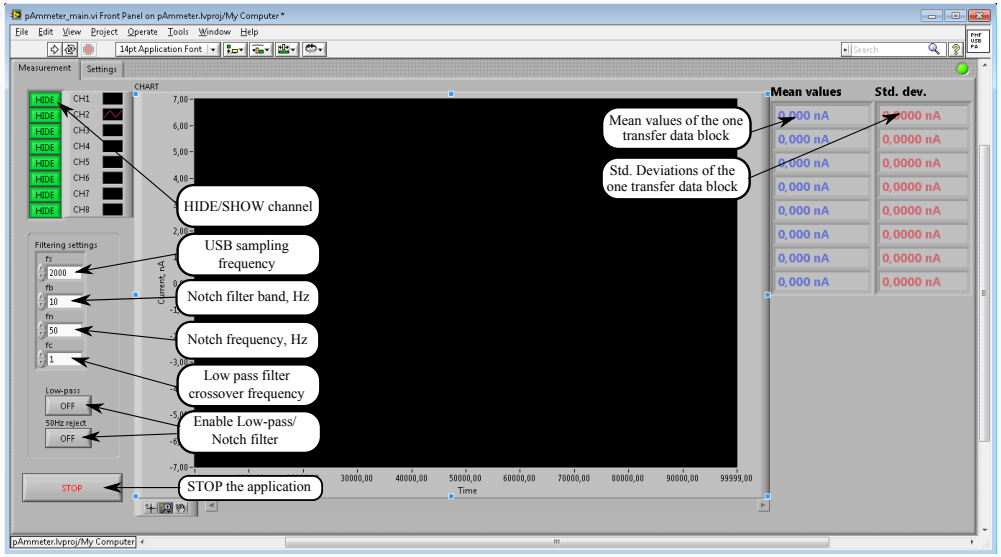
- Data obtained from multiple current sensors is inserted in the packet.
- Packet consists of 16-bit start word, N 16-bit data words and 16 bit XOR checksum.
- 16-bit data words represent current values for each of the current measurement channels.
- As data is received asynchronously at 1 kHz frequency the readout should be at least twice faster.
- Packets with data from all channels are sent to FIFO at 2 kHz frequency.
- To obtain seamless streaming of data to PC over USB, 16 kWord FIFO is implemented in the FPGA.

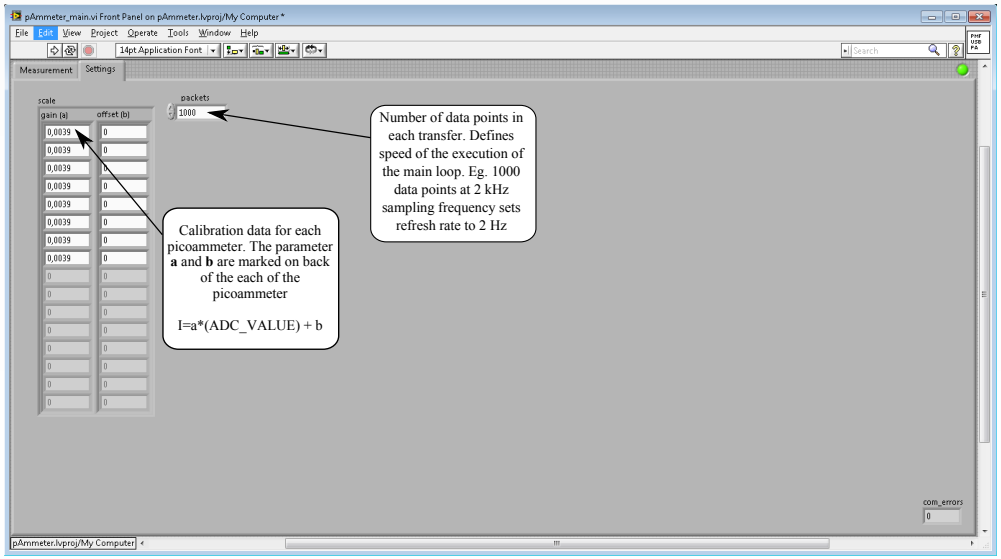
Communication to FPGA trough USB using LabVIEW

- Cypress FX2LP integrated USB phy (CY7C60813) is used for communication to host PC.
- FX2LP is operating in slave FIFO mode with only bulk IN endpoint enabled.
- Additional FPGA FIFO enables proper communication when host CPU is highly loaded.
- Windows driver is based on National Instruments VISA USB RAW bulk transfer, this enables easy integration to the LabVIEW application.
- Transfer speed that can be achieved between FPGA and PC host is circa 20 Mbyte/s on USB2.0 port.

Host application

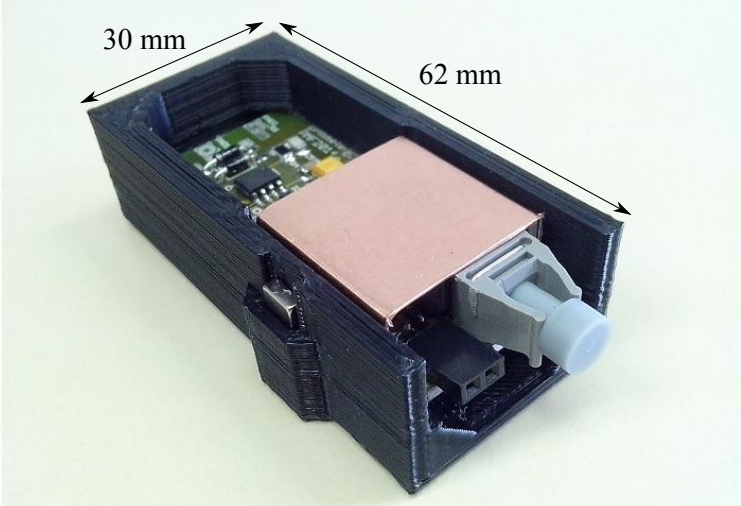
- LabVIEW library for communication to the measurements system was developed.
- Library consists of functions ”FIND, OPEN, READ and CLOSE” and it can be easily integrated in any LabVIEW project.
- It requires NI VISA to be installed.
- Application is organized in two tabs: Measurement and Settings.





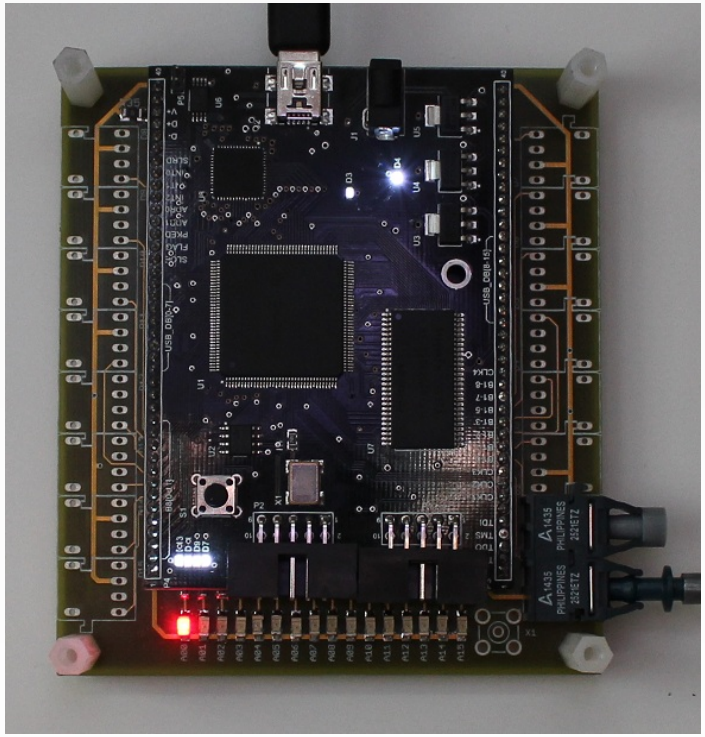
Prototype

- Ten prototypes are currently populated on a 2-layer PCB with dimensions 54×23.5 mm.
- Floating shield tied to the battery negative potential mitigates EMI radiated from the digital circuitry.
- PCB + LiPo (3.7 V, 350 mAh) battery are placed inside plastic housing with dimensions 62×30×19 mm.
- Plastic case has small pocket where NdFeB magnet is located for purpose of turning on/off picoammeter.



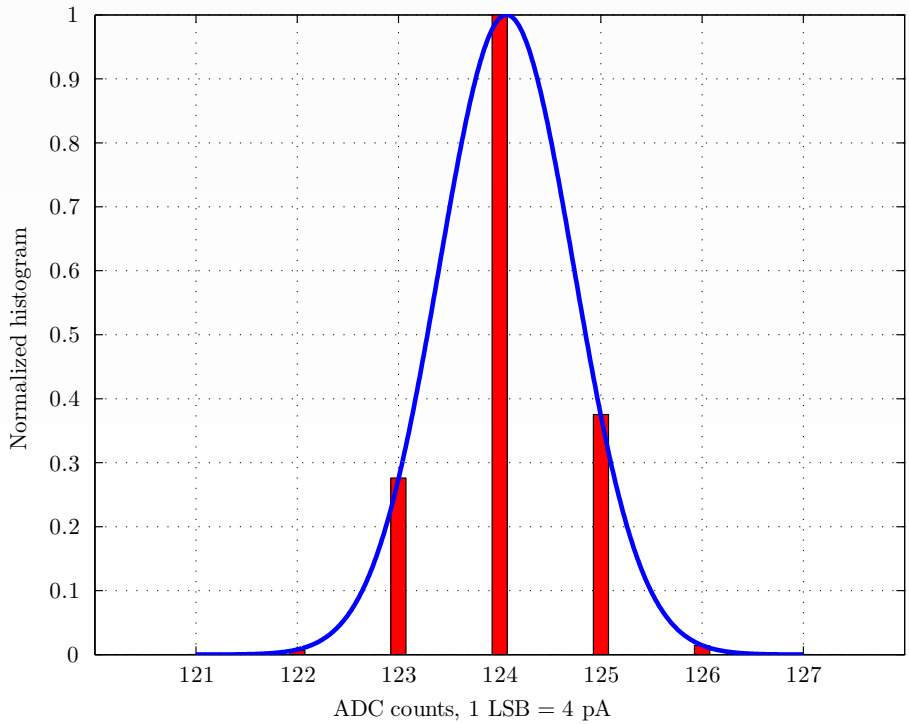
- When battery fully charged it should last approx. 9 days of continuous operation.
- There are two pins left of the optical transmitter for connecting battery charger when battery is depleted.

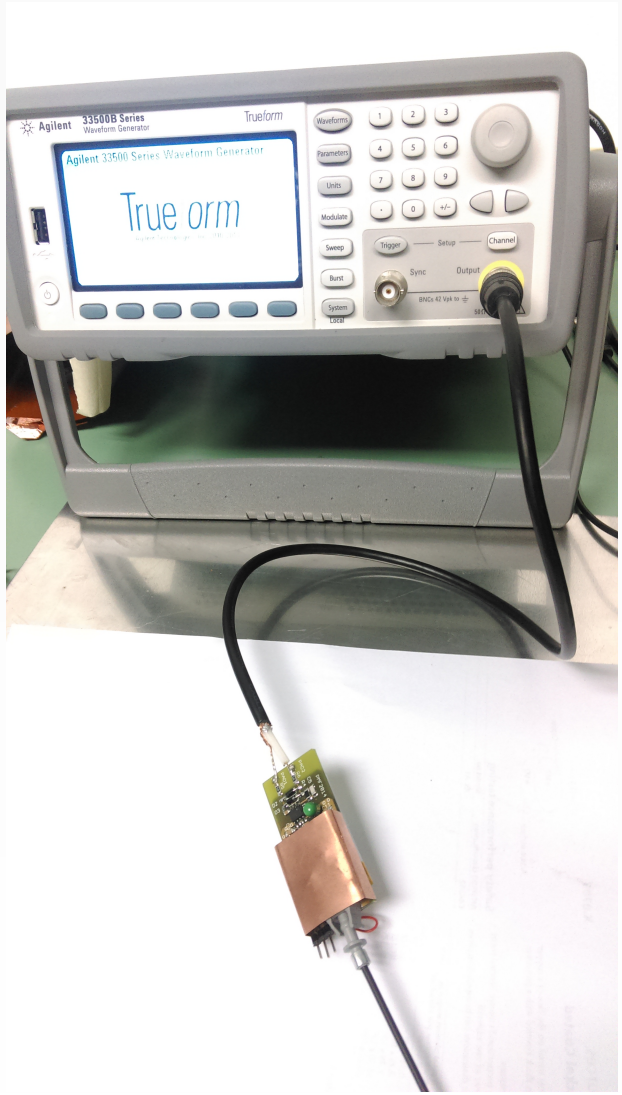
- Low-cost FPGA board with ALTERA Cyclone III, is used to implement multi-channel receiving and buffering.
- Simple optical RX daughter board for the main FPGA-USB board with 16 RX channels has been designed.
- Optical receivers are populated on FPGA daughter board.
- Board has 16 red LED diodes which indicates which channel is active.



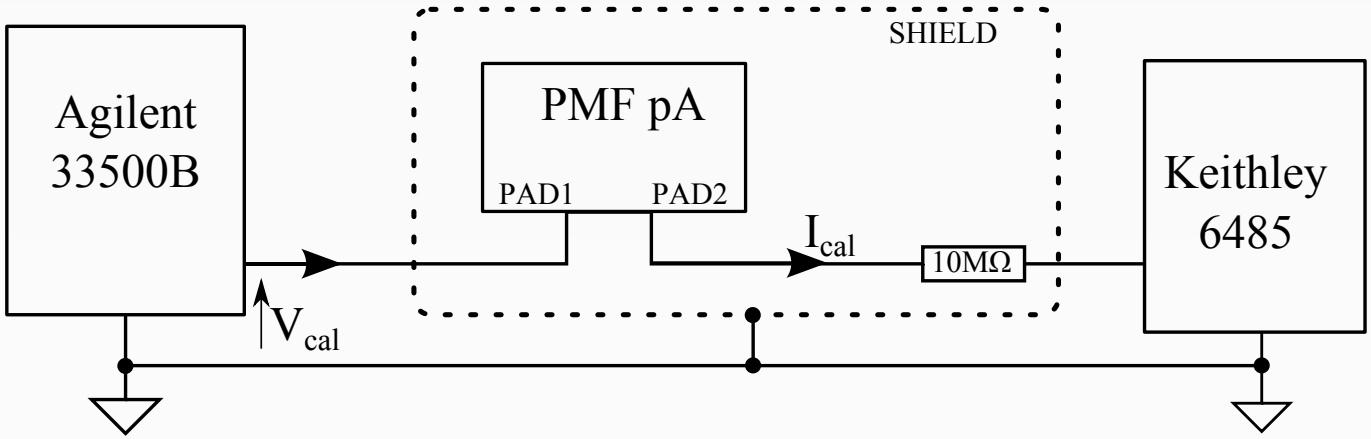
First measurements

- PicoAmmeter was connected to the Agilent 33500B waveform generator.
- Current was set to mean value of 0.5 nA by adjusting the voltage on the protection resistors $R_1 + R_2$ and recorded for 15 min.
- Histogram of the RAW signal from the ADC was fitted to the gaussian.





Calibration procedure



- Keithley 6485 picoammeter was connected in series with our picoammeter and 10 MΩ resistor.
- The resistor is necessary to convert voltage from Agilent 33500B waveform generator to current.
- Special care must be taken when connecting picoammeters in series, high impedance terminals of the picoammeters must be connected to each other.
- Low impedance terminals are connected to ground (Keithley) and calibration voltage (PMF pA).
- ADC data is fitted to the Keithley 6485 measurement using LSQ min. fit.

Specification sheet of the prototype

- **Measuring range:** from -125 nA to 125 nA. It can be changed to lower by setting the internal PGA to other that 1x or by modifying R_3
- **Resolution (LSB):** 4 pA at measuring range above
- **FWHM:** 6 pA, RAW signal, 1 kHz sampling, 15 minutes
- **Sampling frequency:** 1 kHz
- **Current consuption:** 1.5 mA at 1 kHz sampling freq
- **Supply voltage:** 3.3 V-5.5 V - single lithium cell
- **Optical connector**: VR - Versatile Link (Avago)
- **PCB dimensions:** 54x23.5x9 mm
- **Isolation voltage:** N/A, defined by casing and length of fibre
- **Battery:** LiPo 3.7 V, 350 mAh

Future work

- Implement autoranging feature by means of PGA (Programmable Gain Amplifier) that is already inbuilt inside the ADC of the μC.
- We have sent prototypes to other groups for the testing purposes and we are waiting for their feedback so we can improve the device.
- To make noise free DC/DC converter that will replace the battery supply and ensure HV isolation.
- As we are depending on the third party FPGA board, we are considering do design our custom FPGA board with optical receivers and RAM.
- We are considering usage of different interfaces to host PC than USB, ethernet?