



# **NEW PS TDC FOR HEP (AND OTHER APPLICATIONS)**

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**Jorgen Christiansen, Moritz Horstmann,  
Lukas Perktold (Now AMS), Jeffrey Prinzie  
(Leuven)**

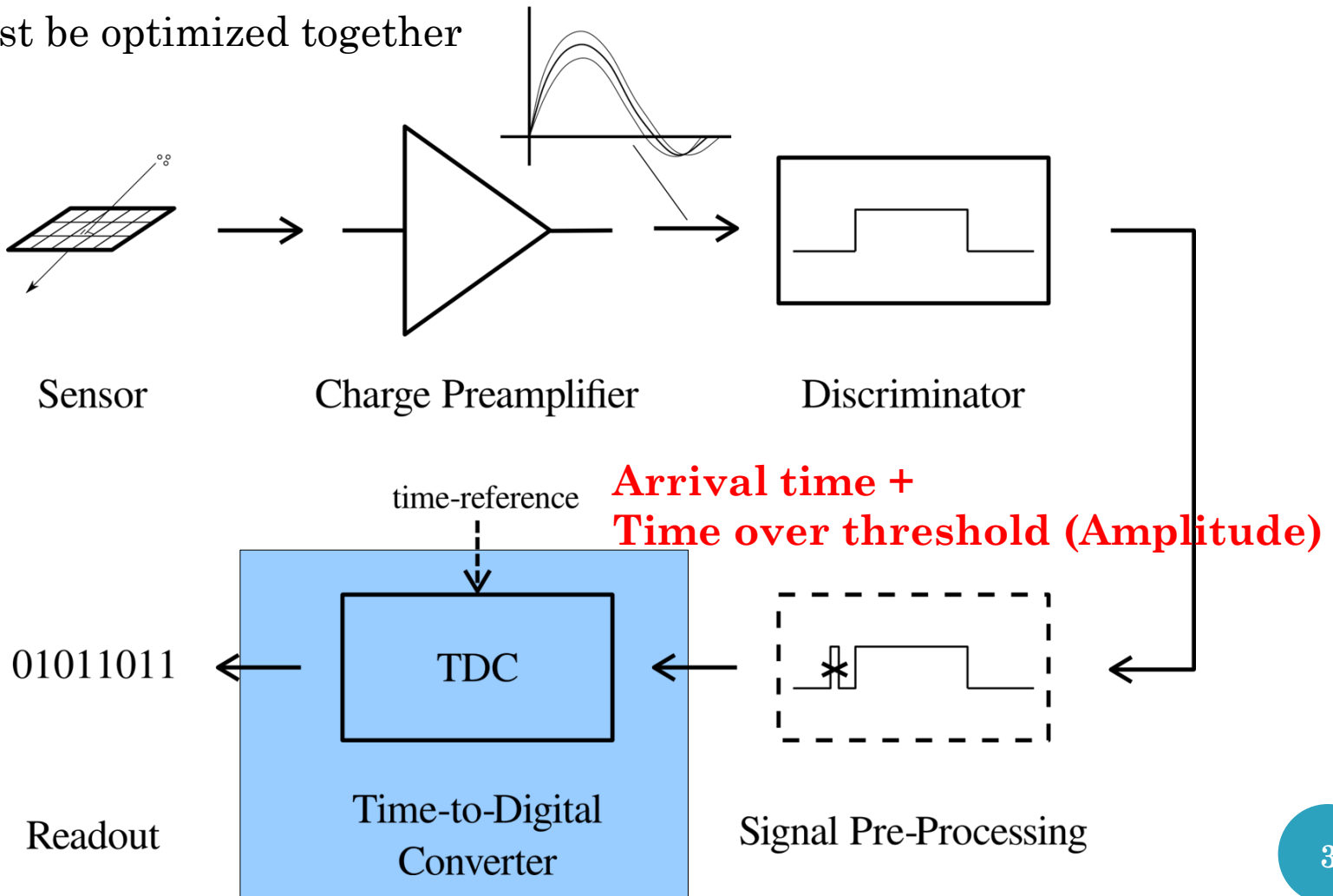
**CERN/PH-ESE**

# TODAYS TDC MEETING 14:00 - ~16:00

- General TDC project overview
- Timing macro in 65nm
- PLL in 65nm
- Short user presentations with specific needs:
  - Time resolution and what measurements (Edges, TOT )
  - Number of channels
  - Hit rates
  - Hit interface: SLVS - LVDS
  - Time reference: 40MHz (other required ?)
  - Trigger functions:
    - Triggered, non triggered, trigger latency, trigger window, overlapping triggers, etc.
  - Readout interface: Formatting, Signal interface, Data rate, ,
  - Power supply: 1.2v only ?.
  - Control/monitoring interface
  - Radiation tolerance
  - How many chips when ?
  - Etc.

# TIME MEASUREMENT CHAIN

Detector and discriminator critical and must be optimized together



# TDC APPLICATIONS IN HEP

Large systems with many channels: 10k-100k

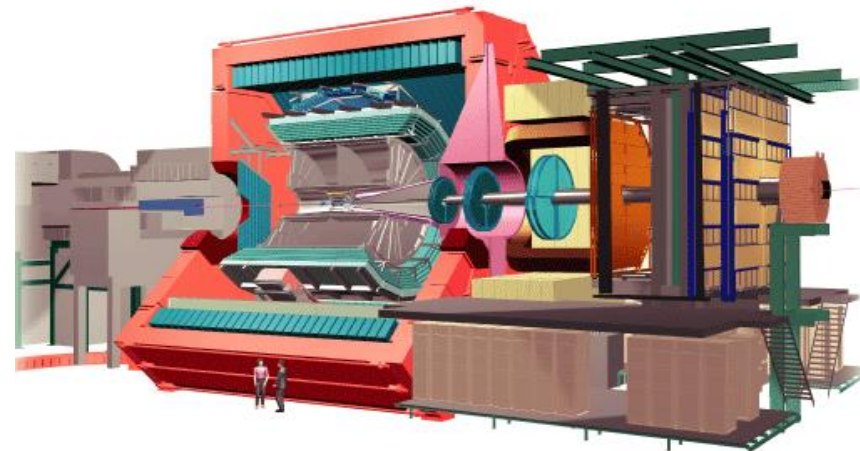
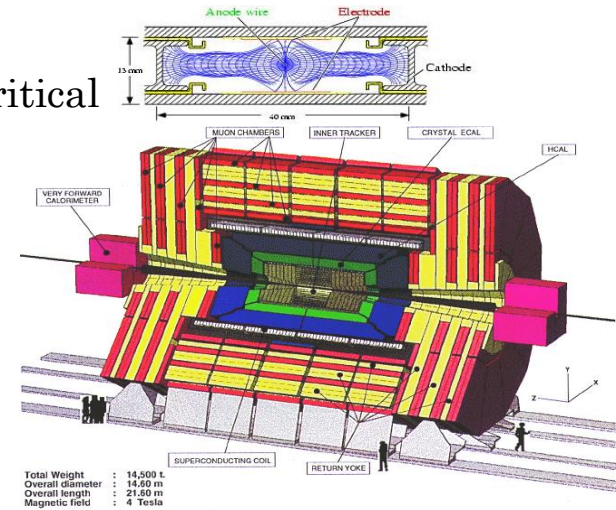
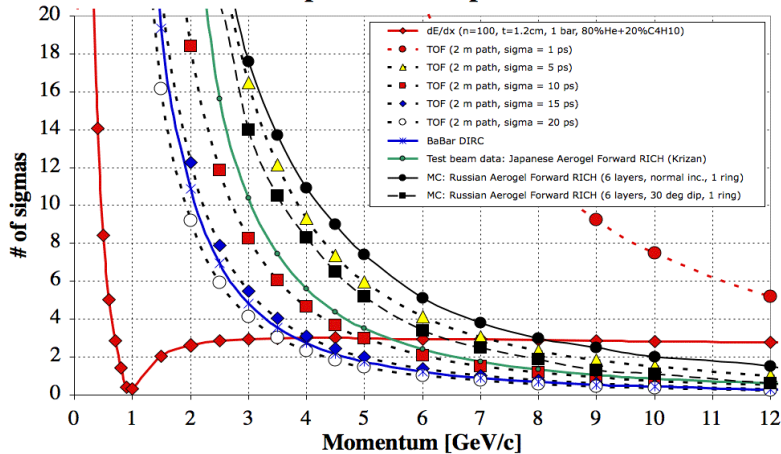
Single shot time resolution/stability across large system critical

- Drift time in gas based tracking detectors
  - **Low resolution: ~1ns**
  - Examples: CMS, ATLAS, LHCb, , , drift tubes
- TOF, RICH
  - **High resolution: 1 – 100ps**
  - Example: ALICE TOF
- Background reduction: **1 – 10ps**
- Vertex identification from timing: **1 - 10ps**
- Signal amplitude and time walk compensation:  
Time Over Threshold (TOT)
  - Or Constant Fraction Discriminator (CDF) in analog FE
- Triggered or non triggered

**New TDC with programmable resolution: 3ps, 12ps, (400ps ?)**

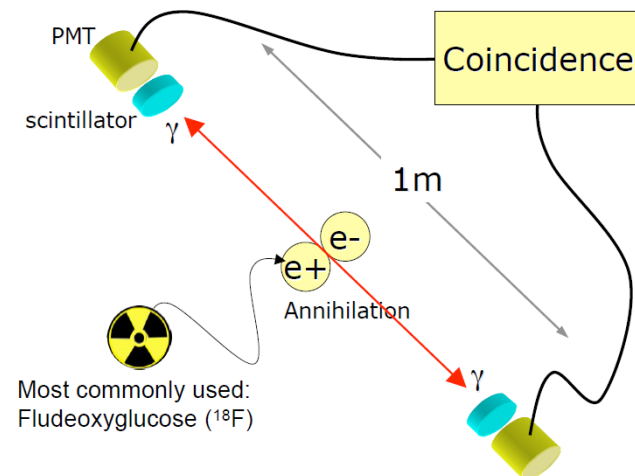
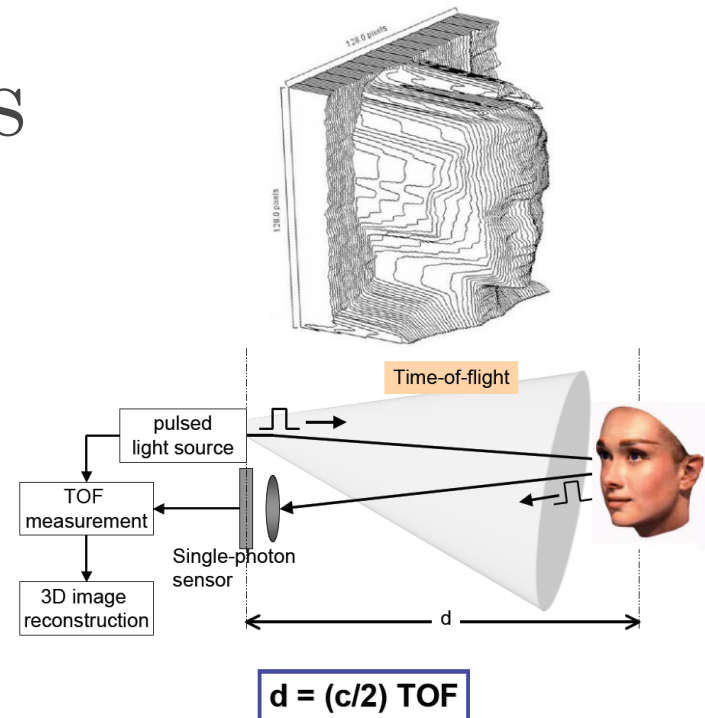
- Power consumption highly resolution dependent

Expected  $\pi/K$  separation



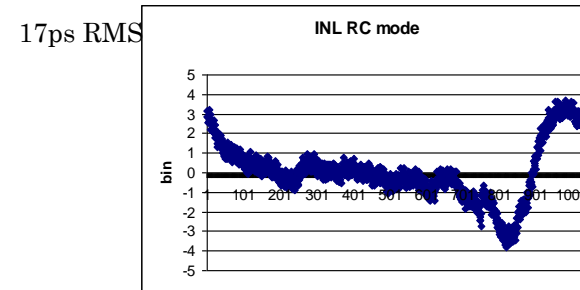
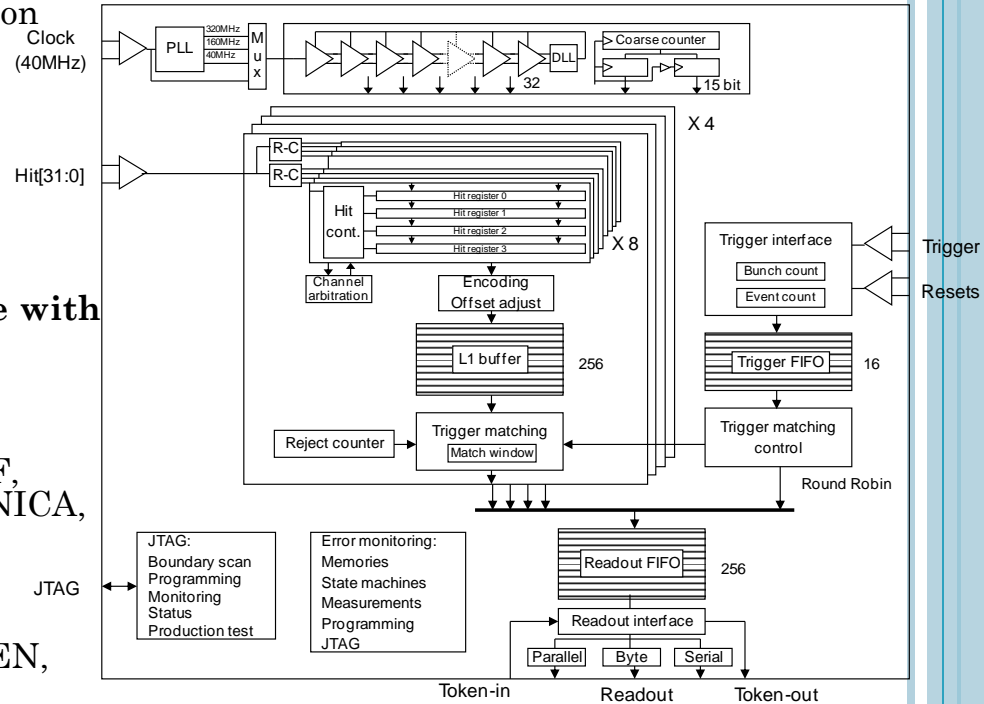
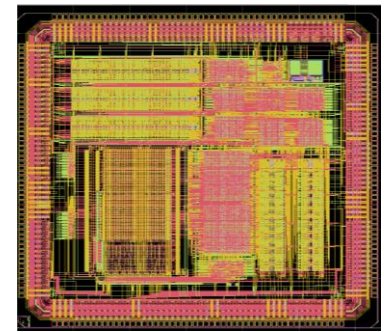
# OTHER TDC APPLICATIONS

- Laser ranging
- 3D imaging
- Medical imaging: TOF PET
  - Improve signal/noise, lower radiation
- Fluorescence lifetime imaging
- General instrumentation.
- Differences to HEP systems
  - Small systems - Few channels
    - Time resolution/stability between few channels on same chip
  - Averaging can in many cases be used to get improved time resolution

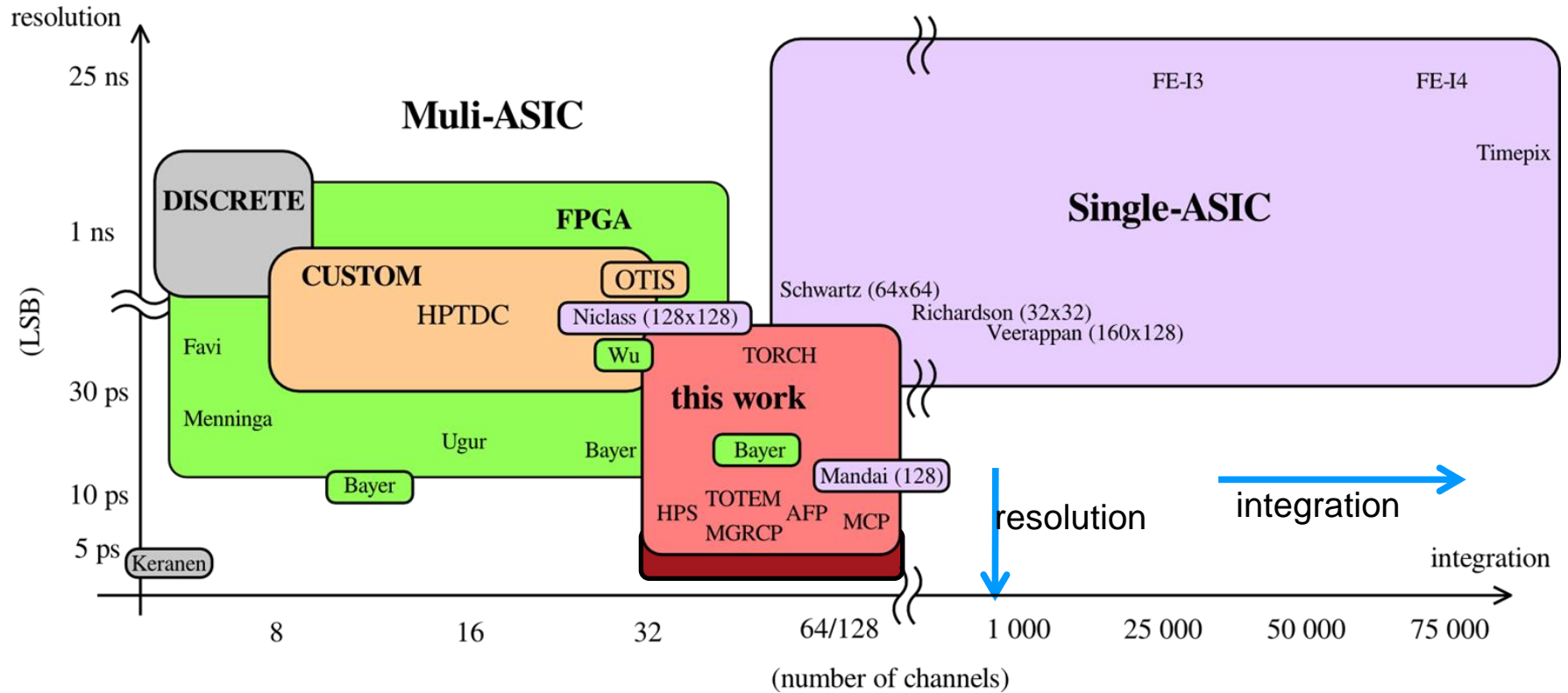


# HPTDC

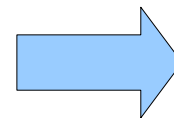
- History
  - Architecture initially developed at CERN for ATLAS MDT (design transferred to KEK)
  - CMS Muon and ALICE TOF needed similar TDC with additional features / increased resolution
- Features
  - 32 channels(100ps binning), 8 channels (25ps binning)
  - 40MHz time reference (LHC clock)
  - Leading, trailing edge and TOT
  - Triggered or non triggered
  - Highly flexible data driven architecture with extensive data buffering and different readout interfaces**
- Used in large number of applications:
  - More than 20 HEP applications: ALICE TOF, CMS muon, STAR, BES, KABES, HADES, NICA, NA62, AMS, Belle, BES, , ,
    - We still supply chips from current stock.
  - Other research domains: Medical imaging,
  - Commercial modules from 3 companies: CAEN, Cronologic, Bluesky
  - ~50k chips produced
- 250nm technology (~10 years ago for LHC)
  - Development: ~5 man-years + 500kCHF.
  - Can not be produced any more
- [http://tdc.web.cern.ch/TDC/hptdc/docs/hptdc\\_manual\\_ver2.2.pdf](http://tdc.web.cern.ch/TDC/hptdc/docs/hptdc_manual_ver2.2.pdf)



# TDC TRENDS



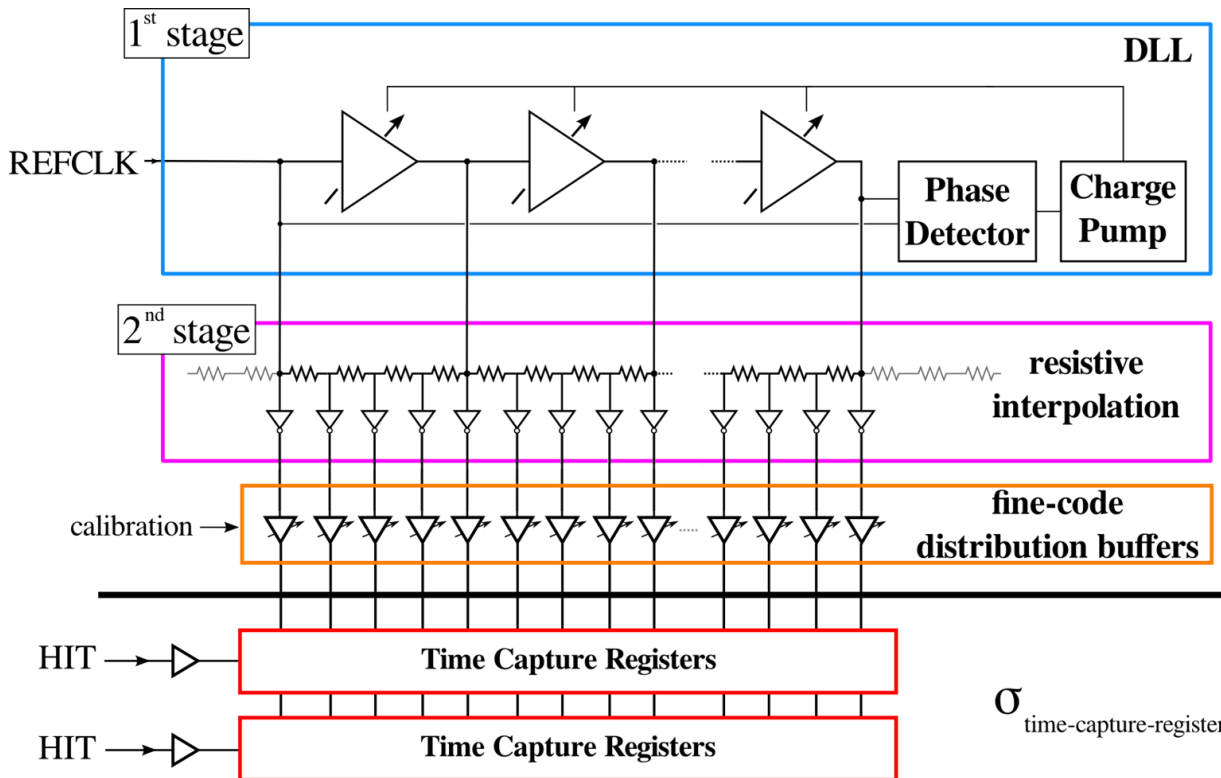
New detectors and sensors require new TDC



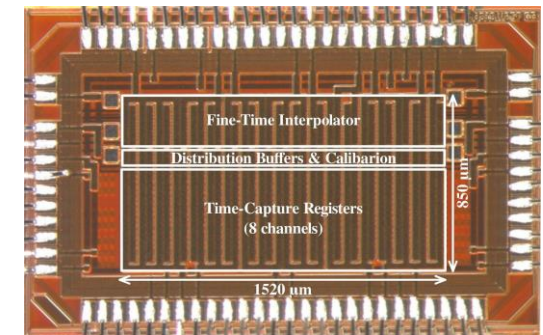
- 3ps binning (1-2ps RMS)
- High integration
- Flexible



# TDC ARCHITECTURE PROTOTYPED IN 130NM



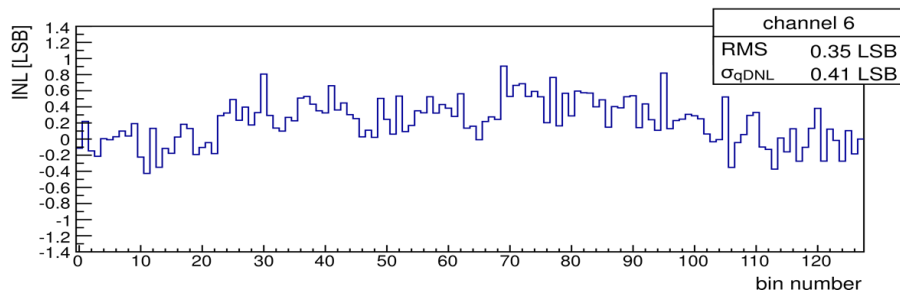
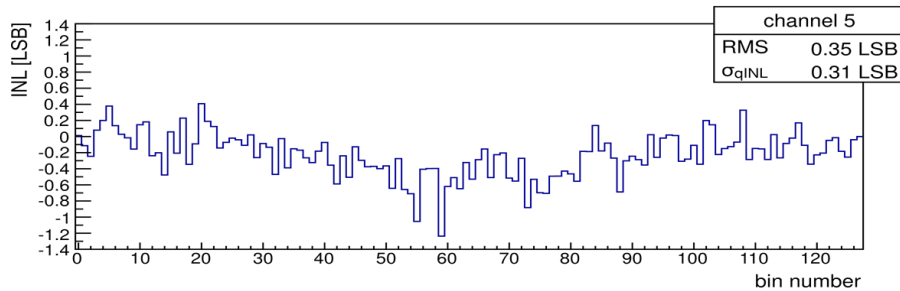
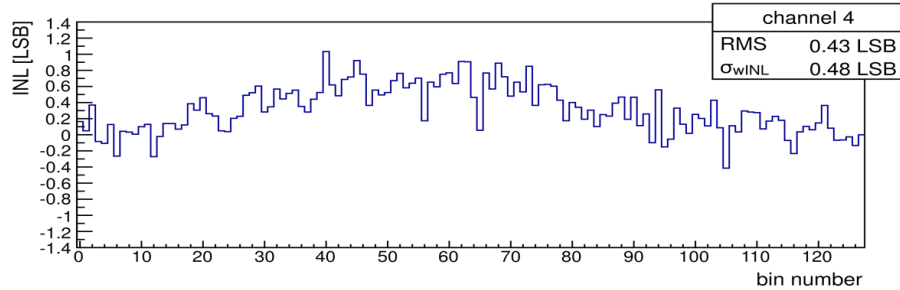
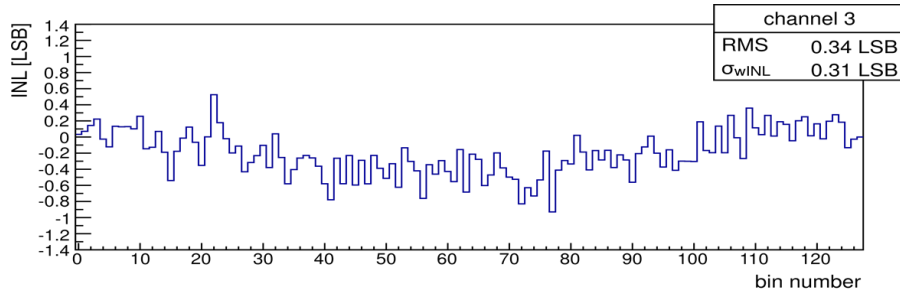
Counter



- External time reference (clock).
- 3 stage time measurement:
  - Counter: 800ps, Delay locked loop: 25ps, Resistive interpolation: 6.25ps (65nm: 400ps, 12ps, 3ps)
- Self calibrating using Delay Locked Loop (DLL)
- Can be scaled to the number of channels required.
- Prototyped in 130nm CMOS and extensively characterized by Lukas Perktold.
- Measured time resolution: 2.5ps RMS



# Measured performance



**INL =  $\pm 1.3$  LSB**

**RMS =  $< 0.43$  LSB (2.2 ps)**

**Expected RMS resolution from circuit simulations:  
including quantization noise, INL & DNL**

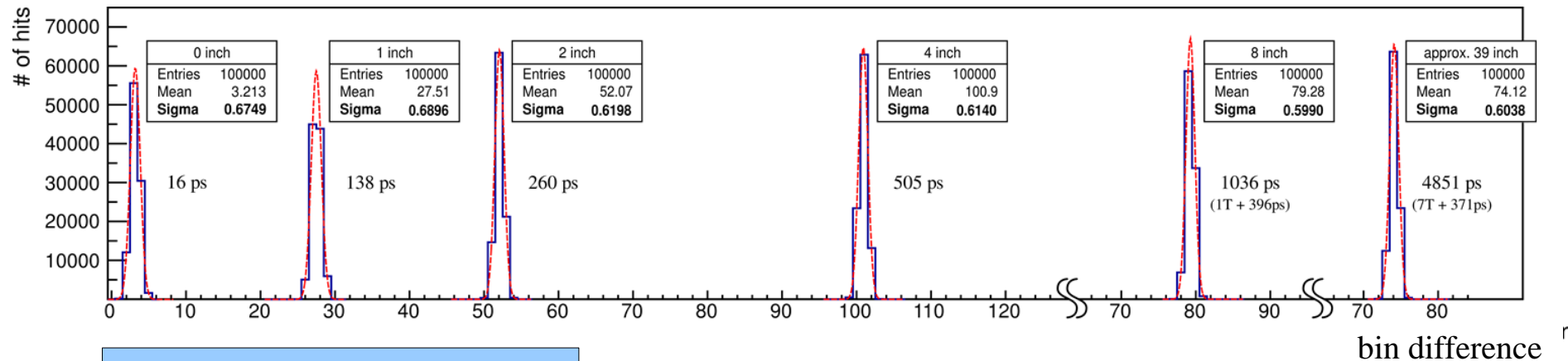
**$2.3$  ps-RMS  $< \sigma_{qDNL/wINL} < 2.9$  ps-RMS**

INL can be corrected for in software

DNL, Noise and jitter can not be corrected  
(single shot measurements)

# Single Shot Precision

- Three measurement series using cable delays
  - Both hits arrive within one reference clock cycle
  - Second hit arrives one clock cycle later
  - Second hit arrives multiple clock cycles later (~5ns)



$$\sigma_{\text{TDC}} < 2.44 \text{ ps-RMS}$$

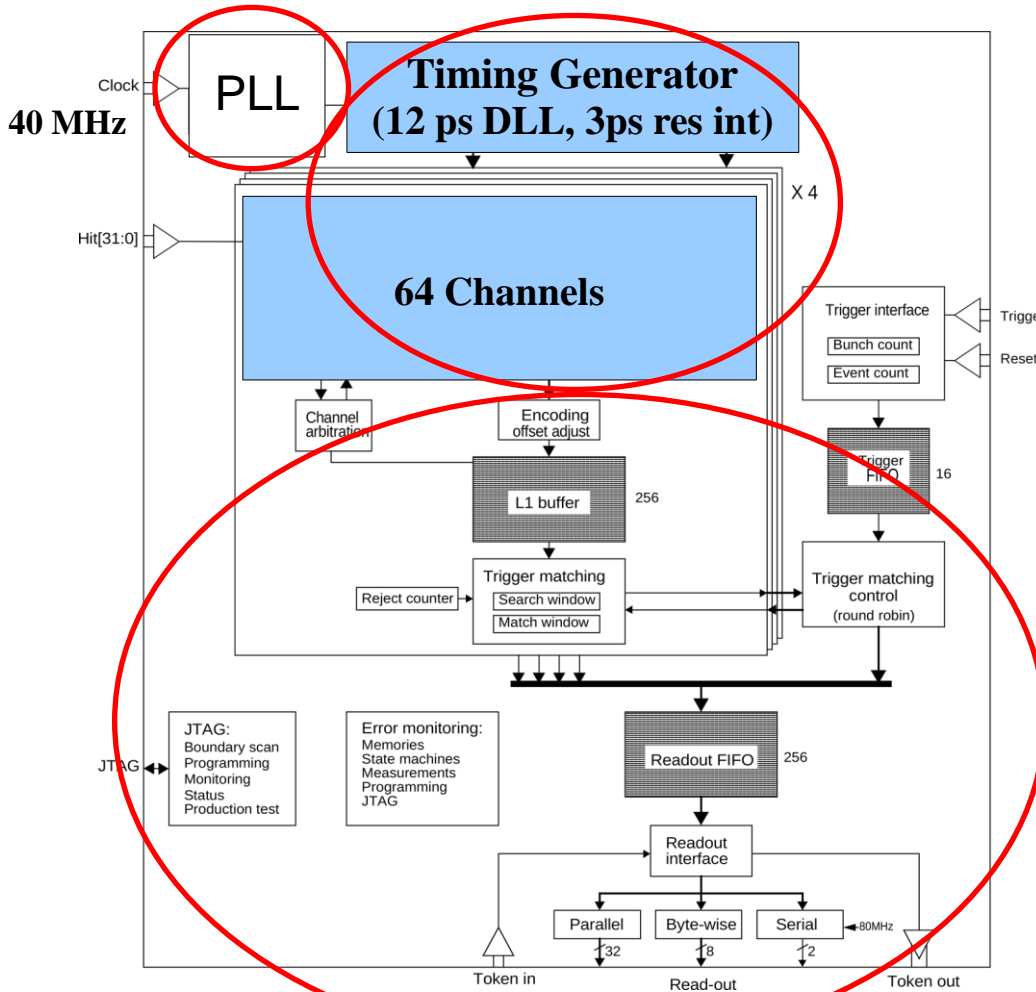
TWEPP2013 slides and paper: <https://indico.cern.ch/event/228972/session/6/contribution/61>  
ESE seminar: <https://indico.cern.ch/event/225547/material/slides/0.pdf>

# MAPPING TO 65NM

- Uncertain long term availability of IBM 130nm
- 2x time performance: -> 3ps binning
- Lower power consumption:  $< \sim 1/2$ 
  - $\sim 1/8$  if DLL binning of 12ps enough (RMS  $\sim 4$ ps).
- Larger data buffers
- More channels
- Smaller chip
- But higher development costs
  - MPW prototyping:  $\sim 80$ k
  - NRE for production masks:  $\sim 500$ kFind other project(s) for shared production masks



# FULL 65NM PS TDC ASIC



Channels: 64 (32)

Binning: 3ps, 12ps, (400ps)

RMS: 1-2ps, ~4ps

Reference: 40MHz clock

Dynamic range: 100us (12bit@40MHZ)

Leading, trailing, TOT

Hit rate: < 320MHz/channel

Data buffers per channel  
(~256 hits per channel)

Triggered/un-triggered

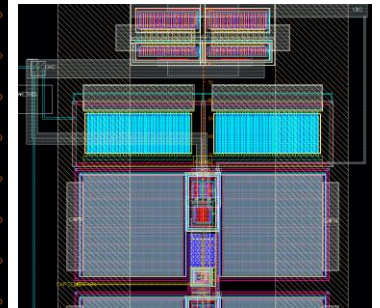
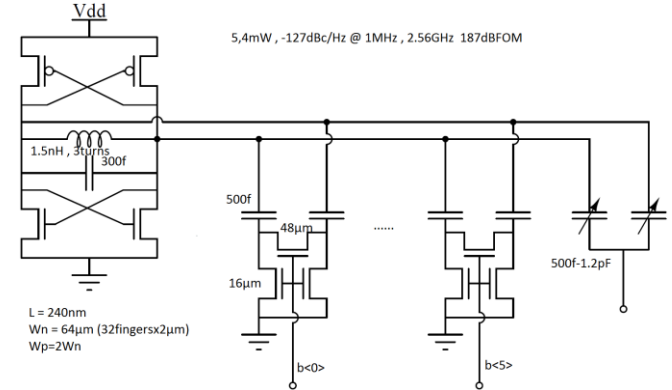
~8 readout FIFOs

Flexible readout interface

Power: ~1W - 1/4 W

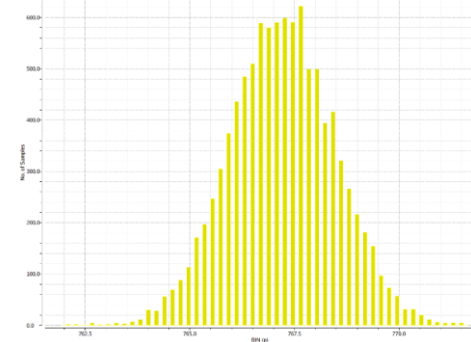
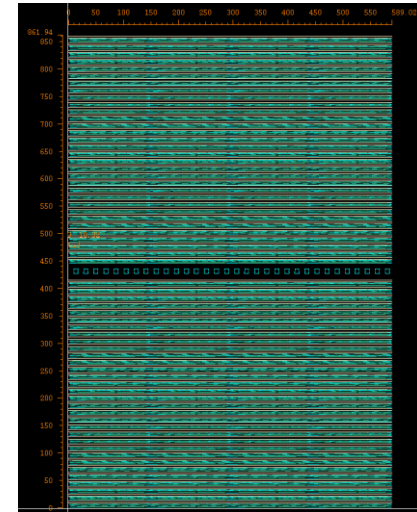
# LOW JITTER PLL

- Clock multiplication from 40MHz to 2.56GHz for coarse time counter and time interpolator
  - Low jitter critical:  $< 1\text{ps}$
  - Jitter filtering of 40MHz clock to the extent possible
    - 40MHz reference MUST be very clean
  - LC based oscillator
- Internal clock for logic and readout: 320MHz
- Design: Jeffrey Prinzie, Leuven
- Status/plans:
  - PLL circuit analysed and simulated at schematic level.
  - Detailed layout and optimization on-going
  - Dedicated prototype planned for Q2 2015 (Synergy with LPGBT PLL)



# TIME INTERPOLATOR AND HIT REGISTERS

- Full custom layout in 65nm
- Done (95%):
  - 12ps binning DLL
  - 3ps binning resistive interpolation
    - Can be disabled for lower power ( $\sim 1/4$ )
- Ongoing:
  - Timing distribution in array
  - INL adjustment/correction
  - Hit register optimization:
    - Critical for power consumption: 64 x 128 = 8K hit registers clocked at 2.56GHz, plus time decoding pipeline ( total  $\sim 24$ K FF)
  - Pipelined time decoding
    - Time critical pipelined time decoding at 2.56GHz
  - Global layout integration, optimization and verification
- Plan: Finalized end February
- Designer: Moritz Horstmann



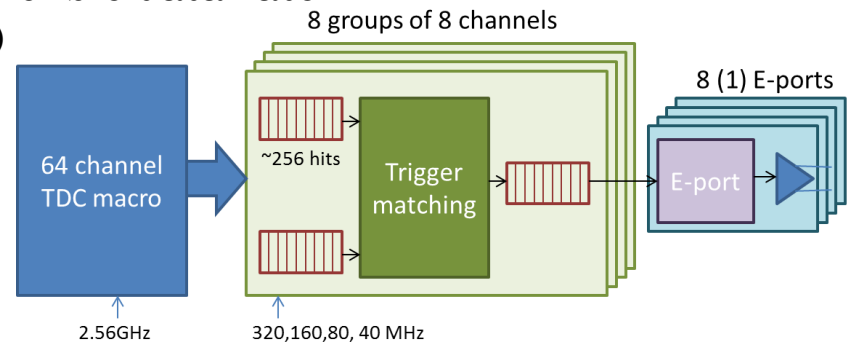
# TDC LOGIC

- Synthesized logic from Verilog RTL
- Based on data driven architecture from HPTDC
  - Simplifications with individual buffers per channel
  - Clocking: 320, 160, 80, 40 MHz (hit rates and power consumption)
  - Trigger matching based on time measurements
  - New/additional features ?
- Reuse of HPTDC verification environment
  - This is  $\sim\frac{1}{2}$  the design effort !.
- New interfaces to be defined and implemented
  - Control/monitoring, Trigger, Readout
- SEU/radiation tolerance
  - 65nm technology TID tolerant
  - SEU detection and minimize effects from SEU when it can have major consequences (system sync)
    - As done in HPTDC
  - Not classified as rad hard
- Planning:
  - Verilog code implementation and simulation: March – December 2015



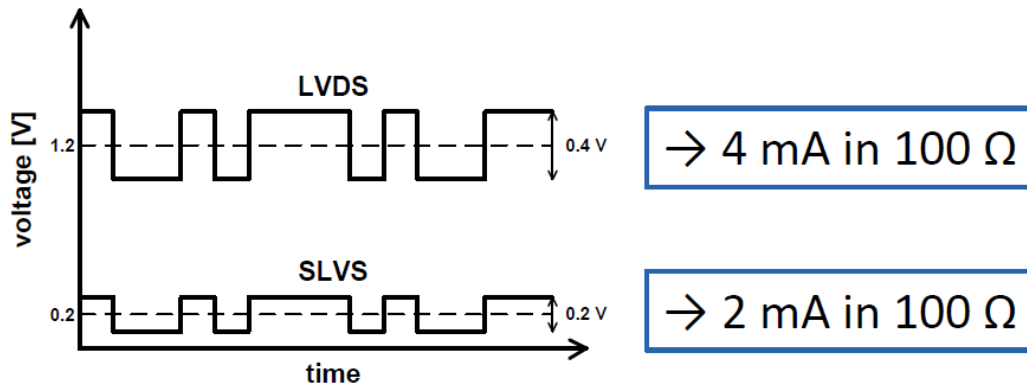
# BUFFERING AND READOUT ARCHITECTURE (INITIAL PROPOSAL)

- Hit buffer per channel: ~256 hits
- Trigger matching/data merging into readout FIFOs organized in groups of ~8 channels
  - 8 readout FIFOs of ~256 hits
  - 1 readout FIFO if only using 1 E-port
- Readout interface: Connecting to GBT and FPGA's
  - E-link: Differential (SLVS), Serial, Double data rate
  - One E-link “clock” (for 1 – 8 E-links)
  - Possibility to hold data stream ?
  - Options:
    - E-link speeds: 320, 160, 80 Mbits/s
    - A. 8 E-links, one for each group:
      - Max:  $8 \times 320\text{Mbits/s} = 2.5\text{Gbits/s}$
    - B. 1 E-link for all channels
  - Details to be defined based on users needs
    - Option of lanes: 1 – 8 bit ?
- Data format: To be defined
  - Triggered: Event frame with header, TDC data, Trailer
  - Non triggered: Stream of TDC measurements



# INTERFACES

- Power: 1.2v, ~1.0W (64 ch, 3ps),  
~0.4W (64ch, 12ps)  
~0.3W (32ch, 12ps)
  - (Not yet defined if 1.5v/2.5v for LVDS IO)
- Hits: Differential SLVS
- Time reference: 40MHz SLVS
  - Other clock frequencies required ?.
  - Low jitter reference critical for high time resolution (especially for large systems time measurements across many channels/chips/modules)
- Trigger/BX-reset/reset: Sync Yes/No (encoded protocol ?)
- Control/monitoring: GBT E-link and I2C
- Readout SLVS: 1-8 E-links
- (JTAG boundary scan + production test ?)
- Packaging: ~250 FPBGA



# SCHEDULE

- Interpolator circuit prototype: Done
- Technology choice: Done
- Final Specifications: Q1 2015
- Finalize TDC macro: Q1 2015
- PLL prototype: Q2 2015
- Final RTL model: Q4 2015
- P&R and Prototype submission: **Q1 2016**
- Prototype test: Q2 2016
- Final production masks/prototype: Q3 2016
- Production lot: **Q4 2016**

# RESOURCES

## ○ R&D

- 2-3 man-years chip design:
- Main designer: Moritz Horstmann (“new” CERN fellow)
- PLL: Jeffrey Prinzie, Leuven (synergy LPGBT)
- Supervision: Jorgen Christiansen
- Low jitter/power SLVS differential: Synergy with LPGBT
- Contribution from others ?
  - Interfaces/RTL/FPGA test board: Paul Davids, Alberta ?
  - Testing/characterization ?.
- ~100k CHF prototyping, packaging, testing: ~Funded

## ○ Put in production

- ~500k: NRE , Packaging, test
- Shared engineering run?
  - We may have to contribute 250k – 100k.
- Funding from clients/users/projects required
  - No large user that can pay it all
  - To be defined in detail in 2016, When full prototype available.
    - Entry price to get access to chips
    - Pro-rata to number of required chips

# USERS/ CLIENTS

- No commercial multi-channel TDC of this type available
  - That's the reason that so many have used the HPTDC
- CERN HEP:
  - TOTEM
  - CMS HPS and ATLAS FP420 (very forward detectors)
  - LHCb Torch (upgrade option)
  - CMS endcap Calorimeter with timing ?
  - ATLAS muon upgrade ? (low resolution)
- Other HEP
  - TICAL
  - PANDA, CBM
  - Many experiments needs multi channel high/low resolution TDC
  - Many would like to explore ps timing as new “dimension” in HEP experiments. Detector and analog FE critical (e.g. CFD)
- Non HEP research
  - Medical imaging: TOF PET
  - Florescence imaging
  - Other
- Instrumentation:
  - CAEN, , ,
- Other “clients” will show up when working device available
- TDC users meeting Feb. 12: <https://indico.cern.ch/event/366097/>



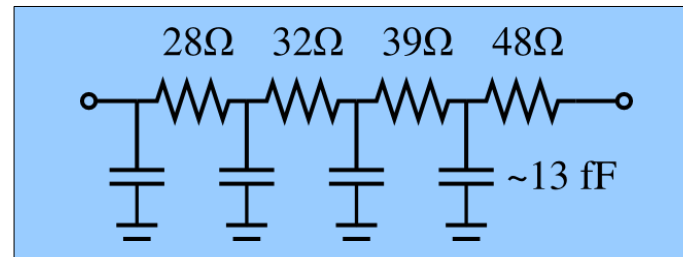
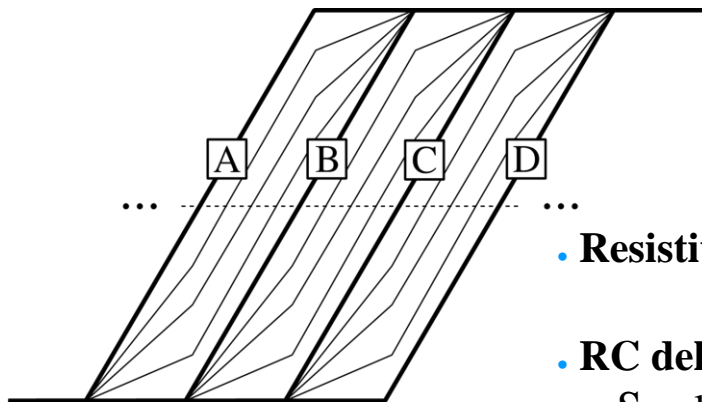
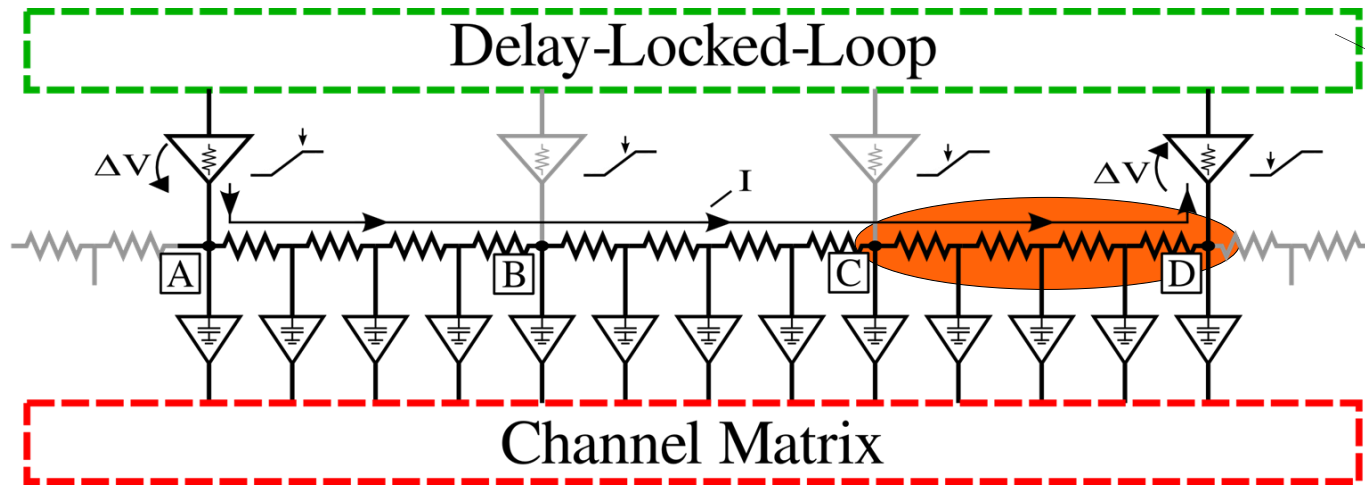
# BACKUP SLIDES



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# RESISTIVE INTERPOLATION



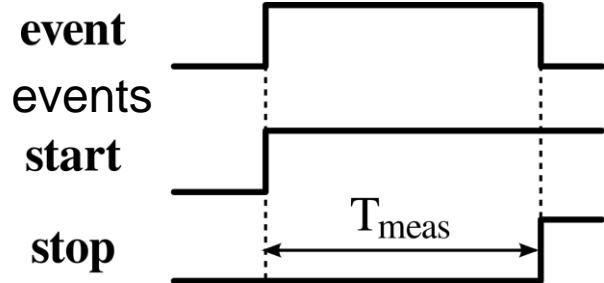
- **Resistive voltage divider**  
-> Signal slopes longer than delay, stabilized by DLL
- **RC delay** (capacitive loading)  
-> Small resistances, small loads  
-> Simulation based optimization of resistor values



# Time Measurements

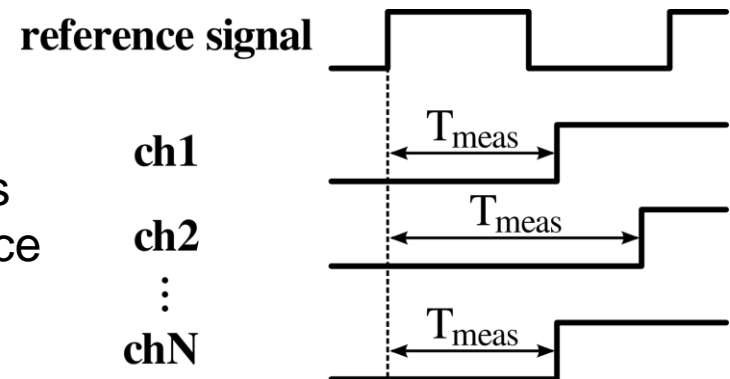
## Start - Stop Measurement

- Measure relative time interval between two local events
- Small local systems and low power applications

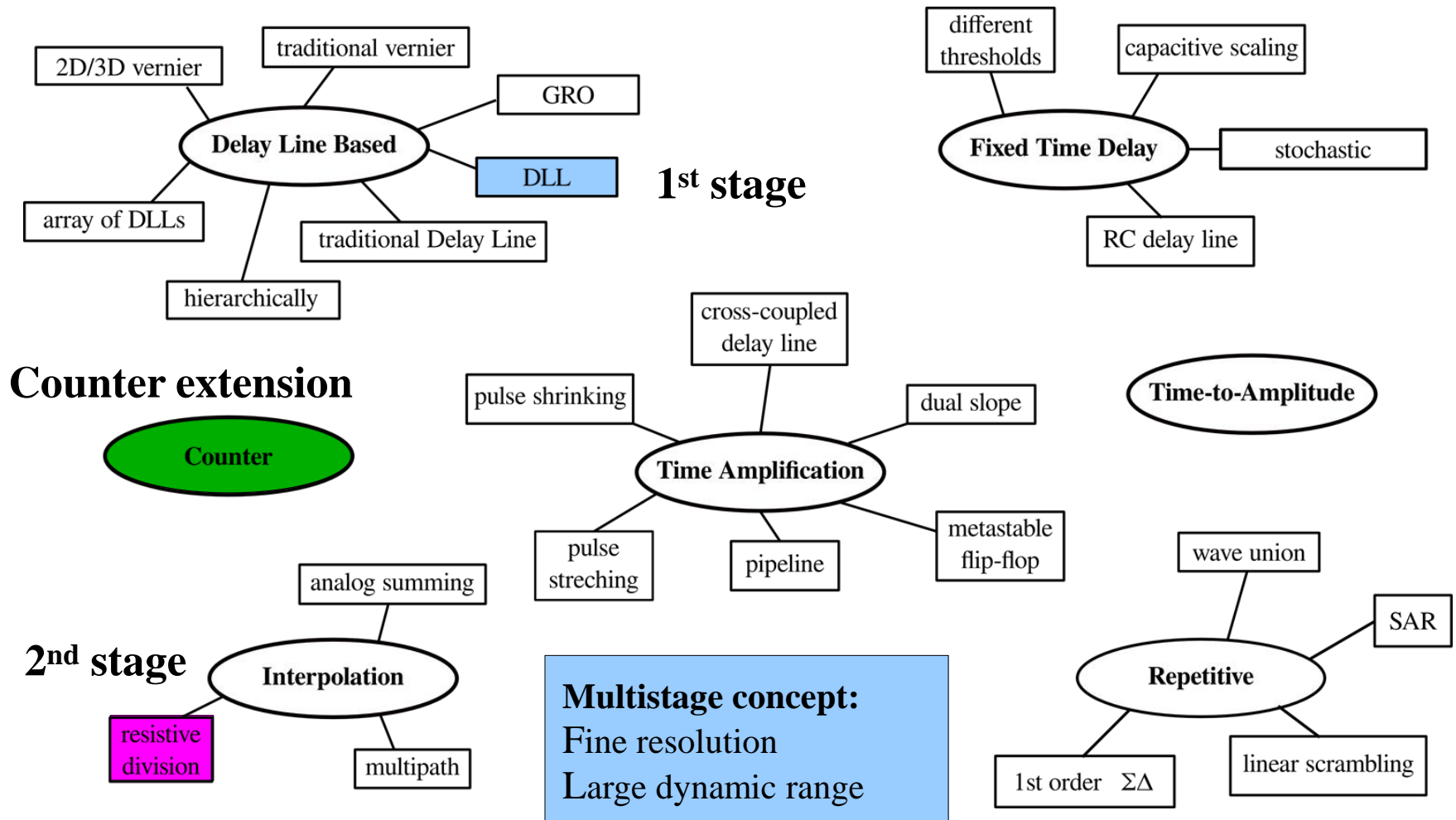


## Time Tagging

- Measure “absolute” time of an event  
(Relative to a time reference: clock)
- For large scale systems with many channels  
all synchronized to the same reference



# TDC Architectures



# DIFFICULTIES IN PS RANGE RESOLUTION

$$\text{LSB}/\sqrt{12} \neq \text{rms}$$

It is not worth making a fine binning TDC if resolution is lost in imperfections/noise

## • Device mismatch

- > Careful simulation and optimization
- > Major impact on design and performance

## • Noise (power supply)

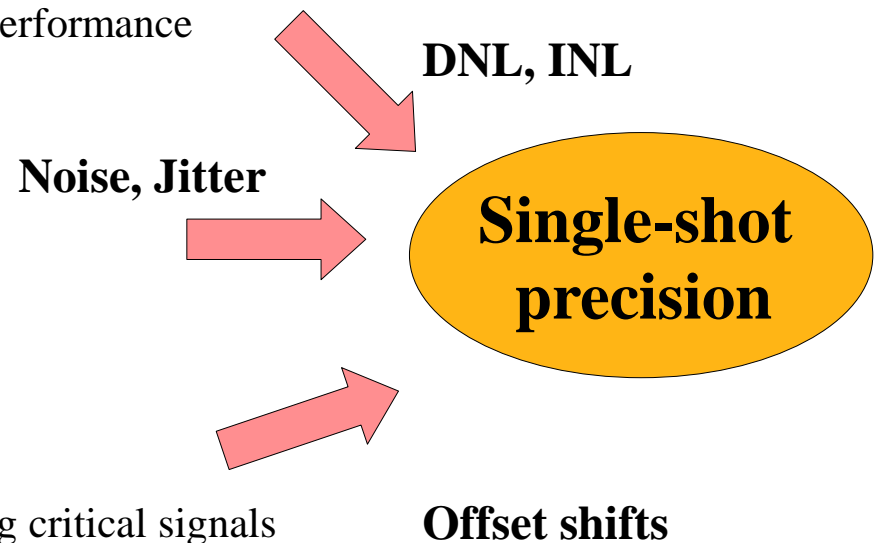
- > **Short delays, fast edges**
- > **Separate power domains**
- > **Substrate isolation**
- > **Crosstalk**

## • Signal distribution critical

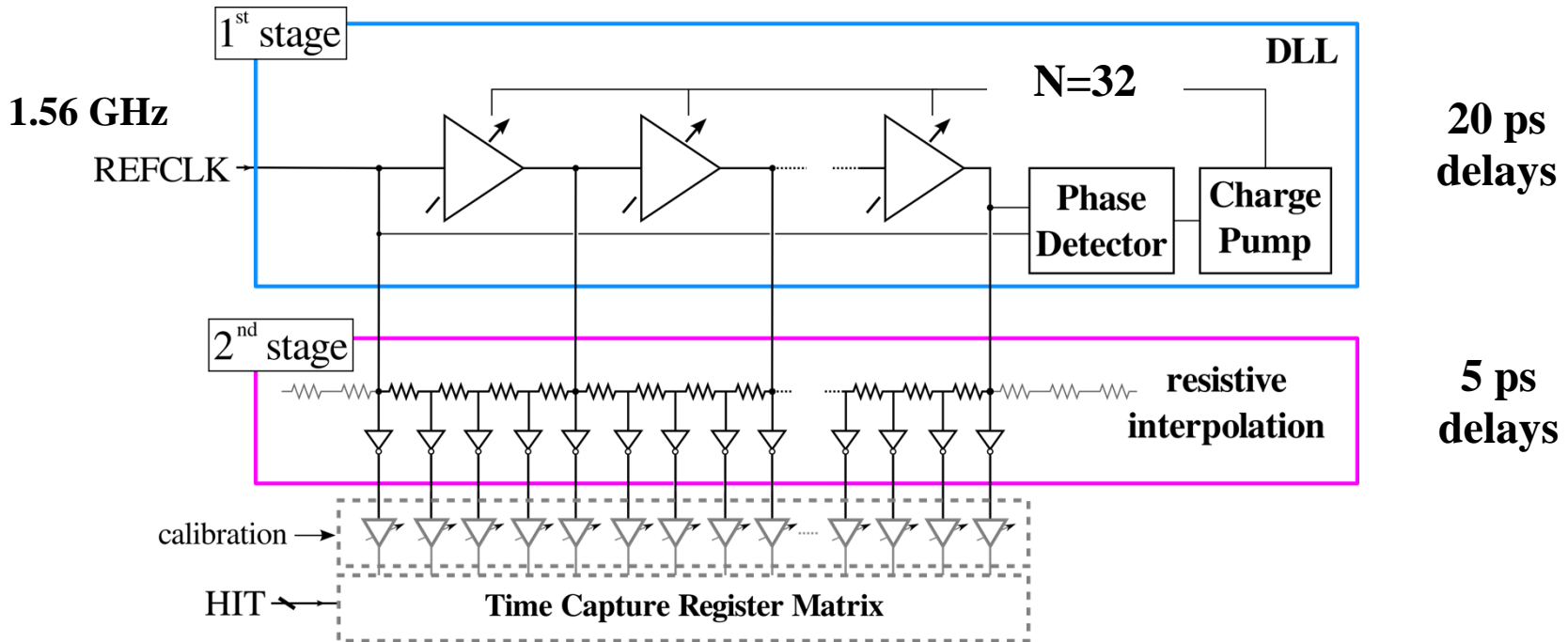
- > RC delay of wires
- > Balanced distribution of timing critical signals

## • Process-Voltage-Temperature variations

- > Auto calibration to compensate for slow VT variations: Delay locked loop
- > Global offset calibration still required



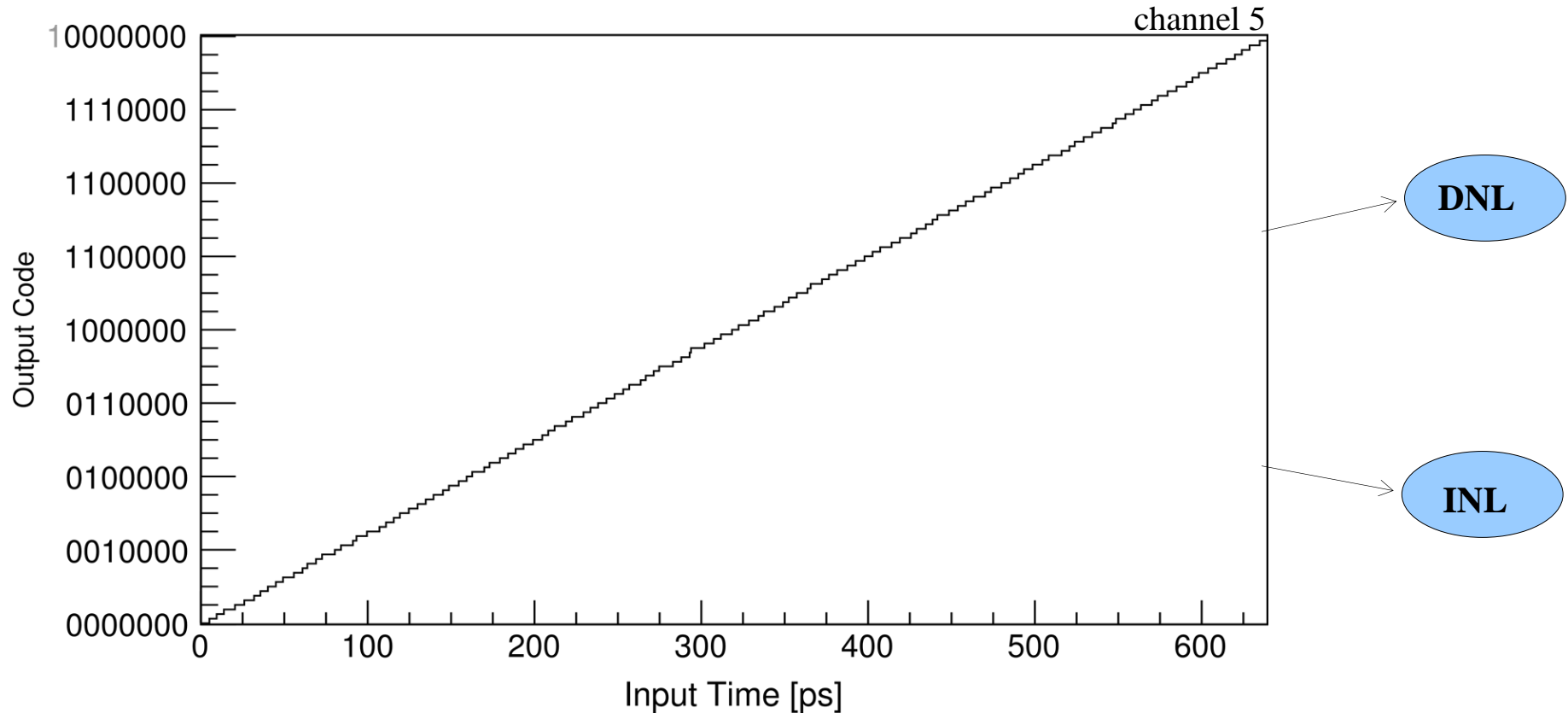
# Fine-Time Interpolator



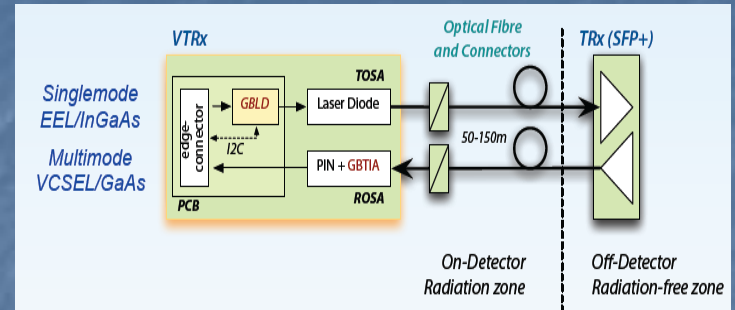
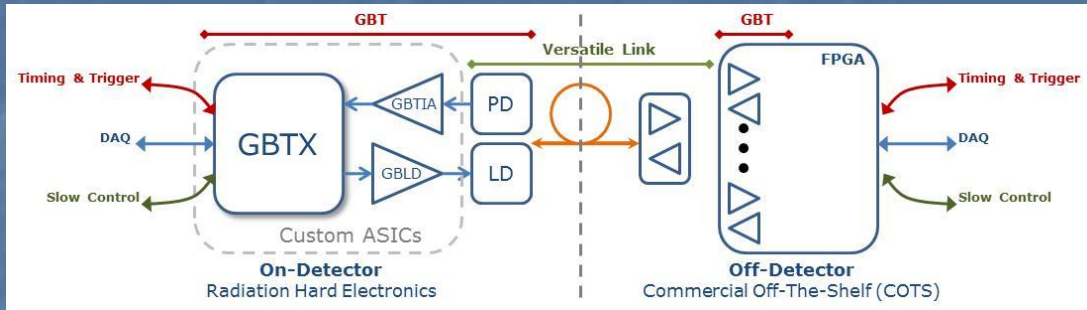
- **DLL to control LSB size**
  - > 32 fast delay elements in first stage - 20 ps
  - > Total delay of DLL 640 ps at 1.56 GHz
- **Resistive Interpolation to achieve sub - gate delay resolutions**
  - > LSB size of 2nd stage controlled by DLL
  - (Auto adjusts to DLL delay elements)

# Reconstructed Transfer Function

after global calibration  
has been applied



# GBT, Versatile, GLIB



**Hardware, Firmware, Software, not only Dream-ware**

