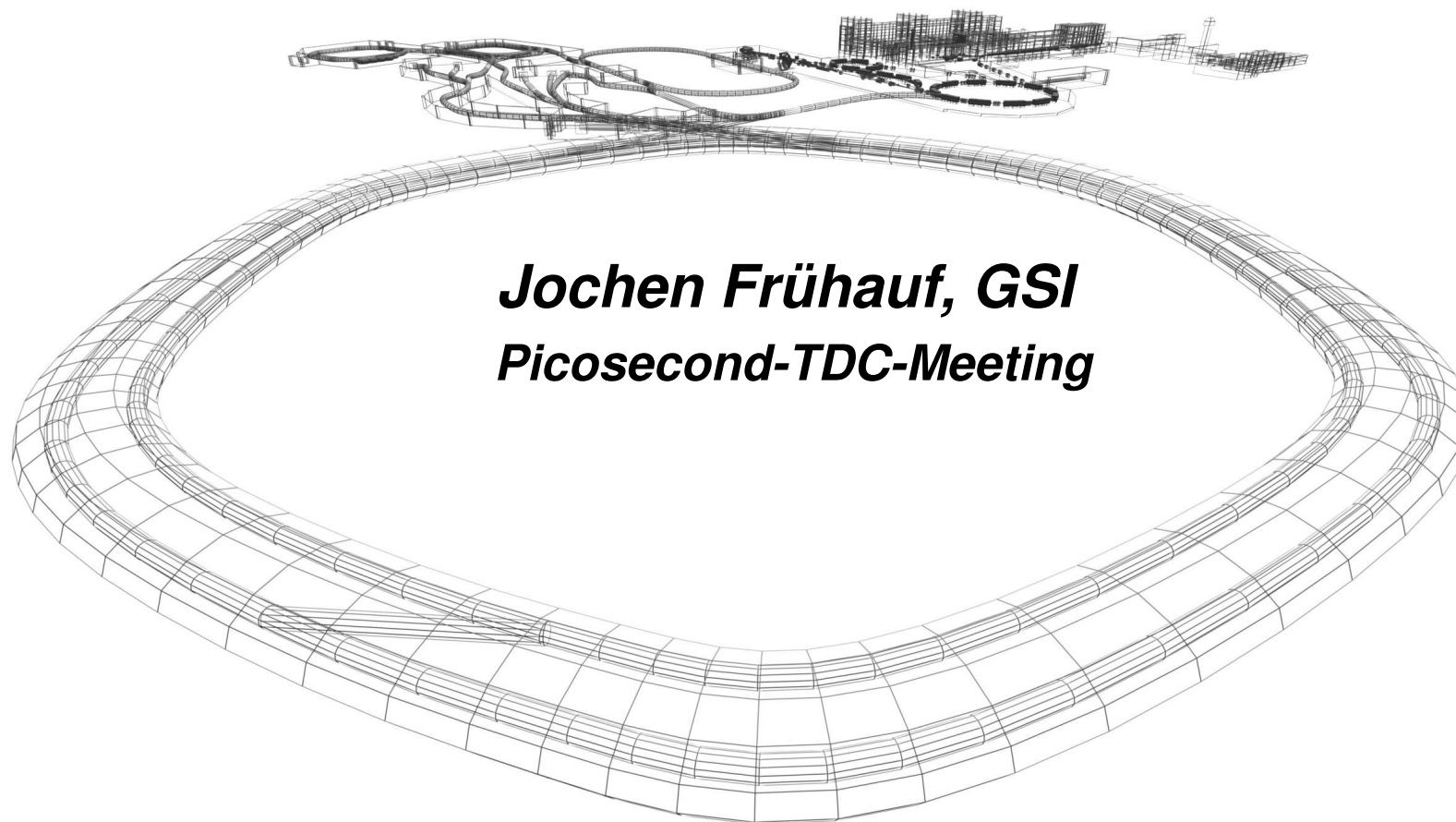
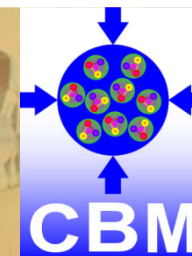


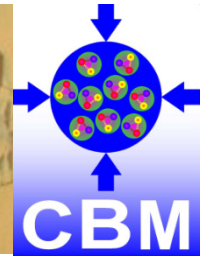


CBM-TOF-FEE

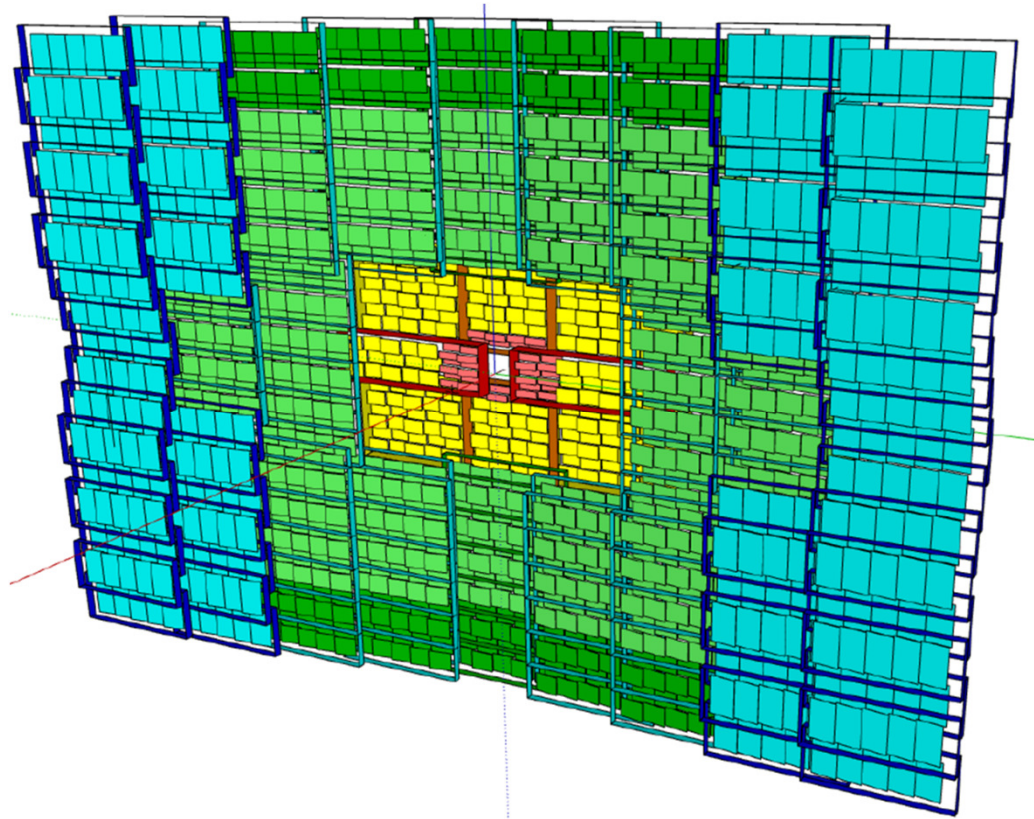


***Jochen Frühauf, GSI
Picosecond-TDC-Meeting***

CBM ToF Overview



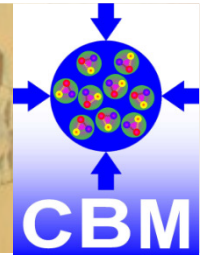
CBM Time of Flight Wall
will be composed out of
Multi-gap Resistive Plate Chambers
(MRPCs)



Requirements

- full system time resolution ~ 80 ps
- surface $\sim 120\text{m}^2$
- Efficiency $> 95\%$
- Rate capability ≤ 25 kHz/cm²
- Free streaming DAQ
- Low power electronics (~ 100.000 CH)

CBM ToF Electronics Requirements



The minimal requirement for the full CBM TOF system is a time resolution of **80 ps**.

This includes Diamond Detector as “Start” and MRPC Wall as “Stop” including the electronics.

However a better time resolution would improve the physics performance!

Start System (Diamond + Electronics) ~ **50ps**

❑ ToF Wall (Counter + Electronics) ~ **60ps**

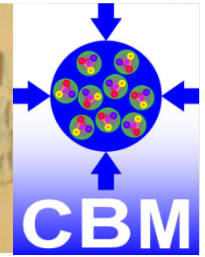
❑ *Contributions MRPC* ~ **50ps**

❑ *Contributions Electronics* ~ **38ps**

➤ Preamplifier & Discriminator ~ **20ps**

➤ TDC at most **32ps** (including CLK distribution)

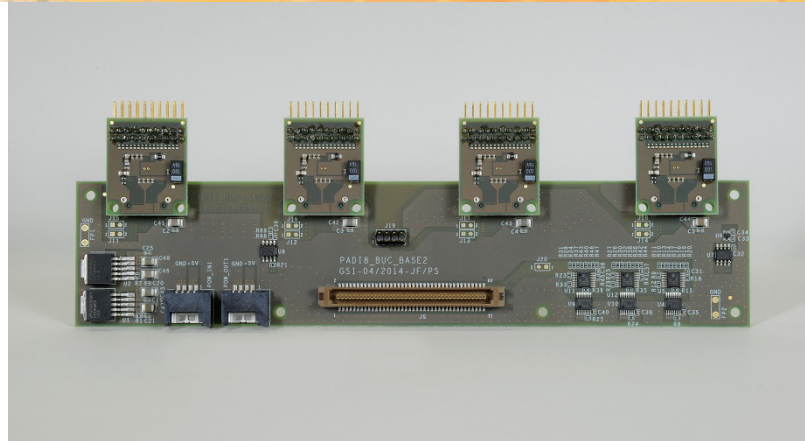
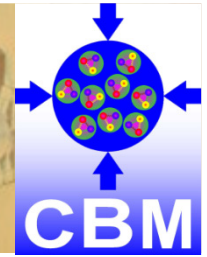
CBM ToF TDC specification



The specifications for the **TDC** of CBM-ToF are the following:

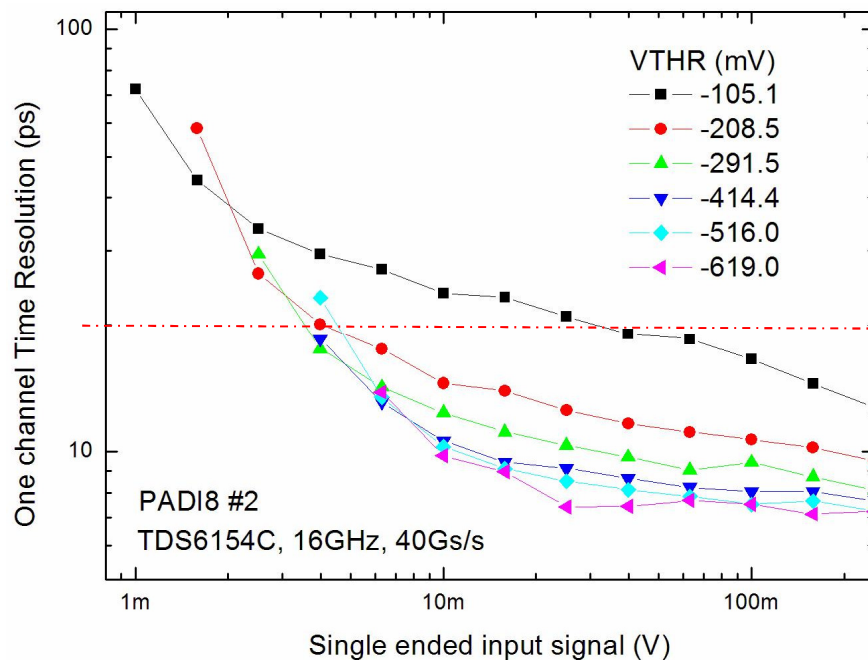
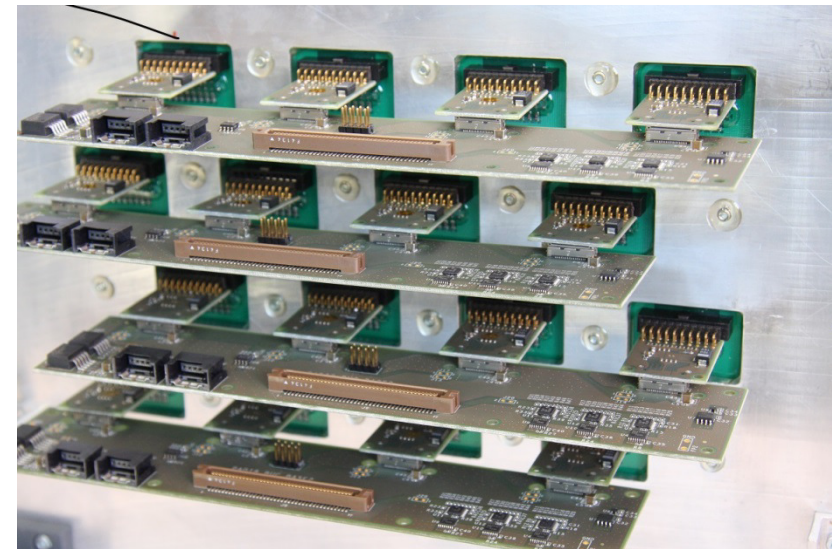
- single channel time **resolution 25ps** or better
- **low power** (less **25mW** / Channel)
- **LVDS Inputs** for Hit Signals / **LVDS Outputs** for Data transport (2.5V LVDS)
- possibility for **Time over Threshold measurement** (pulse width in the order of **~1ns** are possible)
- it should provide a good **double pulse resolution** (GET4 = **3.2ns**)
 - below 1ns would be perfect
- readout has to be **free-streaming** (CBM = trigger less DAQ)
- Channel Hit rate max **600kHz**
- **SPI Master** for Threshold setting of PADI is needed
- external **CLK Input** / **Sync Input** or **Coarse counter Reset Input** (common start)
- **radiation tolerance**

Preamplifier & Discriminator (PADI #8) (UMC 180nm CMOS)



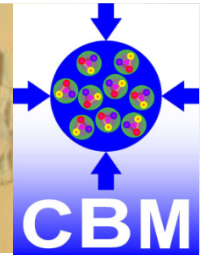
← 4 x PADI8 = 32 Channel

fits to "Feedthrough PCB" of
Bucharest 2013 MRPC Prototype

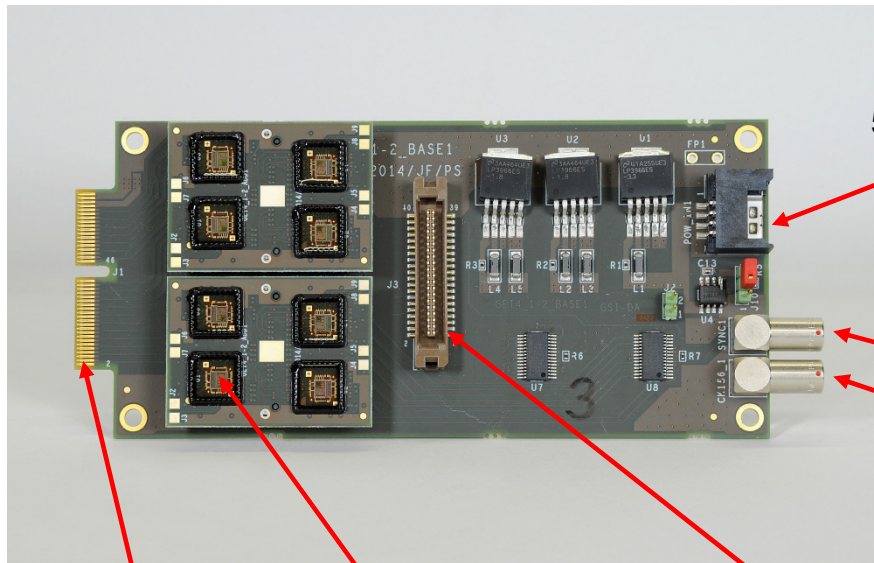


<http://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=6786378>

GET4 (GSI Eventdriven TDC 4 Channel) (UMC 180nm CMOS)



GET4 FEE (8 x Get4 = 32 Channel)



5V Power

pro:

- radiation tolerance
- channel dead time 3.2ns
- free-streaming readout

contra:

- no flexibility for software updates
- not improvable in terms of time resolution

External Sync Input

External CLK Input

GET4 ASIC

Connector to readout Controller

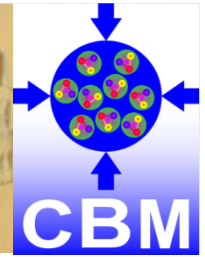
Connection to Feed-Through PCB
of MRPC-Module

- 32 Channel TOT
- precision ~ 28ps between two channels
- SPI Master for PADI

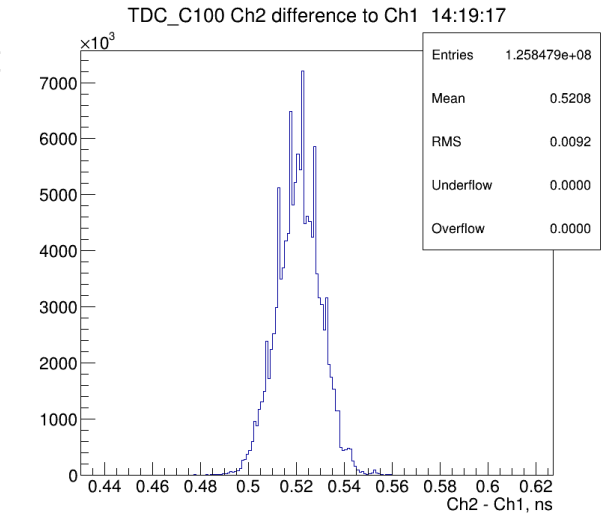
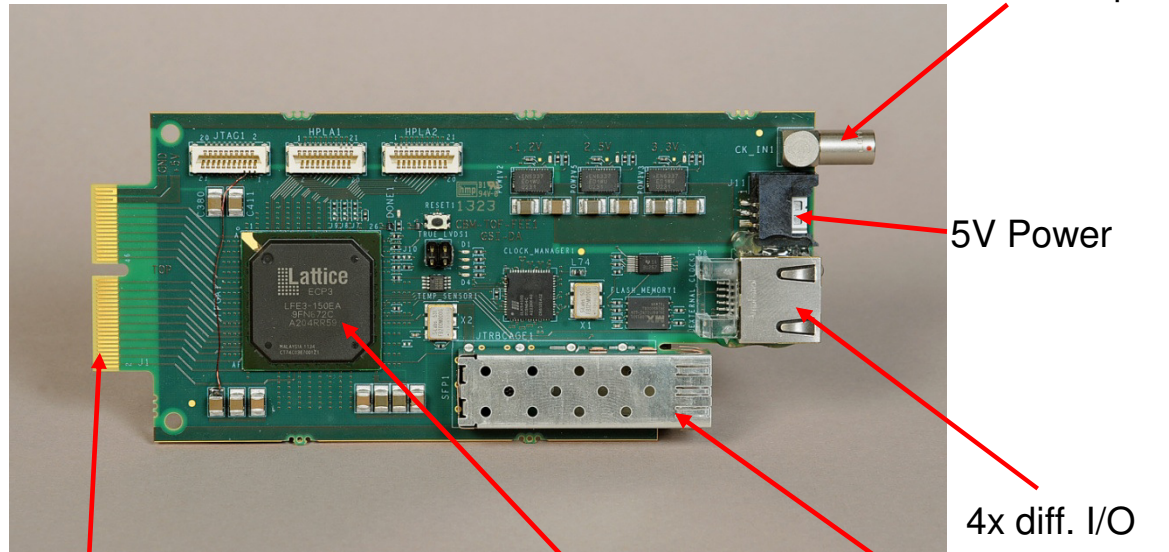
Performance:

	2ch / ps	1ch / ps
chip-level	27.35	19.33
pcb-level	27.69	19.58
pcb-pcb-level	28.70	20.29

FPGA TDC for CBM-TOF



CBM-ToF-FEE (FPGA TDC)



Precision between two Channel one Board ~ 9.2ps

pro:
flexibility due to software update
very good time resolution

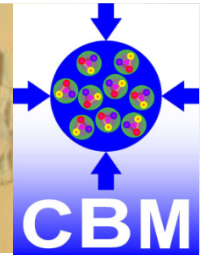
contra:
radiation tolerance
channel dead time ~ 40ns

- 32 Channel TOT
- precision ~ 10ps between two channels
- SPI Master for PADI

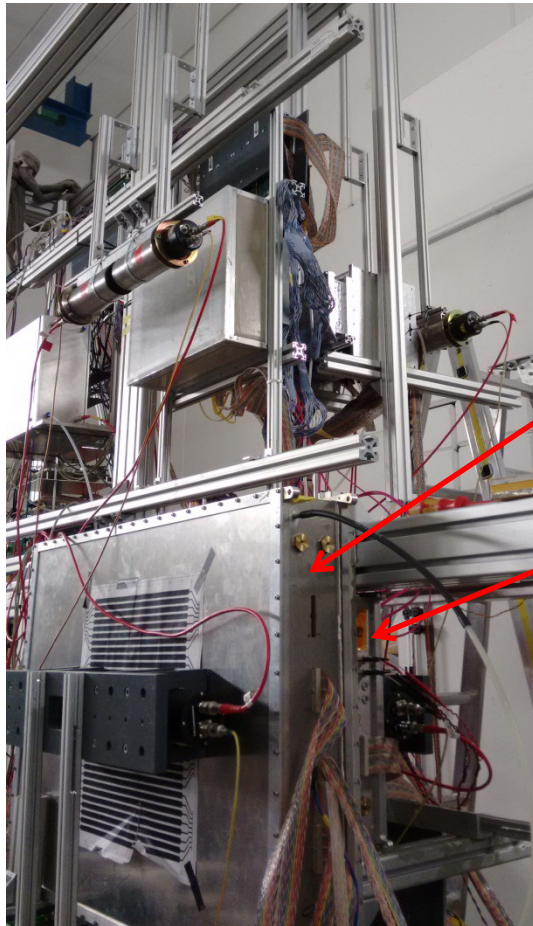
FPGA TDC Programmer: Cahit Ugur
GSI / CS-EE

Beam time @ GSI

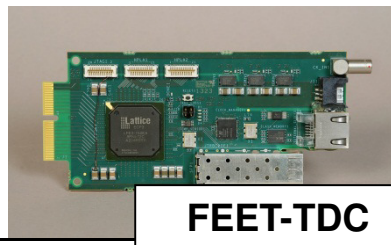
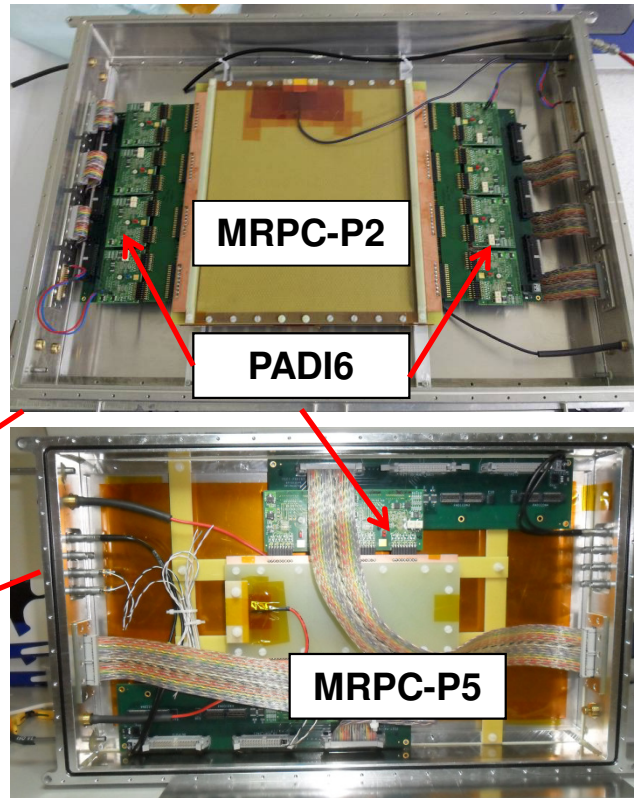
MRPC + PADI + FPGA TDC



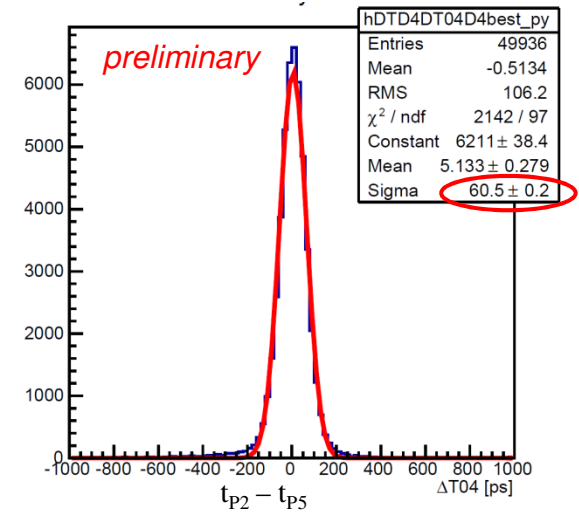
Setup



MRPC + PADIs



System Time resolution obtained between two MRPCs



Measured in a Heavy Ion Beam with full illumination of the counter.

Single counter resolution is about 43ps including FEE

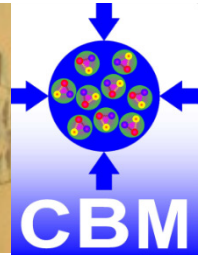
Readout chain

- MRPC
- PADI6
- FEET – TDC (FPGA)



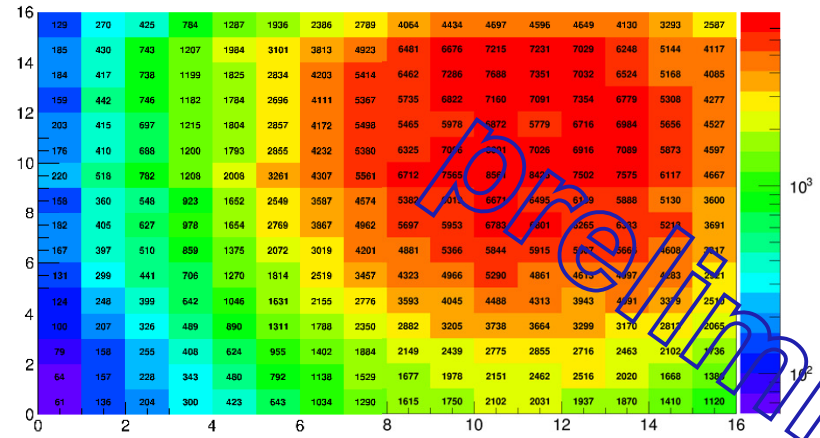
Beam time @ GSI

2x16Channel Diamond+PADI+FPGA TDC



Beam spot / hit entries

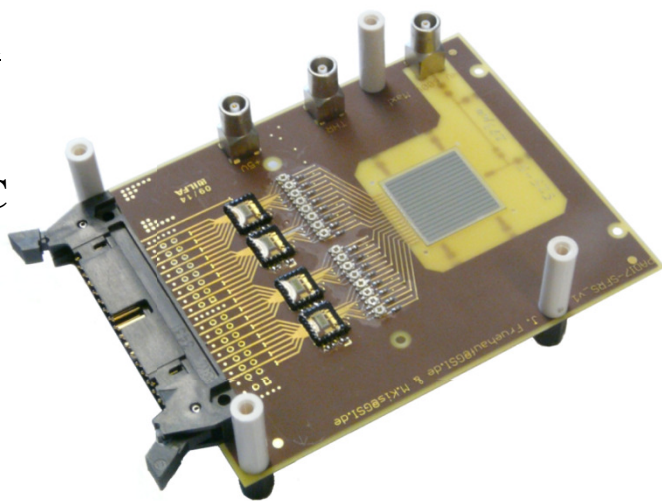
Diamond + PADI



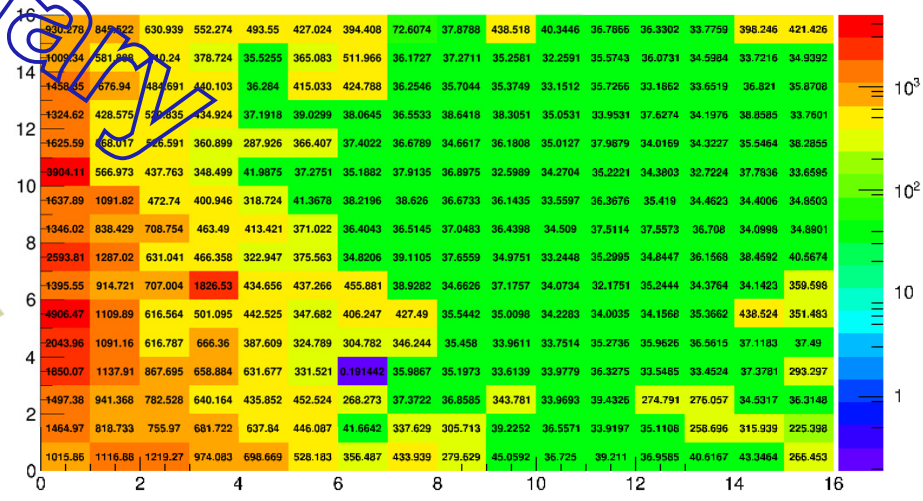
Diamond time resolution is about 25 ps including FEE

Readout chain

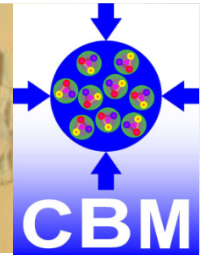
- Diamond
- PADI7
- FEET – TDC



Time resolution

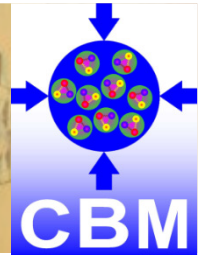


Questions raised by Jorgen



- Time reference: Is 40MHz clock OK or are there requests for other time references (e.g. 50MHz)
 - 40MHz are OK
- Hit interface: Is SLVS OK (0.2v amplitude, 0.2v common mode).
 - PADI has LVDS Output
- Hit rates, Hit pulse width (if using TOT) , acceptable deadtime.
 - max 600kHz / ~1ns / small as possible (GET4 3.2ns)
- Time resolution: Who actually needs 3ps binning and who can “manage” with 12ps binning (lower power)
 - 12ps binning is fine
- Power supply: We aim at only using a 1.2v power supply (but this may give some limitations on IO/LVDS)
- Radiation tolerance requirements.
 - Yes
- Trigger requirements: latency, rate, trigger window, non triggered
 - non triggered
- Readout: Via GBT, FPGA or other ?
 - both possible
- How many TDCs do you need, when (just initial estimate)
 - ~100.000 Channel

Outlook



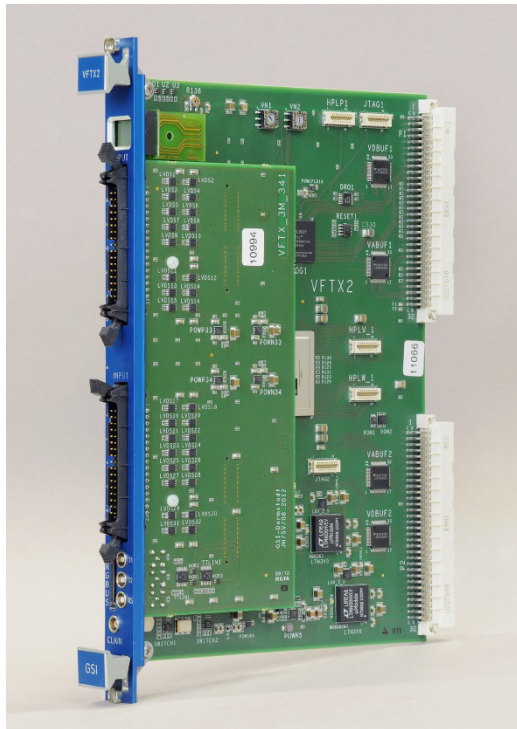
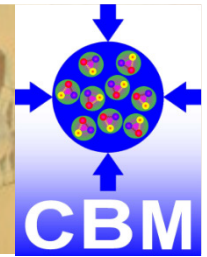
Beam test @ CERN starting next week

- Main DAQ:
 - FPGA TDC ~560 Channel
- Test setup:
 - GET4 TDC ~180 Channel



Thank you for your attention

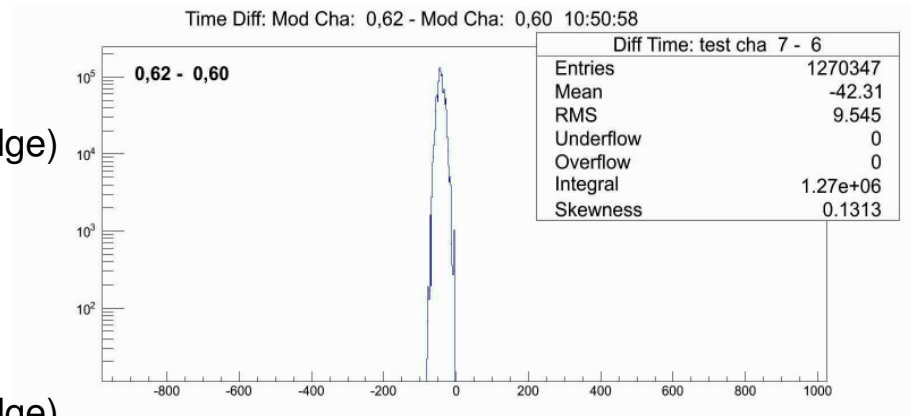
Backup: FPGA TDC: VFTX (VME FPGA TDC 10ps) (Experiment Elektronik GSI)



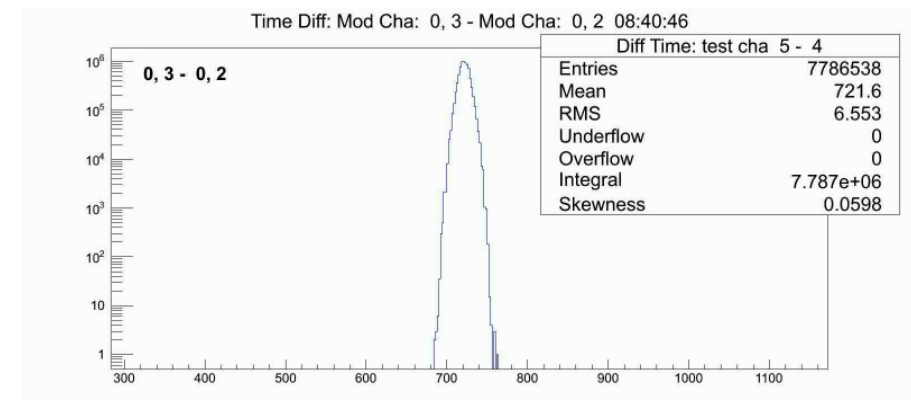
1. 10ps Design
 - 16 CH (TOT)
 - 32 CH (leading edge)
 - CH-DT = 40ns

2. 7ps Design
 - 16 CH (leading edge)
 - CH-DT = 280ns

3. LVDS or NIM
 - NIM = 16CH
 - LVDS = 32CH

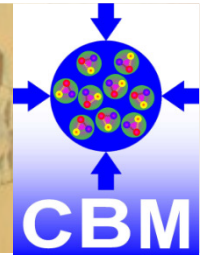


**precision between two channels:
above 10ps Design (9.545ps)
below 7ps Design (6.553ps)**



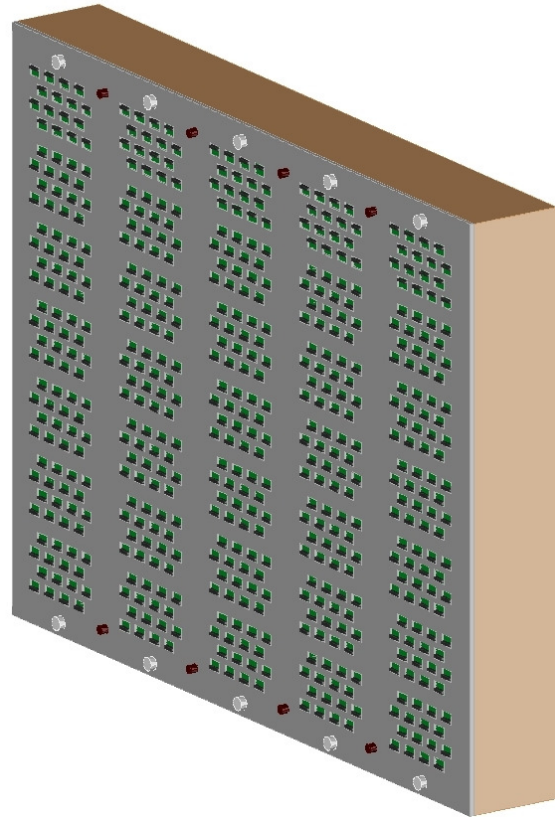
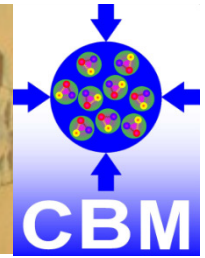
FPGA Code: Eugen Bayer

Backup: PADI Overview

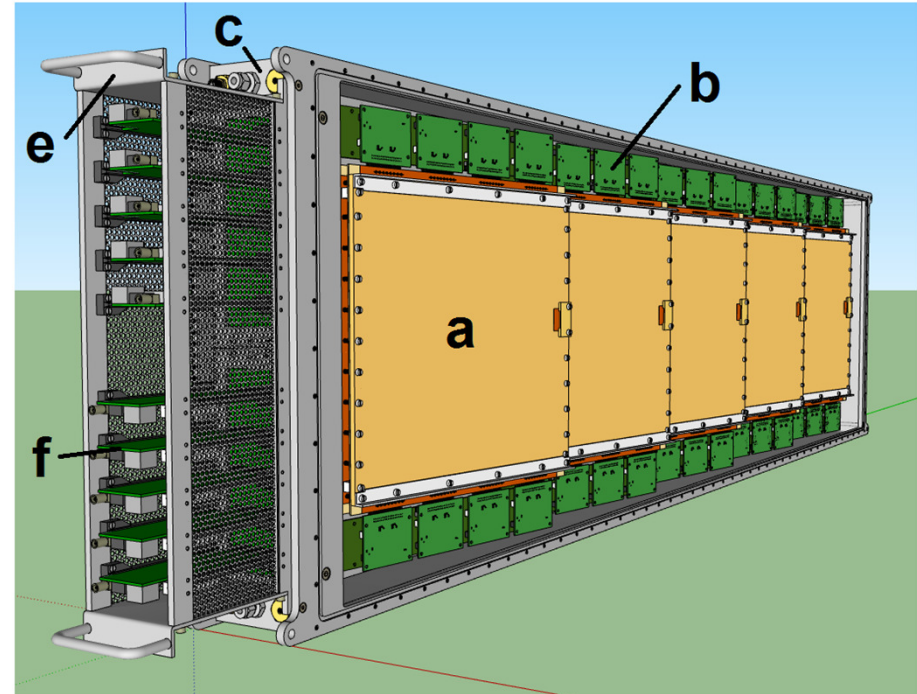


Main parameters comparison	PADI-1	PADI-2	PADI-6	PADI-8
Channels per chip	3	4	4	8
PA Bandwidth (MHz)	280	293	416	411
PA Voltage Gain	74	87	244	251
Conversion Gain (mV/fC)	6.3	7.8	35	30
Baseline DC offset σ (mV)	6.7	21.9	5.9	1
PA Noise (mV _{RMS})	3.37	2.19	5.82	5.5
Equivalent Noise Charge (e _{RMS})	3512	1753	1039	1145
Threshold type	Extern	Extern	Ext. & DAC	DAC
Threshold dynamics (\pm mV)	Non.lin. 280	Non.lin. 300	Lin. 500	Lin. 750
Input Impedance Range (Ω)	30-450	37 - 370	38 - 165	30 - 160
Power consumption (mW/channel)	21.6	17.4	17.7	17

What is planned



MRPC Module of the inner part of the ToF Wall
FEE connected outside



MRPC Module of the outer part of the ToF Wall
PADI (b) connected direct to MRPC (a)
TDC (f) sits outside of the Chamber (c)