

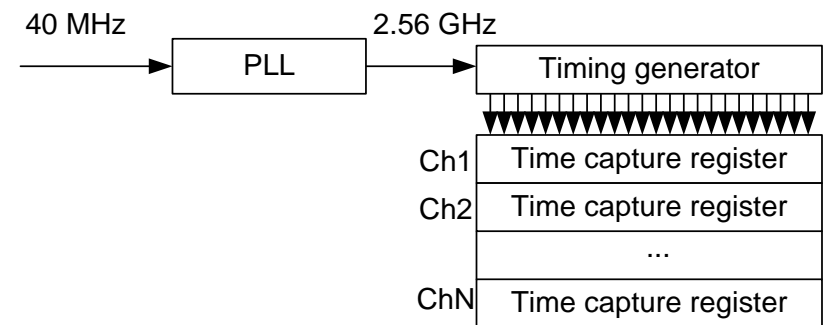


# Low Jitter PLL clock frequency multiplier

Jeffrey Prinzie

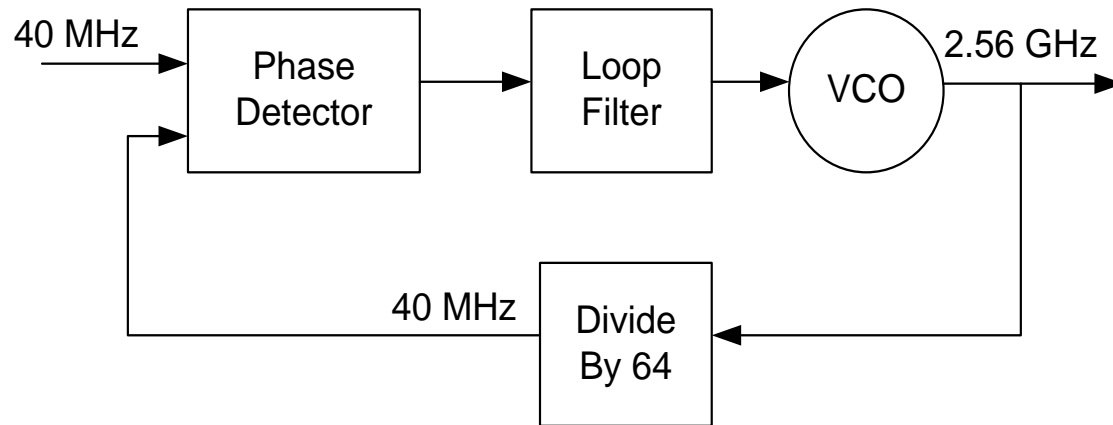
# Frequency generator

- TDC requires high speed clock
  - 2.56 GHz
- Experiments only have low speed clocks available
  - 40 MHz
- Need frequency multiplier
  - 40 MHz  $\rightarrow$  2.56 GHz
  - $f_{\text{out}} = 64 \cdot f_{\text{in}}$
- Synchronised with reference
- $\rightarrow$  PLL



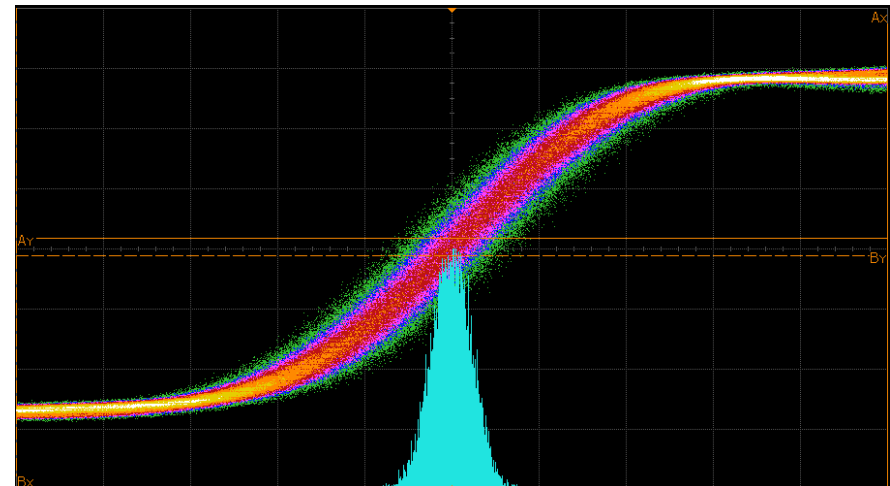
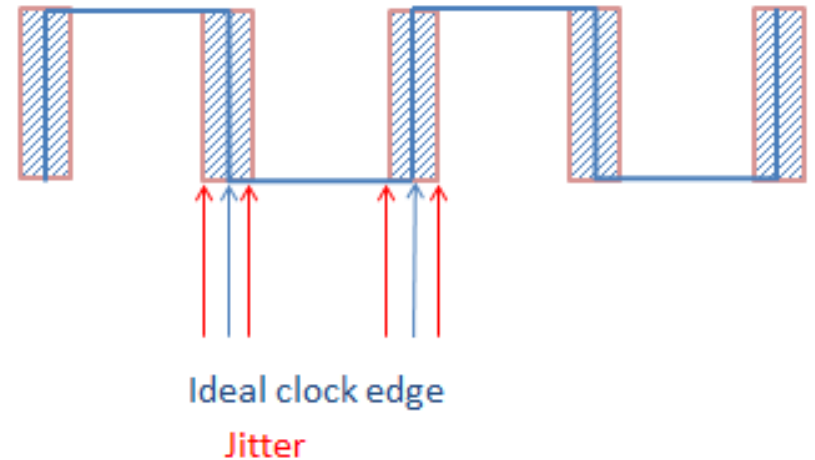
# Phase locked loop

- Negative feedback loop
- Phase detector compares VCO clock with reference
  - Aligns VCO phase with reference phase
  - $\Phi_{in} = \Phi_{out}$  (phase lock)
- Adjusts VCO frequency with error signal

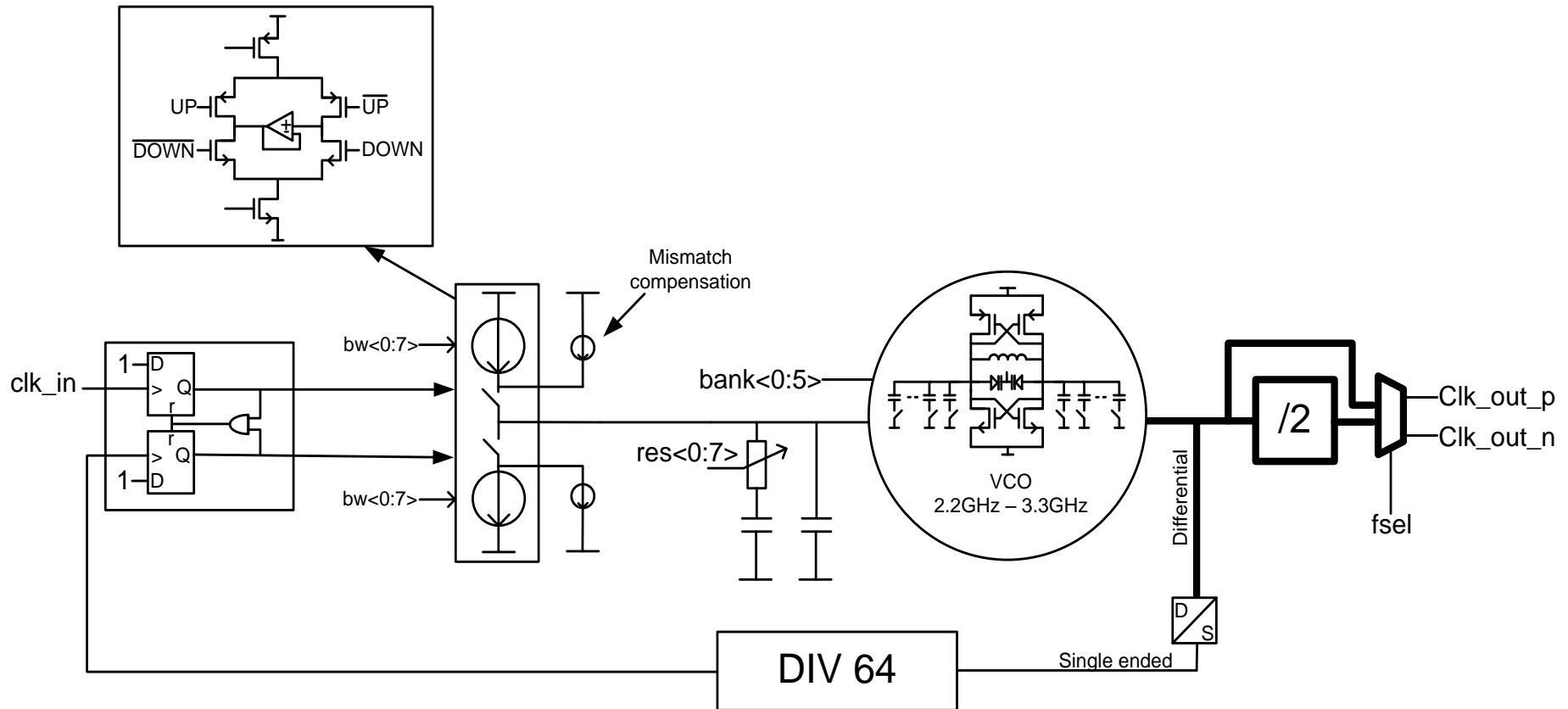


# Jitter

- Random timing noise
- $< 1$  ps RMS
- Reference clock noise
  - Low pass filter
- VCO clock noise
  - High pass filter



# PLL architecture



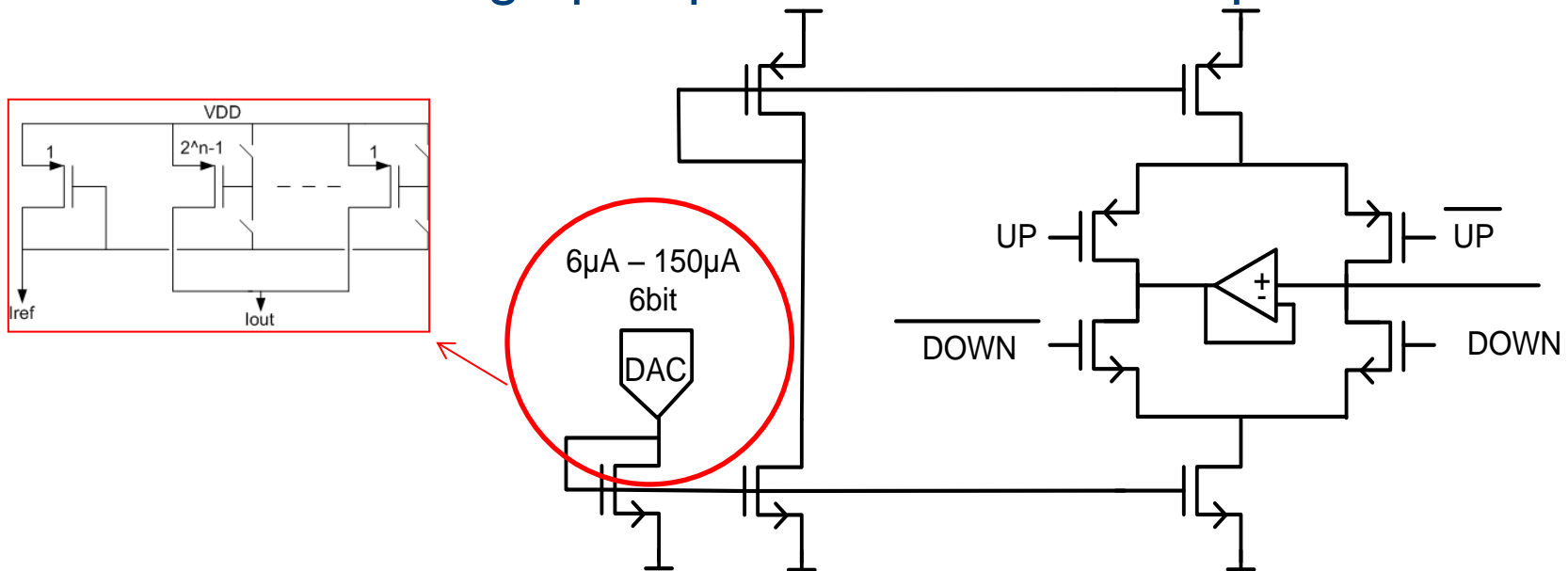
# PLL features

- Automatic frequency bank selection
- Lock detect
  - System initialization done ( xx ms)
- Charge pump (manual) mismatch compensation
- SET tolerant configuration registers
- 40 MHz – 50 MHz reference compatible
- <10 mW power consumption

# PLL features

## Programmable bandwidth

- 100kHz – 1MHz bandwidth
- Tunable charge pump current with on-chip reference

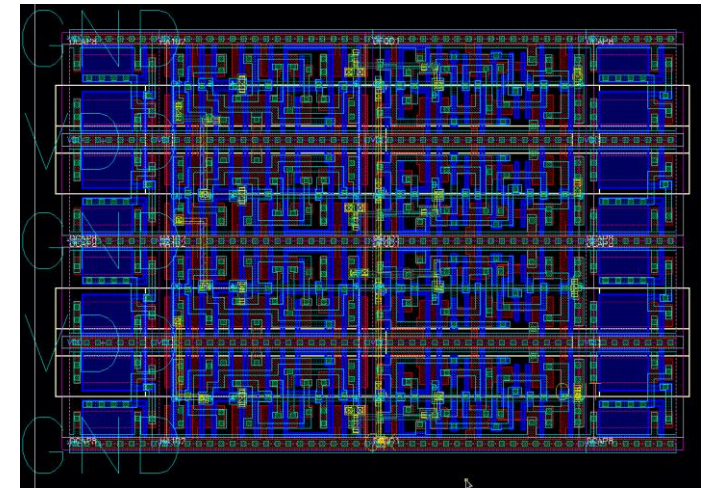
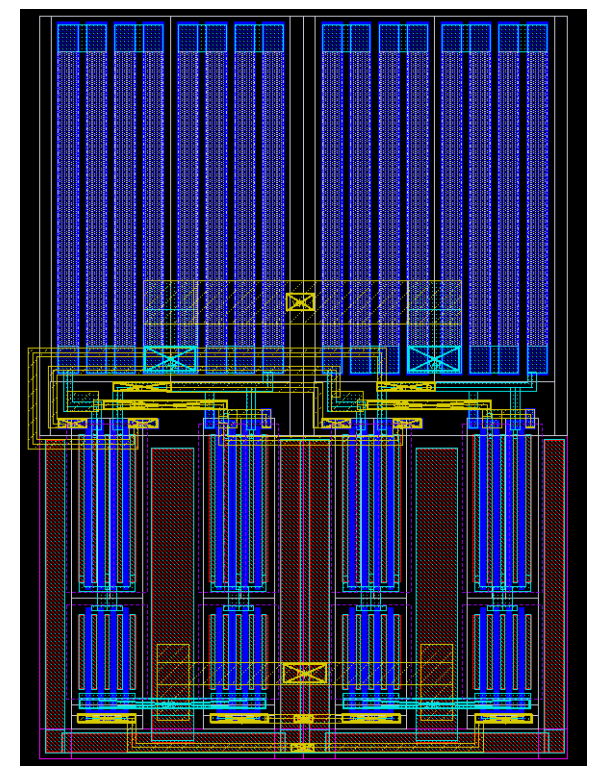


- Adjustable loop resistor

# PLL features

## Divider

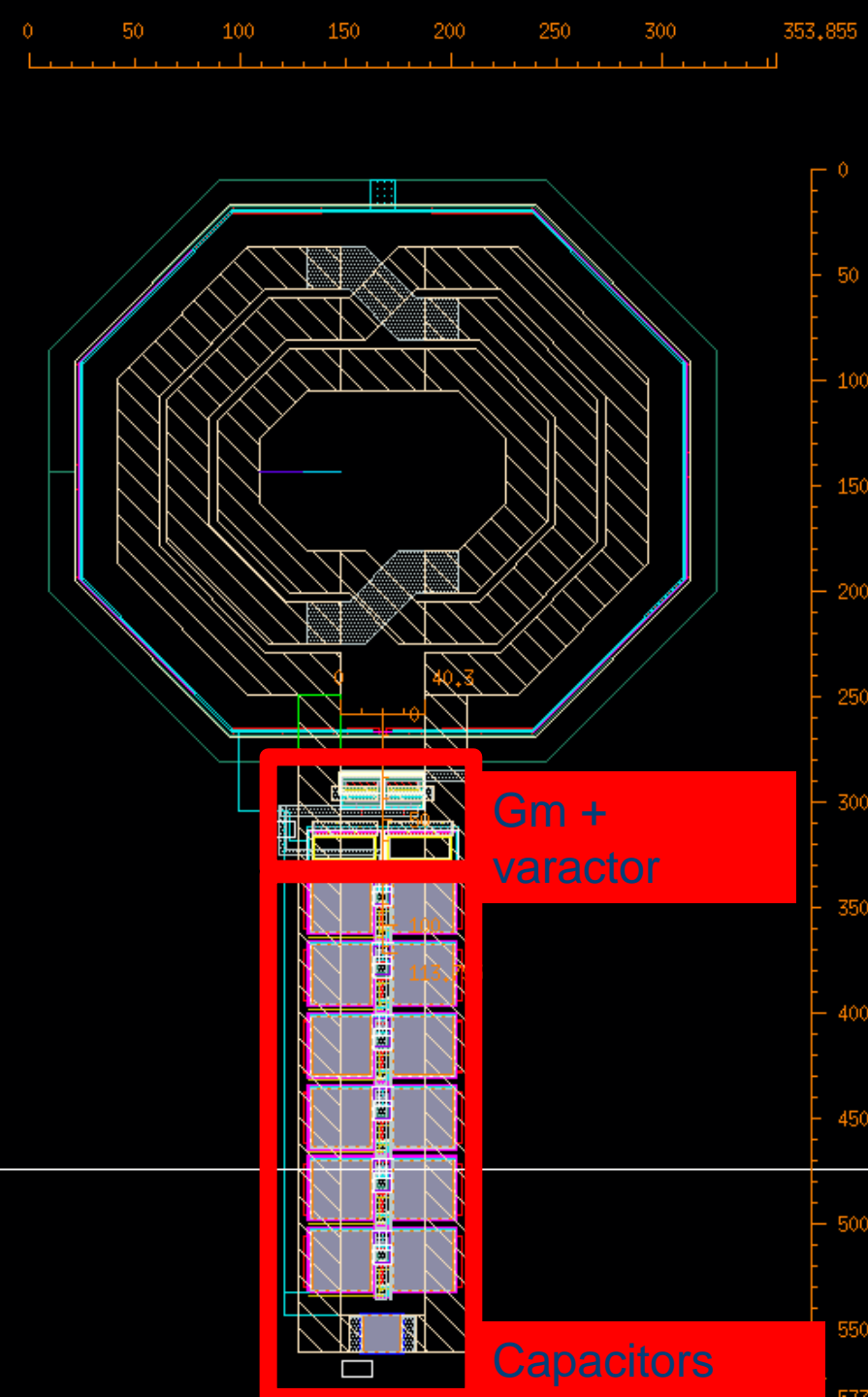
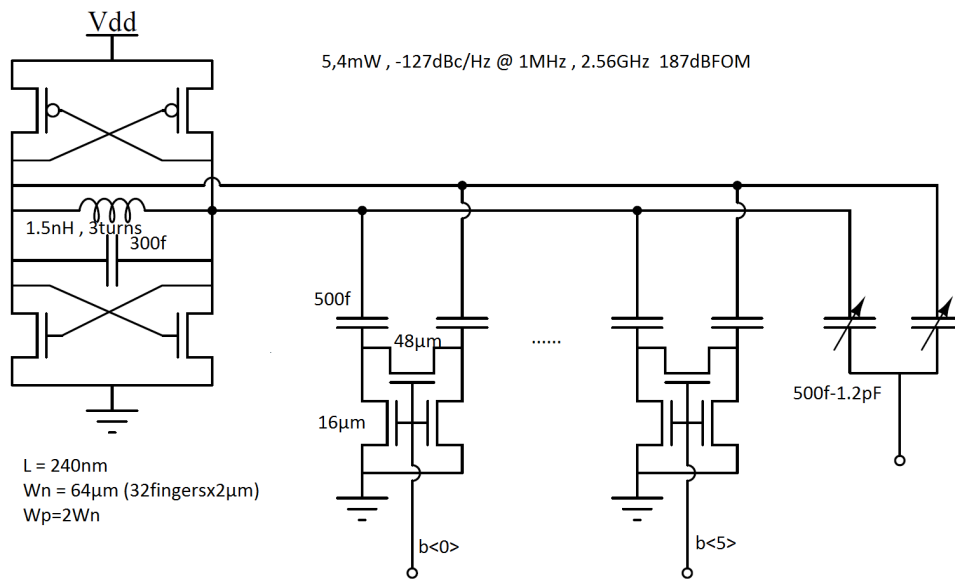
- High speed CML prescaler (DIV4)
- Low speed divider (DIV16)
  - Protection with TMR for SET?
- Fixed division ratio
- Selectable DIV2 at output
  - 2.56 GHz or 1.28 GHz





# PLL features

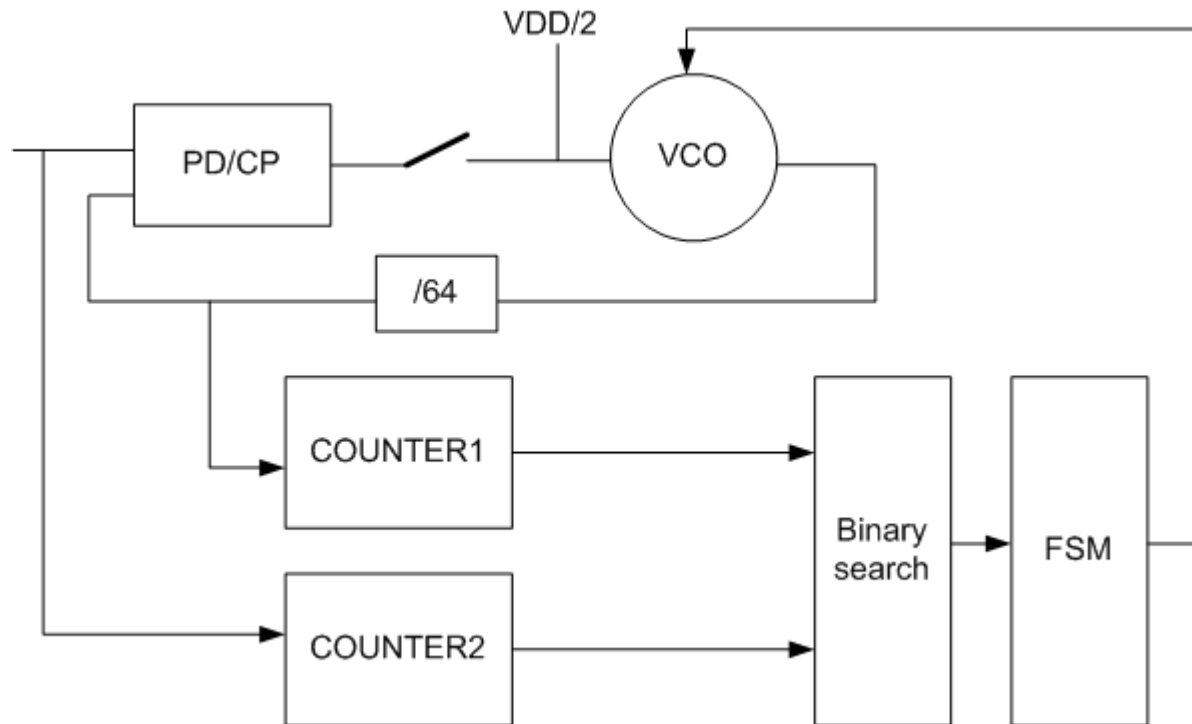
## VCO



# PLL features

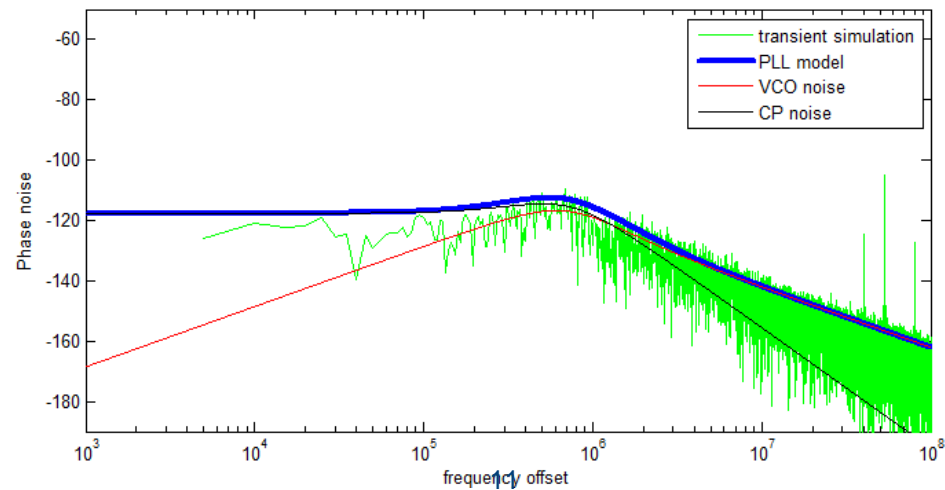
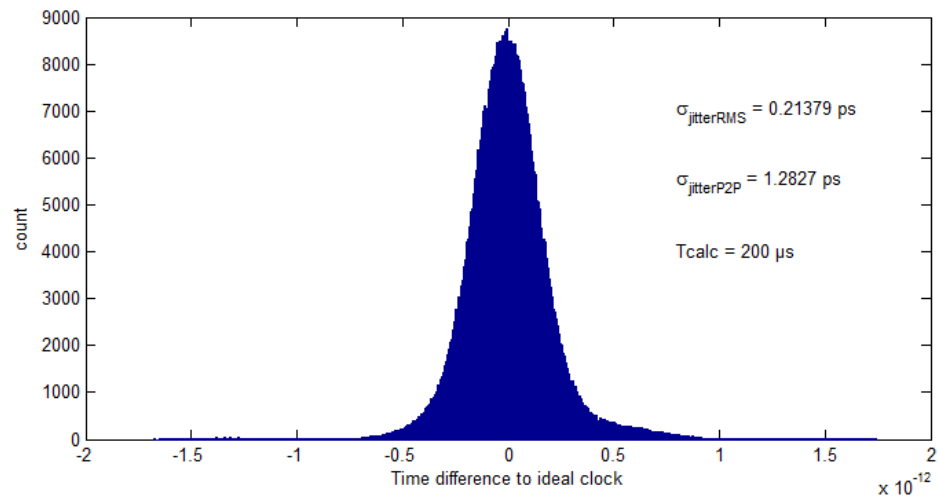
## Automatic frequency selection

- Binary search to select correct capacitors
  - PVT insensitive



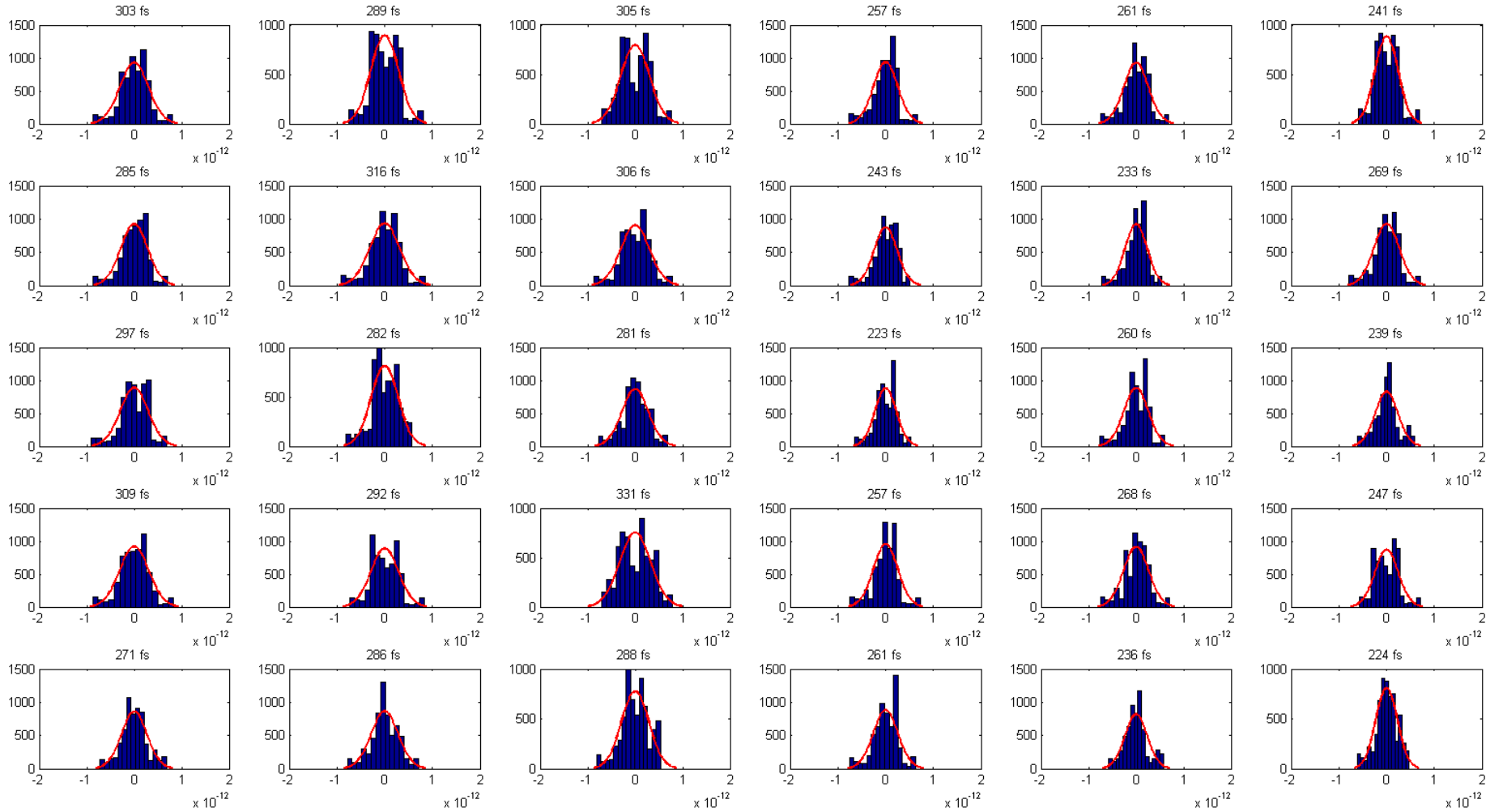
# PLL results

## Output jitter



# PLL results

Corners (-25°C – +85 °C 10% VDD)



# PLL results

## Jitter input filter

