Development and test of the DAQ system to readout a Micromegas prototype to be installed into the ATLAS experiment

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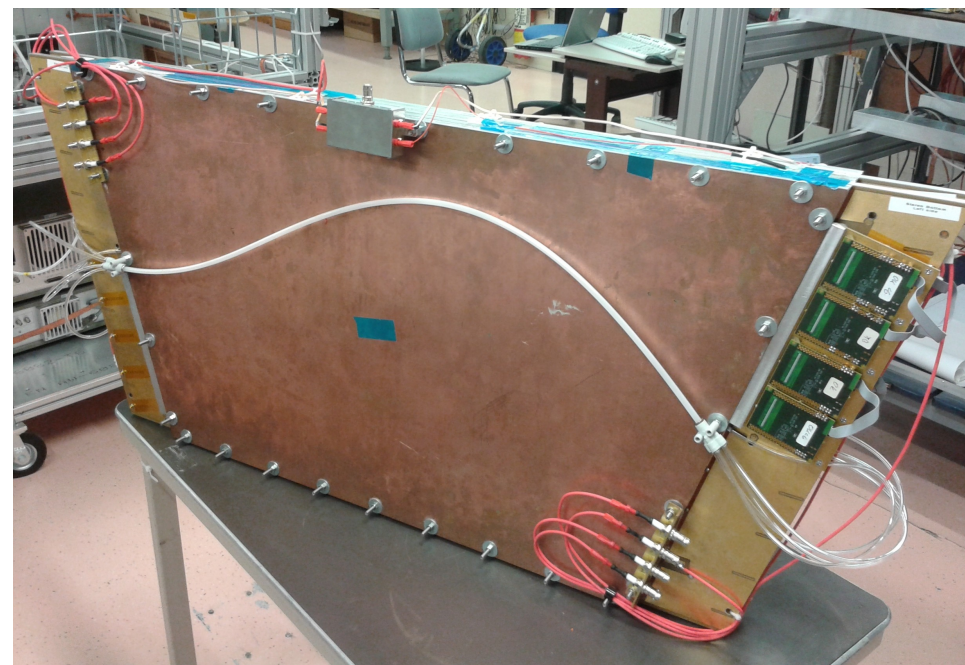CERN, Julius-Maximilians-Universität Würzburg

MicroMegas Small Wheel (MMSW) prototype

- A Micromegas quadruplet prototype (MMSW) with active area of 0.5 m^2 per plane has been built, following the general design foreseen for the upgrade of the ATLAS Small Wheels (New Small Wheel (NSW) project)

- Chosen detector technology is the so-called resistive strip Micromegas, using an additional layer of high-resistivity carbon strips on top of the copper readout strips to improve spark-tolerance (The two layers of strips are separated by one 50μm layer of Kapton® Foil)

- The 4 readout layers have 1024 resistive strips each with a pitch of 415μm
  - 2x horizontal strips
  - 2x stereo strips inclined by ±1.5° to give info for the second coordinate

1 - Drift panel

2 - Read-out panel x2   eta strips

3 - Drift panel x2

4 - Read-out panel x2   stereo strips

5 - Drift panel

MMSW Installation in ATLAS

- Integration of pre-series Micromegas chamber (MMSW) into the ATLAS TDAQ infrastructure
  - Test of detector & electronics (VMM) under real ATLAS environmental conditions
  - Synchronization with ATLAS muon tracks
  - Event-by-event comparison of MMSW data with ATLAS data during RUN II


- Initially will be located in the scaffolding structure of the ATLAS cavern wall
  - Particles from Interaction Point (IP) at ~20° → micro-TPC angular tracking studies
- Relocation of chamber in one of the two Small Wheels during next shutdown

MMSW Installation in ATLAS
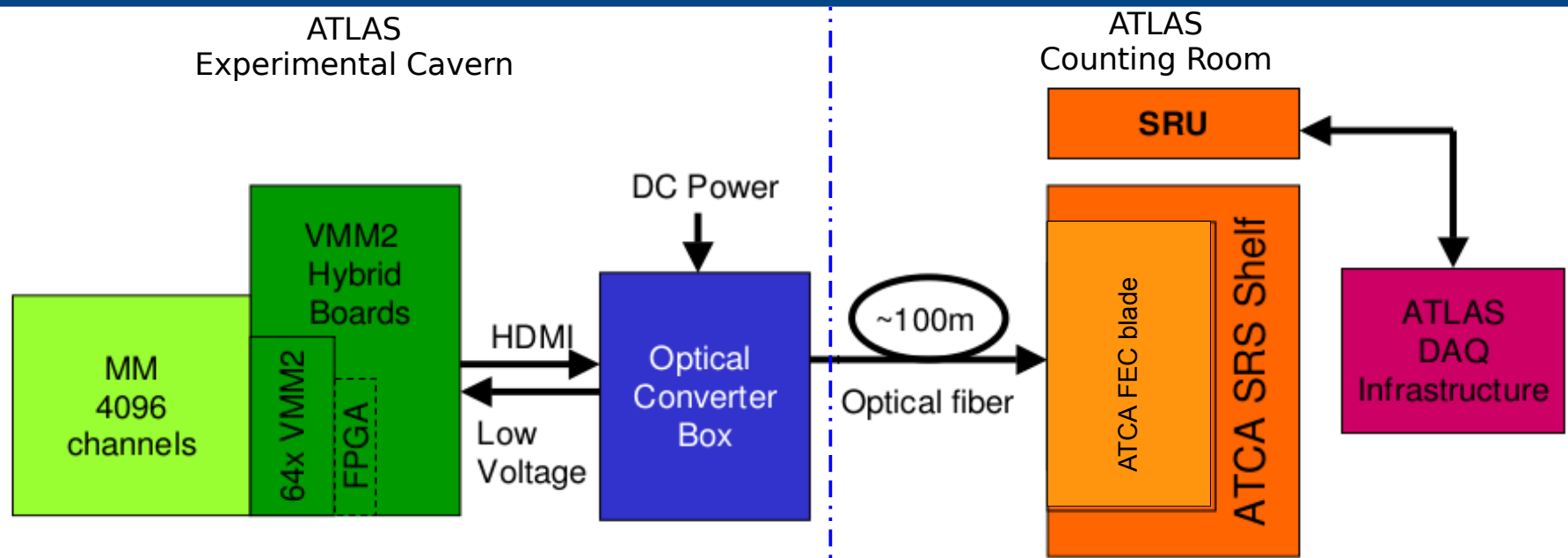
- Scalable Readout System developed within the RD51 collaboration successfully provides the readout of the MMSW prototype (Final NSW electronics under development)
  - Optical Converter (OC) box communicating with FEC blades via optical fiber, allowing to place the back-end electronics in a remote area (counting room) while the detector operates in harsh environment (cavern). An OC box itself is able to represent the functionality of a FEC card, allowing the installation of different mezzanine boards, depending on the frontend electronics in use *(under development)*
  - ATCA FEC blades used to distribute triggers and clock to readout chips, gather respective data, perform additional computing e.g. zero-suppression e.t.c

ATCA: Advanced Telecommunications Computing Architecture

ATLAS TDAQ chain
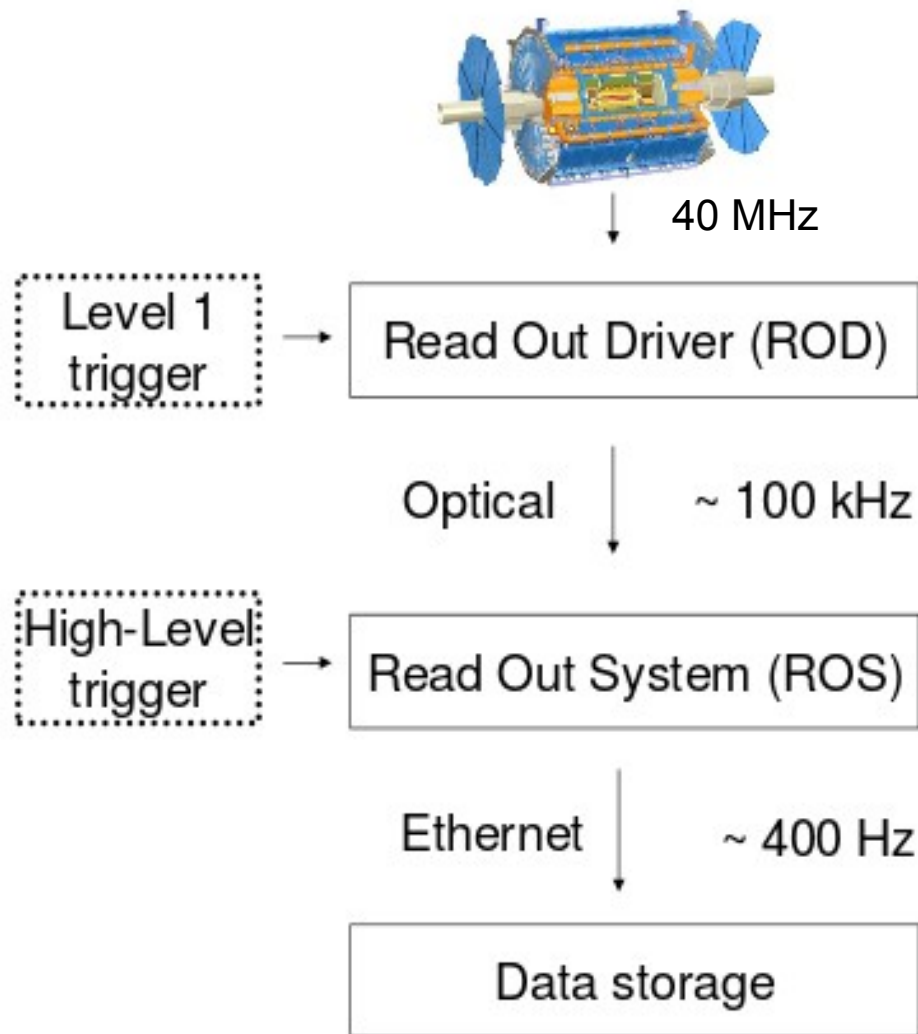
RUN II – New two-staged triggering mechanism to reduce initial collision rate of 40 MHz to ~400 Hz for final storage and analysis

Scalable Readout Unit (SRU)

Detector synchronization and data collection via **DTCC** (Data Trigger Clock and Control) links

SFP+ plugs

Event data is transferred to ROS pc via the ATLAS standard optical fiber **S-Link**

Xilinx Virtex6 FPGA:

customized firmware performing ATLAS like ROD event building

Busy signal generation in case of back-pressure from the ROS (Lemo plugs)

FPGA

Slow control commands for configuration of the SRS components via **GbE**

TTCrx (Trigger, Timing and Control) receiver to pick up LHC bunch crossing clock (synchronous operation), triggers and asynchronous data from ATLAS trigger network

RD51 Custom Unit
Interfaced to ATLAS

DAQ Configuration databases

For ATLAS:

CTP → L1A → LTPi → LTP → TTC → SRU

ROD BUSY

SRU → ROD fragments / S-Link → ROS → serve data → Data Collection Network

data request

slow control communication via UDP protocol

pc

For standalone:

L1A → LTP → TTC → SRU

SRU → ROD fragments / S-Link → ROS

slow control communication via UDP protocol

eos ← pc ← ROS
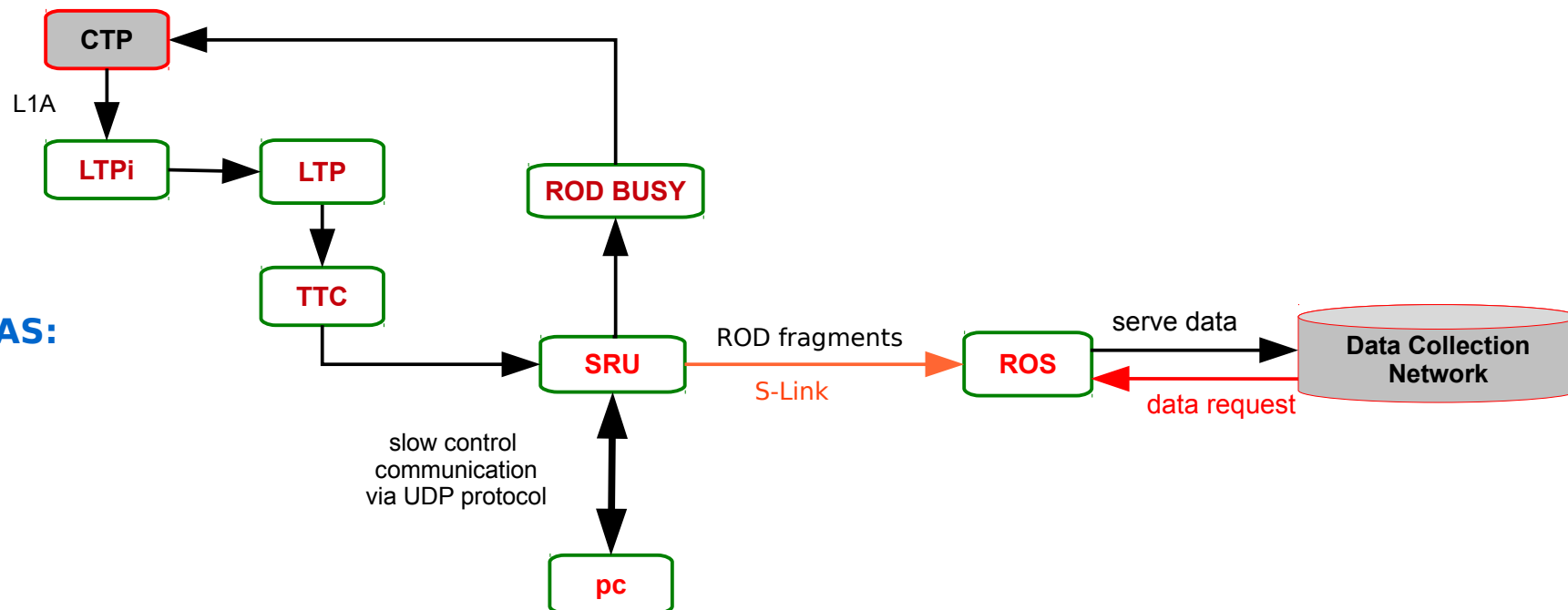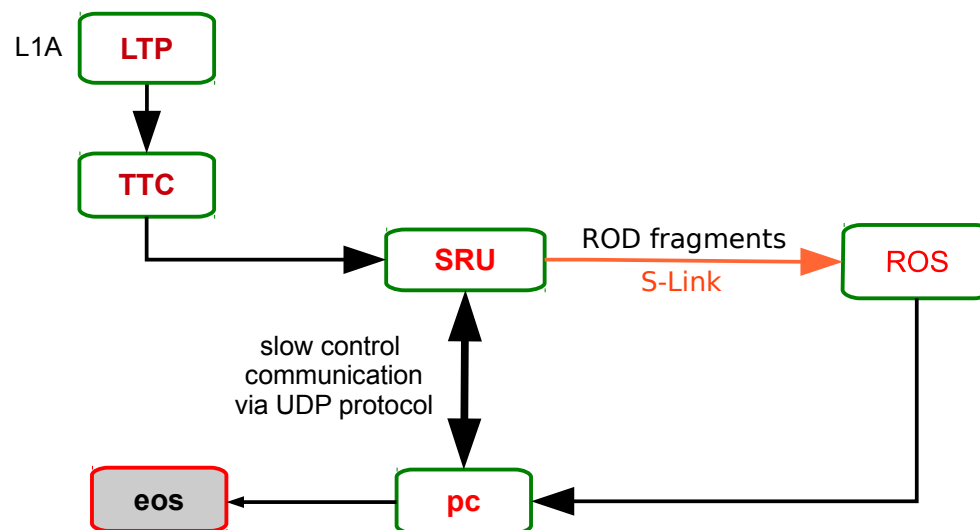
Integration of the MMSW into the ATLAS TDAQ Software

The MMSW DAQ supports the execution of recovery commands that can be issued by a human operator or by the software itself:

- A part of the readout that is blocking the trigger due to a fault can be excluded during RUNNING state **(Stop-less removal)**
- Re-align of ECR/L1ID counters if they went out of sync **(Resynchronization)**
- Complete restart and reconfiguration of the system during RUNNING in case the system is blocking the data acquisition **(TTC restart)**

SRU Performance
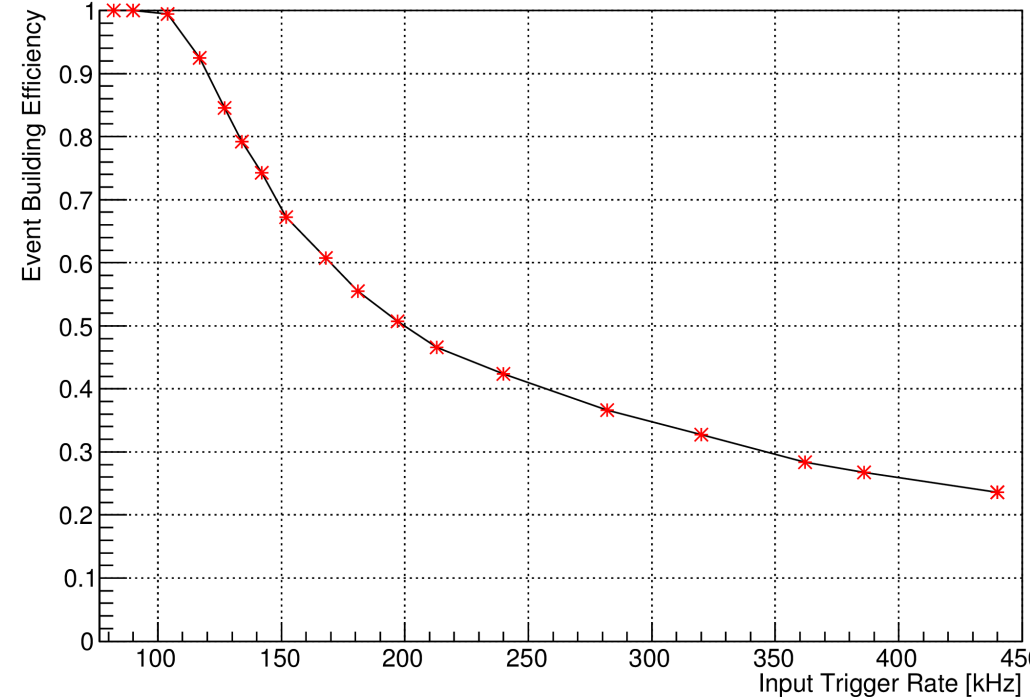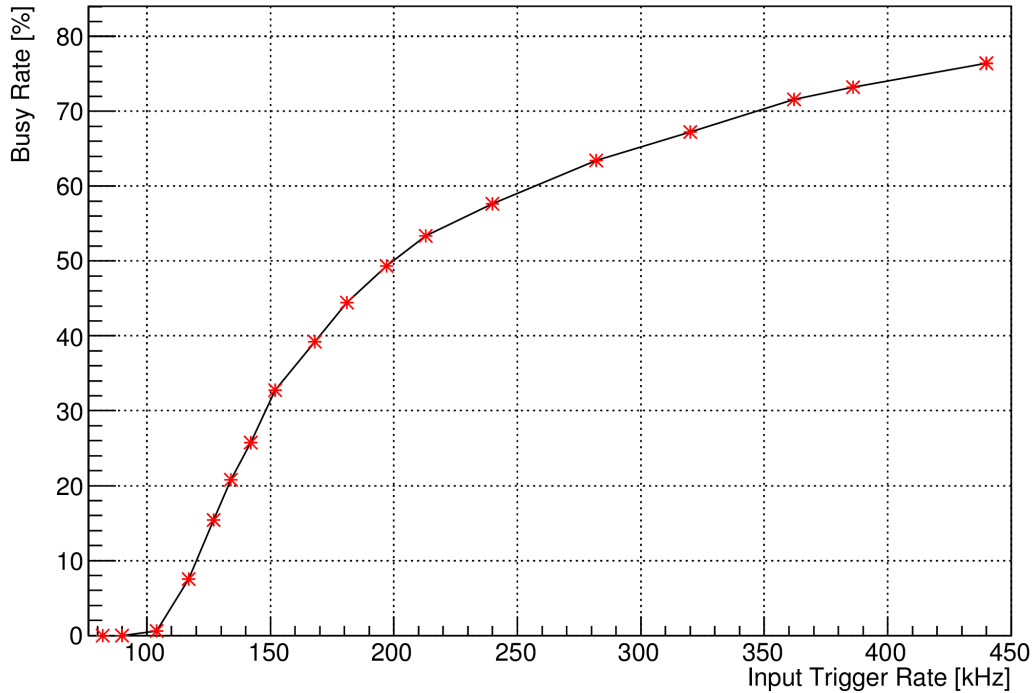
- Expected Level-1 trigger rate during RUN II is ~100 kHz
  - ROD performance depends on ROS back-pressure, all detectors need to raise "busy" in order not to loose events
  - SRU performance → below 1% at ~100 kHz

SRU times

DAQ Performance

Cosmics Run 254530 5/3/15
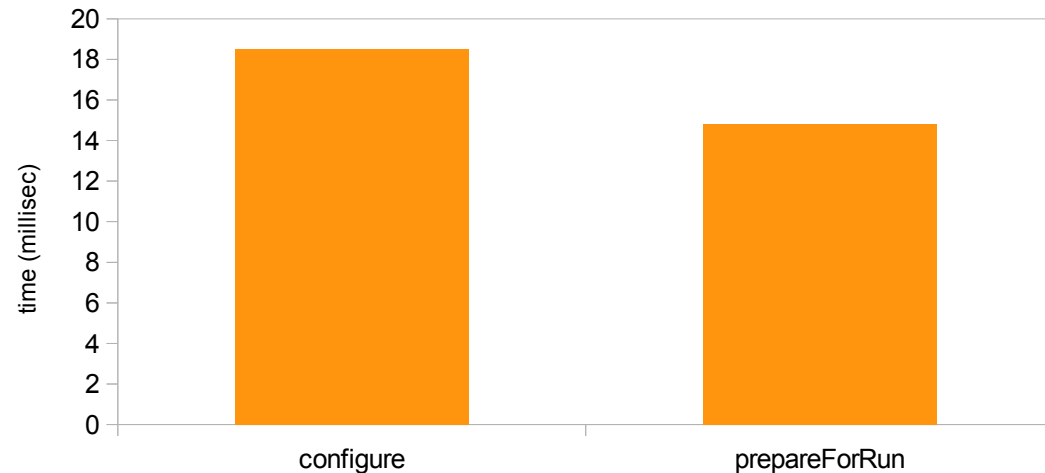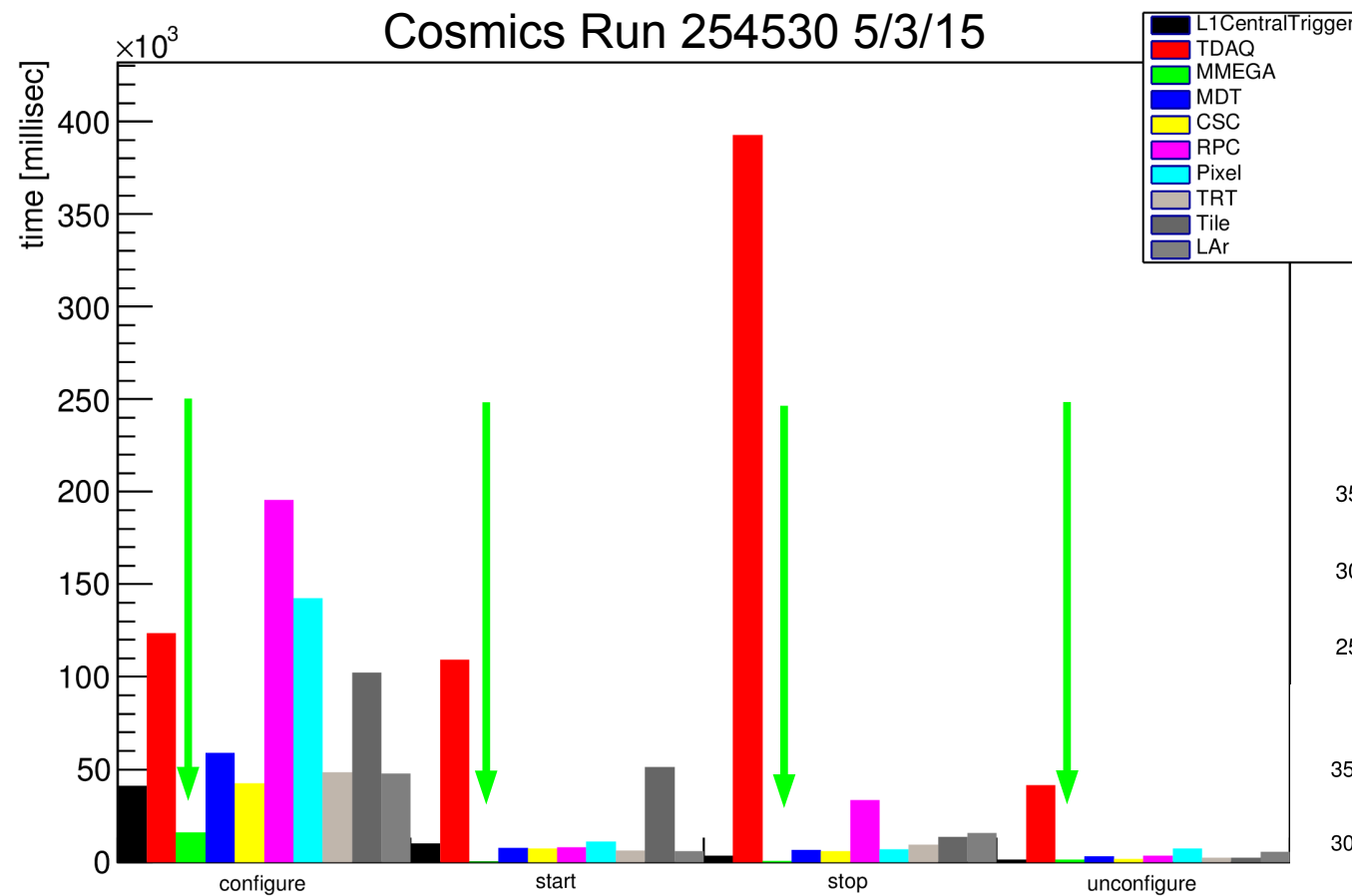
Bunch structure visible in data → TTC & DAQ integration works
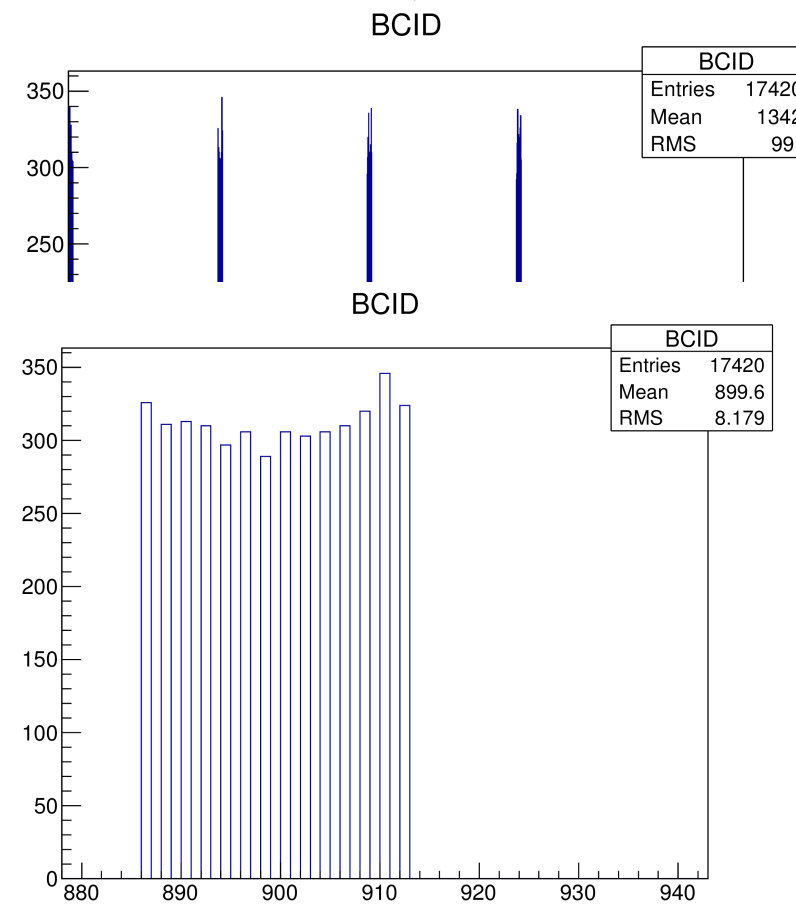
Summary

- A MicroMegas quadruplet prototype chamber with a structure similar to the one foreseen for the NSW has been built and tested in several test-beams during summer 2014
  - → will be installed and integrated into the ATLAS DAQ infrastructure during the RUN II period (2015-2017)
  - → OC box under development
  - → ATCA FEC firmware under development

- The MM DAQ system based on the ATLAS Online TDAQ Software has been developed and tested
  - → Two different configurations exist for both standalone and ATLAS partition
  - → Tested in the ATLAS TDAQ infrastructure successfully during cosmic combined runs & will be tested also during splash events until physics collisions start
  - → Recovery actions have been implemented and can be executed by the shifter or by the software itself

Thank you!

BACK UP SLIDES

Integration of the MMSW into the ATLAS DAQ System

VMM2 hybrid

analogue ASIC with digital output, 64 front-end channels, spark protected. Provides charge and timing measurements along with:

- The address of the first event in real time for trigger information
- Time-over-Threshold measurements with zero suppression

(BNL development)
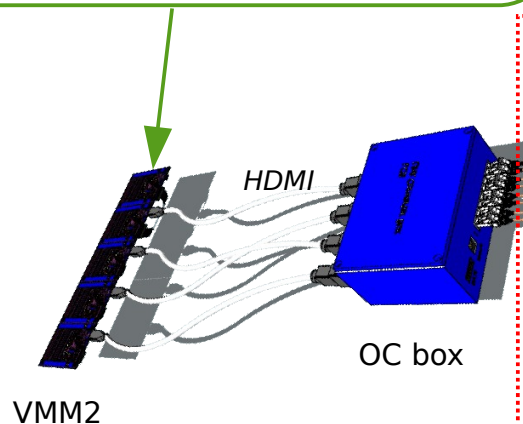
➡ *The ATCA based on high bandwidth fiber point-to-point technology was adopted the last years by many experiments and is about to replace VME off-detector equipment in the LHC experiments*

Scalable Readout System

(RD51 collaboration)

HDMI

OC box

VMM2

R.T.M.   BLADE

DDR3 FPGA   Mezzanine 1

DDR3 FPGA   Mezzanine 2
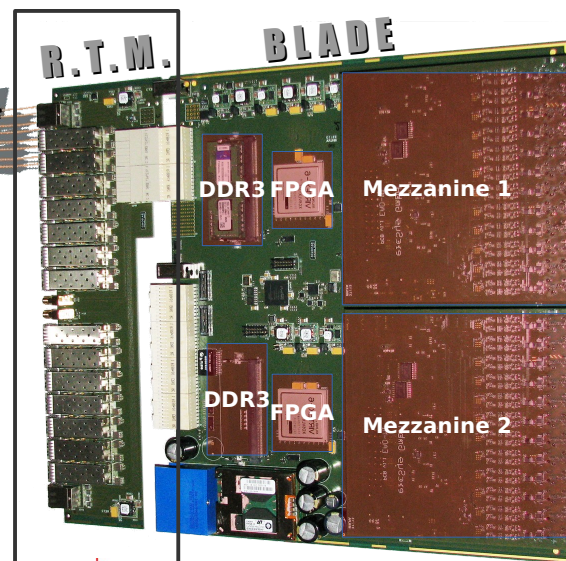
Rear Transition Module (RTM) I/O extension card

- 2 x 7 SFP+
  (up tp 5Gbps at the moment)
- 2 x Rj45 (DTCC)
- 2 x NIM (LEMO 00)

Blade main board

- 2 x Virtex-6 FPGA
- 2 x DDR3 up to 4GB
- 2 x Mezzanine ports (work independently)
- ➡ *The 2 FPGAs can also be interconnected*

Mini ATCA SRS self

SRU

DTTC

ATLAS Combined Cosmic Run

TTC restart test

Busy connection to CTP

Controllers Times

Cosmics Run.Num:254530 5/3/15
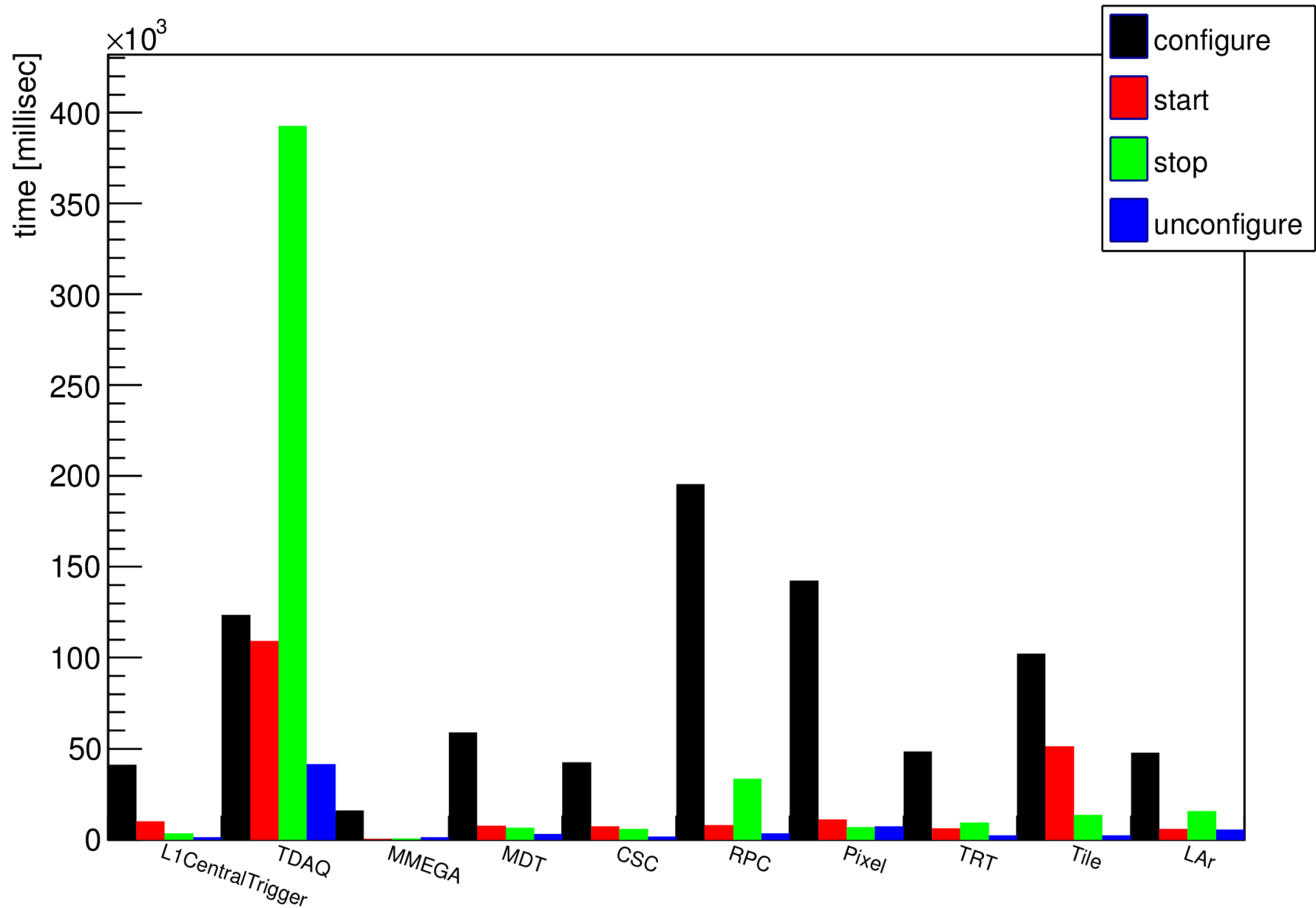
Expert Panel

SRU registers values, port:6010

Address	Value
0x00	241b
0x01	1
0x02	6b0001
0x03	8034f21
0x04	0
0x05	0
0x06	34ab6c4
0x07	60004000
0x08	0
0x09	0
0x10	21b58f
0x11	21b59a
0x12	1
0x0a	61a7f01
0x0b	1
0x0c	3fa2c
0x0d	0
0x0e	ff1000
0x0f	55256270

Commands to MMEGA ROD

HARDWARE ERROR

RECOVER HARDWARE

ASSERT BUSY

RELEASE BUSY

GET NEW REG VALS