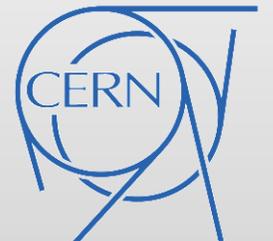
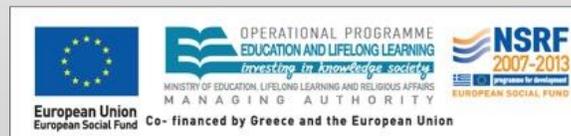


Level-1 Data Driver Card of the New Small Wheel ATLAS experiment

Panagiotis Gkoutoumis
National Technical University of Athens

HEP 2015, Athens

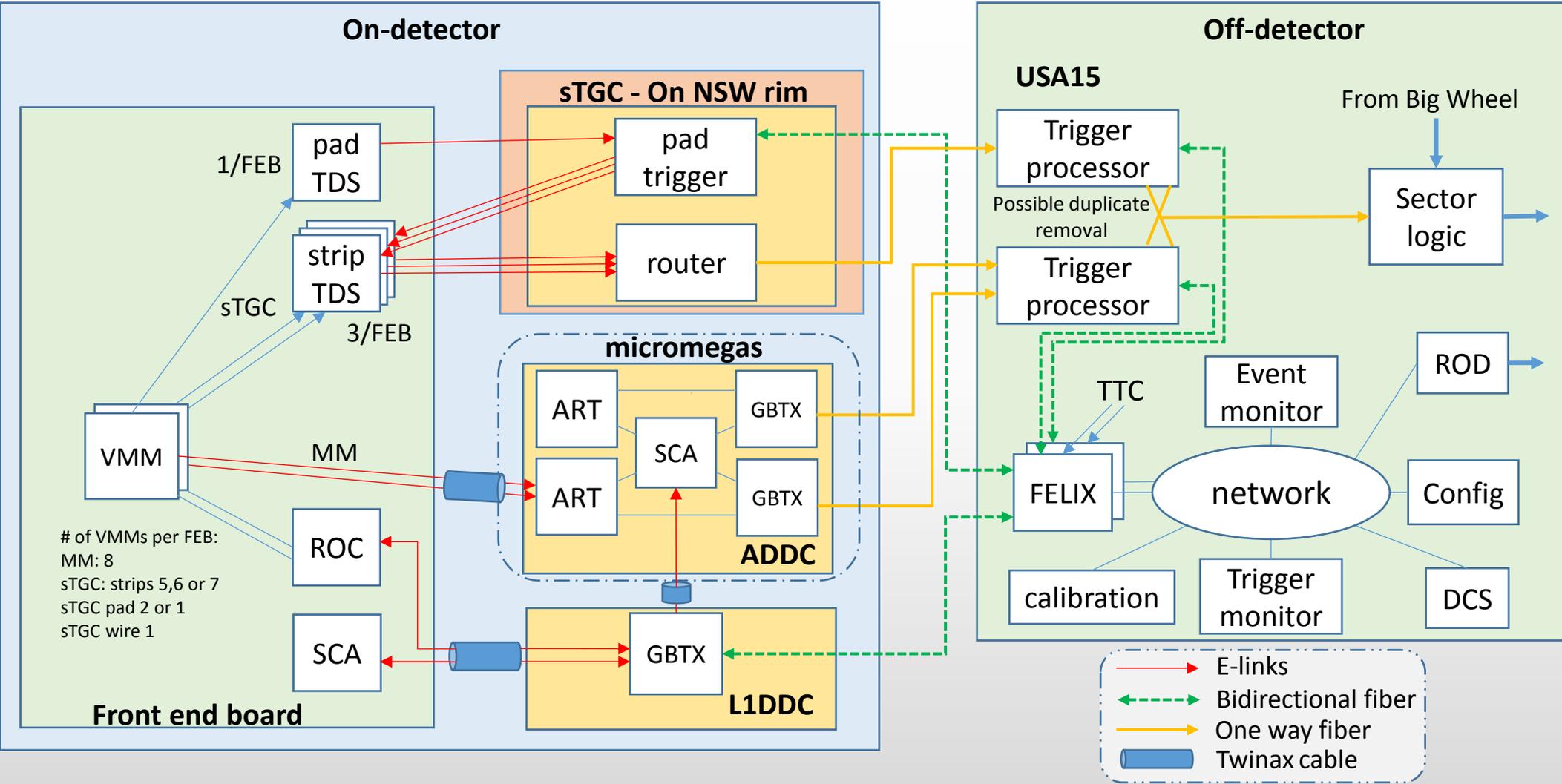
18/04/2015



Overview

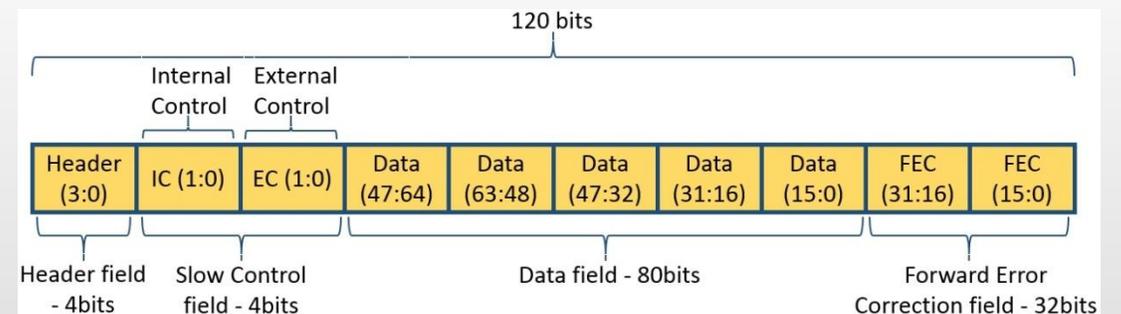
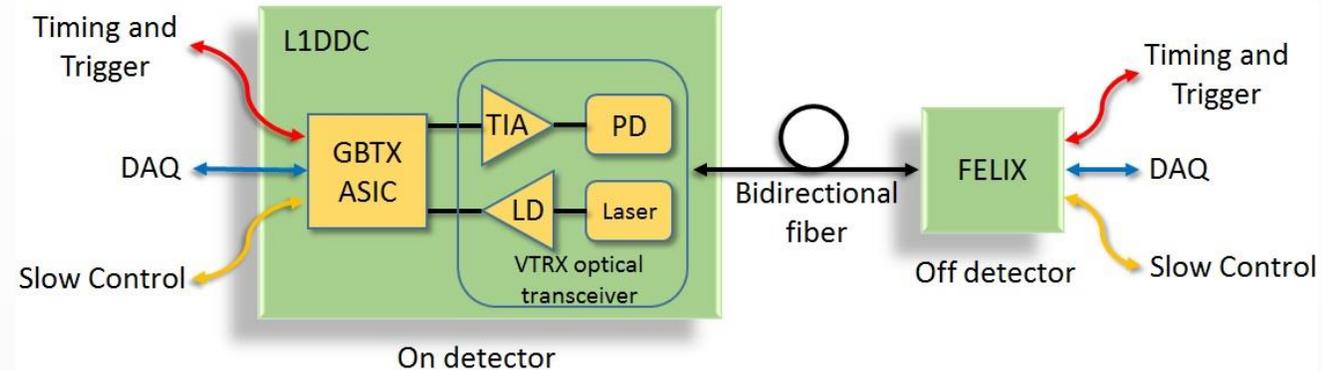
- NSW electronics
- L1DDC
 - General description
 - Connectivity
 - Rates
 - Placement
- L1DDC prototype 1
- Roadmap to L1DDC prototype 2
- Summary

NSW electronics trigger and dataflow



L1DDC connectivity

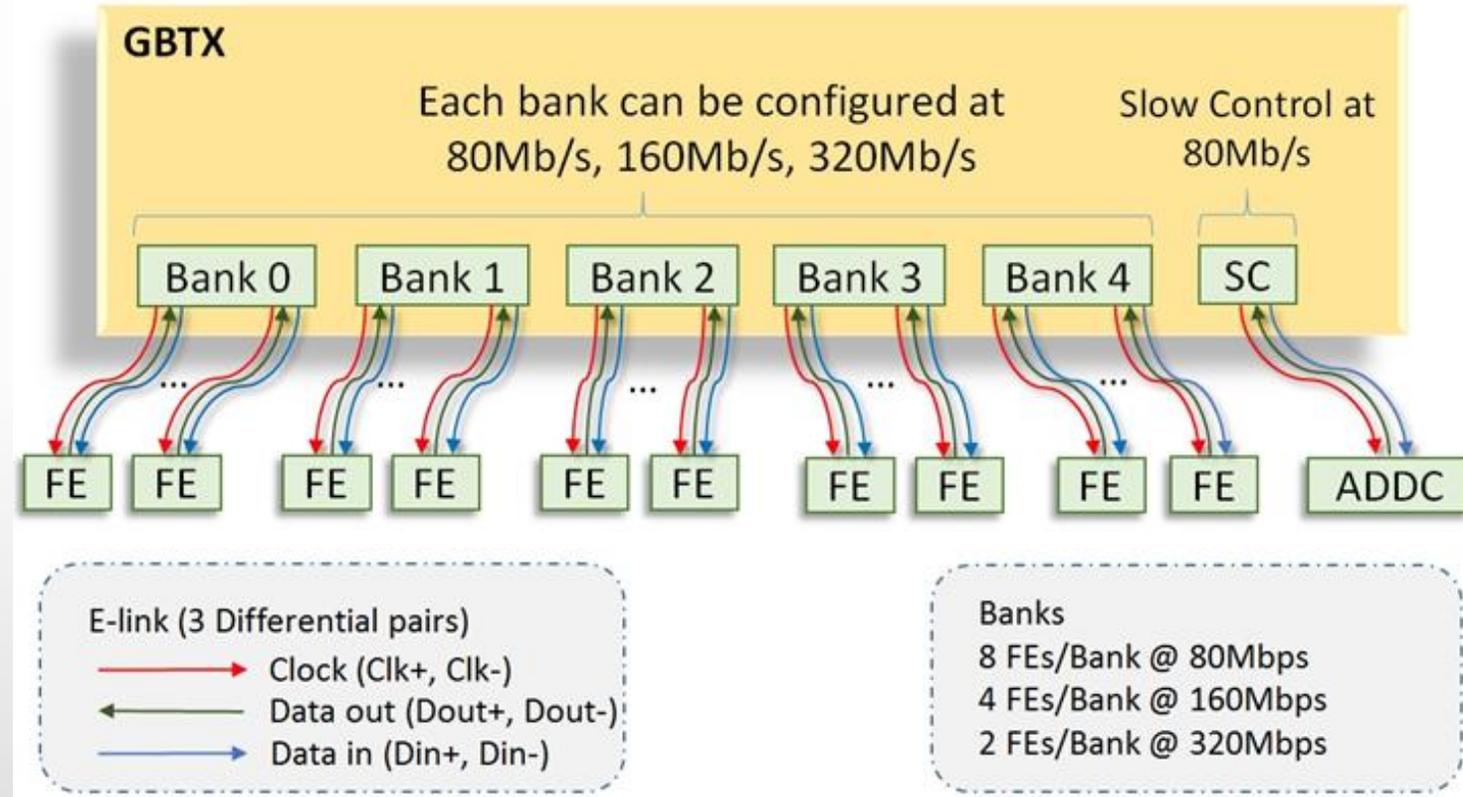
- 3 distinct paths to the front ends through one bidirectional link
- DAQ data
 - Level-1 data (Time, charge and strip address)
 - Configuration data
- ASICS
 - GBTX
 - GigaBit TransImpedence Amplifier (GBTIA) – Photo Diode
 - GigaBit Laser Diode (GBLD)) - Laser
- Line rate 4.8Gbps
- 1 frame of 120bits @ 40MHz (25ns)
 - Header 4 bits
 - Slow control 4 bits
 - Data 80 bits
 - FEC 32bits (2 interleaved Reed-Solomon encoding)
- Error correction and error detection
 - Up to 16 consecutive corrupted bits can be corrected
- User bandwidth 3.36Gbps



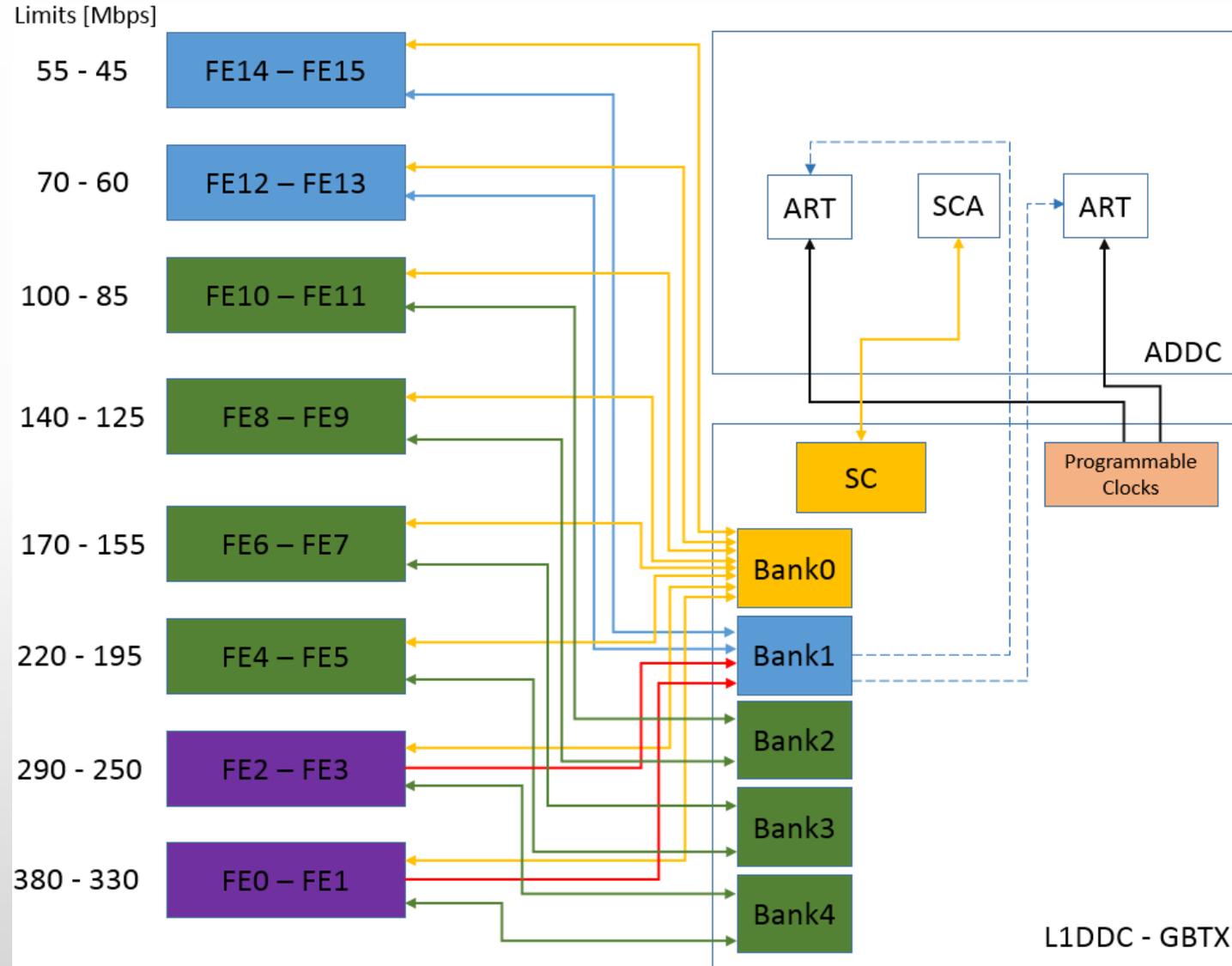
Frame format

GBTX ASIC Connectivity

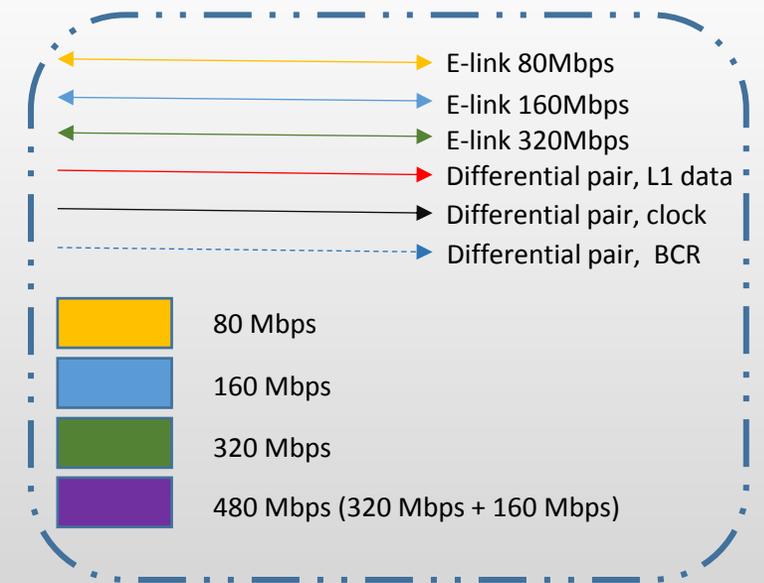
- 1 e-link has 3 differential pairs: Clock, Data out, Data in
- Up to 40 front-ends can be connected to 1 GBTx combined in 5 banks
- Each bank can support
 - 8 front ends @ 80Mbps
 - 4 front ends @ 160Mbps
 - 2 front ends @ 320Mbps
- Each bank can be configured at different rate
- 1 L1DDC is connected to 8 micromegas FEs and 3 sTGC FEs
- 1 cable for FE to L1DDC connection
 - 1 e-link for the ROD
 - 1 e-link for the SCA
- Slow Control channel @ 80Mbps dedicated to ADDC
- E-links use Scalable Low-Voltage Signaling (SLVS), $V_{cm} = 0.2V$, swing 200mV



L1DDC connectivity with the MMFE8 and ADDC boards



- SCA ASIC will be added to the ADDC board
 - Slow Control channel of the GBTX will be used for the configuration of the SCA.
- 2 extra differential pairs (clocks) will be send from the L1DDC to the ADDC
 - Either from the 8 programmable clocks of GBTX.
 - Either form the two spares of the bank1.



L1DDC

- Different designs

- Micromegas
 - 200mm x 50mm
 - 9 mini SAS connectors (8 for FEs, 1 for ADDC)
- sTGC
 - 90mm x 50mm
 - 3 mini SAS connectors (3 for FEs)

- Voltage levels

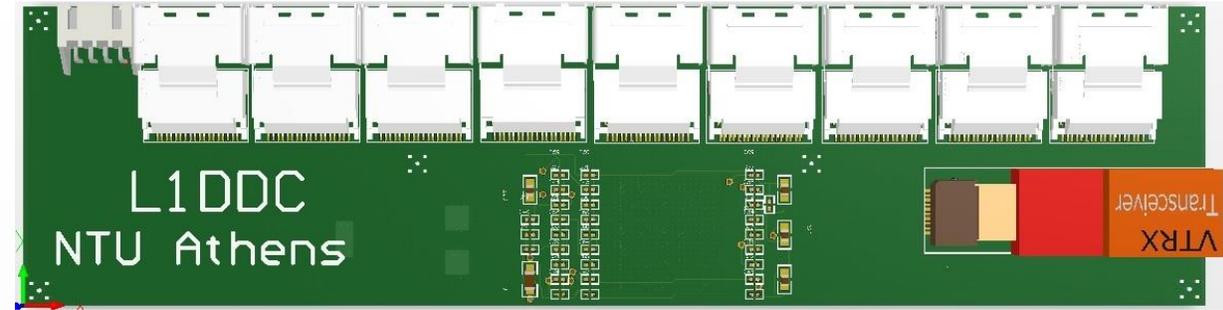
- 2.5V Digital (VTRX)
- 1.5V Analog (GBTX)
- 1.5V Digital (GBTX)

- Components

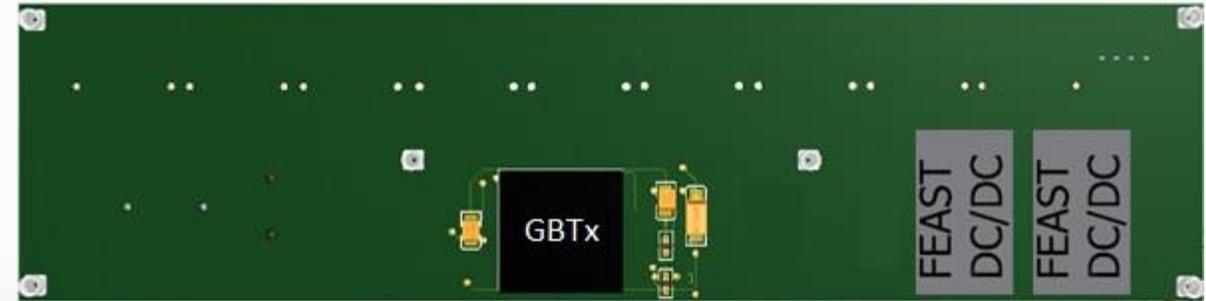
- GBTx ASIC, VTRX optical transceiver, 2 x FEAST DC-DC converter
- Power connector - Molex 0015912025
- Total power consumption: 3.5Watts (estimated)

- 1024 L1DDC boards

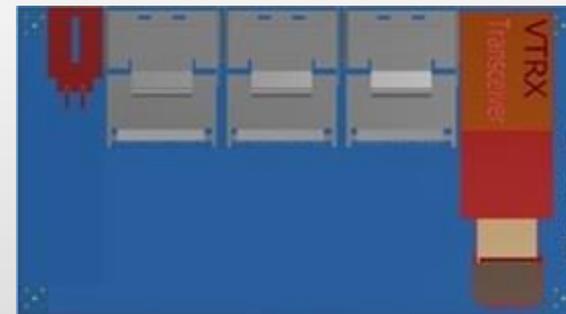
- 16 front ends/plane
- 1 L1DDC serves 8 front ends => 2 L1DDC/plane
- 16 planes/sector -> 16 sectors/wheel -> 2 wheels in NSW



Top side of micromegas L1DDC



Bottom side of micromegas L1DDC



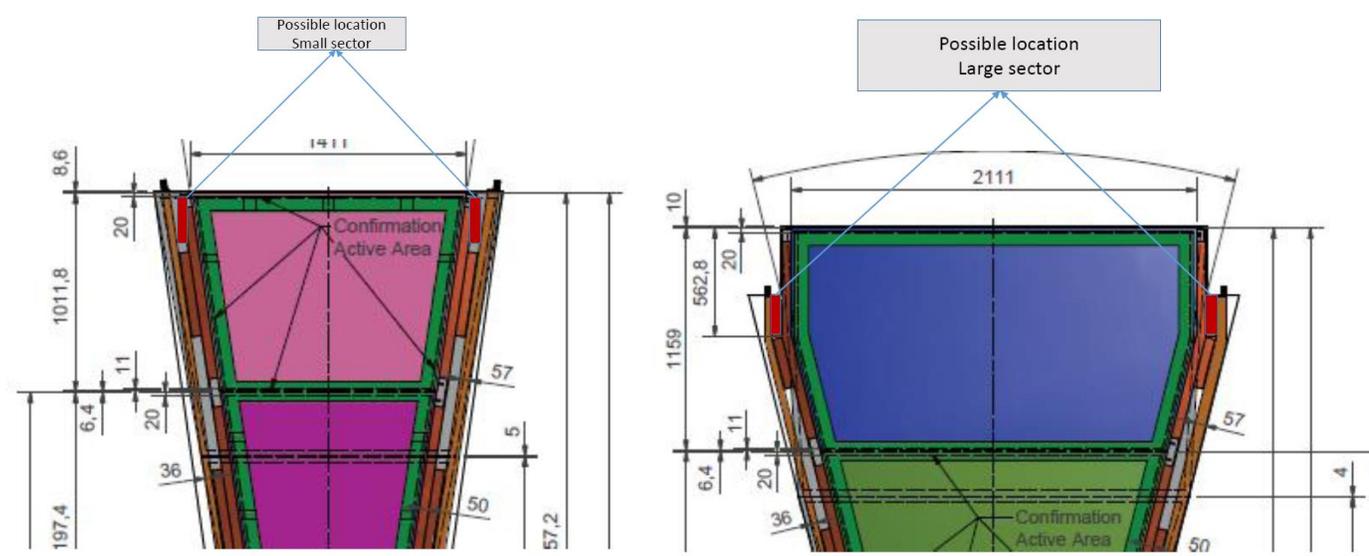
Top side of sTGC L1DDC



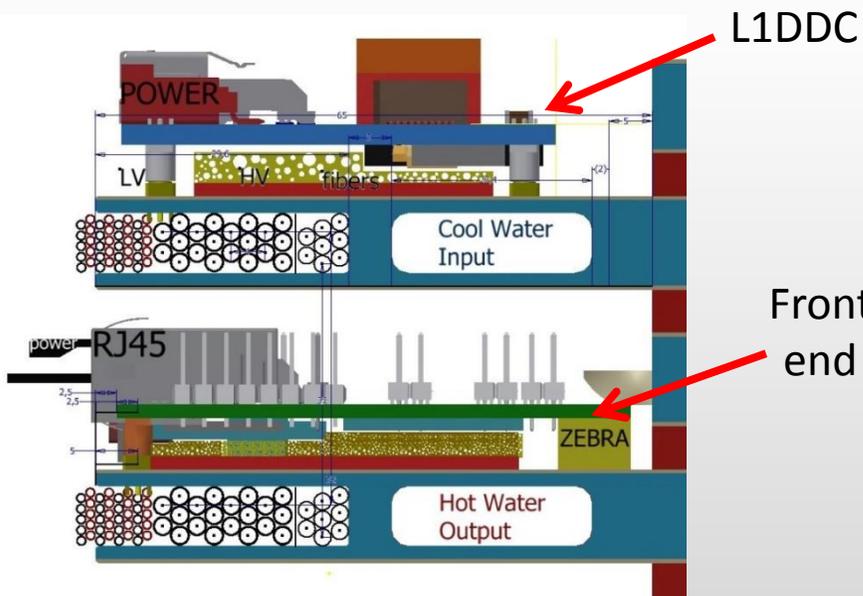
Bottom side of sTGC L1DDC

L1DDC placement

- L1DDC will be placed radially on both sides of micromegas and sTGC detectors
- 1 L1DDC will serve the 8 front ends of the one side of each plane
- For the micromegas L1DDC will be placed on the center to minimize the cable length
- Elastic thermal foam will be used for better connectivity to the cooling channel

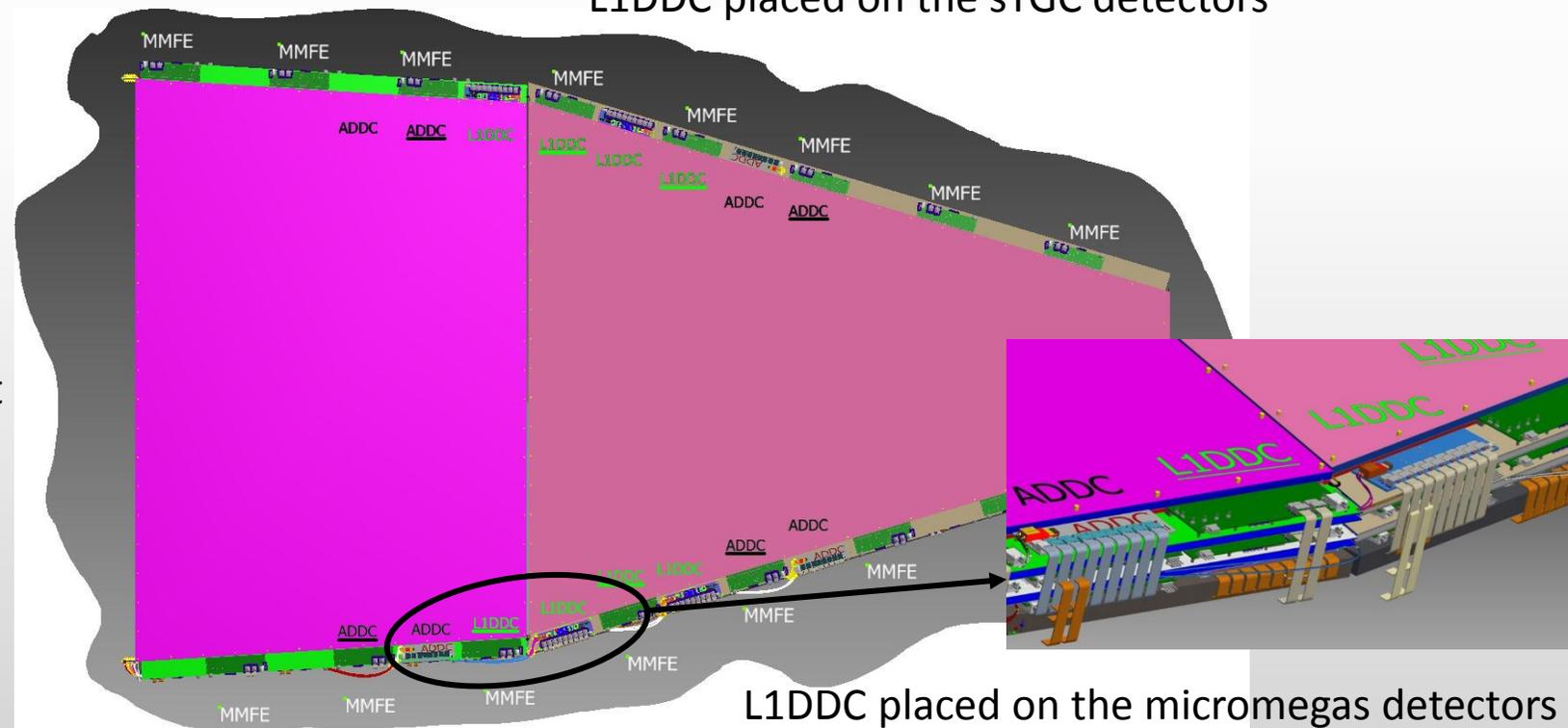


L1DDC placed on the sTGC detectors



3D representations by A. Koulouris

18/4/2015



L1DDC placed on the micromegas detectors

HEP 2015

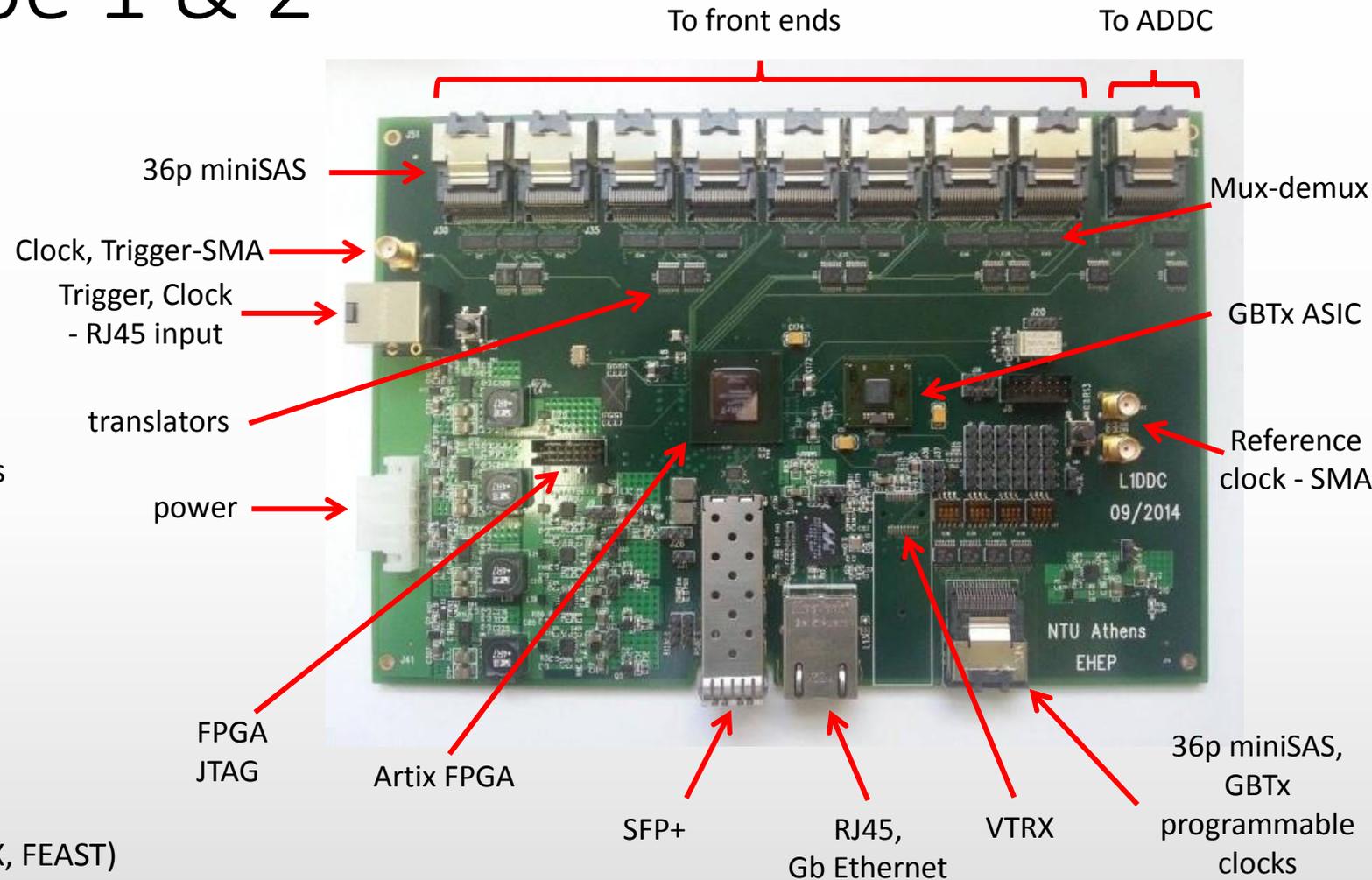
L1DDC - Prototype 1 & 2

• Prototype 1

- Already fabricated
- Size 210mm x 144mm
- Layers used : 14
- Alternative paths in case of GBTX failure
- Input voltage 3.6V - 42V
- GBTx, GBTIA & GBLD (VTRX) ASICs
- Xilinx FPGA Artix7 - xc7a200t-3FBG484
- SFP+, Gigabit Ethernet, VTRX, miniSAS 36p, SMAs
- Still in debugging process
- Board is functional
- No radiation tolerant board

• Prototype 2

- Design in progress (same as final board)
- Size 200mm X 50mm
- 12 Layers will be used
- Input voltage 5V - 12V
- Use only radiation hard components (GBTx, VTRX, FEAST)
- Can be tested in radiation and magnetic fields
- Estimate final power consumption



Top side of L1DDC prototype-1 board

Summary

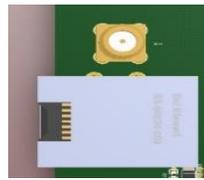
- L1DDC collects the Level-1 Data and distributes the TTC data to the front end and ADDC boards
- L1DDC is a fully radiation tolerant board
- Fulfills all ATLAS NSW upgrade requirements
- Fully compliant with LHC rates
- Has SEU mechanisms to assure signal integrity
- Different L1DDC boards will be fabricated for micromegas and sTGCs detectors

Thank you

- Questions?

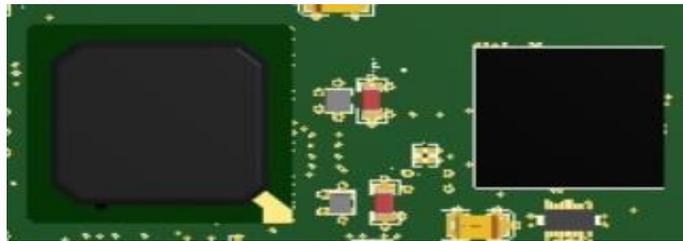
Backup Slides

SMA - Trigger
RJ45 - Trigger and Clock

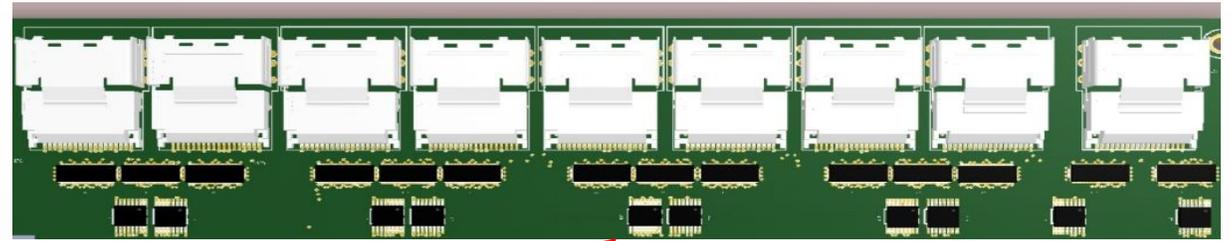


Artix-7

GBTx

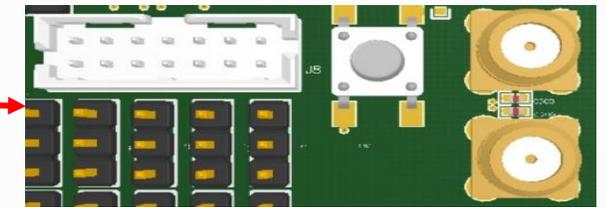


eLinks

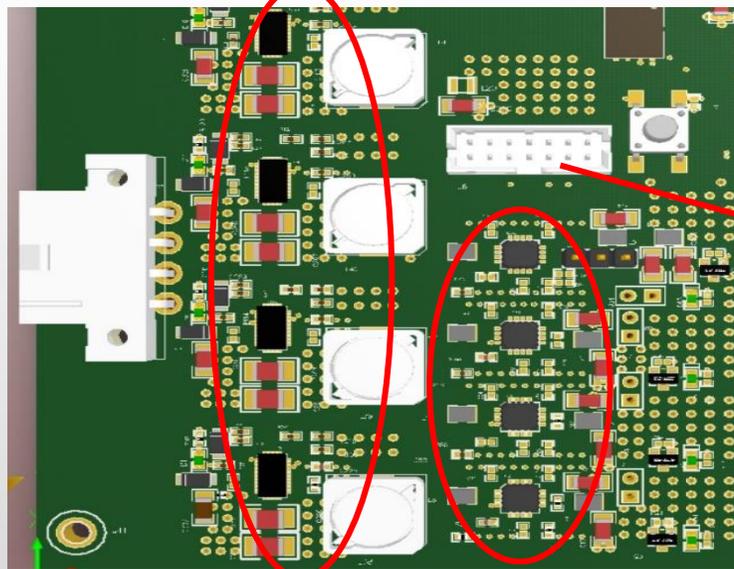


SMA - Reference clock

JTAG



DC-DC

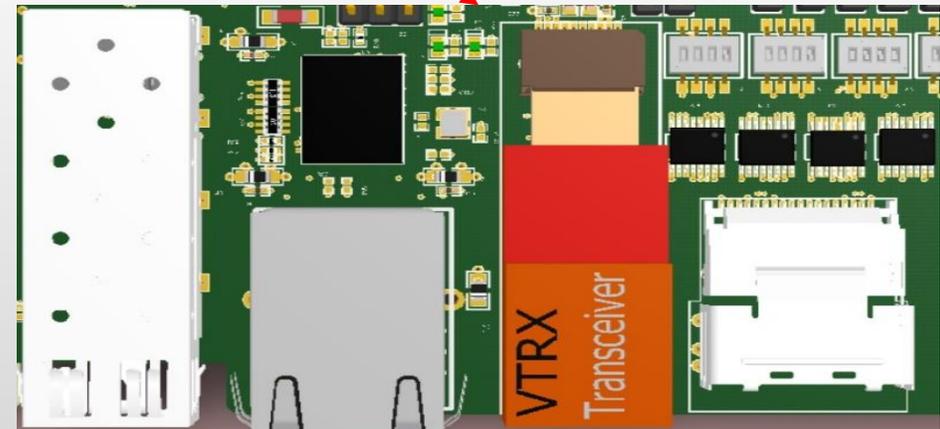


JTAG



Power in

LDOs



Clock outputs

SFP+

RJ45

VTRx

Technical characteristics

- **FPGA Artix 7**
 - Configures the GBTx
 - Implements the I2C protocol for the communication with the configuration registers
 - Reads and sends the data in case of GBTx failure
- **Inputs & outputs**
 - Detector side
 - Elinks (LVDS or SLVS differential)
 - Counting room side
 - VTRX optical transceiver
 - 10/100/1000 ethernet
 - SFP
 - SMA
- **Anything to LVDS translators (SN65LVDT122)**
 - Convert GBTx output (SLVS) to LVDS standard

Technical characteristics

- **Voltages Levels**

- 1.5V Digital (GBTx)
- 1.5V Analog (GBTx)
- 2.5V Digital (VTRx, FPGA) Direct from LTM4619
- 3.3V Digital (efuses, SN65LVDT122) Direct from LTM4619
- 1.2V Analog MGTAVTT (FPGA)
- 1.0V Analog MGTAVCC (FPGA)
- 1.0V Digital VCCINT, VCCBRAM (FPGA)
- 1.8V Digital VCCAUX (FPGA)

- **4 LT8612 DC-DC Converters (replaces LTM4619)**

- Single 6A output

- **Use of 6 ADP1755 LDOs to step down the voltage**

- Single output @ 1.2A

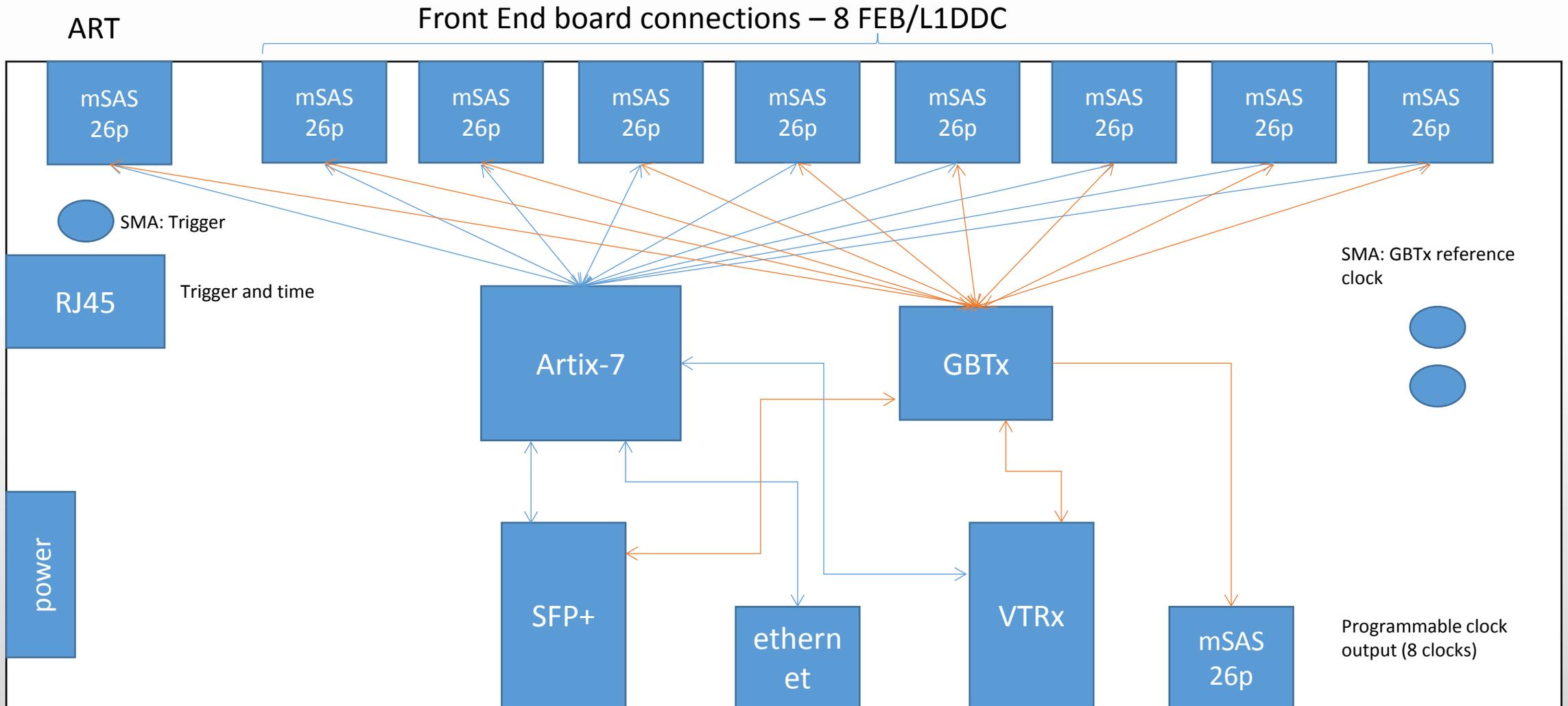
- **JTAG port**

- **SMA & RJ45 for reference clock and trigger**

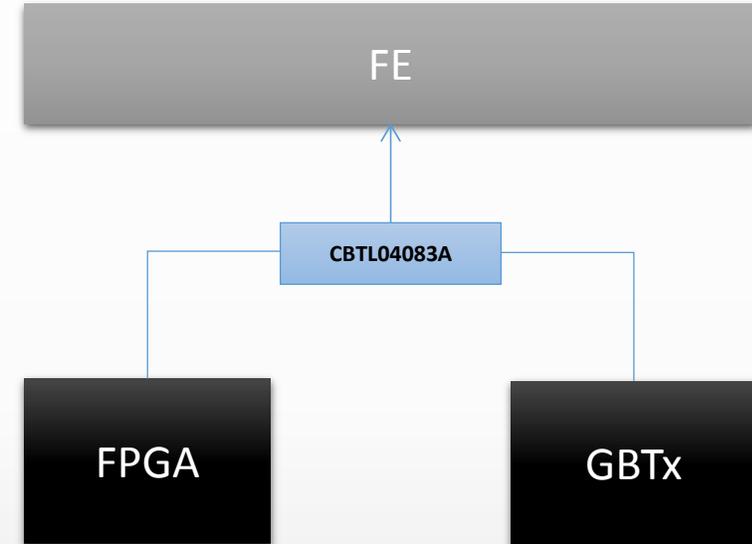
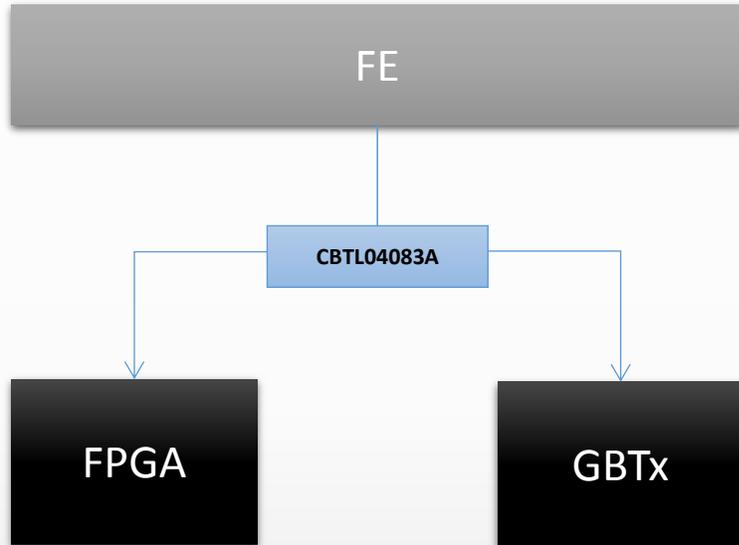
Differential impedance

PCB Stack Up				Impedance			
Layer	Type	Thickness (mil)		Single ended	OHM	Differential	OHM
Top side solder mask		0,5 mils					
L1	Top	copper + plating	1,4 mils			4/4/4mils · 100Ω +/- 10%	97.48Ω
		prepreg	4 mils				
L2		copper	0,7 mils				
		core	8 mils				
L3		copper	0,7 mils			4/4/4mils · 100Ω +/- 10%	99.24Ω
		prepreg	8 mils				
L4		copper	0,7 mils				
		core	6 mils				
L5		copper	0,7 mils			4/4/4mils · 100Ω +/- 10%	97.85Ω
		prepreg	5 mils				
L6		copper	0,7 mils			4/4/4mils · 100Ω +/- 10%	97.85Ω
		core	6 mils				
L7		copper	0,7 mils				
		prepreg	4 mils				
L8		copper	0,7 mils				
		core	6 mils				
L9		copper	0,7 mils			4/4/4mils · 100Ω +/- 10%	97.85Ω
		prepreg	5 mils				
L10		copper	0,7 mils			4/4/4mils · 100Ω +/- 10%	97.85Ω
		core	6 mils				
L11		copper	0,7 mils				
		prepreg	8 mils				
L12		copper	0,7 mils			4/4/4mils · 100Ω +/- 10%	99.24Ω
		core	8 mils				
L13		copper	0,7 mils				
		prepreg	4 mils				
L14	Bottom	copper + plating	1,4 mils			4/4/4mils · 100Ω +/- 10%	97.48Ω
Bottom side solder mask		0,5 mils					
TOTAL			90,2 mils				
			2,291 mm				

L1DDC functionality



Send & receive data (FE side)



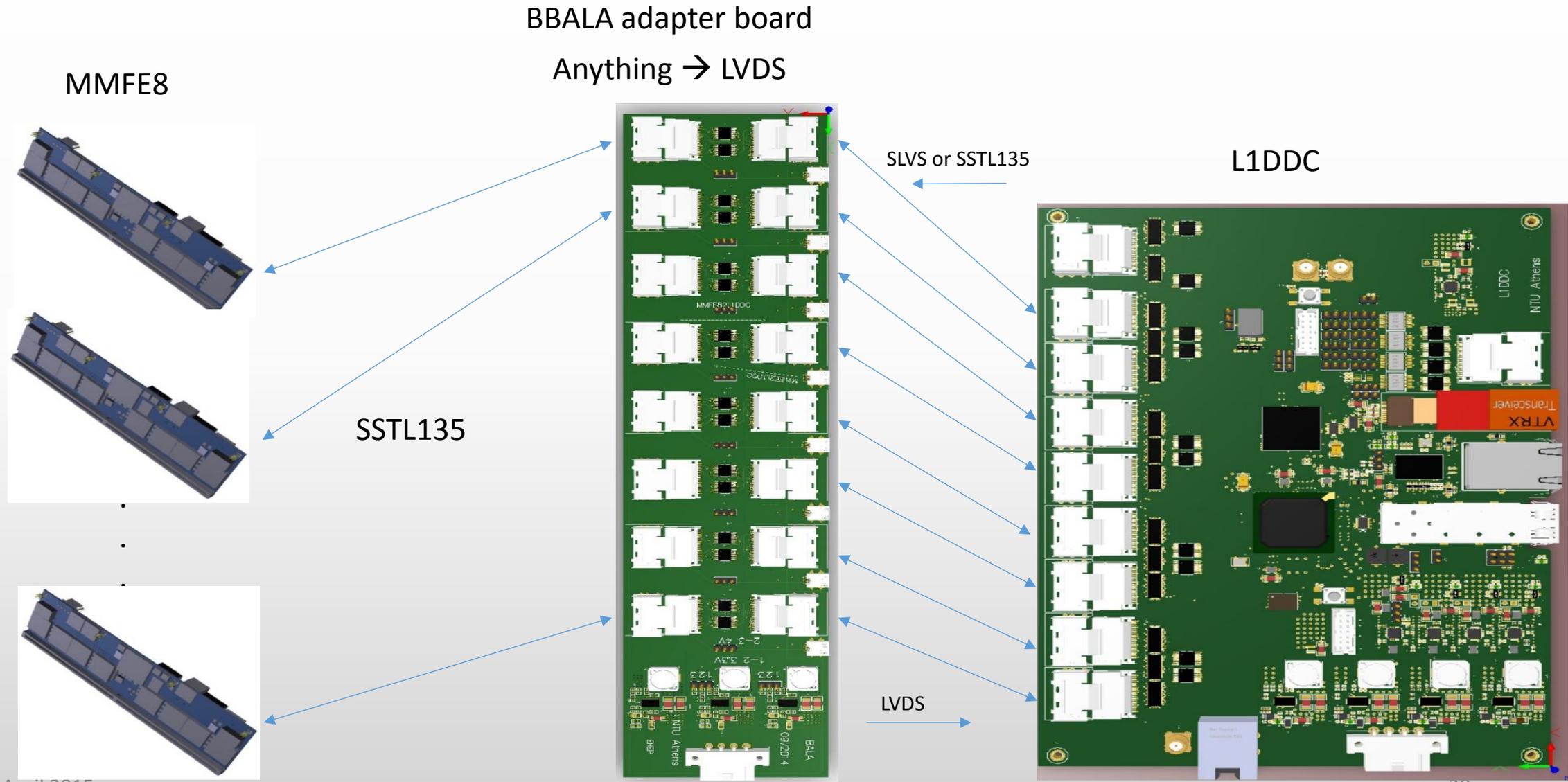
2 alternative paths to read and send the data

- From FPGA in case of failure of GBTx
- Directly from GBTx

CBTLO4083A PCI Express Gen3 switch up to 8.3Gb/s

- Low intra-pair skew: 5 ps typical
- Low inter-pair skew: 35 ps maximum

Connection with Mini2 Bucharest Board

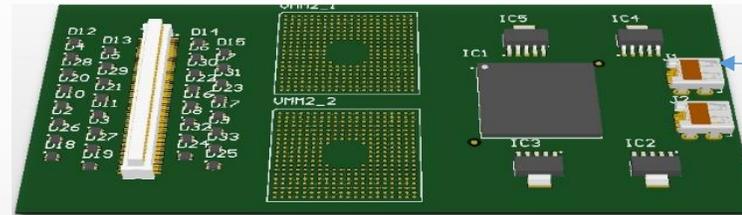
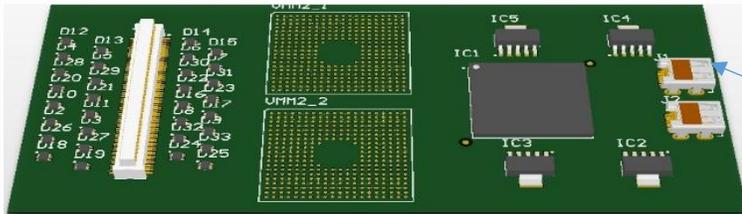


Connection with Mini2 Bucharest Board

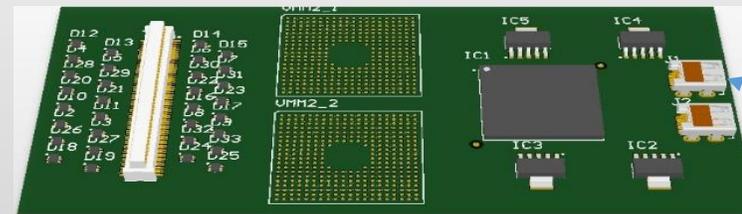
BBALA adapter board

LVDS ← Anything

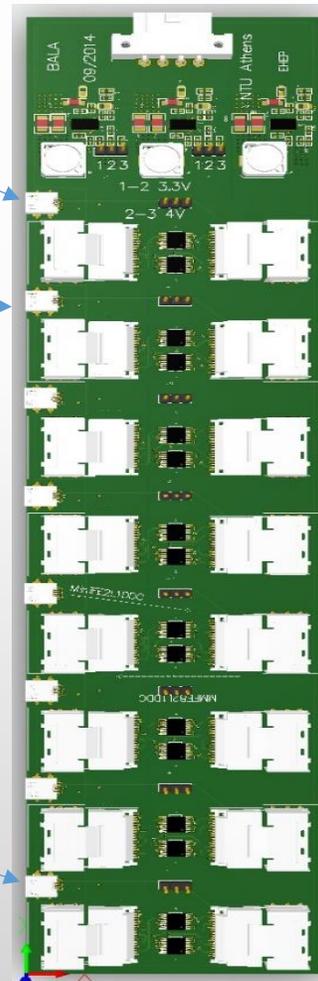
mini2



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•
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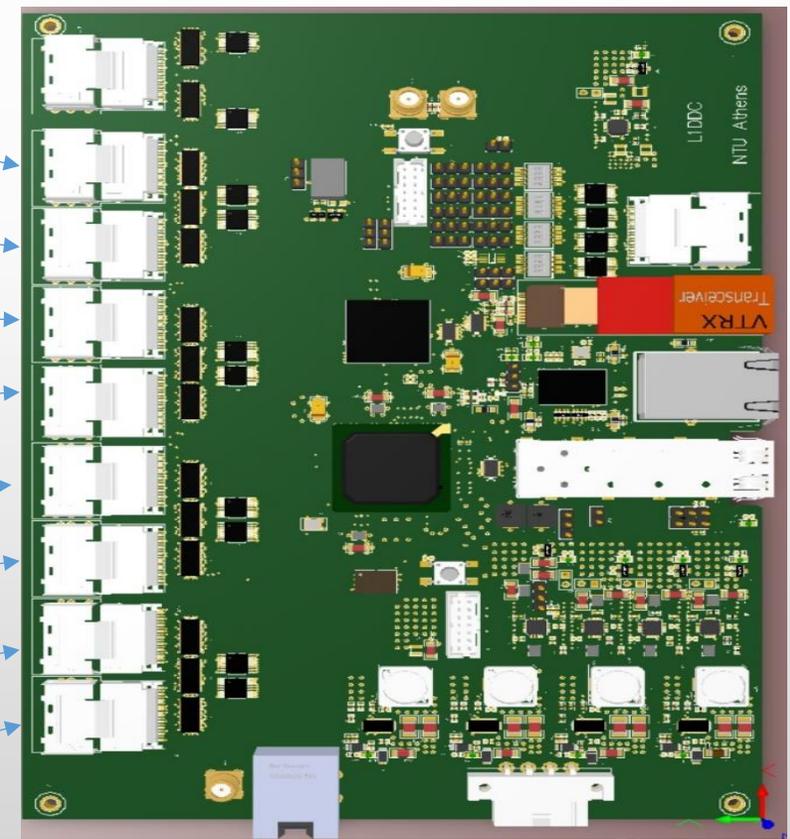


LVDS

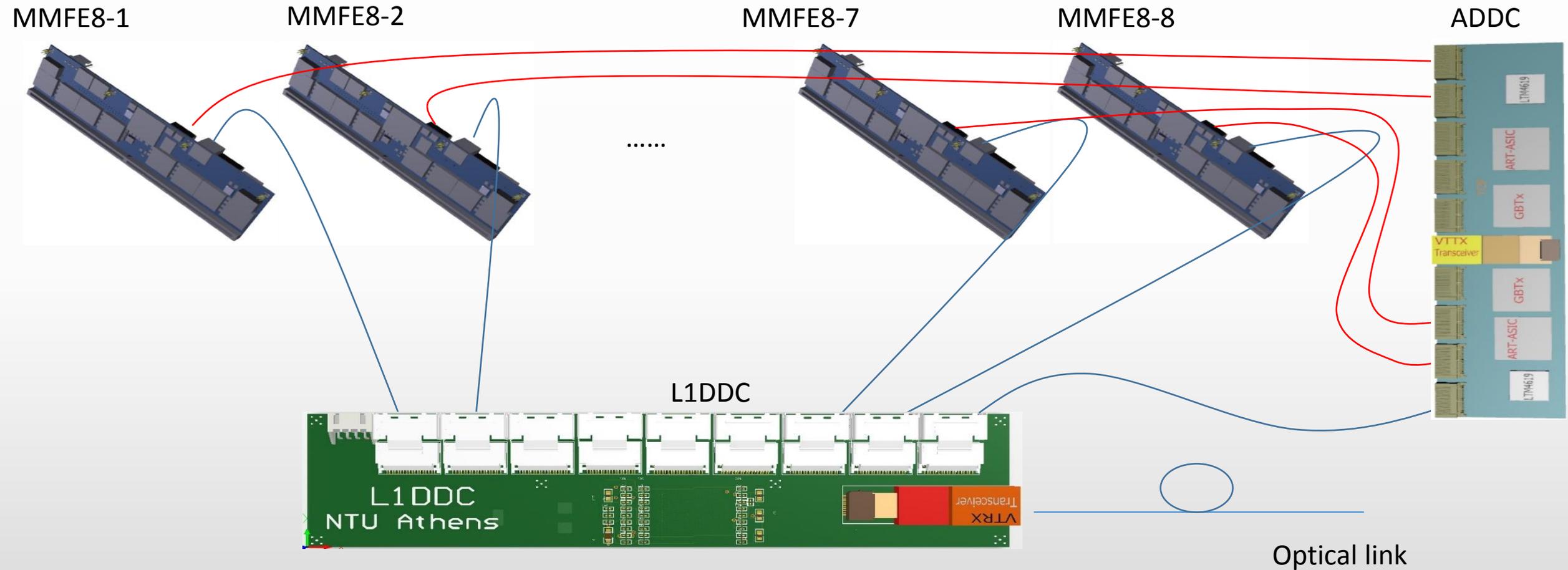


LVDS-SLVS-SSTL135

L1DDC

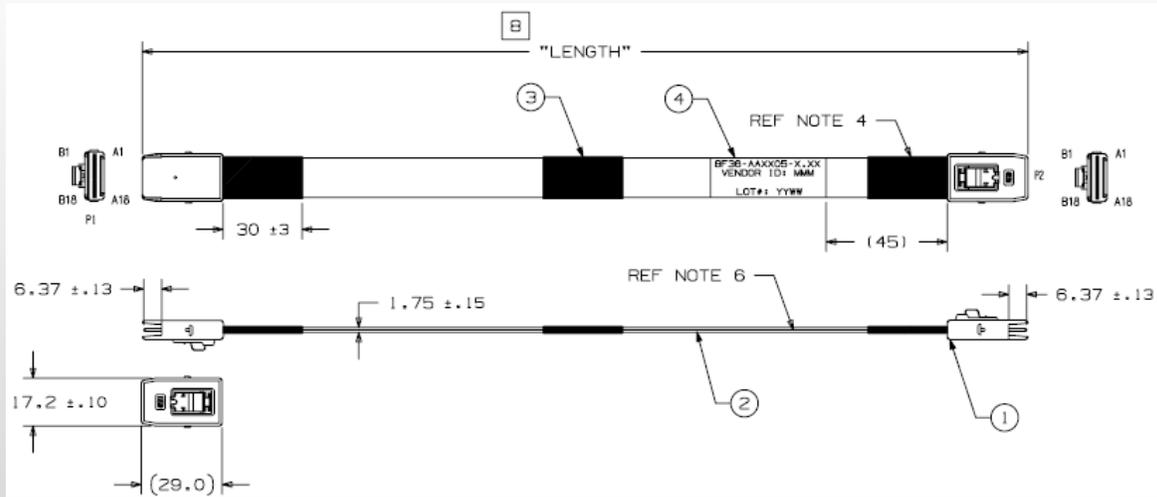


Connectivity: MMFE8 – L1DDC – ADDC



Twinax cables

- 3M mini SAS cables
- 36p positions
- Part No 8F36-AAA105



PINOUT 1

BACKPLANE-TO-CONTROLLER

P1		P2	
A1	GND	B1	GND
A2	Rx 0+	B2	Tx 0+
A3	Rx 0-	B3	Tx 0-
A4	GND	B4	GND
A5	Rx 1+	B5	Tx 1+
A6	Rx 1-	B6	Tx 1-
A7	GND	B7	GND
A8	SIDEBAND	B8	SIDEBAND
A9	SIDEBAND	B9	SIDEBAND
A10	SIDEBAND	B10	SIDEBAND
A11	SIDEBAND	B11	SIDEBAND
A12	GND	B12	GND
A13	Rx 2+	B13	Tx 2+
A14	Rx 2-	B14	Tx 2-
A15	GND	B15	GND
A16	Rx 3+	B16	Tx 3+
A17	Rx 3-	B17	Tx 3-
A18	GND	B18	GND

P1		P2	
B1	GND	A1	GND
B2	Tx 0+	A2	Rx 0+
B3	Tx 0-	A3	Rx 0-
B4	GND	A4	GND
B5	Tx 1+	A5	Rx 1+
B6	Tx 1-	A6	Rx 1-
B7	GND	A7	GND
B8	SIDEBAND	A8	SIDEBAND
B9	SIDEBAND	A9	SIDEBAND
B10	SIDEBAND	A10	SIDEBAND
B11	SIDEBAND	A11	SIDEBAND
B12	GND	A12	GND
B13	Tx 2+	A13	Rx 2+
B14	Tx 2-	A14	Rx 2-
B15	GND	A15	GND
B16	Tx 3+	A16	Rx 3+
B17	Tx 3-	A17	Rx 3-
B18	GND	A18	GND