Design of a new front-end electronics test-bench for the upgraded ATLAS detector's Tile Calorimeter

C O Kureba, M Govender, I Hofsajer, X Ruan, C Sandrock, M Spoor
School of Physics, University of the Witwatersrand, Johannesburg 2050, South Africa
E-mail: Chamunorwa.Kureba@wits.ac.za

Abstract. The year 2022 has been scheduled to see an upgrade of the Large Hadron Collider (LHC), in order to increase its instantaneous luminosity. The High Luminosity LHC, also referred to as the upgrade Phase-II, means an inevitable complete re-design of the read-out electronics in the Tile Calorimeter (TileCal) of the A Toroidal LHC Apparatus (ATLAS) detector. Here, the new read-out architecture is expected to have the front-end electronics transmit fully digitized information of the detector to the back-end electronics system. Fully digitized signals will allow more sophisticated reconstruction algorithms which will contribute to the required improved triggers at high pile-up. In Phase II, the current Mobile Drawer Integrity ChecKing (MobiDICK) test-bench will be replaced by the next generation test-bench for the TileCal superdrawers, the new Prometeo (A Portable ReadOut ModulE for Tilecal ElectrOnics). Prometeo is a portable, high-throughput electronic system for full certification of the front-end electronics of the ATLAS TileCal. It is designed to interface to the fast links and perform a series of tests on the data to assess the certification of the electronics. The Prometeo's prototype is being assembled by the University of the Witwatersrand and installed at CERN for further developing, tuning and tests. This article describes the overall design of the new Prometeo, and how it fits into the TileCal electronics upgrade.

1. Introduction

Scientists and engineers at the European Organization for Nuclear Research (CERN) probe the fundamental structure of matter. Here, the LHC accelerates and collides protons, and also heavy ions. ATLAS [1] is one of two general purpose detectors used for detecting the sub-atomic particles produced during these high-energy collisions. TileCal [2] is the central hadronic calorimeter of the ATLAS detector. Alternating steel plates and plastic scintillator tiles make up each cell of TileCal. The energy of the detected particles is sampled by the scintillators and signals are collected from the photomultipliers (PMTs) by the front-end electronics located in the superdrawers, which is the outermost part of the detector.

In order to certify the TileCal as being ready for data collection, an evaluation must be made on each of its modules, hence, the need for an electronics test-bench. Currently, the MobiDICK4 test-bench is being used for the certification process. The High Luminosity LHC will lead to an inevitable complete re-design of the read-out electronics in the TileCal. Figure 1 shows a comparison of the current and future front-end electronics set-up for the TileCal. In the current set-up, pipeline memories are used to store digitized data samples before they can be trigger-selected. The read-out electronics systems in each superdrawer are daisy-chained, resulting in the sharing of a data connection to the Read-Out Driver (ROD). In the future electronics design,

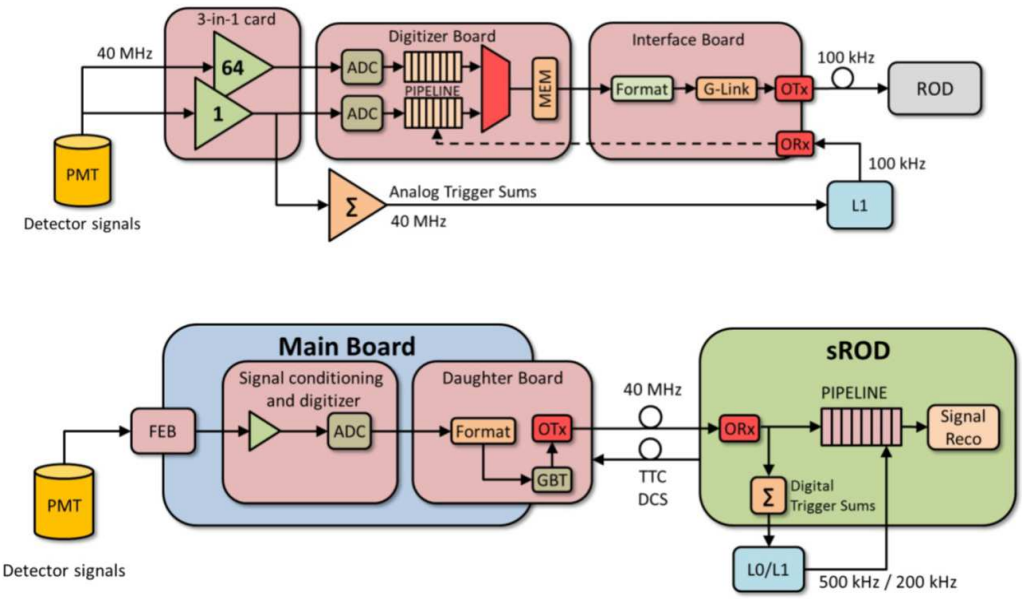

Figure 1. *Top*: Current front-end electronics; *Bottom*: Equivalent electronics for Phase-II upgrade.

each superdrawer has been divided into 4 minidrawers. One minidrawer hosts 12 PMTs and 1 daughter board. Each daughter board has one link to the super Read-Out Driver (sROD), thereby reducing failure rate by 25% with respect to ATLAS. There are up to 48 PMTs in one superdrawer, grouped in groups of 6 in a digitizer board. There are 16 digitizers for one superdrawer, interfaced by 1 interface card. It is envisaged that the future electronics will have:

- a super Read-Out Driver (sROD), capable of receiving data at 40 MHz as opposed to the current Read-Out Driver (ROD) which only handles 100 kHz,
- an increase in the number of point-to-point links with the front-end electronics,
- improved radiation tolerance,
- a higher read-out bandwidth due to the need to read-out all sampled data to avoid corruption in the front-end pipeline memories.

An evaluation of this new proposed architecture is currently being carried out in the demonstrator project, where a small fraction of the detector (1/256) will be evaluated in test beams and inserted into ATLAS at the next shutdown of the LHC. In Phase II, the current Mobile Drawer Integrity CheckKing (MobiDICK4) system [4, 5] test-bench will be replaced by the next generation test-bench for the TileCal superdrawers, the new Prometeo (A Portable Read- Out ModulE for Tilecal ElectrOnics). The MobiDICK system faces challenges against ageing and new technologies [6]. The Prometeo is designed to certificate the TileCal front-end electronics by performing multiple tests. The Prometeo's prototype is being assembled by the University of the Witwatersrand and installed at CERN for further developing, tuning and tests.

2. MobiDICK4 (Current test-bench)

Figure 2 shows a layout of the components of the MobiDICK4 test-bench, currently being used at CERN for the certification of the TileCal front-end electronics. Its main board is a Xilinx ML507 evaluation board, whose backbone is a Virtex-5 Field Programmable Gate Array (FPGA). The MobiDICK4 test-bench has a server running on Power PC, which connects to the client via

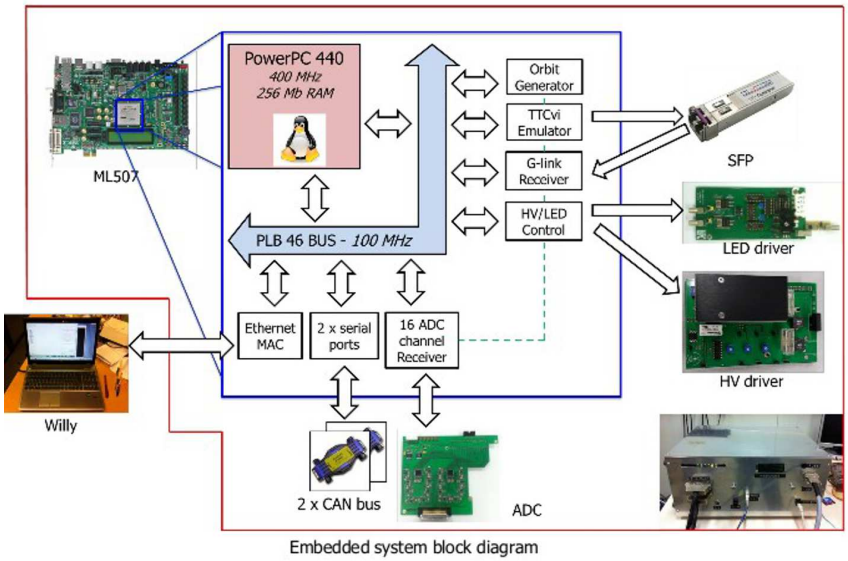

Figure 2. Layout of the MobiDICK4 test-bench, currently being used at CERN.

ethernet. It records digital data at a maximum rate of 100 kHz. It uses "slow" canbus to control the current integrator circuit and the HV applied to every PMT and a custom designed ADC board to sample the analogue signals.

3. Prometeo (new test-bench): Hardware design

Prometeo has been designed to have the ability to: read-out all channels at the LHC bunch crossing frequency, assess the quality of data in real-time, diagnose malfunctions in each minidrawer be self-contained and portable for maintenance inside the detector, and be low-cost and scalable for network usage. In the current design being deployed for the hybrid demonstrator that will also have analogue output, Prometeo will make use of an ADC board. The current version is using a VC707 board. The prototype for 1 superdrawer will use the sROD demonstrator, which is limited to 2 minidrawers. Figure 3 shows a schematic layout of the Prometeo. The Prometeo consists of several parts as follows:

- Main board: Xilinx VC707, Virtex-7 FPGA chip, 1 GB DDR3 RAM, two FMC connectors, received through SFP on the mainboard,
- Dual QSFP FMC card for digital communication with 2 minidrawers,
- Analogue to Digital Converter (ADC) FMC card: for the digitization of data in the hyprid demonstrator,
- High Voltage (HV) board: to turn on/off the HV and provide the -830 V voltage to power on the photo-multipliers (PMTs),
- Light Emitting Diode (LED) board: to illuminate the PMTs,
- Commercial ATX power supply,
- Ethernet router,
- Aluminum enclosure: whose dimensions are 50 cm $\times$ 35 cm $\times$ 20 cm in terms of length, width and depth, thickness of 3 mm and weight of 8 kg.

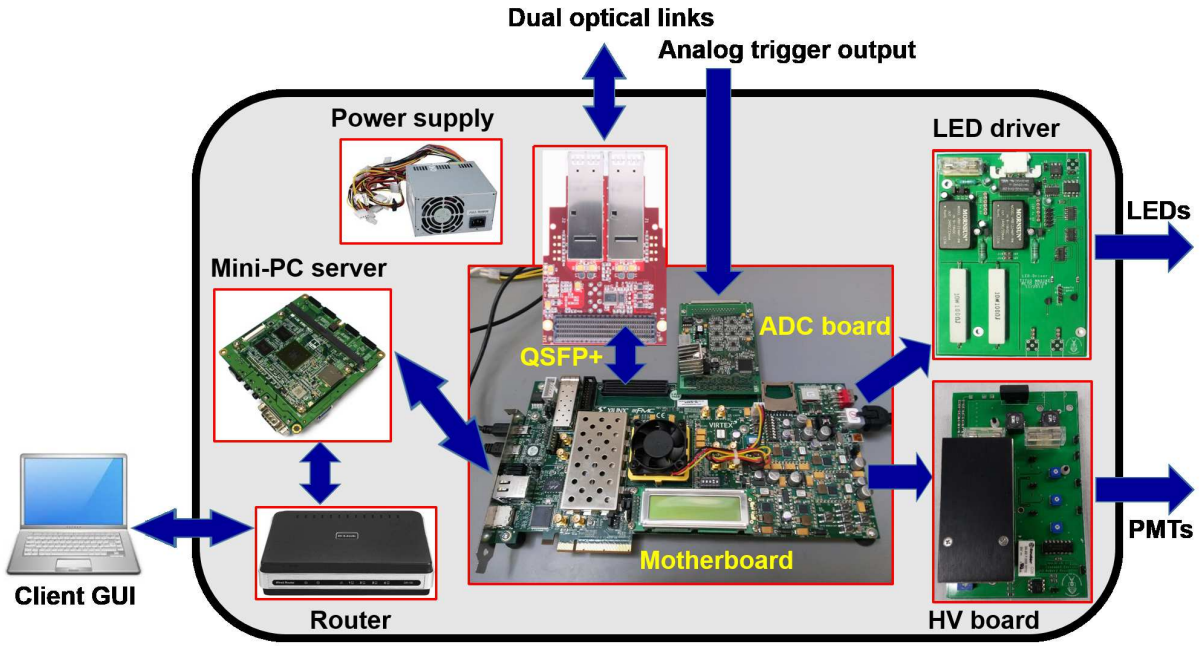

Figure 3. Schematic of the Prometeo.

4. Prometeo: Software design

The software design of Prometeo is based on direct hardware access technology for FPGAs with direct ethernet connection. We use an IPbus [7] ip-core module on the FPGA that enables direct communication of the registers through VOP. A custom built software version of the IPbus client that is implemented in C++, Java and Python is used to allow multiple developments and tests to perform in parallel. At this stage there are two implementations of the software being developed, namely, one in pure Java and another one in C++/Python. The Java software is inspired by the one in the MobiDICK GUI where a core window loads different tests as plugin tabs, and each one executes and displays a different test. The C++ one implements the tests directly as command line applications. A front-end HTML/Python interface is used to execute the tests and assess the results. Figure 4 shows snapshots of the Java and HTML GUIs used by the client to execute the Prometeo tests.

The Prometeo has been designed to perform both linearity and stability tests on each of the following:

- Charge Injection System (CIS)
- High Voltage (HV)
- Integrator
- Pedestal

These results are used for diagnosis of faulty PMTs, 3 in 1 cards, mainboards, daughter boards, optical links and analogue cards. Most of the tests are implemented in the HTML interface, thereby leaving Java as an excellent tool for debugging at expert level.

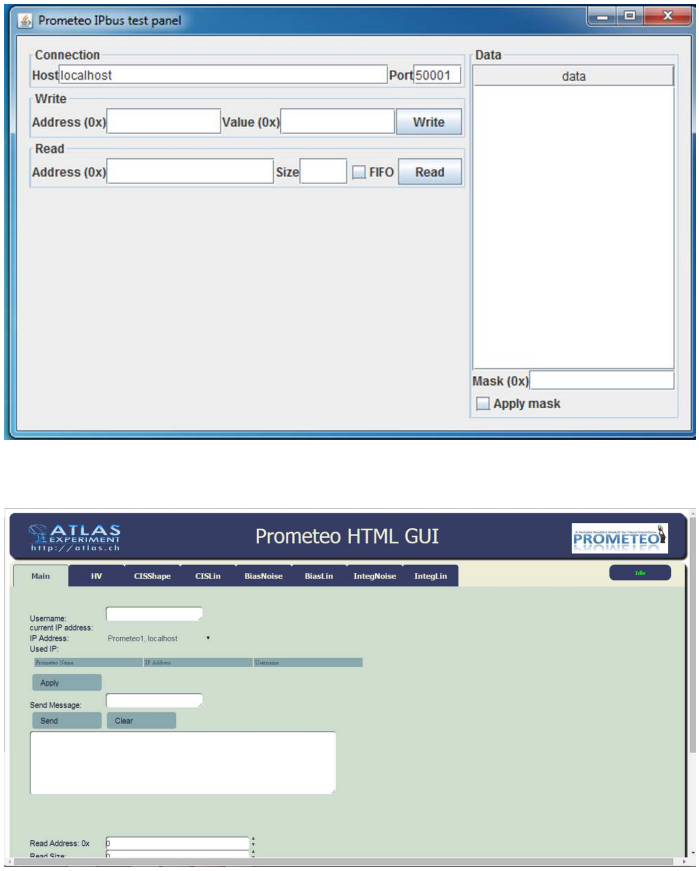

Figure 4. *Top*: Java GUI for Prometeo; *Bottom*: HTML GUI for Prometeo.

5. Conclusion

Prometeo, the next generation test-bench for the certification of the new TileCal electronics has been designed, in preparation for the LHC phase-II upgrade. Prometeo is inspired by the current MobiDICK4 test-bench. It is capable of performing multiple tests on the electronics modules of the upgraded superdrawers. Prometeo is currently in a prototyping phase and currently serves a hybrid demonstrator of the future Phase-II electronics. All components of Prometeo have been manufactured and are undergoing tests as they are added to the system. Further tests are being developed and tested in parallel with the development of the demonstrator. Prometeo software is well advanced and used everyday to assess the stability of the first demonstrator.

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