The Data Acquisition system for a fixed target experiment at the NICA complex at JINR and its connection to the ATLAS TileCal readout electronics.

Tomiwa Kehinde

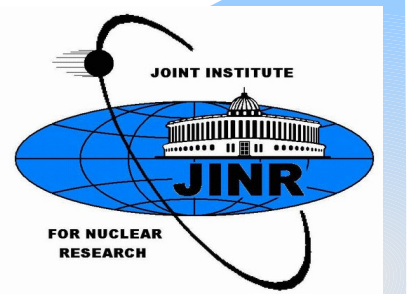
kehinde.gbenga.tomiwa@cern.ch

University of the Witwatersrand, Johannesburg

HEP 2015

People involved:

- Bruce Mellado (Wits)
- Ilja Slepnev (JINR)
- Sergey Bazylev(JINR)
- Slava Golovatuk(JINR)
- Tomiwa Kehinde (Wits)



Outline

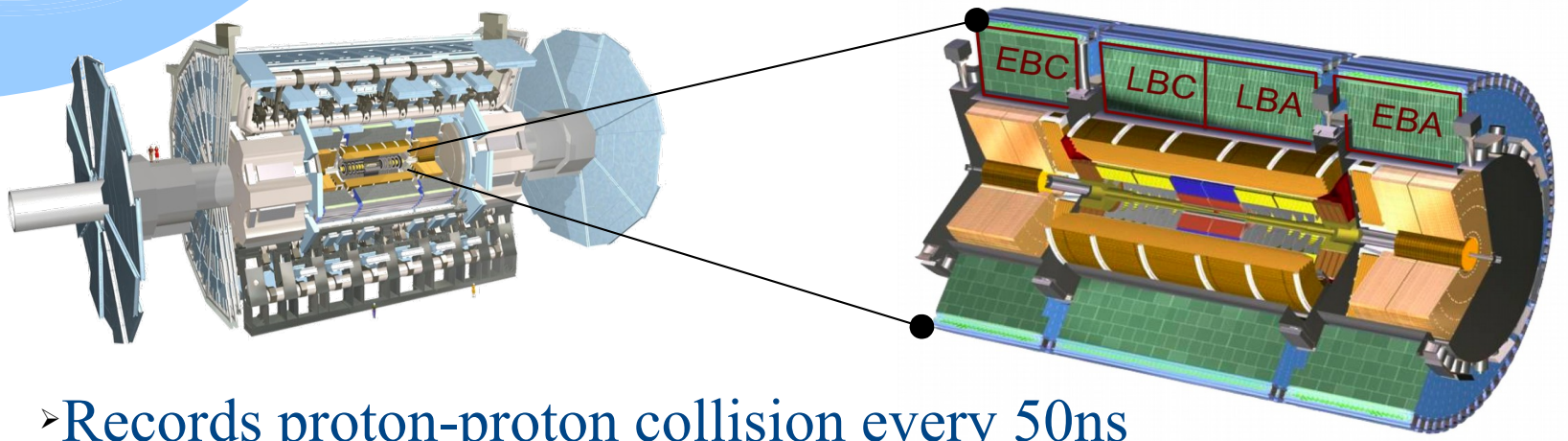
- Introduction
- TileCal Readout Electronics
- BM@N Detector
- DAQ System
- DAQ module
- Trigger and Timing Architecture
- BM@N Data flow
- Estimated data throughout for 2017
- Data structure
- Conclusion

Introduction

Particle physics/Data/High-Throughput electronics

ATLAS Detector

TileCal



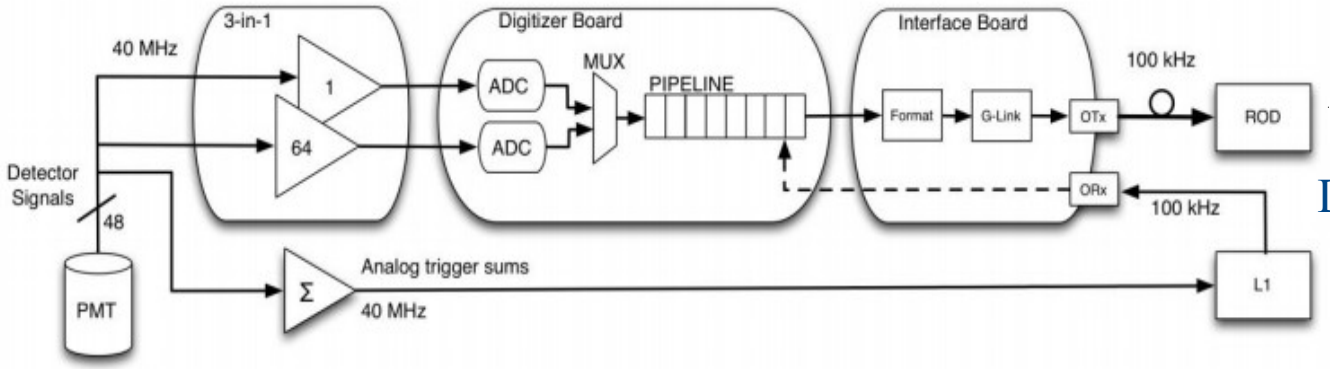
- Records proton-proton collision every 50ns
- Resulting to data flow of about 10Pb/s. – Big Data

Development of High-throughput Electronics. -Way out

- Reduces Big data to scientific data at high rate.
  - With maximum readout efficiency
  - Data selection and compression
  - No dead time

TileCal Readout Electronics

TileCal current Readout chain



ROD with digital processing units DSP

Digital signal processor

Current Readout drive(ROD)

- Performs online reconstruction
- Synchronization of data and trigger
- Computation of total transverse energy
- Digital error detection
- Monitoring task

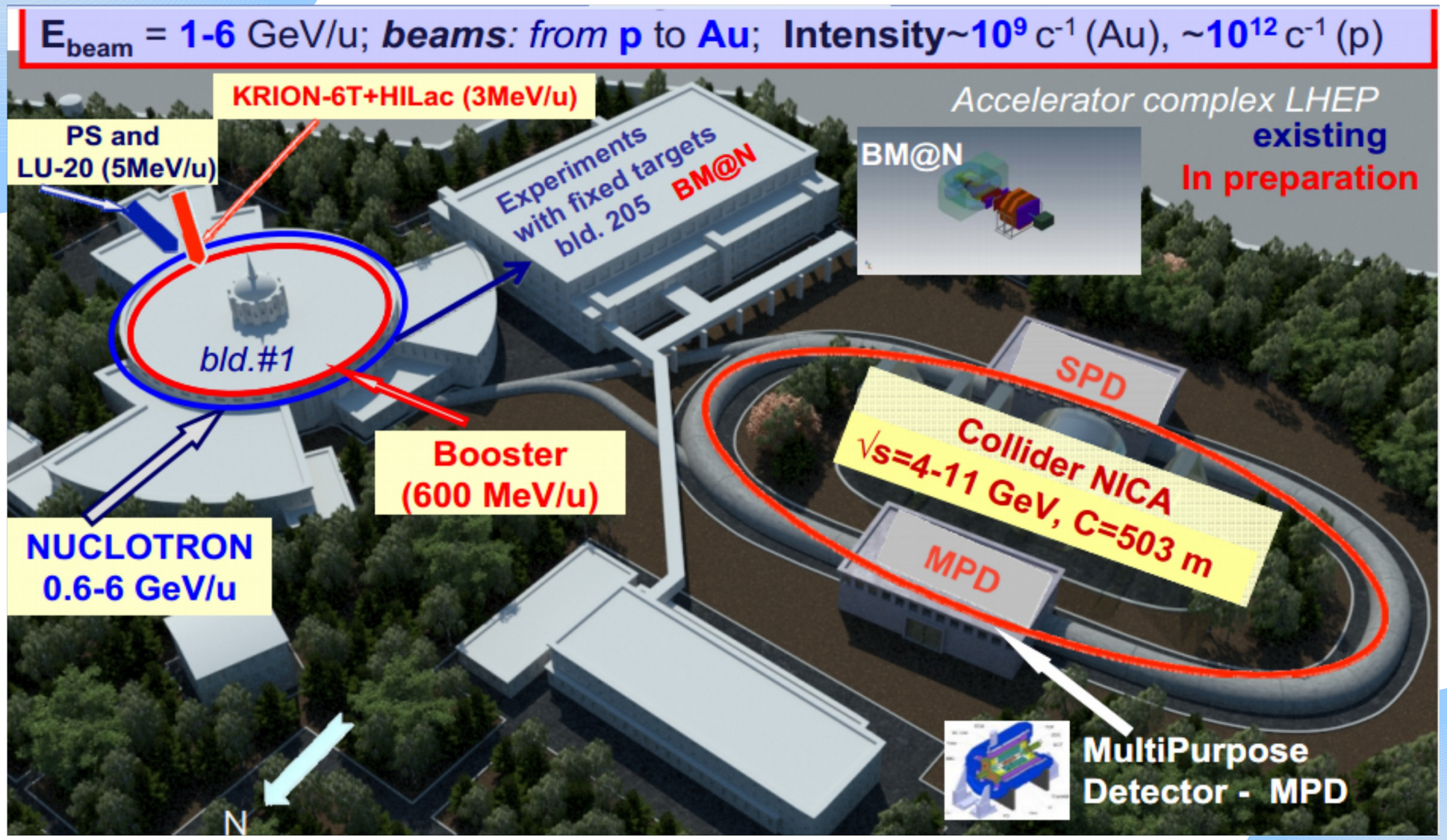
Future super ROD (sROD)

- sROD to manage L1 trigger (digital)
- Configure frontend electronics.

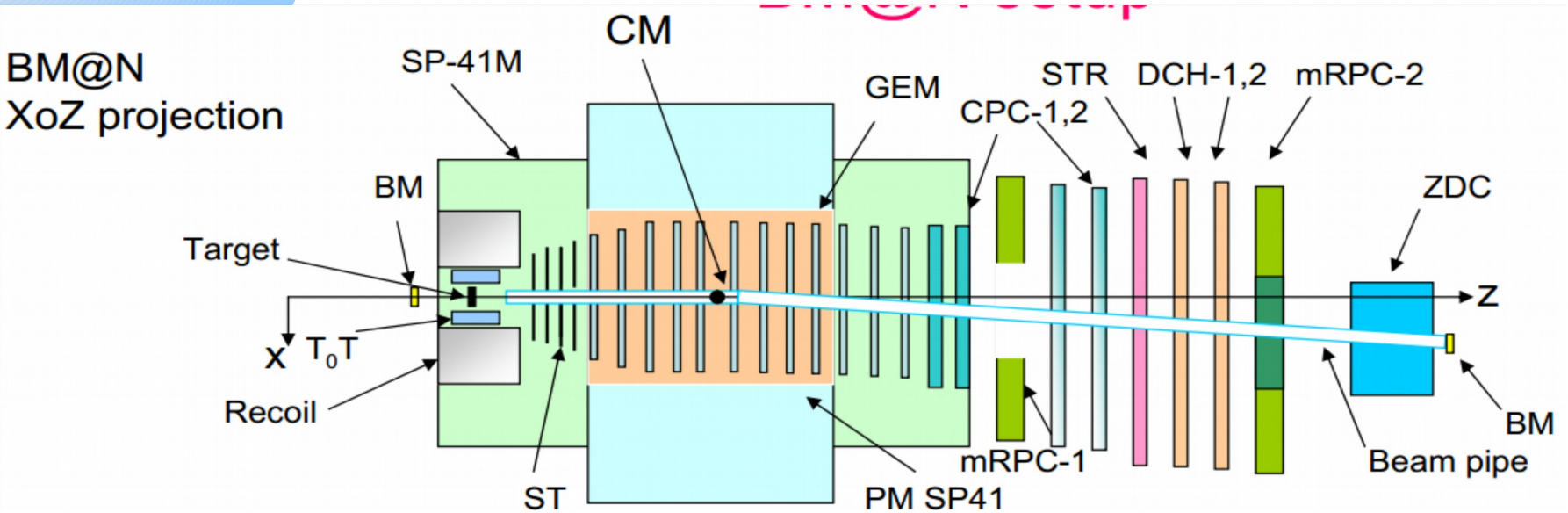
General purpose processing unit (PU) for BM@N project

- A general purpose PU is being developed at Wits for the BM@N project

Baryonic Matter at Nuclotron (BM@N) Project



BM@N detector

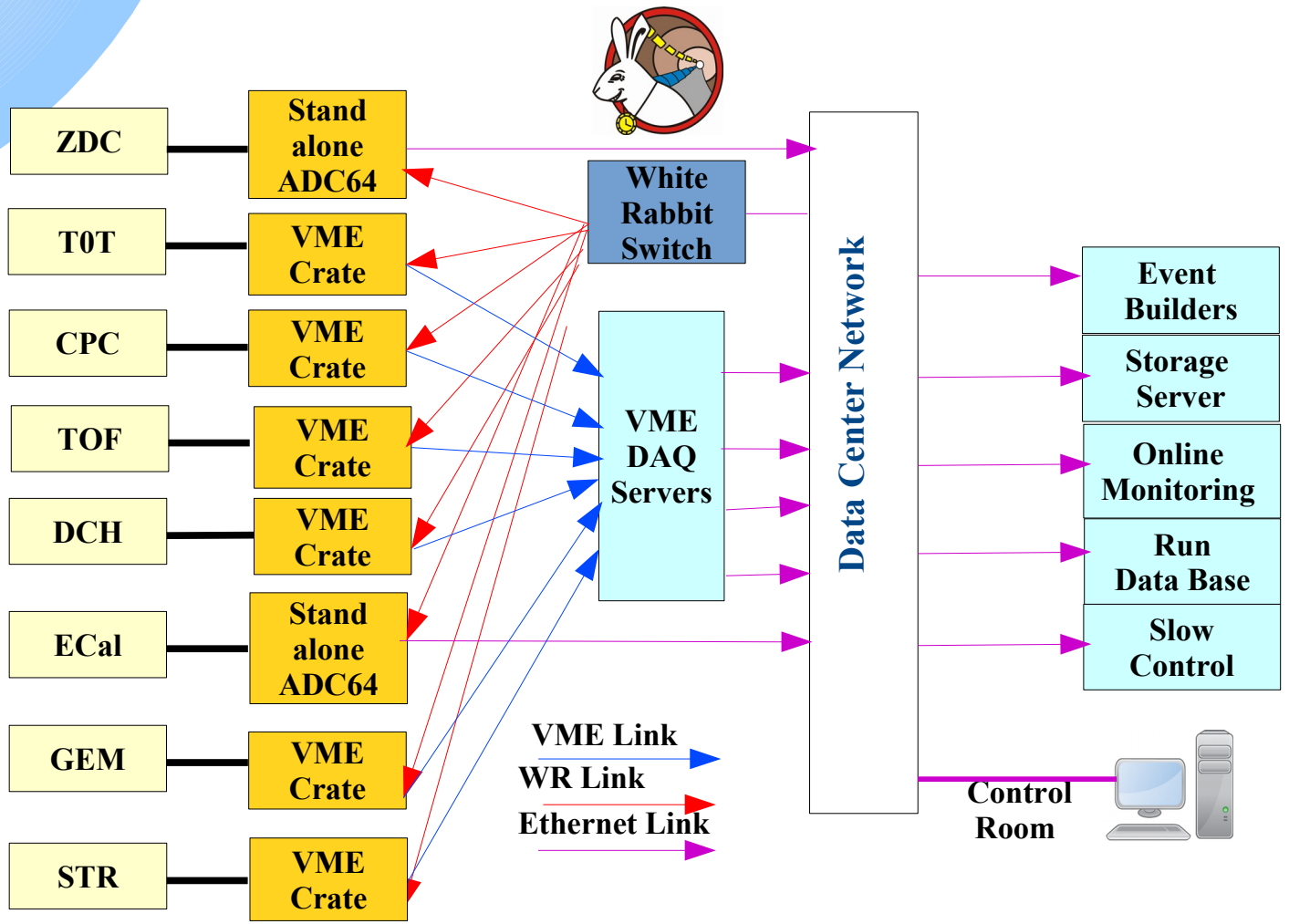


- GEM → Gaseous Electron Multipliers
- TOF → Time of Flight Detector
- T0T → Fast Start Detector
- DCH → Drift Chamber
- ST → Straw tubes

- ZDC → Zero Degree Calorimeter
- CPC → Cathode pad chamber
- Ecal → Electromagnetic Calorimeter

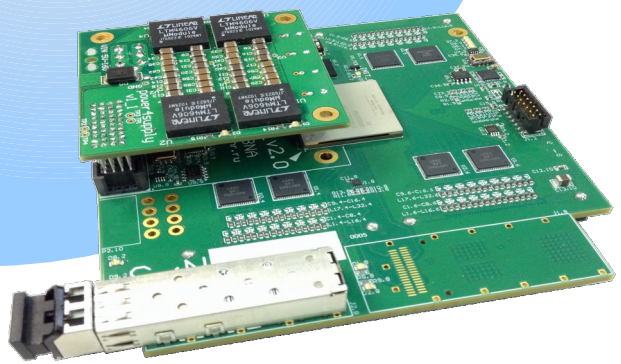
Photo: BM@N project

DAQ System


ZDC
T0T
CPC
TOF
DCH
ECal
GEM
STR
Stand alone ADC64
VME Crate
VME Crate
VME Crate
VME Crate
Stand alone ADC64
VME Crate
VME Crate
White Rabbit Switch
VME DAQ Servers
VME Link
WR Link
Ethernet Link
Data Center Network
Event Builders
Storage Server
Online Monitoring
Run Data Base
Slow Control
Control Room

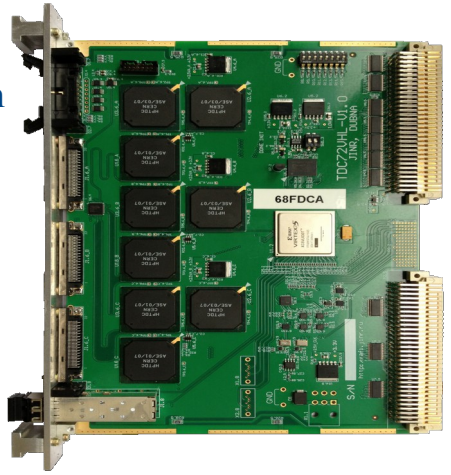
DAQ modules Description

ADC64V

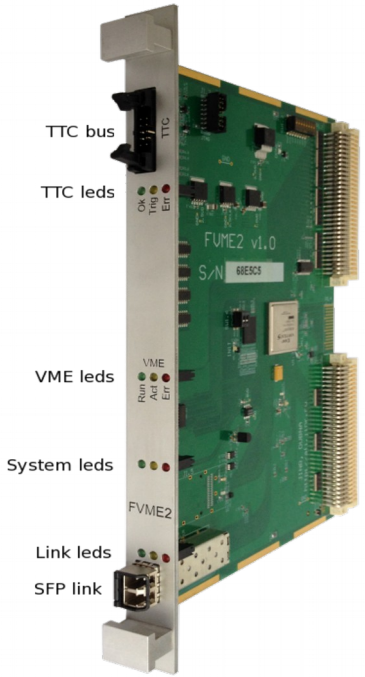


- 64 channels 12-bit, Waveform digitizer
- 62.5 MS/s with signal processing core/FPGA
- White Rabbit support.

TDC72VHL

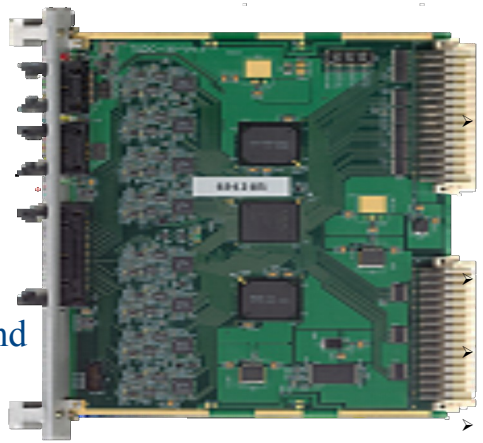


- 72 channels module based on HPTDC chip.
- Identify event and present time representation of occurrence
- Timestamping, multihit and trigger matching capability. 25Ps bin size
- VME64x interface



FVME2

- VME64 Master
- Automatic readout of VME modules in chain mode
- VME system controller
- TTC LVDS input for spill and trigger



TQDCV

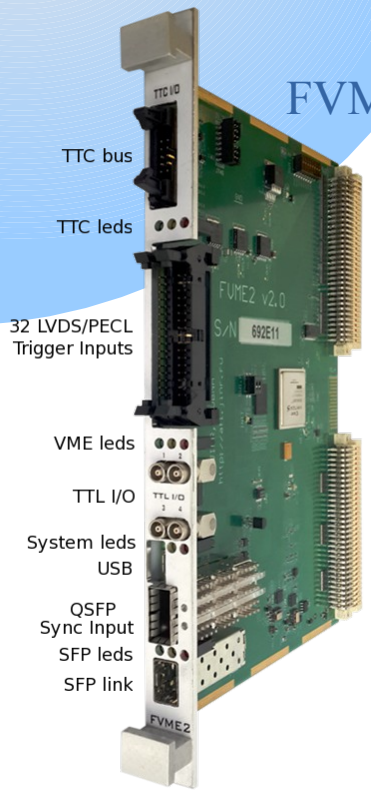
16 channel discriminator, multihit time stamping TDC (25ps bin size) and waveform digitizer

Onboard trigger matching

VME, clock, trigger and reset interface

Used to measure pulse arrival time

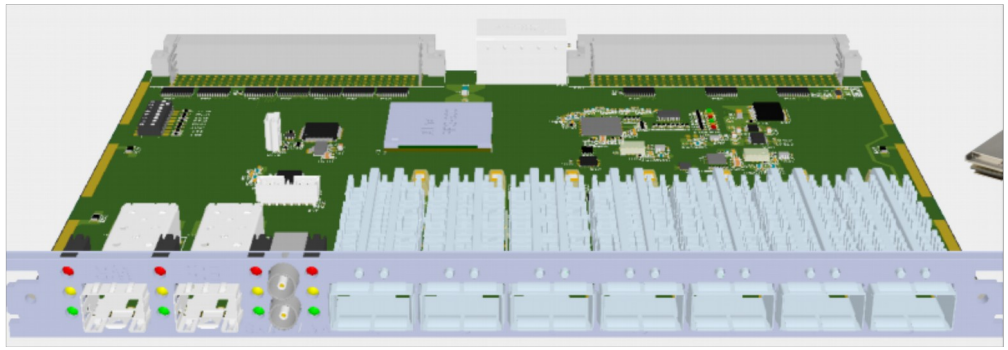
DAQ modules Description Cont.



FVME2TM/FVME2TMWR

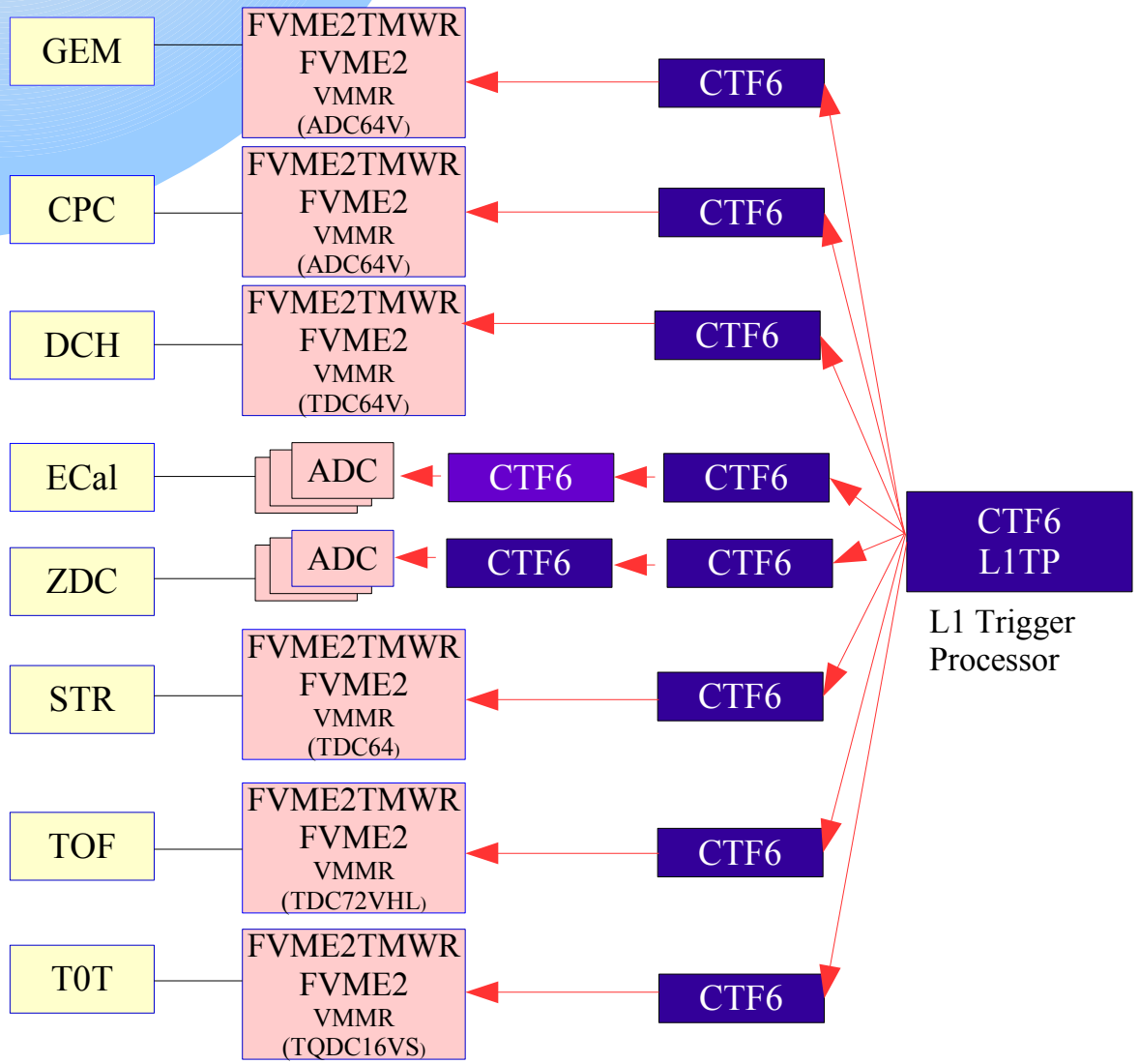
- TTC module for VMEDAQ system
- 41.667 MHz onboard generator
- Input/Output for Spill, Parity and Trigger.
- FVME2TMWR is FVME2TM with White Rabbit support

CTF6



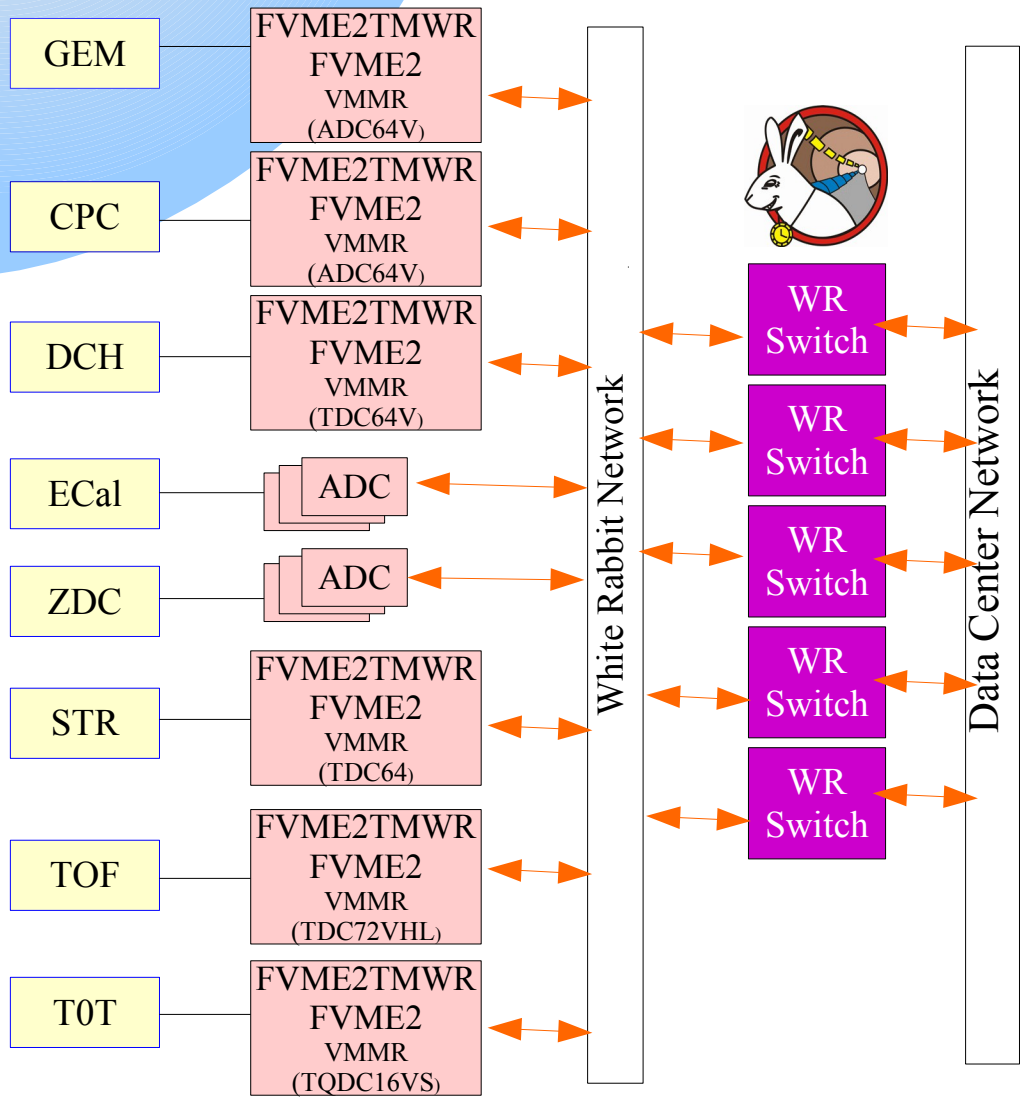
- L1/L2 Clock and Trigger Distribution module
- 2 x 3.2Gb Serial lines (Encoded L1, L2 and Timecode)
- LVDS clock 125MHz
- LVDS 1 PPS(Pulse per Second)

Hardware LI Trigger



- Implemented by Hardware
- High speed serial links
- VXS crates with CTF6
- 5..10 micro-seconds Latency
- For most detectors L1 acceptance move events to a Ring Buffer.
- Every set of events (spills) in the ring buffer has timestamps, used by the L2 trigger.

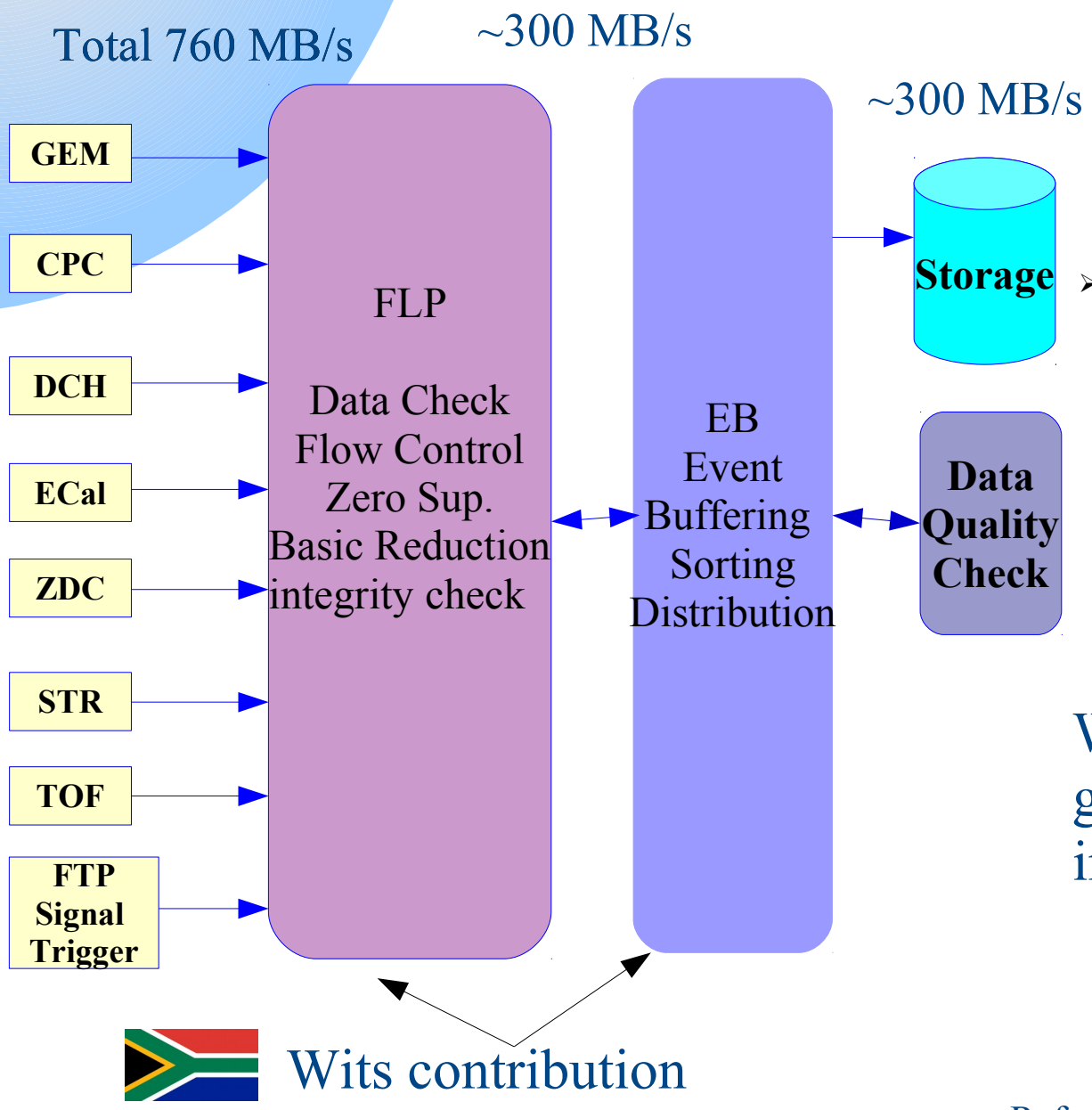
L2 Trigger over White Rabbit Network



- High latency trigger 10...100 μs
- Digital software trigger decision on dedicated CPUs.
- Used for selective readout of event from device's ring buffer.

Reference: Ilya Slepnev JINR, 2014

BM@N Data flow



First Level Proceses (FLP):

- Reduces data flow by eliminating unimportant data and background noise.

Wits developing a general purpose PU to implement FLP and EB

Reference: Ilya Slepnev JINR, 2014

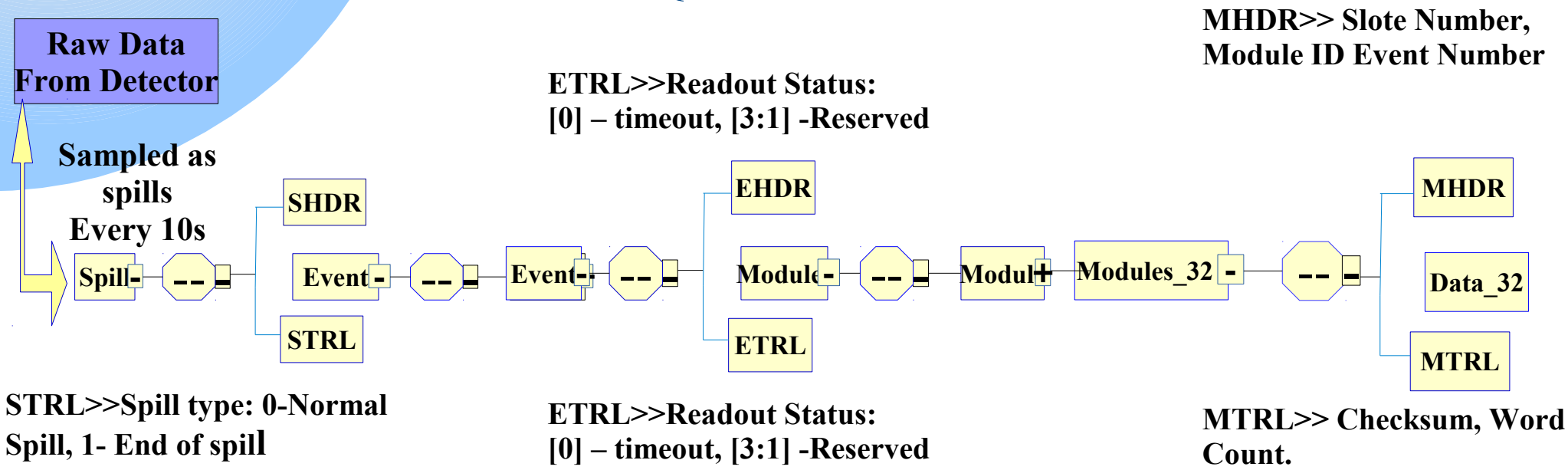
Event Size of 2017 Experiment

Detector	Readout card	Geometry	DAQ CH	Occupancy	Bytes/ch	Bytes/Event
CPC	ADC 64V	2*9129/64	285	3.84	4	4400
DHC	TQDC64V	2*2048	4096	0.06	4	1500
ECAL	ADC64	9*360	3240	0.30	44	44000
GEM	ADC64??	96000/64	1500	3.84	4	23000
STR	TDC64V?	2*6*450	5400	0.06	4	1700
TOF	TDC72V	2*2*1536	6144	0.06	8	3700
ZDC	ADC64	104	104	0.30	44	1400
Trigger	TQDC16V		1	1	100	100
Other			1	1	500	500
Total						~80,000

Reference: Ilya Slepnev JINR, 2014

Data Structure

VME DAQ Raw data format



- Each module with its specific data format
- Standalone ADCs use M-Stream Waveform Diditizer Raw data format

Conclusions

- The total raw data from the frontend electronics to FLP is estimated 760MB/s and about 300MB/s at EB.
- The PUs will be the hardware platform to implement FLP and EB.
  - Synchronize data and trigger
  - Digital error detection
  - Monitoring task
  - Zero suppression
- February 2015 Experiment
  - Plan to develop and deploy DSP based ROD to the experement.
  - Improve data throughput and computing
- Bigger Setup for 2017
  - Test run

Questions

or

Comments?

Acknowledgments

- Schoool of Physics, University of the Witwatersrand (ZA)
- Vladimir Sidorenko
- Members of AFI group at JINR