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The Data Acquisition system for a fixed target experiment at the NICA complex at JINR and its connection to the ATLAS TileCal readout electronics

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Today's large-scale science projects have been always encountered challenges in processing large data flow from the experiments, the ATLAS detector records proton-proton collisions provided by the LHC at CERN every 50 ns which results in a total data flow of 10 Pb/s, the SKA is a radio telescope consisting of several thousand antennae, the data rates from the individual antenna at SKA results in a total data flow of up to 9 Pb/s. These data must be reduced to the science data product for further analysis, thus a very fast decisions need to be executed, to modify this large amounts of data at high rates. The capabilities required to support this scale of data movement is involving development and improvement of high-throughput electronics. The upgraded LHC will provide collisions at rates that will be at least 10 times higher than those of today due to the luminosity increasing by a factor of ten at 2022, however, this will require a complete redesign of the read-out electronics (ROD) in the Tile-calorimeter (TileCal) of the ATLAS experiment. The ROD system is a high-throughput system, it is capable of handling large data throughputs and to apply advanced operations at high rates, ROD system are functionally decomposed in two building blocks: the Field Programmable Gate Arrays (FPGA) and Digital Signal Processors (DSP). The aim of this work is to have a look at the ROD architecture for the fixed target experiment at the NICA complex at JINR, by compiling the data-flow requirements of all the subcomponents. Furthermore, the FPGAs boards characteristics to control, triggering and data acquisition will be described in order to define the data acquisition system (DAQ) with maximum readout efficiency, no dead time and data selection and compression.

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