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PGAS in-memory data processing for the Processing Unit of the Upgraded Electronics of the Tile Calorimeter of the ATLAS Detector

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Advances in new technologies, high speed and more accurate instrumentation for data acquisition have given rise to the accumulation of massively large amount of data typically referred to as Big-Data. The ATLAS detector, operated at the Large Hadron Collider (LHC) records proton-proton collisions at CERN every 50ns resulting in a sustained data flow up to Pb/s.
The upgraded Tile Calorimeter of the ATLAS experiment will, sustain about 5PB/s of digital throughput. These massive data rates require extremely fast data capture and processing. Although there has been a steady increase in the processing speed of CPU/GPGPU assembled for high performance computing, the rate of data input and output, even under parallel I/O, has not kept up with the general increase in computing speeds. The problem then is whether one can implement an I/O subsystem infrastructure capable of meeting the computational speeds of the advanced computing systems at the petascale and exascale level.
We propose a system architecture that leverages the Partitioned Global Address Space (PGAS) model of computing to maintain an in-memory data-store for the Processing Unit (PU) of the upgraded electronics of the Tile Calorimeter for high throughput data processing. The physical memory of the PUs are aggregated into a large global logical address space using RDMA- capable interconnects such as PCI-Express to enhance data processing throughput. The technique allows for seamless addition of global memory for high throughput data processing based on the memory requirements of the data stream being processed. Research challenges being addressed concern memory-to-memory data copying, fault-tolerance, as well as optimisations for high throughput data processing.

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