Development & Testing: ADC board for the Prometeo Test-bench

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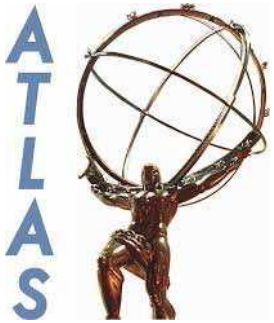
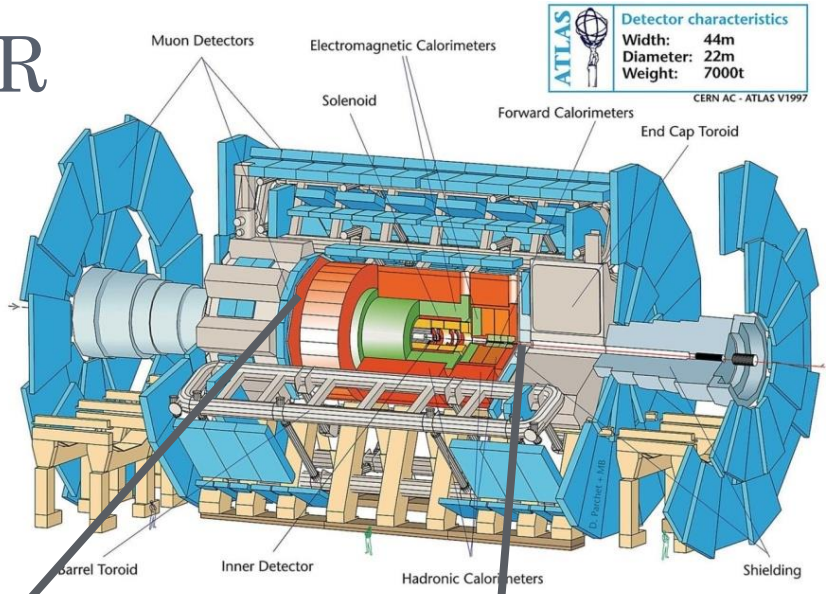


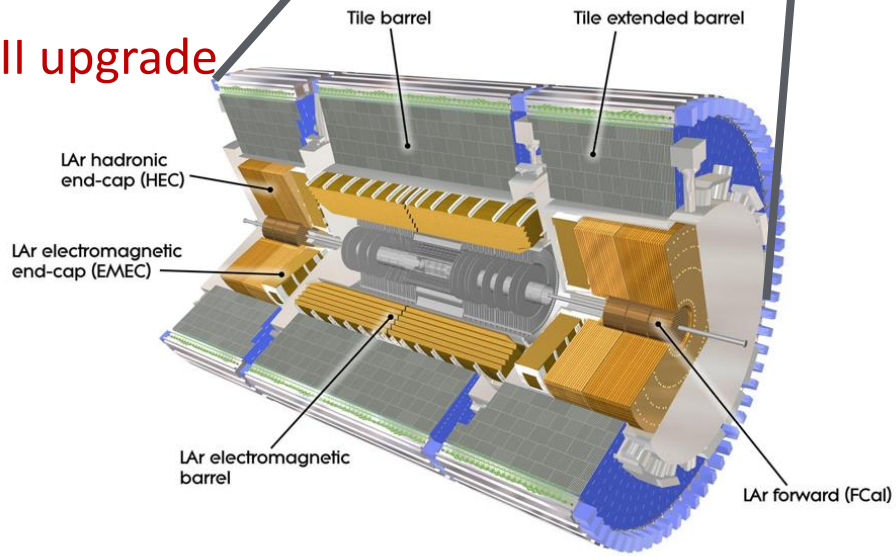
Overview

- ATLAS Tile Calorimeter
- Hybrid demonstrator
- Prometeo Test-bench
- Prometeo ADC board
- Outlook

ATLAS Detector

- General purpose particle detector (Multiple sub- detectors)
- 40 MHz bunch crossings
- Petabytes of raw data per second
- Preparing for Phase-II upgrade

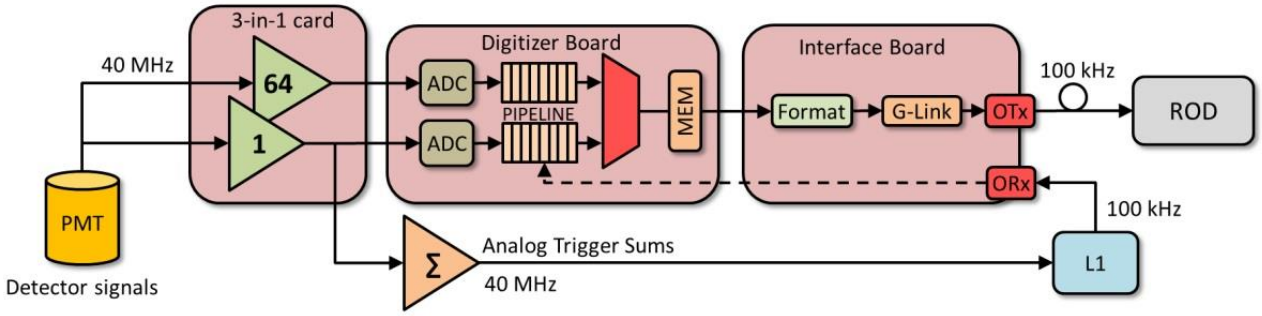




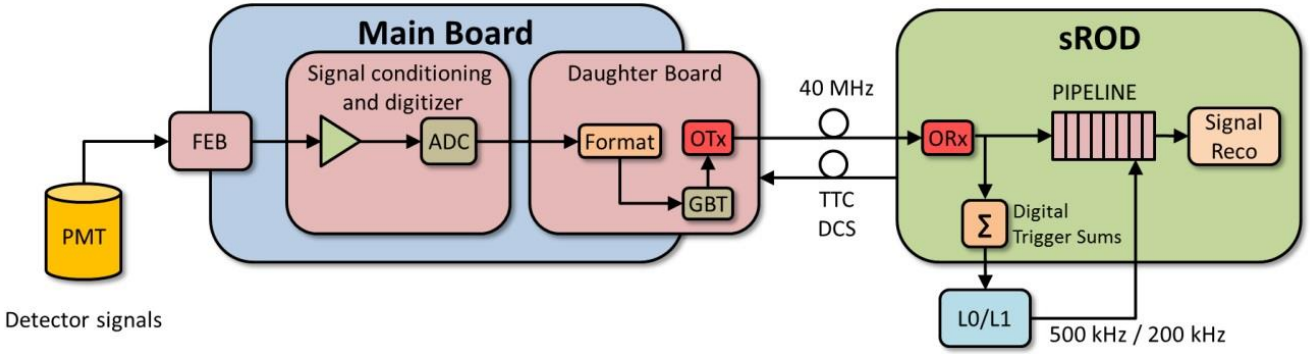
Tile Calorimeter

Phase-II Upgrade

Present front-end electronics



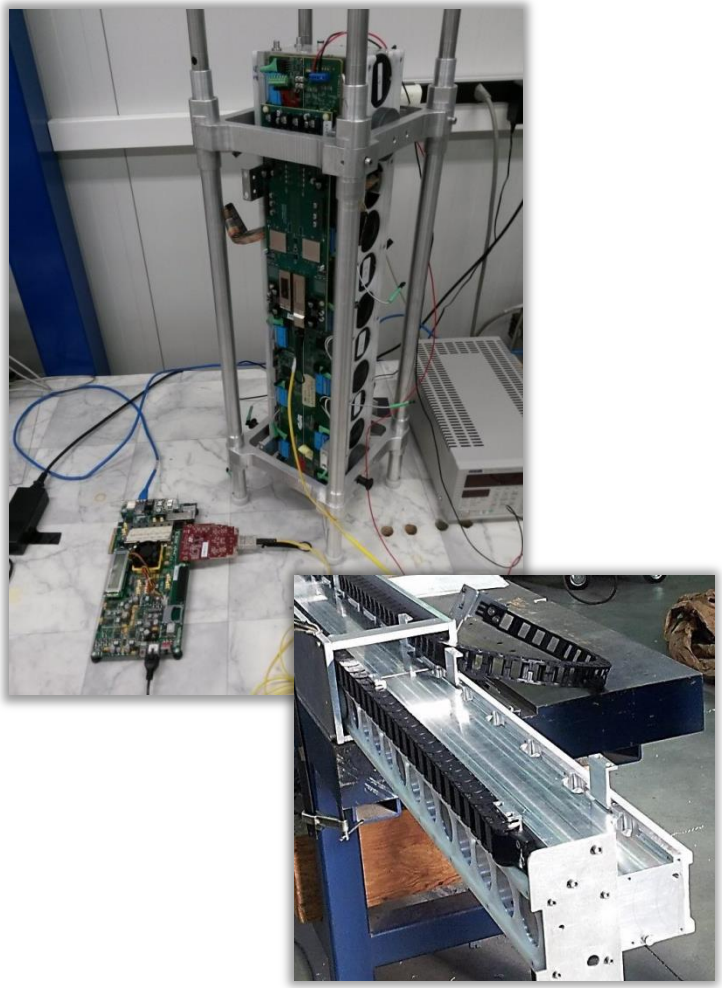
Equivalent Phase-II upgrade electronics



Complete replacement of the front-end and back-end electronics introducing a new read-out architecture

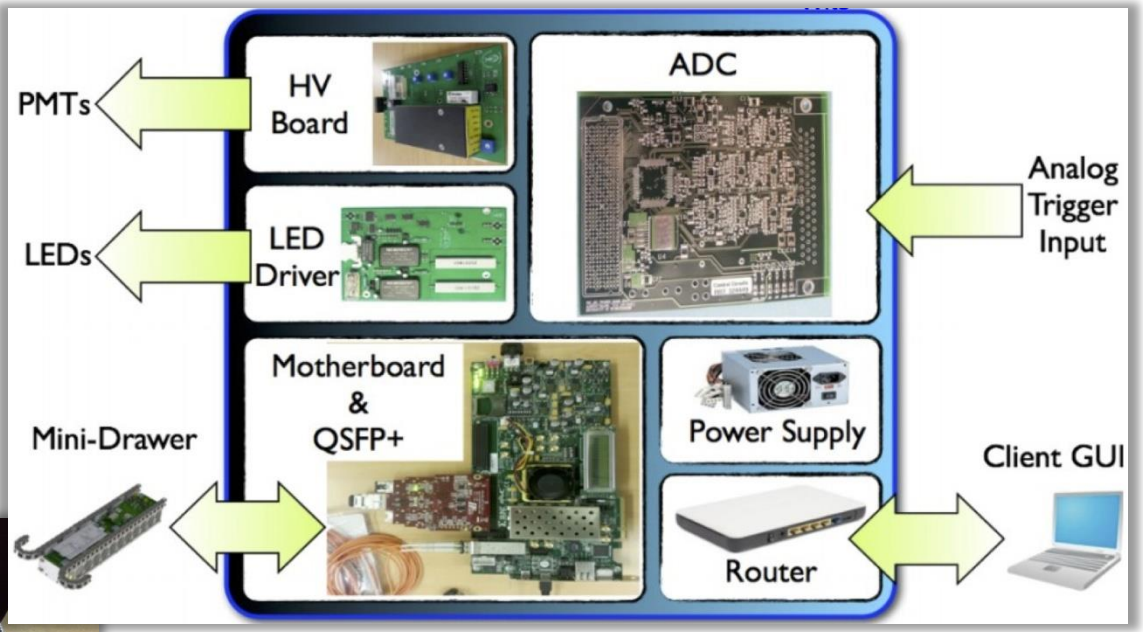
Hybrid demonstrator

- Validation of the new readout architecture, trigger system interfaces.
- Divides each TileCal module into 4 independent mini-drawers.
- Mini-drawer: Mainboard, Daughterboard, 12 PMTs, HV card and Adder board
- Compatible with old architecture.
- High level of redundancy



A Portable ReadOut ModulE for Tilecal ElectrOnics

PROMETEO



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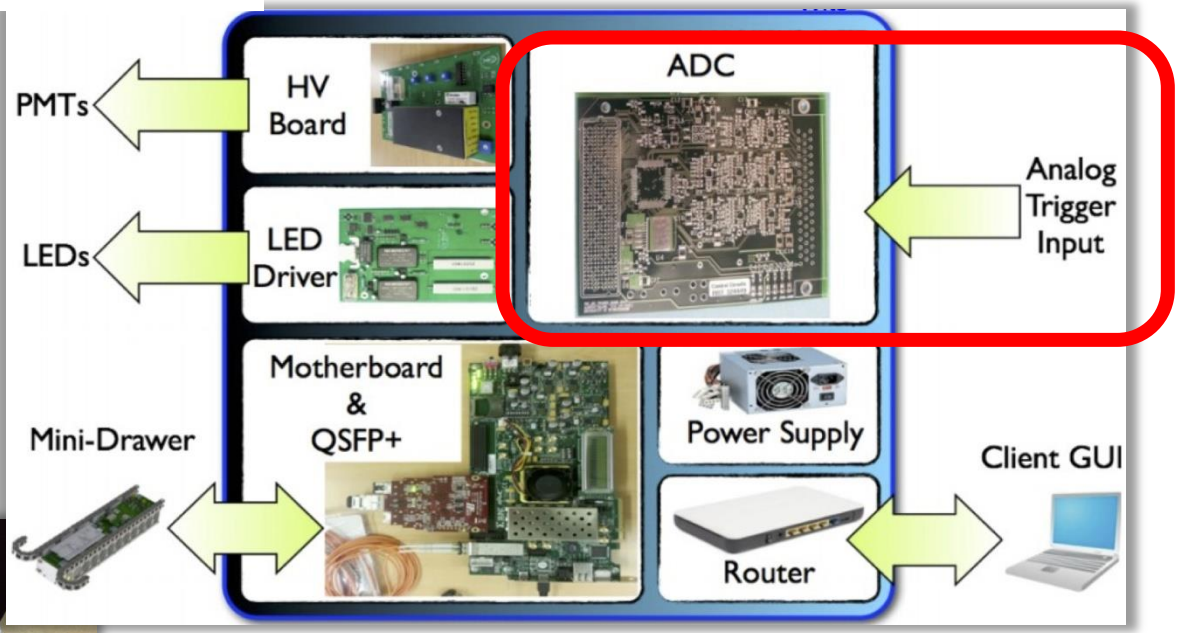
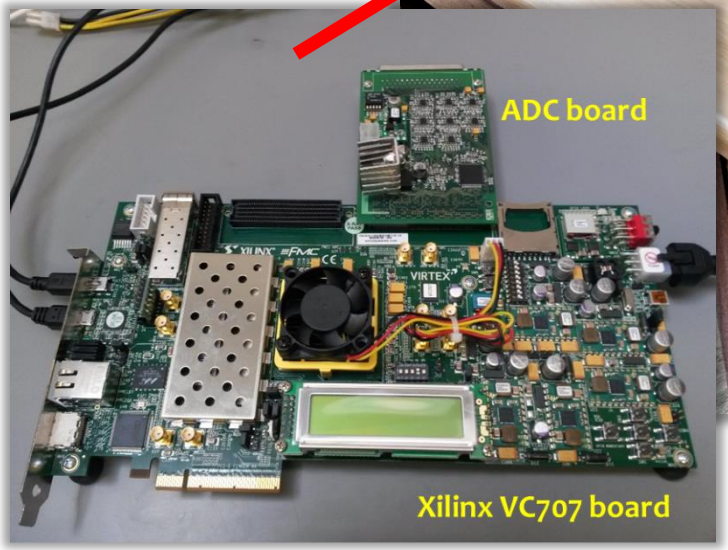


Development of the ADC Board



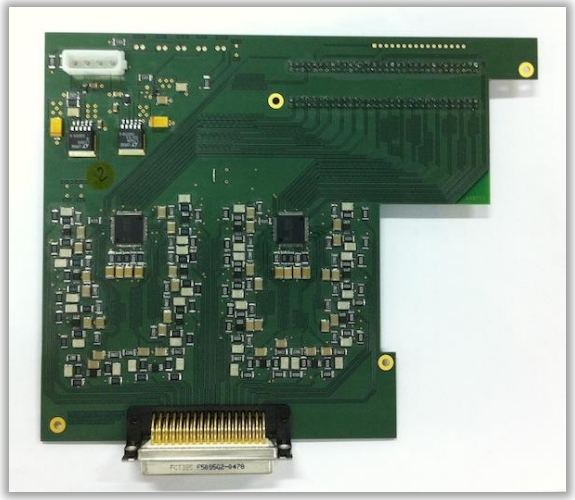
AIM: Test and Validate the design of the new ADC board.

- Firmware needs to be re-designed to work on modern FPGAs. (Xilinx Virtex 7)
- Identify and fix any design faults found in prototype design for next production.
- Perform system function testing in new electronics Laboratory.

ADC Board

- Custom board that receives and digitises analog signals from the trigger outputs of the super drawer at 40 MHz
- Trigger data used for Hadron and Muon selection
- Four layer PCB with two ADS5271 chips
- 8-channel, 12-bit, 50 MSPS analog-to-digital converters
- PCB redesigned to connect to the VC707 via FMC connection
- LVPS channels transfer serialised data at 480 Mbps

MobiDICK4 ADC



More than 2/3 size reduction

Prometeo ADC

FIRMWARE

New firmware had to be built to interface the ADC board with the Virtex 7 FPGA

All FPGA firmware is designed using HDL

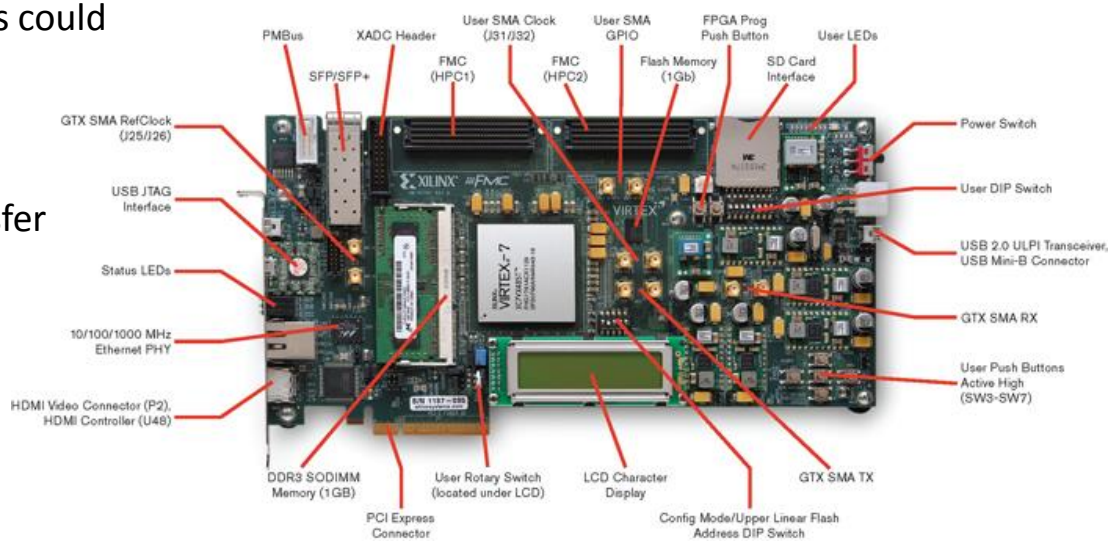
- Describes hardware interconnects
- Bit Level programming
- Non-sequential language
- Exceptionally efficient

```
55  end sROD_system_module;
56  architecture rtl of sROD_system_module is
57
58     signal clk125_fr, clk125, clk100 ,clk200, clk_locked, locked, eth_locked, s
59     signal rst_125, rst_eth, onehz,rst_ipbi: std_logic;
60     signal mac_tx_data, mac_rx_data: std_logic_vector(7 downto 0);
61     signal mac_tx_valid, mac_tx_last, mac_tx_error, mac_tx_ready, mac_rx_valid,
62
63     signal mac_addr: std_logic_vector(47 downto 0);
64     signal ip_addr: std_logic_vector(31 downto 0);
65     signal pkt_rx, pkt_tx, pkt_rx_led, pkt_tx_led: std_logic;
66     signal SYS_CLK200 : std_logic;
67
68  begin
69
70     clk200o <= clk200;
71     ipb_clk <= ipb_clki;
72     rst_ipb <= rst_ipbi;
73
74     process(ip_mac_config)
75     begin
76     case  ip_mac_config is
77        when "000" => -- VALENCIA LAB
78           mac_addr <= X"020ddba11599"; -- Careful here, arbitrary addresses do
79           ip_addr <= X"c0a80001"; -- 192.168.0.1
80        when "001" => -- CERN LAB
81           mac_addr <= X"020ddba11599";
82           ip_addr <= X"898ad895"; -- 137.138.216.149
83        when "010" => -- CHICAGO LAB 128.135.102.102 = 1DD5727E96
```

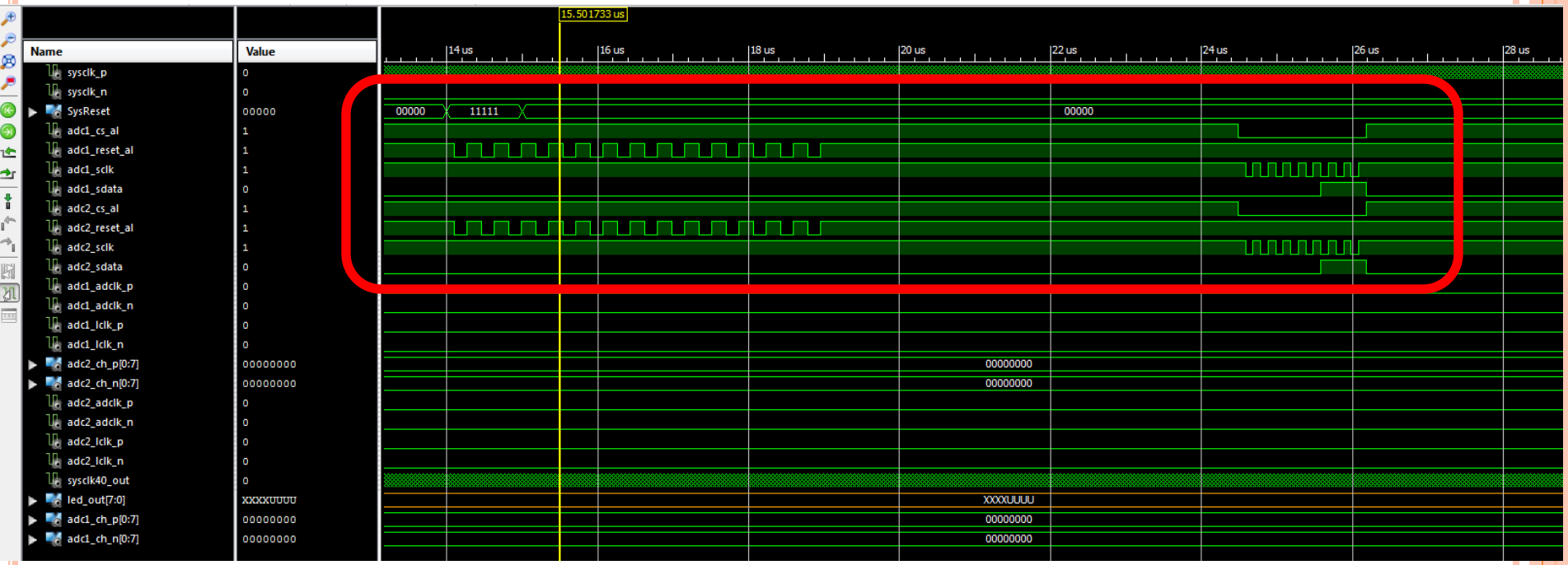
As the same ADCs chips themselves have not changed the similar design algorithms could be used.

Data lines to/ from the ADC board.

- 16 Differential pairs for Data transfer (240MHz)
- 8 Differential pairs for clock synchronisation
- 10 signals to ADC for board setup

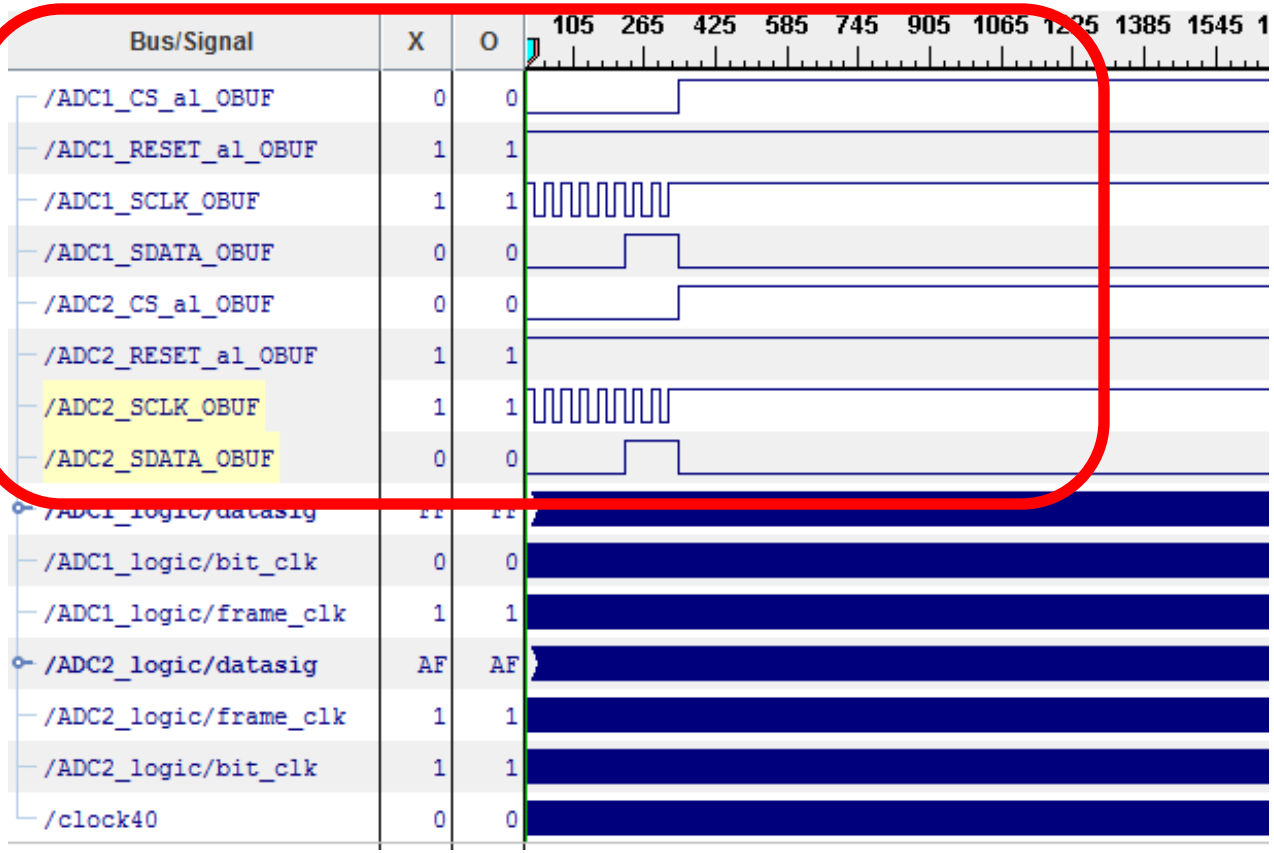


Firmware Simulations

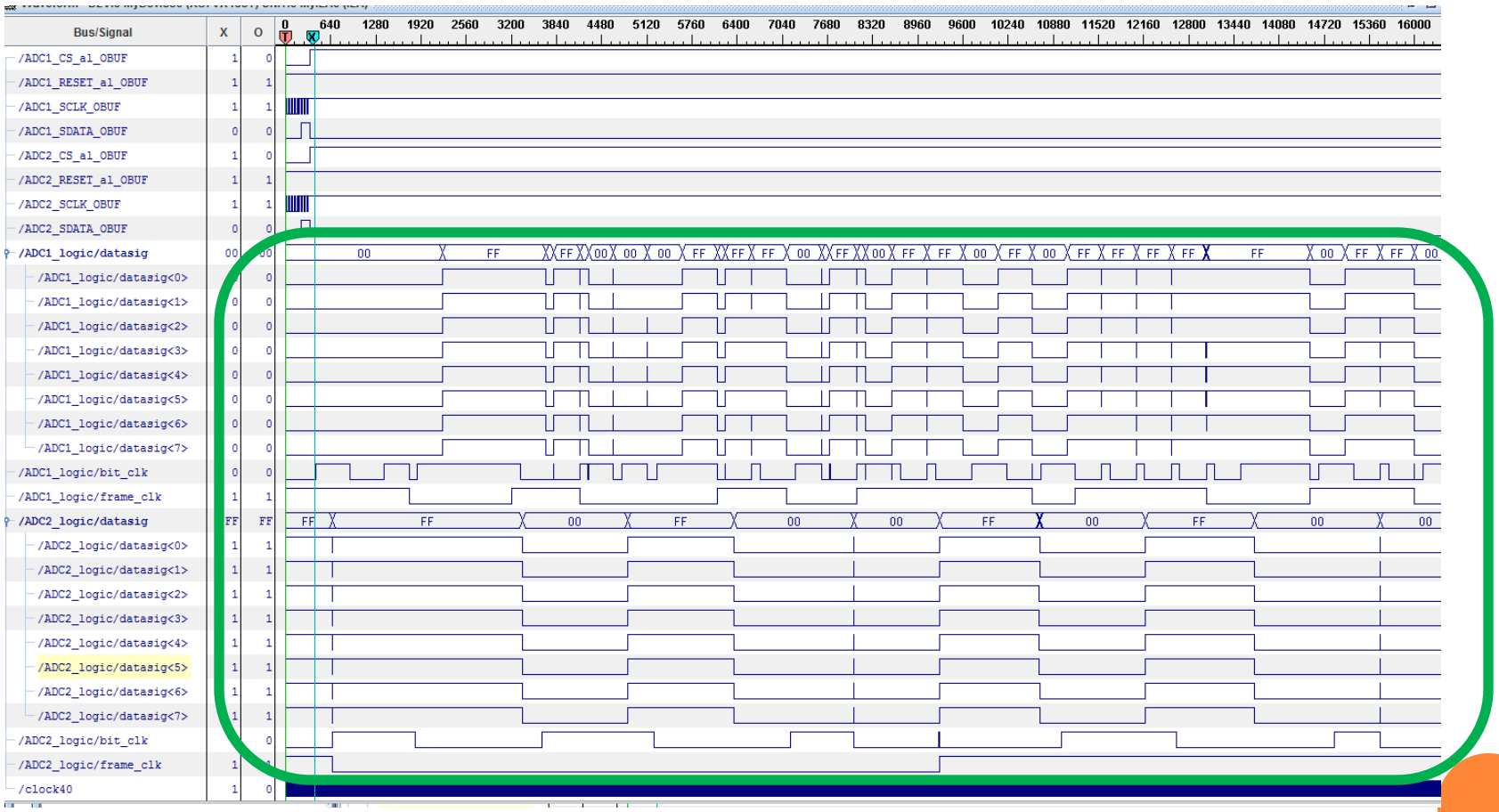


Precise timings needed to set up ADC chips correctly

CHIPSCOPE SIMULATIONS

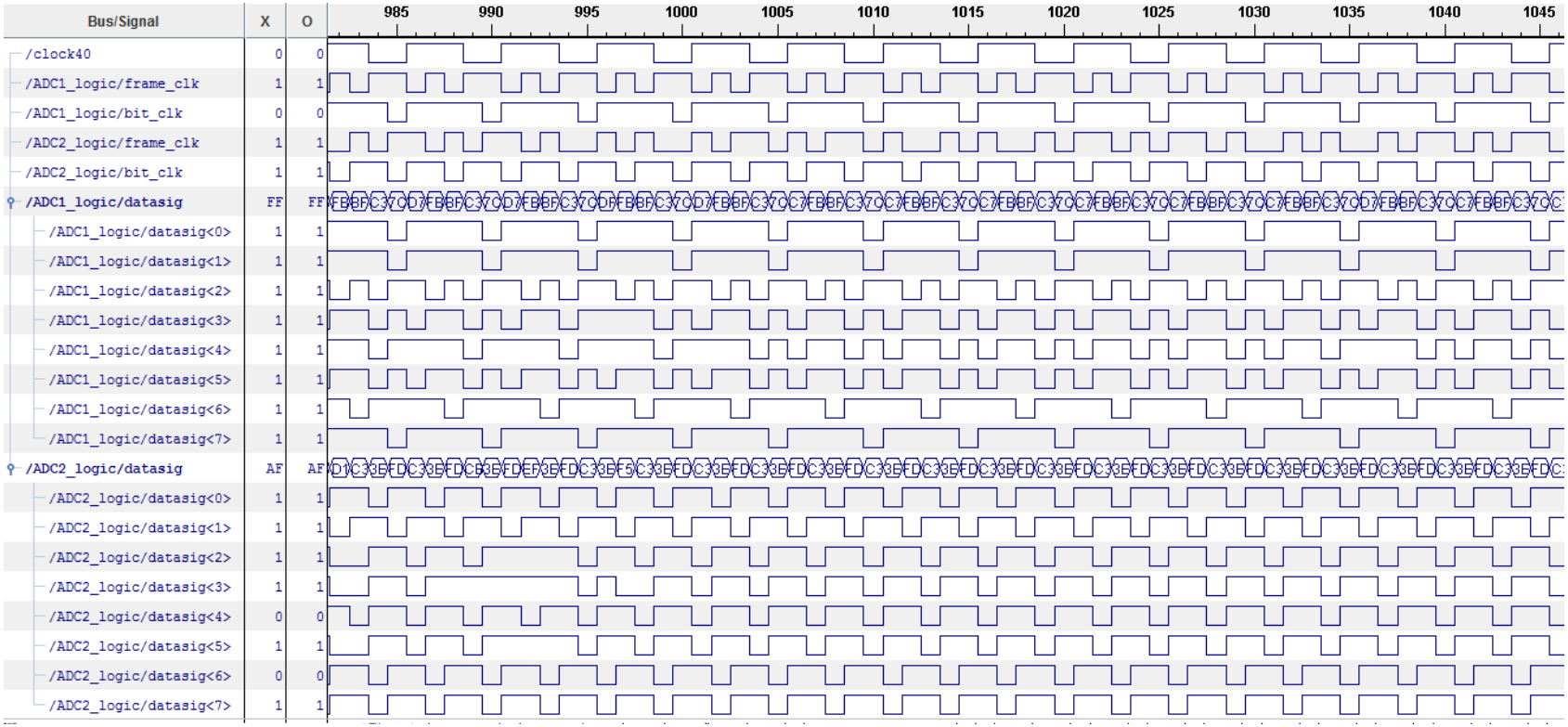


Chipscope Board Testing



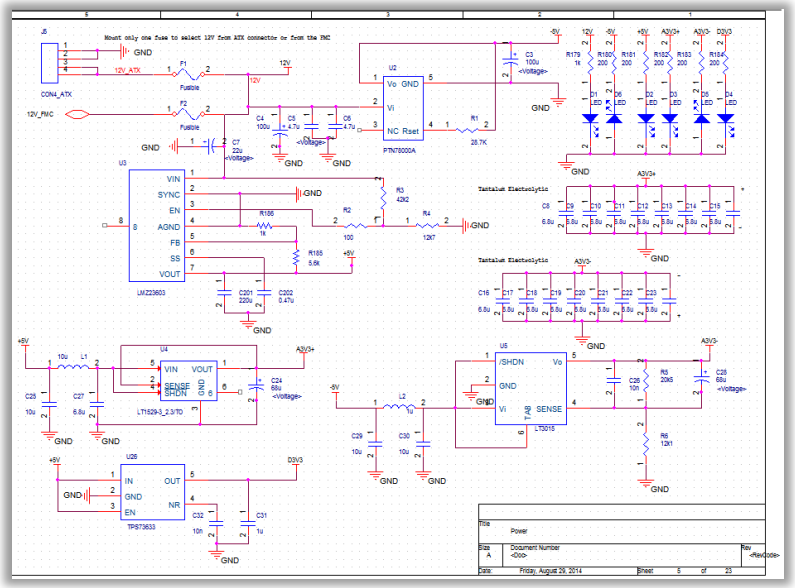
Clocking Issues: 40 MHz not reaching ADCs

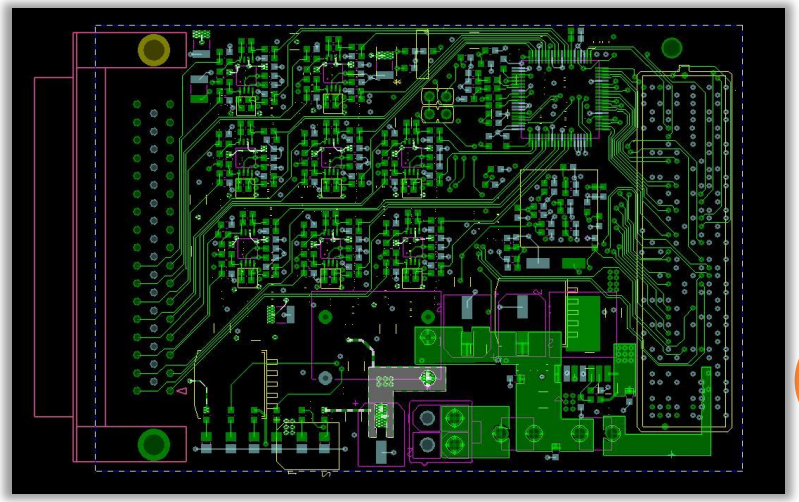
Fixed clocking problems



PCB AND CIRCUIT DESIGN CHANGES

- PCB redesigned to be compatible with VC707 Dev board
- Improved power regulation systems
- Various component footprints changed.
- Repositioned indicator LEDs for easier viewing
- Component & Wire shifting to improve signal quality
- New 20 PIN output added to allow the Prometeo LED driver board to attach





Outlook

- Finalisation of next iteration of ADC board schematics and PCB design (Feb)
- Get quotations for the production of **2 new ADCs boards** (Feb)
- Manufacture of the next ADC board prototype in South Africa (April)
- Finalisation of firmware development (April)
- Testing and validation of the next version of ADC board (July)

Manufacture of 2 new ADC Boards

Questions?