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ATLAS pixel upgrade for the HL-LHC

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Contents

- Introduction
- Layout options of the ATLAS HL-LHC pixel system
  - Challenges
- Pixel module development
  - FE chip
  - Sensors
  - Interconnect
- Mechanics

High Luminosity LHC (HL-LHC)

- Collisions start mid-2025
- Maximum leveled instantaneous luminosity of 7.5 x 10^{34} cm^{-2} s^{-1}
  - from 2×10^{34} cm^{-2} s^{-1}
- 3000 fb^{-1} Integrated luminosity to ATLAS over ten years
  - 6 times LHC operation
- 200 (mean number of) interactions per bunch crossing.
  - Increasing from 55 (2×10^{34} cm^{-2} s^{-1})
  - for bunch crossing time of 25 ns

- Large luminosity extends the energy scales
  - high energy boson-boson scattering,
  - to study the EWSB mechanism,
  - probe for signatures of new physics predicted by models such as SUSY and extra dimensions well into the multi-TeV region
- Large data sample will allow significant improvements in the precision of the measurements of the Higgs couplings
- Requires a detector able to operate after exposure to large particle fluences.
  - **Increased detector occupancy**
  - **Radiation damage**
  - **Bandwidth saturation**

Goal: maintain or improve tracking efficiency and small fake rate + b-tagging capabilities

ATLAS Phase-II Tracker Upgrade

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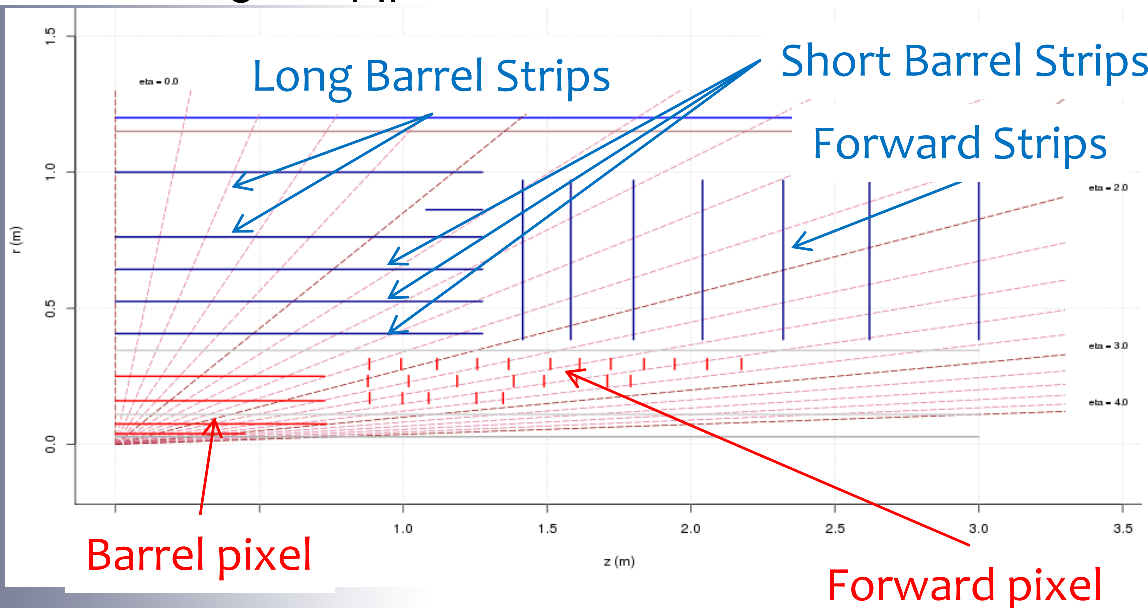
All-silicon inner detector (strips + expanded pixel system)

Full coverage to |η| = 2.7



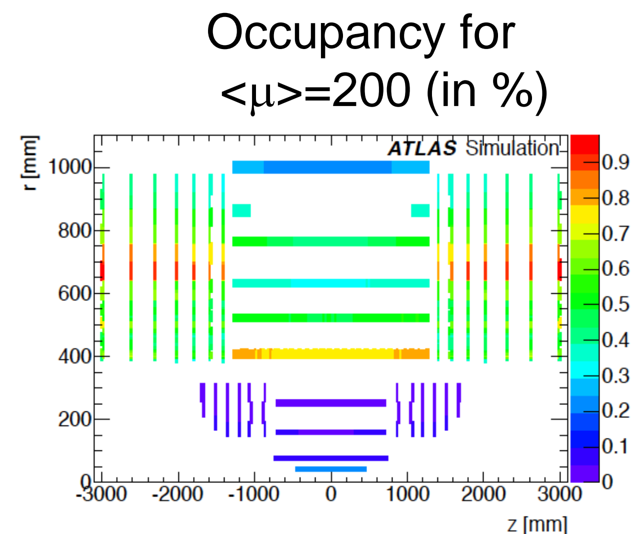


Figure 6.7: Channel occupancies (in percent) with 200 pile-up events.

Baseline IDR layout of the new ATLAS inner tracker for HL-LHC
Aim to have at least 14 silicon hits everywhere (robust tracking)

	Radius (mm)
L1	39
L2	78
L3	155
L4	250

Very high occupancy of first strip layer

ATLAS Letter of Intent
CERN-2012-022
LHCC-I-023

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Layout options beyond the baseline

Higher η coverage

- Track charge particles $2.7 < |\eta| < 4.0$
- Requires extensions to pixel system
  - More end-cap rings
  - Longer inner barrels
- Performance advantages
  - Tracks at high η : Additional information for VBF and soft physics, diffraction events in forward region.
  - Muon reconstruction : need track parameters from ITK.
  - Impact parameter, secondary vertex tagging of heavy flavours : 50 x 50 µm pixels for excellent vertex separation.
  - Jets and E_T^{miss} : pile-up suppression & correction, improved understanding of soft physics.

More pixel layers

- Aim for cost neutrality
- Pressure on on-line & off-line reconstruction performance
- 5 pixel / 4 strip layers should have huge advantage to seed a track over 4 P / 5S
- Better two-particle separation in high pT - jets.
  - Increase track efficiency and reject fakes, improve flavour tagging in dense environment, resolve ambiguities due to photo-conversions

Much work is taking place in the ITK and ATLAS to understand the performance gains and costs of different layout options

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Scale of the extended ATLAS pixel system

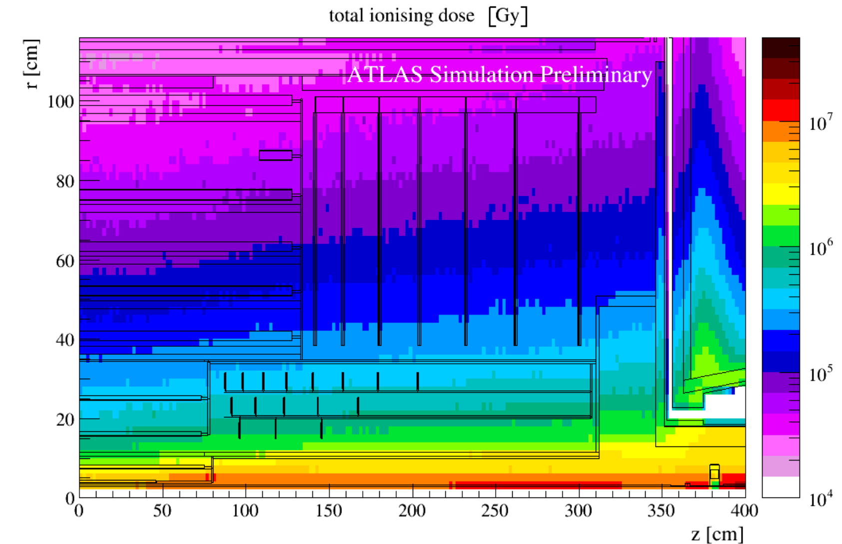
	Yield (%)
Sensor wafers	90
FE wafer	60
Bump-bond	90
Assemblies	95

- An extended pixel system requires low cost pixel modules
- Assumed here a 6th pixel layer
  - 5 pixel layers area = 14 m^2

Item	Baseline (area = 8.76m^2)	Maximum Pixel system extension (area = 18m^2)
Number of good 2&4 chip modules	6436	13033
Number of 2&4 chip module flip-chip starts	7528	15244
Number of FE wafer bump deposition starts	333	684
Number of sensor wafer starts	1356	2785

Radiation modeling
Pixel baseline ring layout

- **Silicon damage (1 MeV) fluences** used to model Pixel and SCT leakage currents and depletion voltages, which allow us to anticipate detector performance over its lifetime, including S/N estimates, and required cooling performance
- **Ionizing dose** measurements important for predicting front-end chip performance
- **Charged particle fluences** allow us to estimate occupancies
- **Radio-activation** estimates can dictate procedures for cavern access and detector installation and maintenance



Pixel structure	Dose (MGy)	Fluence (1MeV neq 10^{14} cm^{-2})
Inner Barrel	7.8	134.6
4th Barrel	0.43	9.4
1st Inner ring	0.95	17.0
Last inner ring	1.13	16.1
1st Outer ring	0.44	8.2

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Data rates

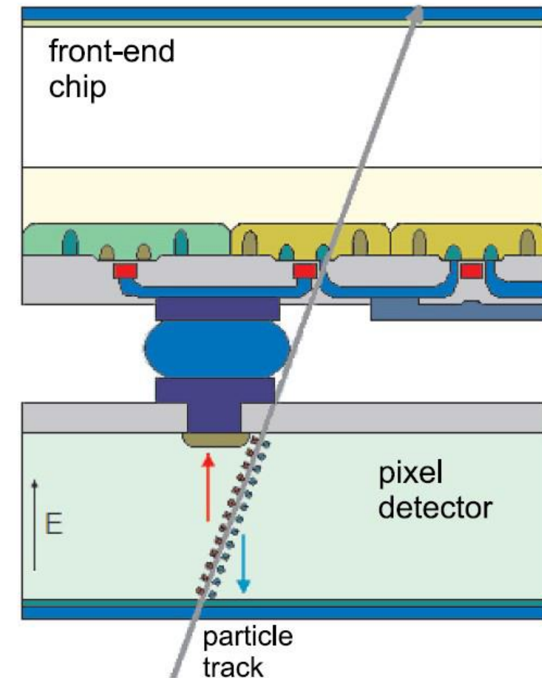
- Trigger requirement
  - BC : 40 MHz
  - <L0 accept rate> : 1 MHz
  - Latency : 6 μs
- Readout pixel detector fully at L0
- Simulation say for inner barrel layer :
  - Hit rate = 2 GHz/cm^2
- 1 MHz trigger rate
  - ➔ 50 MHz/cm^2 hit rate
  - ➔ 168 MHz/chip (FEI4 size)
- Data size : 16 bits/hit
  - ➔ 2.7 Gbps/chip
- But need low latency
  - need to account for hit rate and trigger rate fluctuations
  - ➔ **5 Gbps/chip** for inner barrel layer

Pixel Detector	Module type	Rate/module (Mbps)
Barrel L1	2 chip	5120/chip
Barrel L2	Quad	2 x 4000
Barrel L3	Quad	5120
Barrel L4	Quad	2560
Inner Ring	Quad	2560

Assumes data on a quad multiplexed together

Pixel Module

- Baseline is well understood hybrid pixel module concept
  - 50 µm x 50 µm Pixel size
- FE chip
  - New chip required
  - Smaller pixels due to increased occupancy
  - Higher data rates
  - Higher radiation hardness
- Sensor
  - Higher radiation hardness
  - Higher efficiency with smaller pixels
  - Cheaper for higher radii
  - Planar, 3D-silicon, diamond
  - CMOS sensor coupled to FE chip
- Interconnect
  - Same minimum pitch as before, but 5X more per die
  - Cheaper & faster solutions for outer radius
  - Thinner FE chips for inner radii



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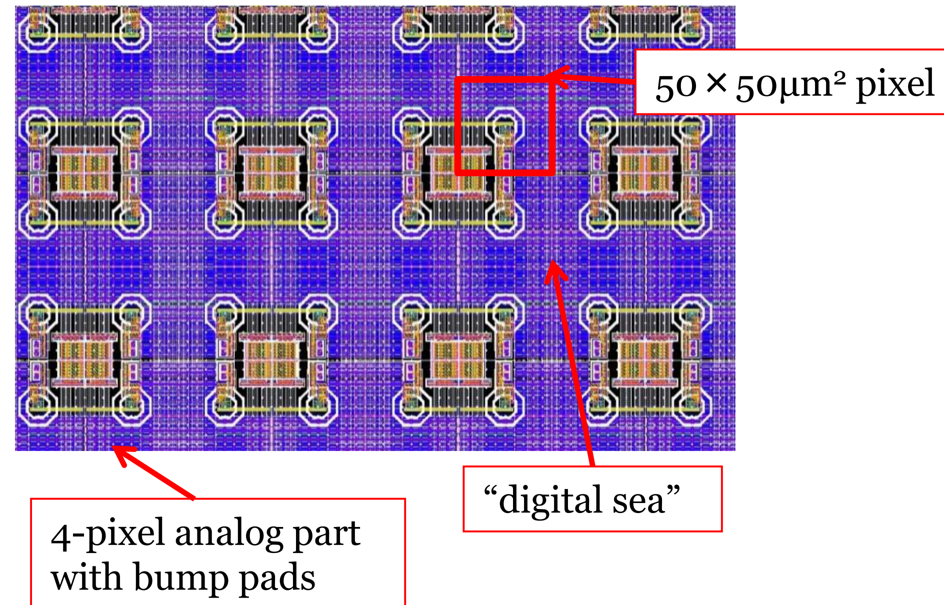
Pixel module development – FE chip

- Format & power similar to FEI4
- “New” CMOS node and vendor
  - 65 nm with TSMC
- Joint development ATLAS & CMS
  - RD53 – share resources
  - Several prototypes fabricated and under test
- Radiation tolerance challenge
  - Damage mechanism empirically characterized
  - Can produce design spec for required 1 GRad target
- Pixel layout
  - 4-pixel analogue section
  - Surrounded by synthesized Digital sea
  - 50 μm minimum pitch to allow “standard” flip-chip
- Timescale
  - First 12 x 12 mm prototype RD53-P1 chip April 2016

- 50 x 50 μm pixel size
- Pixel recovery time 200 ns
  - Gives 1% inefficiency
- Nominal pixel capacitance 100fF
  - Less room ∴ simpler design
- Nominal pixel current 10 nA
  - -20°C at max fluence



See talk on Friday
by Mauricio Garcia-Sciveres
RD53: new developments

Pixel module development – Planar sensor Outer layers

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Cost reduction the main driver

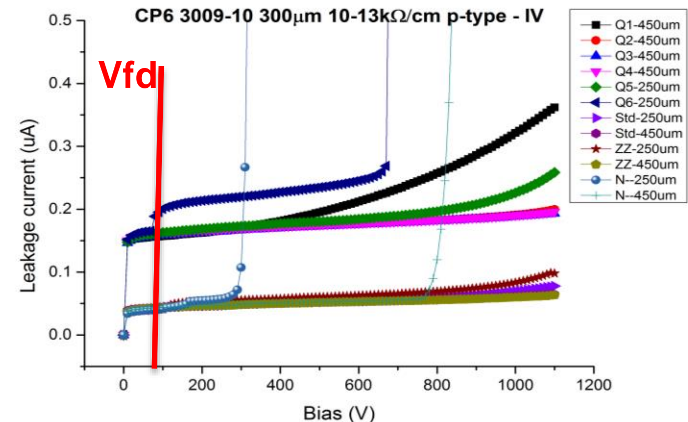
- Largest wafer size possible
  - Reduces processing costs
  - 150 mm today, 200 mm in future?
- Largest module size from single sensor
  - Quad 40 x 40 mm^2
  - Reduces flip-chip costs
  - Additional benefit from large format FE chip
- n-on-p sensor technology
  - Single sided processing - reduces costs
  - Lower resistivity wafers as don't need to full deplete
- Charge collection
  - n-on-p allows operation under depleted after irradiation
  - Reduces power dissipation (lower V required)
  - Thickness ~ 200 μm to keep costs reasonable

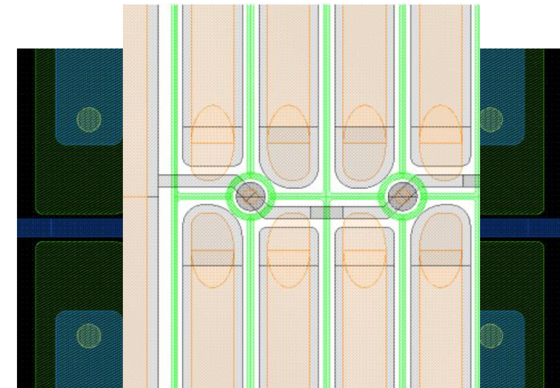
Development focused on yield

- Optimization of bias and edge implants to get near 100% sensor yield

Layout challenge for Quad modules and 50 x 50 μm^2 pixels

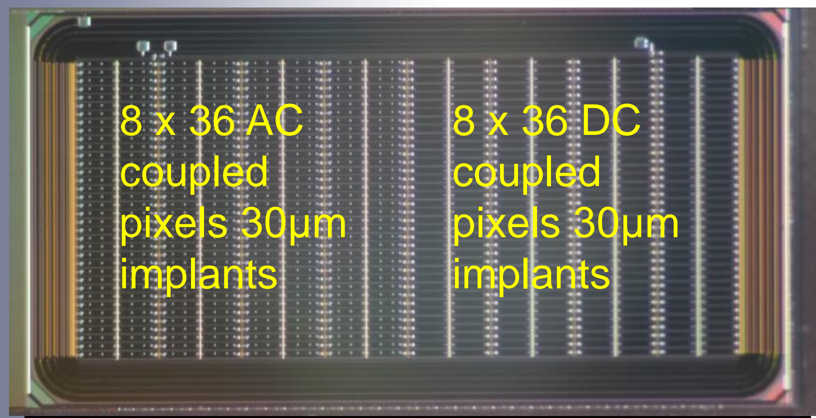
- Need to avoid dead space between FE chips
- Additional load capacitance constraint an issue (<100 fF per pixel)

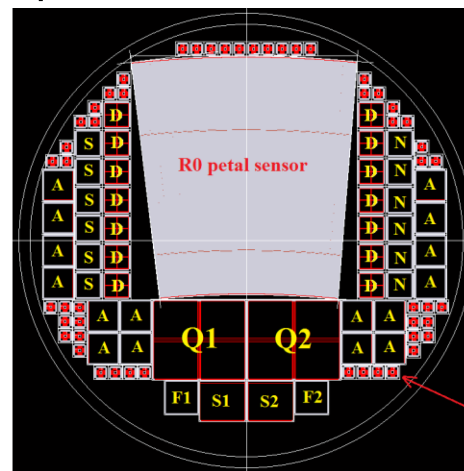




Pixel module development – Planar sensor Outer layers

- CMOS passive sensors for lowest cost option
- Largest wafer size (200 mm)
- Higher throughput lower cost industrial production facilities
- Resistors and capacitors available
  - Resistive biasing networks and AC coupling options easily implemented
- Multiple metal layers possible for signal routing
- Prototypes being produced at LFoundry and Infineon
  - High resistivity p-type substrates (kΩ cm)
  - AC and DC coupled versions
  - Variation of implant width to study capacitive load and detection efficiency



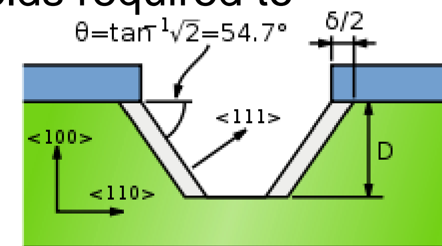


R0 petal sensor
Q1 - quad FE-I4 pixel
Q2 - quad FE-I4 pixel NO bias
S1 - single chip FE-I4 pixel AC
S2 - signle chip FE-I4 pixel DC
F1 - 50x50 pixel sensor AC
F2 - 50x50 pixel sensor DC
A - 15x15 mm strip sensors 50u pitch (256 channels)
S - 10x10 mm strip sensors 80u pitch 800u edge
N - 10x10 mm strip sensors 80u pitch 450u edge
D - 10x10 mm diodes with different passivation options
5x5 mm photodiodes

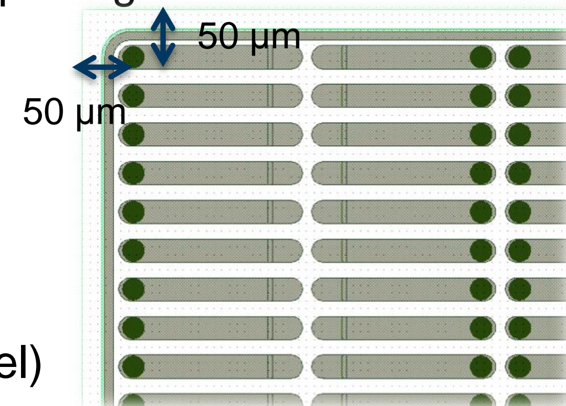
Pixel module development – Planar sensor Inner layers

Radiation hardness and material are the main drivers

- Thin sensors
  - Thin sensors reduce applied bias voltage to obtain high E-fields required to maximize charge collection
  - Less power dissipation
  - Further from breakdown voltage
  - Additional benefit of reduced material
  - Processing thin free standing wafers at 150 µm (Micron, HPK)
  - 50 µm thick from Advacam with wafer bonding process
  - 75 - 100 µm thick from CIS with backside etch into supporting wafer
- Bias structure optimization
  - Efficiency drops due to bias dot / rail after irradiation
  - Poly-silicon bias resistors rather than bias dots
  - Bias rail inside pixels or shielded by p-stop
- Better efficiency via reduced dead edge
  - Dicing close to the guard ring (Micron 250 µm from pixel)
  - Side wall implantation to make active edges at Advacam & FBK



Anisotropic wet Etching (KOH) on <100> wafers



FE-I4 with 50 µm edge, 1 GR, no punch-through structure

Pixel module development – 3D sensor

Successful installation of 3D sensors in ATLAS IBL

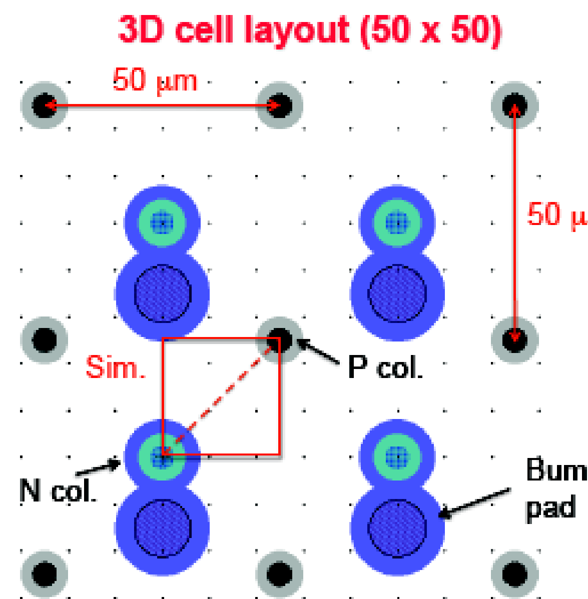
- 3D an option for innermost ATLAS ITK layer
  - Requires less bias voltage and therefore dissipates less power
    - Lower thermal conductivity of support structure before thermal run-away
  - Active edge (or very slim) increase efficiency of device.
    - Slim edge of 100 μm
  - Smaller clusters than planar at high track incident angles, high η

ATLAS ITK Requirements

- Smaller pixels and higher radiation hardness require:
  - Smaller inter-electrode spacing & ∴ small column diameter
- New FE ➔ low capacitance sensor <100 fF / pixel

Developments

- Thinner 3D sensors
  - Reduces cluster size at high eta, avoids cluster merging in the dense HL-LHC environment
- Smaller inter-electrode spacing from reduction in 3D column diameter
  - Minimize dead material
  - Reduces capacitance load to < 50 fF per 50 x 50 μm^2 pixel
  - Thinner sensors with a fixed aspect ratio (FBK)
  - Improving the aspect ratio (CNM)



See talk on Wednesday by Joern Lange
Recent Progress on 3D Silicon Detectors

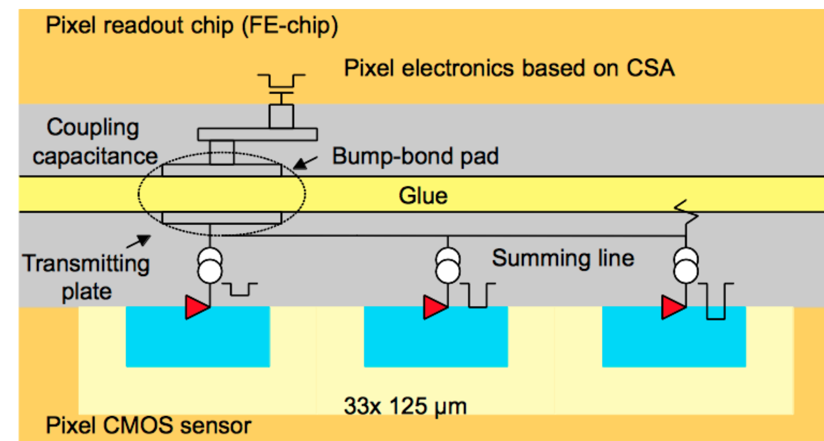
Pixel module development – CMOS sensor

- CMOS imaging sensors existed since many years
- CMOS active pixels (MAPS) Signal generation in epi-layer & collection by diffusion : 1997 ➔
  - Dierickx, Meynants, Scheffer (1997), Turcheea (2001), Deptuch, Dulinski, Winter (2001) ... -> STAR pixel detector (2006 – 2014)
- CMOS pixels with "fast charge collection" (depleted) : 2007 ➔
  - Peric (2007), Snoeys (2009), Hemperek (2012)
  - Drift collection
  - Suitable for high rate (in-time collection) and high radiation environment
- Attach CMOS to standard FE and gain a "smart sensor"

See talks on Wednesday by Steven Worm & Mathieu Benoit
HR-CMOS & HV-CMOS Developments

CMOS advantages

- Cheap sensor : Commercial CMOS process on 200 / 300 mm wafers
- Cheap interconnect : AC coupled with glue → no bumps ?
- Very thin (15 μm !) ∴ less material, reduces cluster size at large eta
  - Improves two track separation
- Sub-FE pixel resolution possible
  - CMOS pixel can be smaller than FE & output encoded signal to FE

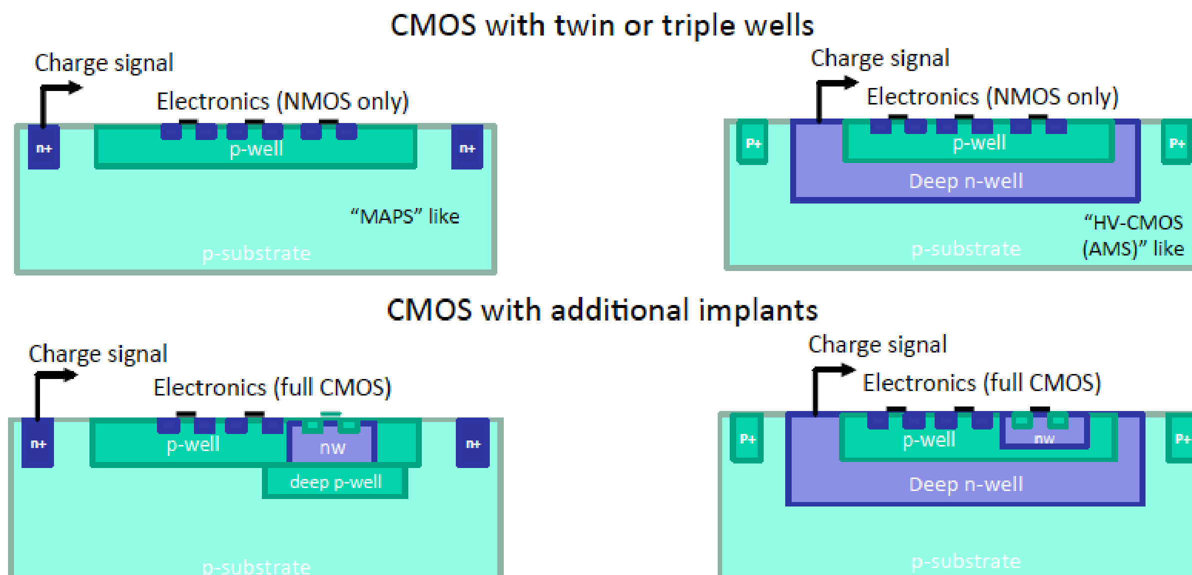


CMOS pixels in ATLAS Pixels

Collaboration inside ATLAS pixels to develop demonstrator

- Outside (Inside) electronics
  - Small (Large) sensor capacitor
  - Low (High) noise
  - Low (High) power
  - Small (Large) fill factor
  - Less (More) rad hard

- Many design issues to address
  - In-time charge collection
  - R/O in 1 BC (25 ns)
  - Homogeneous charge collection to avoid zones with low efficiency
  - Minimize input capacitance to amplifier (for speed and noise)
  - Rad hard & sufficient signal for FE
  - Coupling to FE : Glue or SnAg bumps

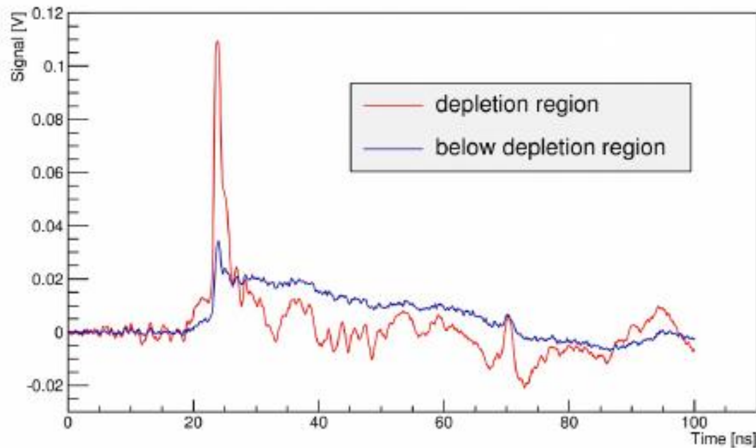


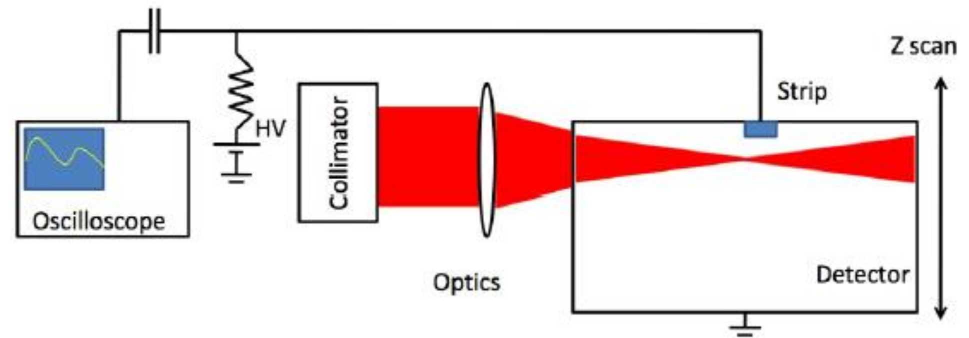
Electronics outside collection well

Electronics inside collection well

Edge TCT results on depletion zone AMS-180nm HV CMOS (10 Ωcm)

- Measure charge from 100x100 um diode on the edge
- Clearly see timing difference between depleted and diffusion regions





U_{bias} [V]

t<2.5ns Drift

t>2.5ns Diffusion

~20µm

-z [mm]

x [mm]

Collected charge [a.u.]

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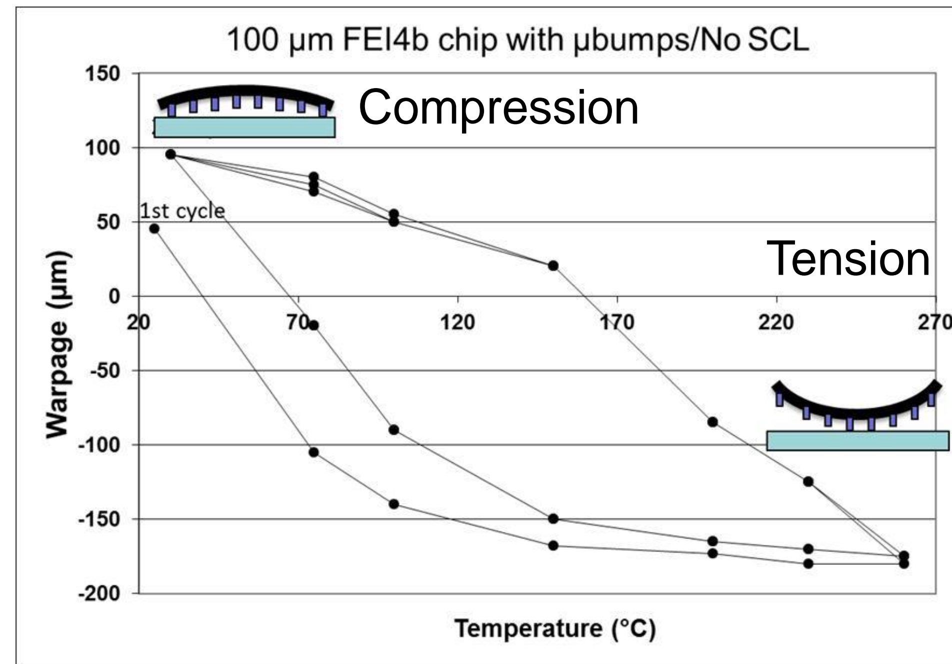
Pixel module development – Interconnect

- 2 challenges
  - Thinner (lower material) modules for inner radius layers
  - Cheaper interconnect processing for outer layers
- Thin ROIC bow during solder reflow process
  - Results in many open bumps
- Solutions
  - Low temperature solder

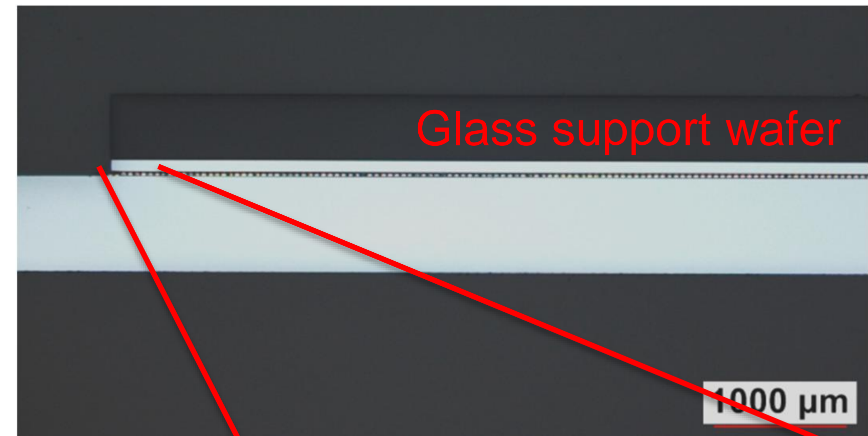
  Indium room temp compression
  - Reflow under vacuum chuck (Selex)
  - Temporary wafer bonding for ROIC stability (IZM)
  - Backside compensation layer to counteract bow from front side stack (HPK, CEA LETI)

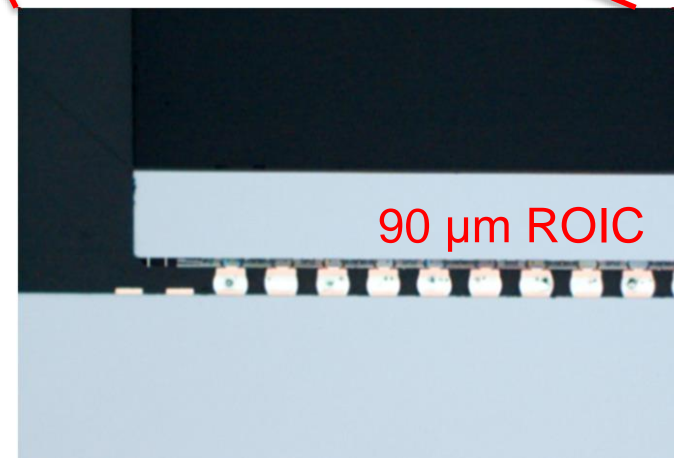


How to live with bow issue

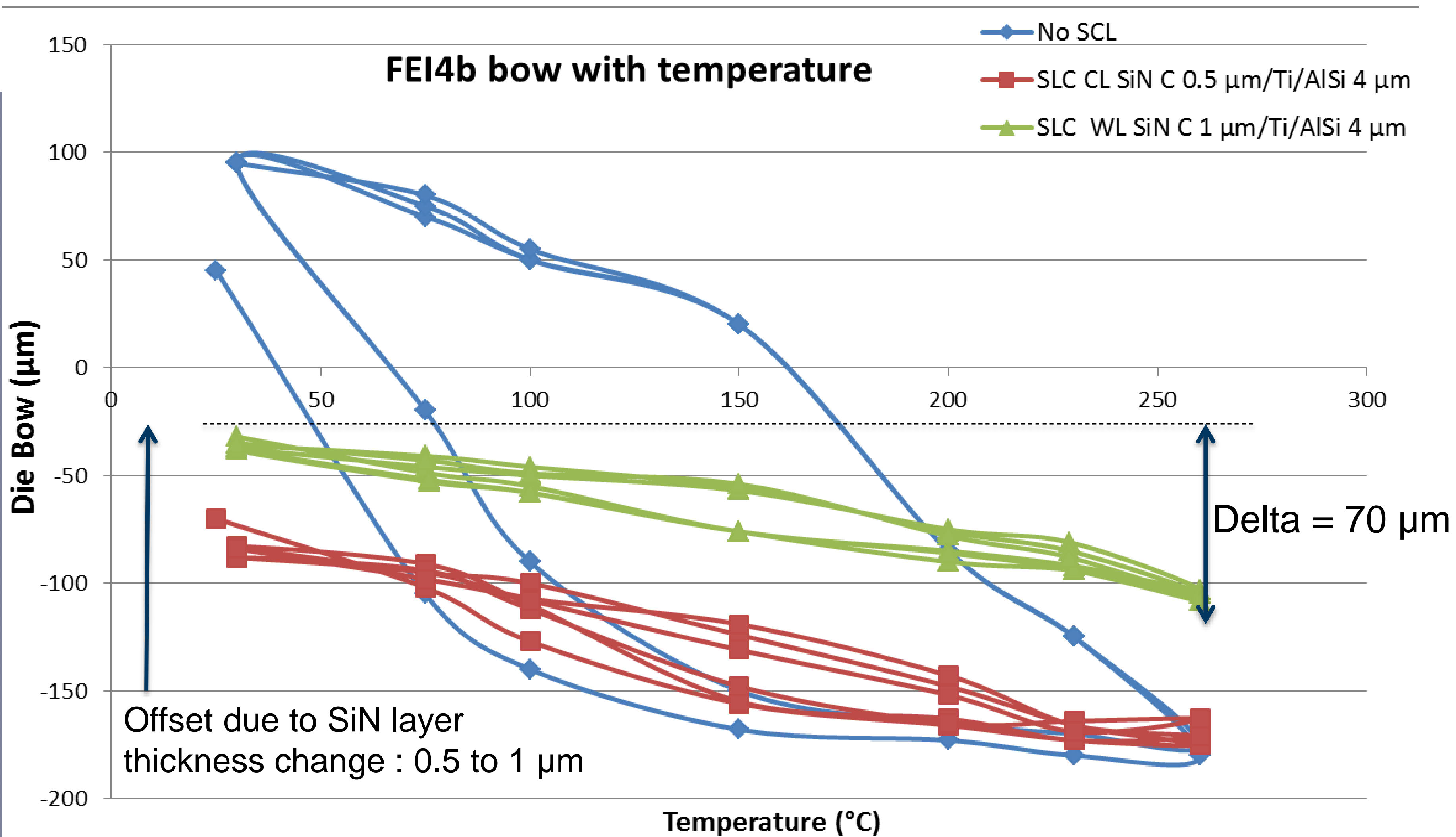
- Temporary bond thinned ROIC (150 µm) to thick glass support wafer
- Process wafer and flip-chip
- Laser Release support wafer
- Used for IBL
  - ~850 modules
- Limitations
  - speed & cost of processes
  - Heat, laser/UV glue removal, melts bumps with very thin ROIC
- Work on going to improve yield, throughput, cost.

- No open bonds



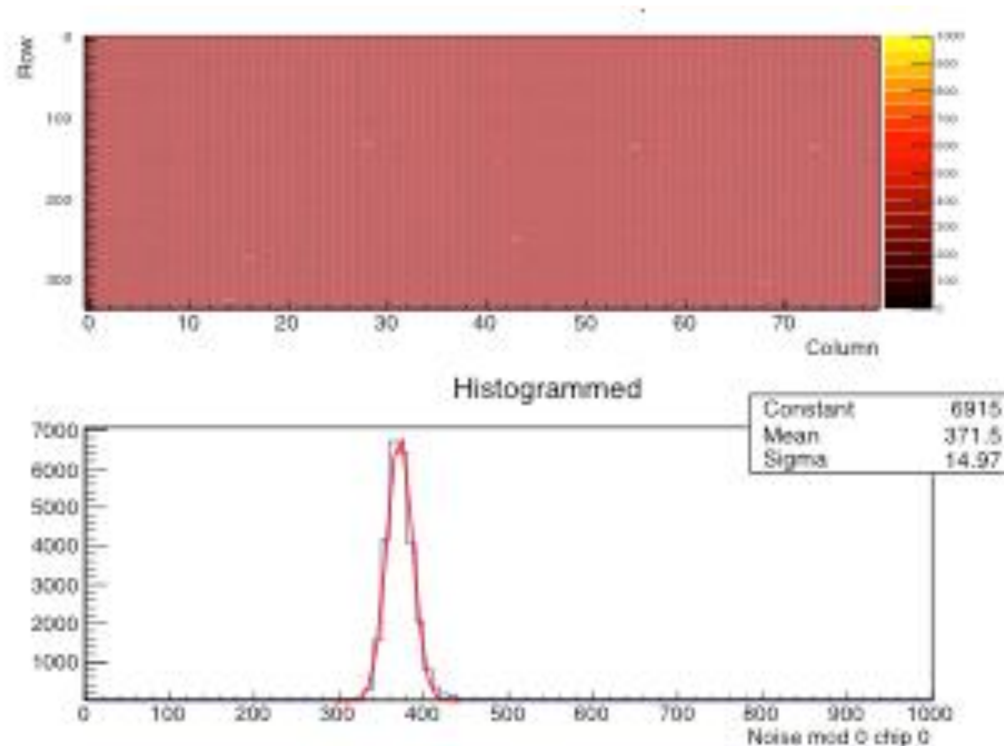


Backside stress compensation + bumps CEA LETI - Summary of bow with Al SCL



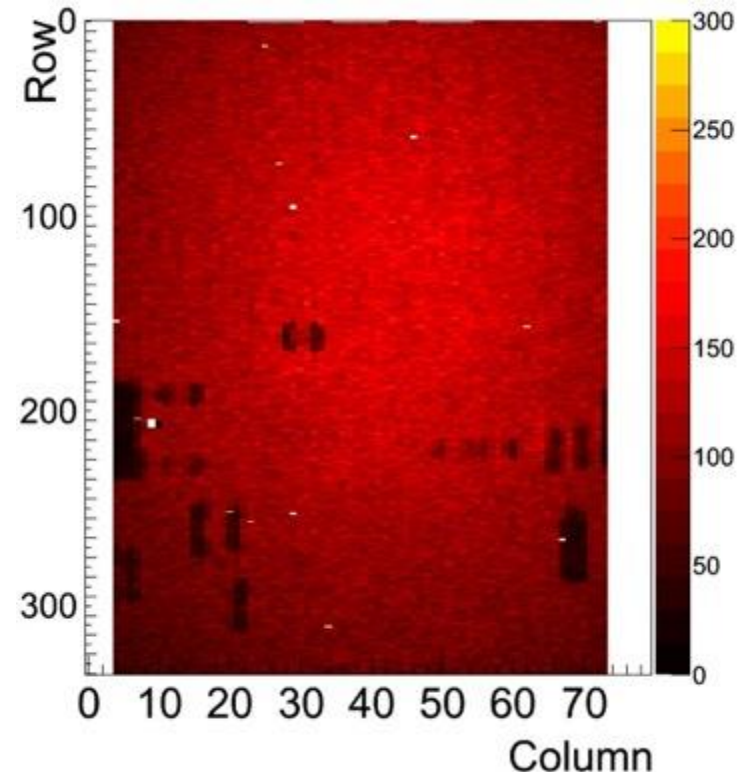
Fully bonded 100 µm thick ROIC with SCL

- 300 µm thick sensor, 100 µm thick ROIC
- Noise plot with detector bias = 0V
  - High capacitance load on FE (370 electrons)
  - HV on noise is 120 electrons
- All pixels show high noise ∴ all pixels bonded



Pixel module development – Interconnect Indium bumps

- "Indium" bump bonding
  - Low temperature process
    - Reduced warpage
- HPK
  - Sensor/ASIC thickness: 150/150 μm
    - no back-compensation in ASIC
  - Thin Quad-module, 3 samples
    - with the "Matrix" jig for both sides.
  - No large area bond opens after flip-chip and thermal cycling
- RAL-STFC
  - Indium bumps through thick resist
    - Lift-off process
  - Room temperature mechanical compression (30C)
  - Mechanical scrub during flip-chip
  - To date working thick assemblies
- Selex Indium
  - Stress relief process is applied to wafer after thinning
  - Flip-chip step slightly modified, temperature to below 50° C before releasing the pressure



100 μm thinned FE-I4A

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Pixel module development – Interconnect Low cost options

- UBM at sensor foundry
  - UBM presently produced as an additional process at bump deposition vendor
  - UBM deposited at sensor foundry will reduce costs
  - For example: CIS mask-based electroless Ni-Au UBM, shown to work on SnAg solder bumps, or cheaper still mask-less Ni-Au UBM
- Chip to Wafer bonding
  - Large sensors and large ROIC die are an intermediate step
  - Bond chip to sensor wafers and dice after flip-chip
    - Can't bond to ROIC wafer as yield too low
  - Requires TVSs
    - Need to be able to route signals from edge of ROIC which overlap sensor
- Adhesive bond
  - Either Anisotropic glue or AC coupling
  - AC coupling better suited for CMOS sensors than planar
    - With planar need very thin glue layers to prevent charge loss to neighbouring pixels

Mechanics

- Several different approaches under investigation
- Same goal
  - Low mass, thermally conductive and stable supports for pixel modules
- All carbon solutions (CFRP, carbon foams, TPG, C-C)
  - With Ti cooling pipes
- CO_2 cooling refrigerant : -35°C coolant temperature
- Thermal Figure of merit defined to avoid thermal run-away
  - Additional requirement to avoid excessive detector current / pixel
  - < 10nA / pixel after max fluence
- Classic Barrel + Endcap design
  - I-Beams to maximize stability / unit mass of material
- More dynamic layouts with module orientation changing along longitudinal direction to minimize particle path through silicon

Design Activity

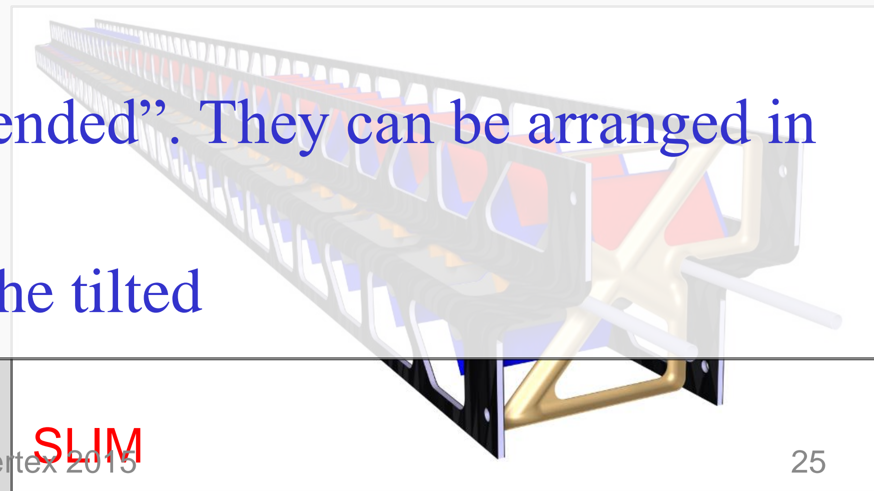
- There are several concepts for the local supports…

Note

- The different designs can be grouped into two families: **tilted** or **classic**
- *This is the only difference that has an impact to the layout.*

For example:

- all the classic staves can be "extended". They can be arranged in almost all radii, etc …
- Same consideration is valid for the tilted



CLASSIC

TILTED

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Summary

- HL-LHC Pixel system is under development
- Much to be decided in the next year
  - Layout – higher eta coverage, number of pixel layers
- Many challenges still ahead
  - FE chip design and production
  - Sensor choice
  - Interconnect optimization for sensor and layer
  - Mechanics (still many options)
- Schedule driven by
  - TDR in 2017
  - Module build & stave loading to take ~ 2 years from 2020
  - Install in 2023-24