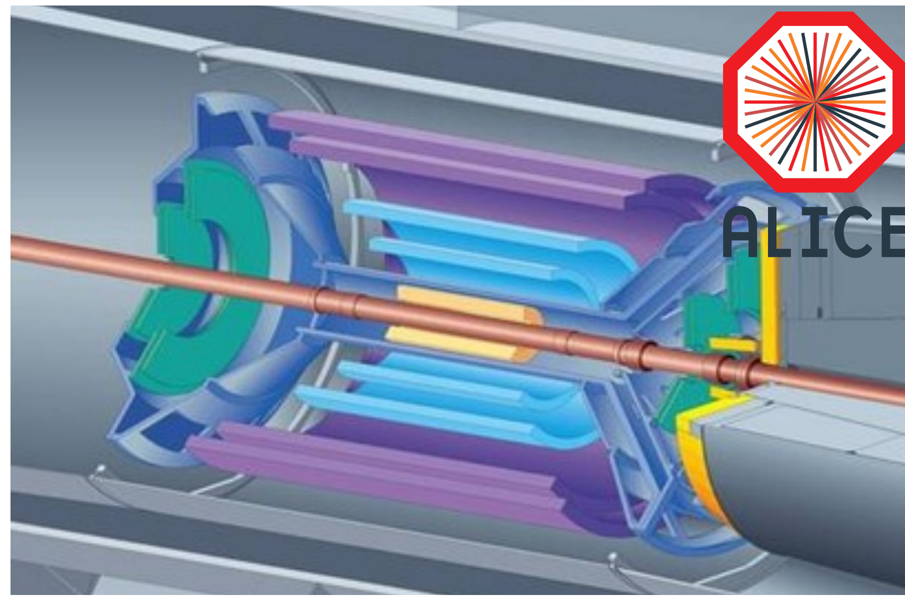
VERTEX 2015

THE 24TH INTERNATIONAL WORKSHOP ON VERTEX DETECTORS

1-5 JUNE 2015

SANTA FE, NEW MEXICO, USA

ALICE ITS: the Run1 to Run2 transition and recent operational experience



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on behalf of the ALICE Collaboration

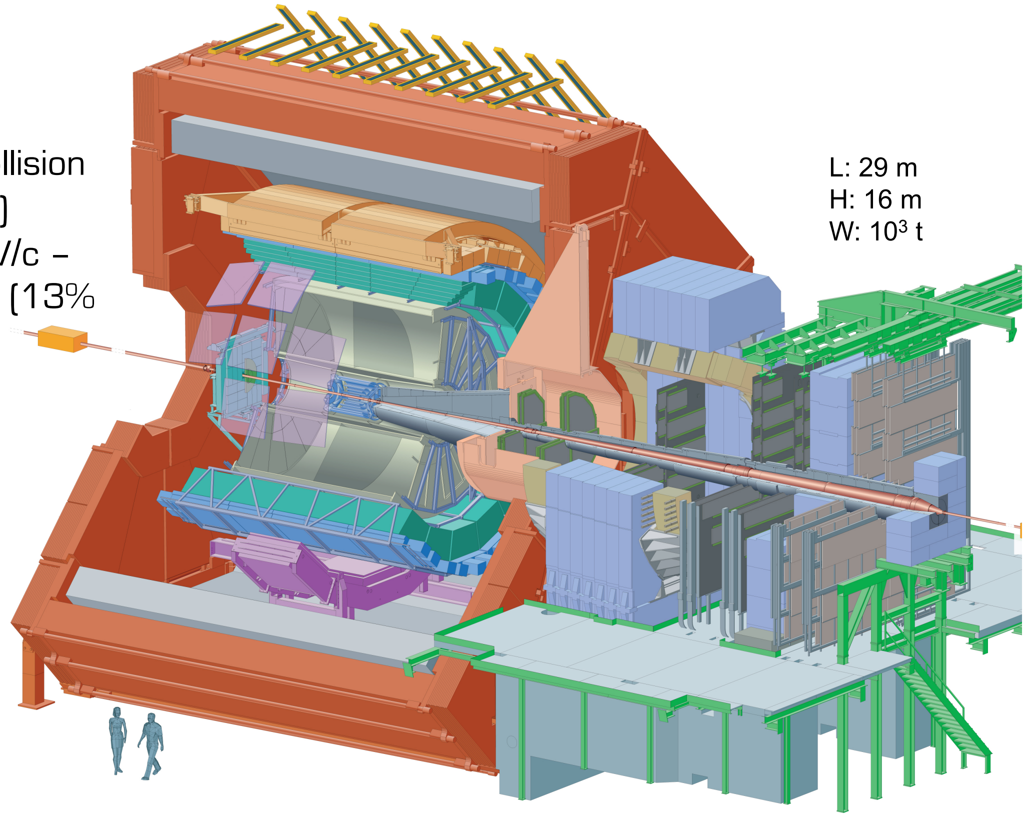
Contents

- ALICE experiment
- ITS layout
- Run1 performances
- Operations from Run1 to Run2
- Summary

ALICE experiment

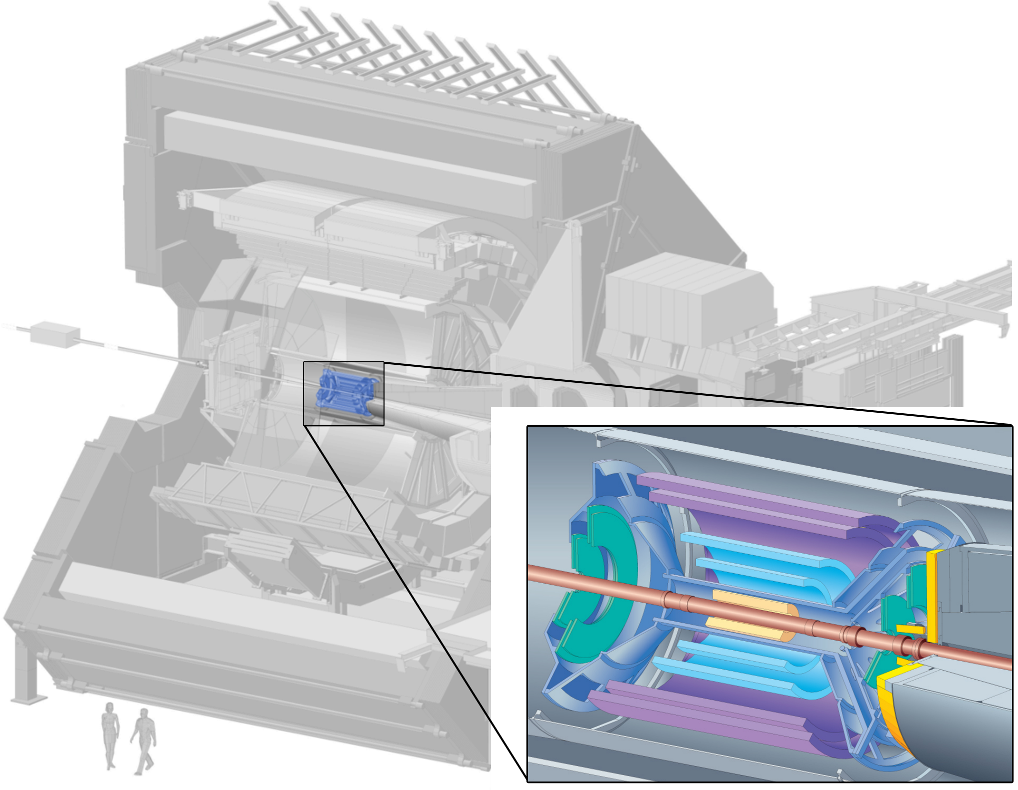
- **A L**arge **I**on **C**ollider **E**xperiment at the LHC
  - Dedicated to the study of strongly interacting matter under extreme conditions of energy density and temperature
  - pp and p-Pb collisions study intended as a reference for understanding of heavy-ion physics and as genuine physics interest

- Tracking in central barrel
  - Pseudo-rapidity coverage $|\eta| < 0.9$
  - Powerful tracking in the high density Pb–Pb collision environment (up to150 points along the track)
  - Wide transverse momentum range (100 MeV/c – 100 GeV/c) thanks to the low material budget (13% X_0 for ITS+TPC) and the moderate solenoidal magnetic field (B = 0.5 T)



- Particle identification
  - Combined PID based on several techniques: dE/dx, time of flight, transition and Cherenkov radiation, calorimetry and topological reconstruction

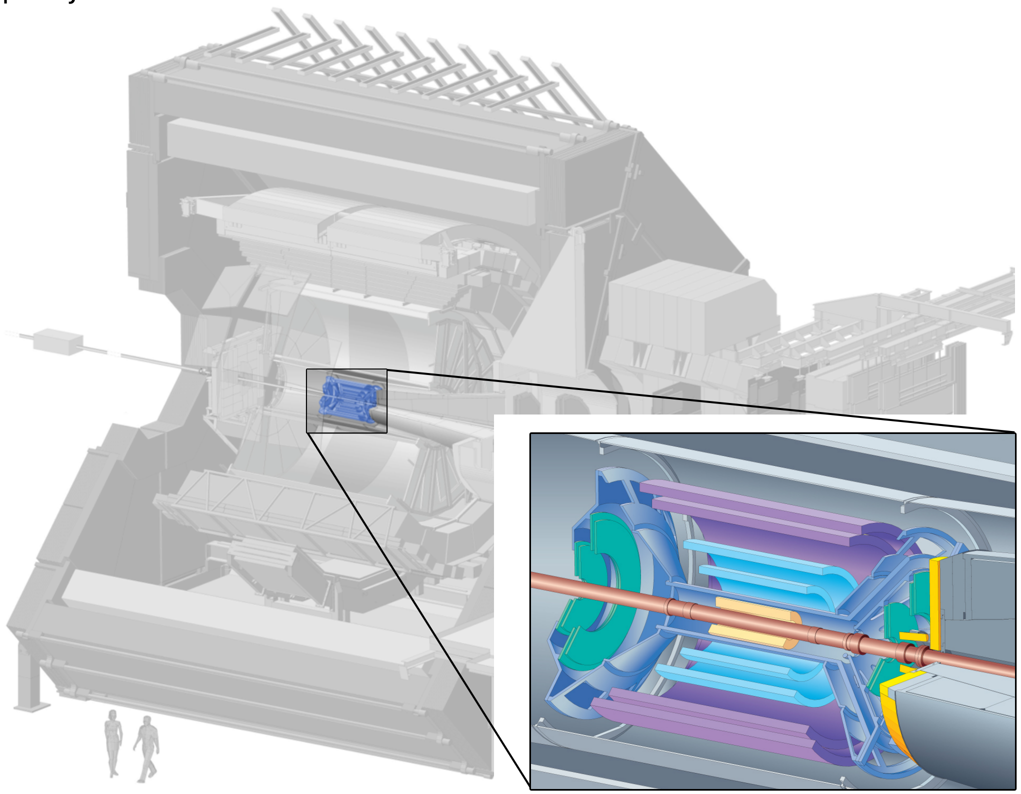
Inner Tracking System



Inner Tracking System

- The ITS tasks in ALICE
  - Improve primary vertex reconstruction, momentum and angular resolution of tracks from outer detectors
  - Secondary vertex reconstruction (c, b decay) with high resolution
  - Tracking and PID of low p_T particles, also in stand-alone
  - Prompt trigger capability (< 800 ns latency) → contribution to ALICE Level-0 trigger
  - Measurement of charged particles pseudo-rapidity distribution
  - Pileup rejection

- Detector features
  - Capability to handle high particle density
  - Good spatial precision
  - Minimize distance of the innermost layer from beam axis
  - Limited material budget
  - Analogue information for particle identification via dE/dx (outermost 4 layers)



Inner Tracking System

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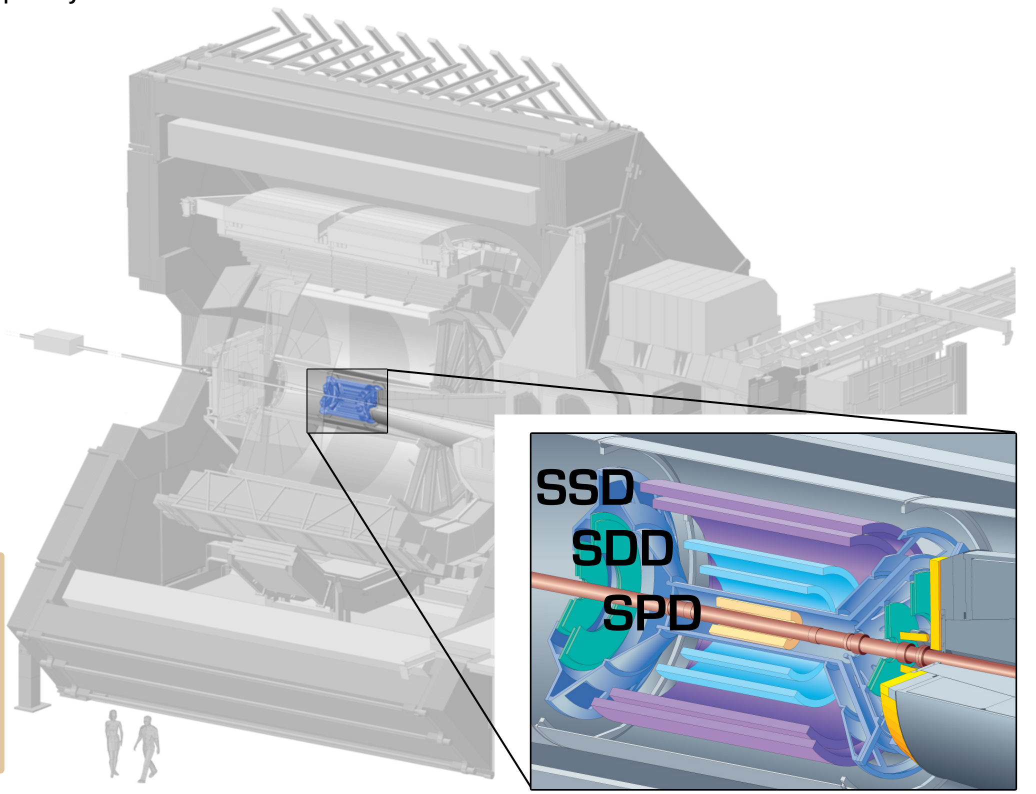


3 different technologies

① 2 layers of Silicon Pixel Detector (SPD)
② 2 layers of Silicon Drift Detector (SDD)
③ 2 layers of double side Silicon Strip Detector (SSD)

Inner Tracking System

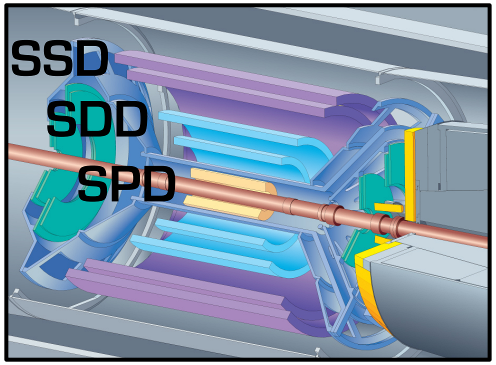
Layer	Det.	Radius (cm)	Length (cm)	Surface (m²)	Chan.	Spatial precision		Cell (μm²)	Max occupancy central Pb-Pb (%)	Power dissipation (W)		Material Budget (% X/X_0)
						rφ (μm)	z (μm)			barrel	End-cap	
1	SPD	3.9	28,2	0.21	9.8M	12	100	50x425	2.1	1.35k	30	1.14
2		7.6	28.2						0.6			1.14
3	SDD	15.0	44.4	1.31	133k	35	25	202x294	2.5	1.05k	1.75k	1.13
4		23.9	59.4						1.0			1.26
5	SSD	38.0	86.2	5.0	2.6M	20	830	95x40000	4.0	850	1.15k	0.83
6		43.0	97.8						3.3			0.86

Design constrains

- Radius defined by beam-pipe (inwards) and requirements for track matching with TPC (outwards)
- Average material traversed by a straight track perpendicular to the surface is ~1% X_0 per layer

Control, calibration and monitoring systems

- Detector Control System (DCS) dedicated for each sub-detector to remotely control the underground hardware
- Specific calibration strategy for each sub-system:
  - SPD: Noisy pixels map
  - SDD: baseline and Noise, Gain, Drift speed
  - SSD: Baseline and Noise
- Independent data monitoring to control the quality of the data and promptly spot mis-configuration during data-taking



Inner Tracking System - SPD

Layer	Det.	Radius (cm)	Length (cm)	Surface (m^2)	Chan.	Spatial precision		Cell (μm^2)	Max occupancy central Pb-Pb (%)	Power dissipation (W)		Material Budget (% X/X$_0$)
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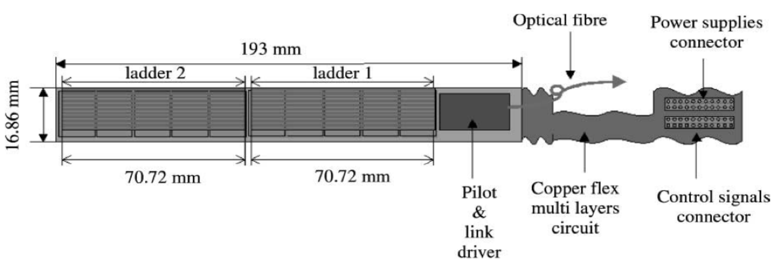
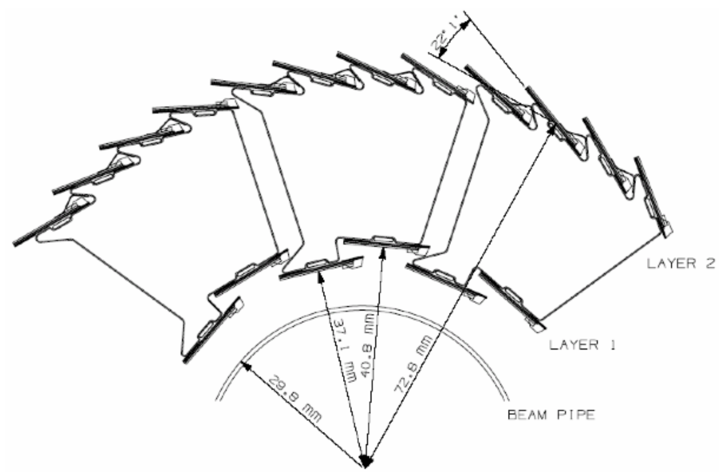
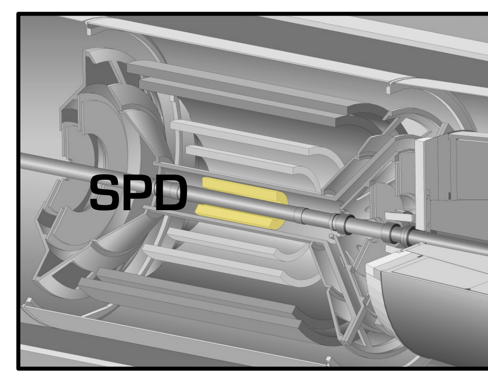


- 120 modules (half-staves, HS) grouped in two half barrels
  - Each semi-barrel divided in 10 semi-sectors containing 6 HSs
  - Each HS containing 2 ladders
  - Each ladder containing 1 sensor (200 μm) and 5 readout chips (150 μm)
  - p+n reverse biased (50 V) sensor with pixel size 425x50 μm^2
- Evaporating C_4F_{10} cooling system
- Fast-OR signals from each chips (every 100 ns) combined to give L0 trigger capability (unique in the ITS)





Inner Tracking System - SDD

Layer	Det.	Radius (cm)	Length (cm)	Surface (m^2)	Chan.	Spatial precision		Cell (μm^2)	Max occupancy central Pb-Pb (%)	Power dissipation (W)		Material Budget (% X/X_0)
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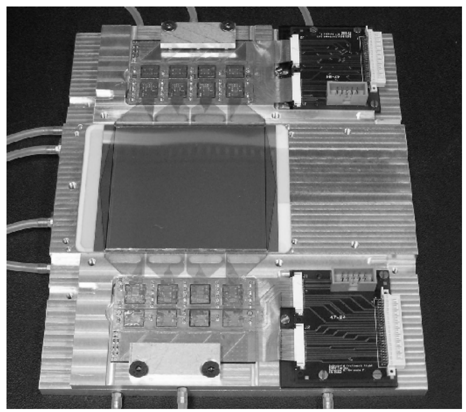
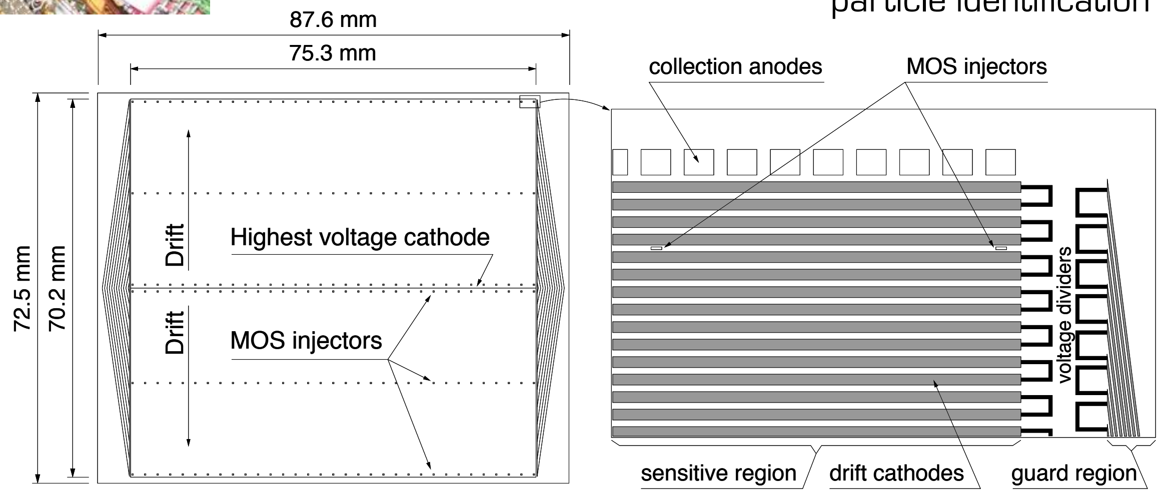
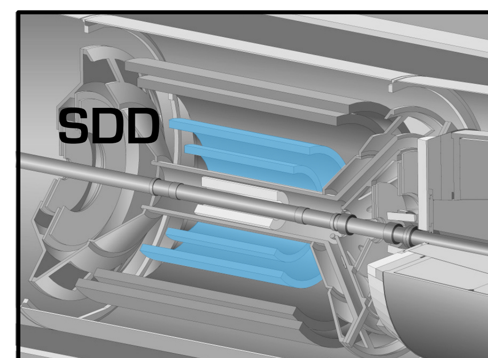


- 260 silicon drift sensors (300 μm)
  - 14 ladders (with 6 modules) in layer 3
  - 22 ladders (with 8 modules) in layer 4
  - Anode pitch (z): 294 μm
  - Drift HV: 1.8 kV
  - Drift velocity: 6.7 μm/ns
- Leak-less water cooling system
- dE/dx measurement through charge collection for particle identification





Inner Tracking System - SSD

Layer	Det.	Radius (cm)	Length (cm)	Surface (m^2)	Chan.	Spatial precision		Cell (μm^2)	Max occupancy central Pb-Pb (%)	Power dissipation (W)		Material Budget (% X/X_0)
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5	SSD	38.0	86.2	5.0	2.6M	20	830	95x40000	4.0	850	1.15k	0.83
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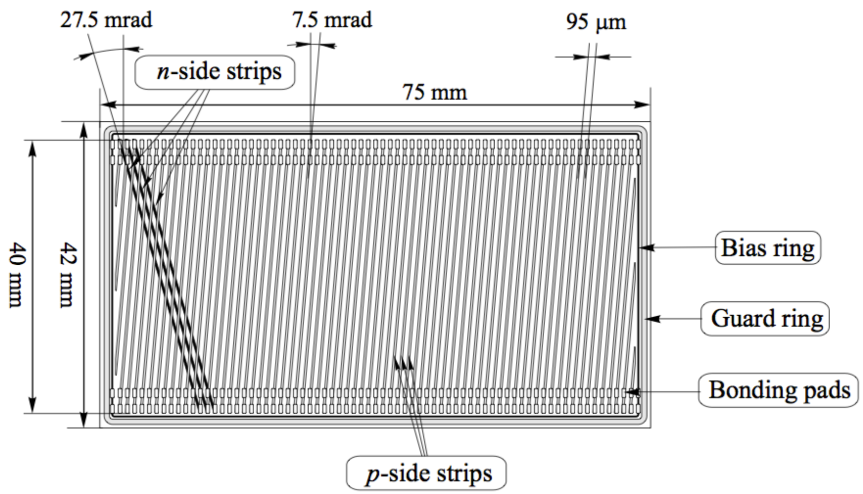
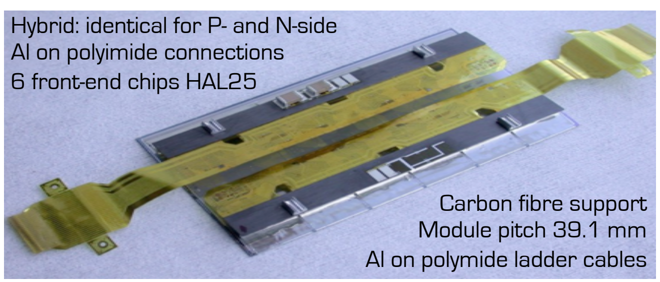
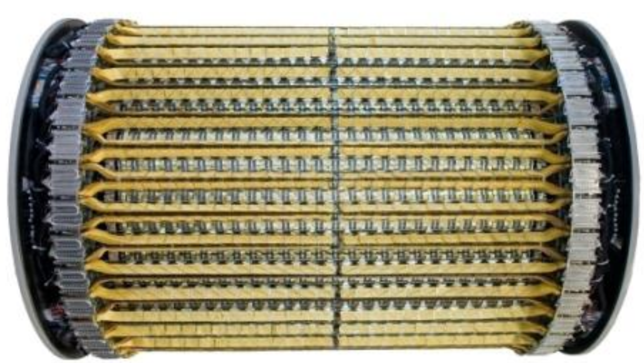
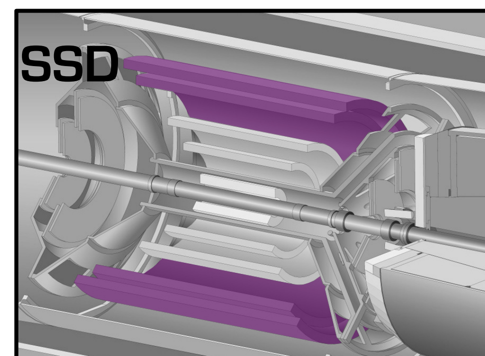


- 1698 silicon strip sensors (300 μm)
  - 34 ladders (with 22 modules) in layer 5
  - 38 ladders (with 25 modules) in layer 6
  - Strip pitch (rφ): 95 μm
  - Strip length (z): 40 mm
  - Stereo angle: 35 mrad
- Leak-less water cooling system
- dE/dx measurement through charge collection for particle identification



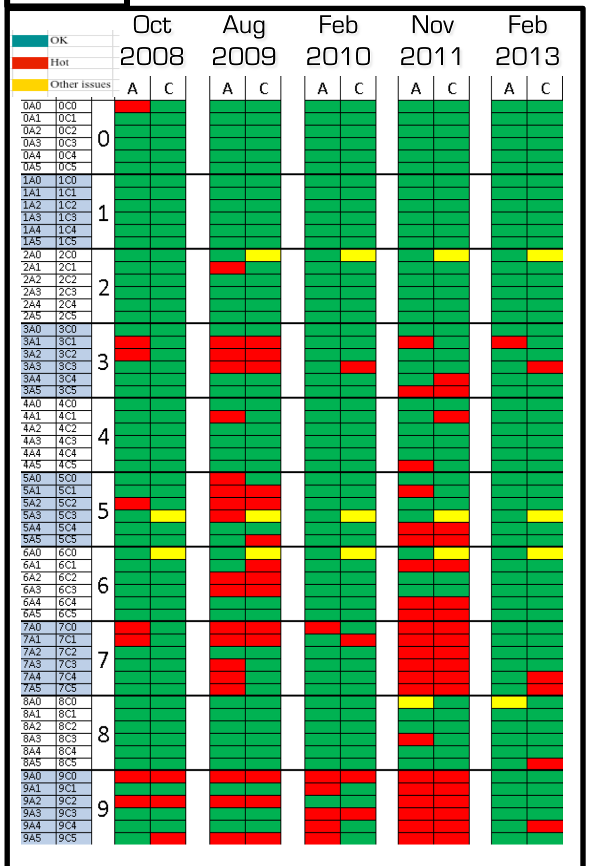




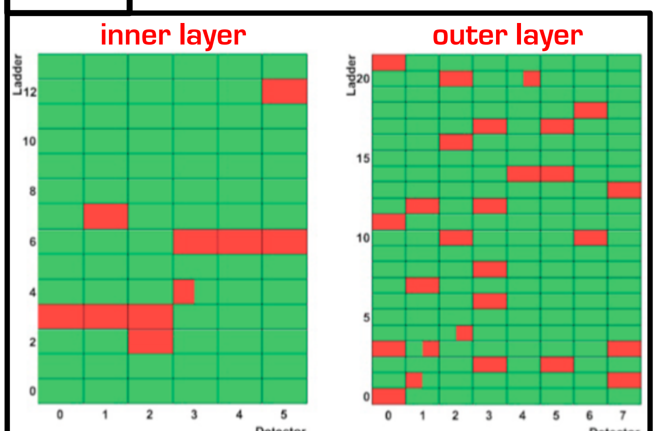
ITS Run1 status and performances

Det.	Availability in the run (%)	Detector acceptance
SPD	96	decreasing to 63%, later 93%
SDD	92	87% modules, with 98% working anodes on average
SSD	96	91%

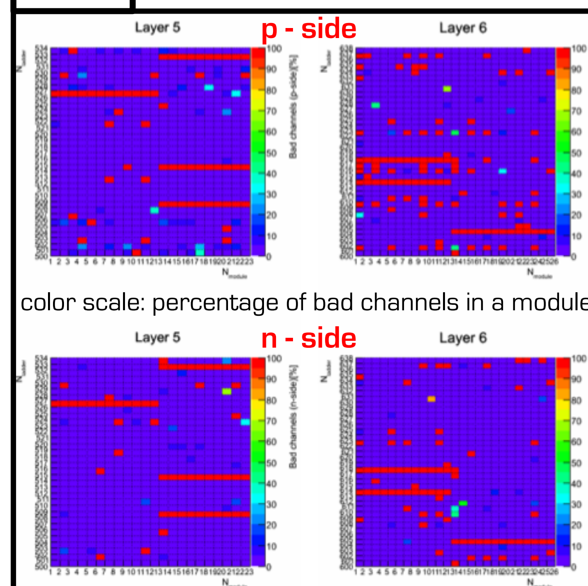
SPD



SDD

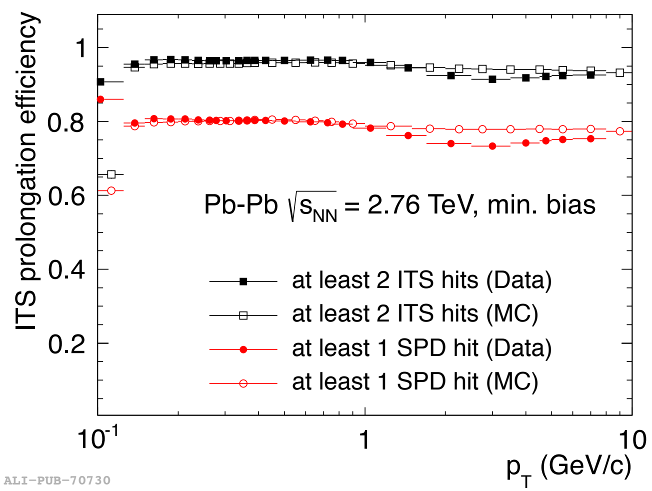


SSD

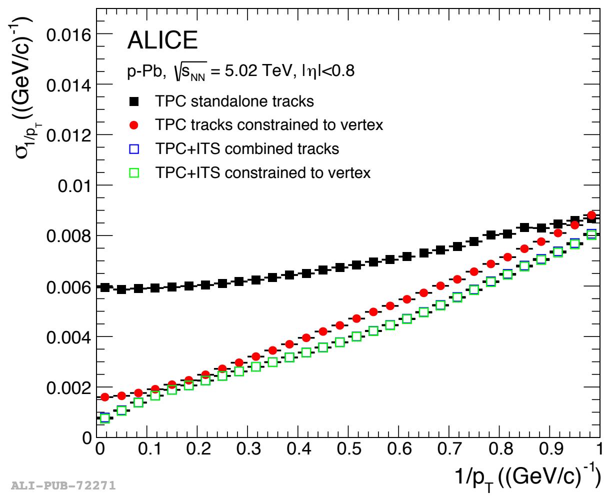


ITS Run1 status and performances

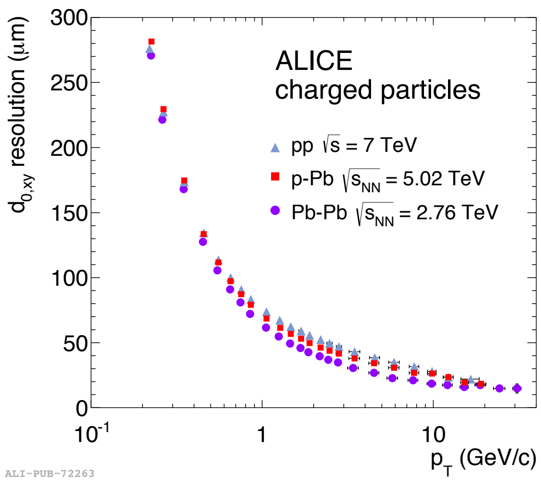
Tracking performance



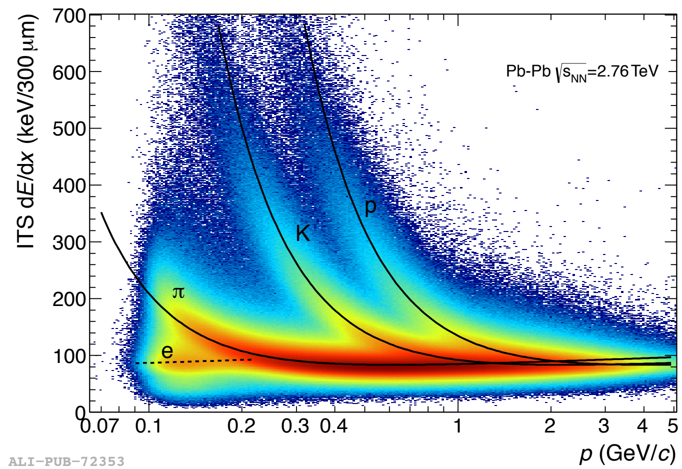
Transverse momentum resolution



Impact parameter resolution



PID performance



Tracking performance

- ✓ Almost perfect track matching between TPC and ITS

Transverse momentum resolution

- ✓ ITS extends the p_T range down to 80 – 100 MeV/c

Impact parameter resolution

- ✓ σ_d = 60 μm at p_T = 1 GeV/c
- ✓ weak dependence on the colliding system

Particle Identification performance

- ✓ K-π separation in the range of 0.1 – 0.45 GeV/c
  K-p separation in the range of 0.1 – 1 GeV/c

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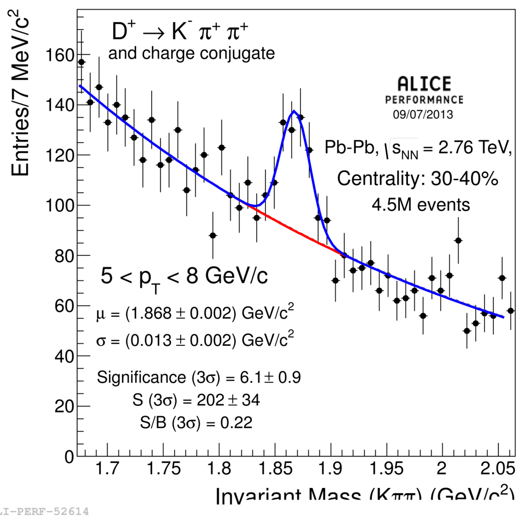
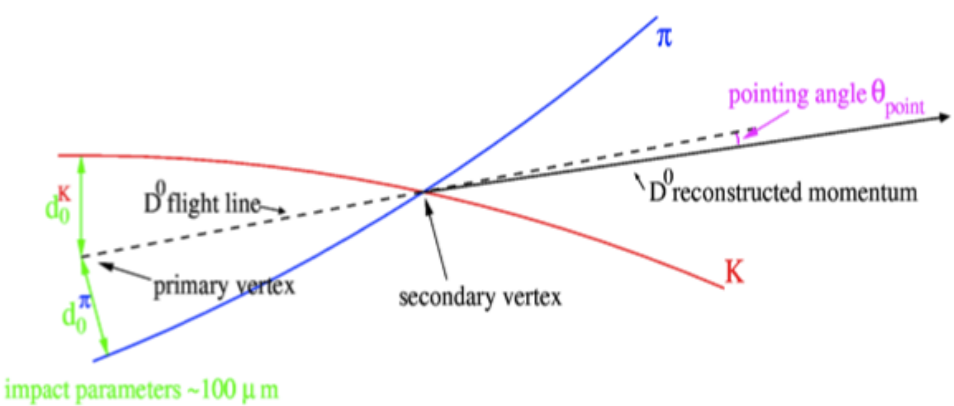
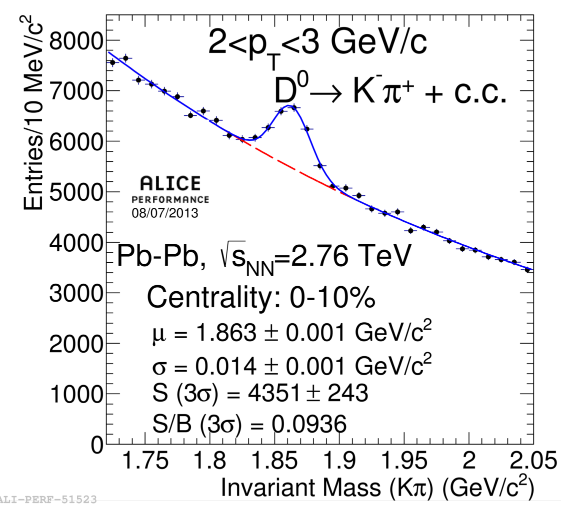
ITS Run1 status and performances

Secondary vertex reconstruction

- Very good impact parameter resolution allows reconstruction of secondary vertices
- Open-charm meson measured
  - ✓ D^+ (cτ~312 μm)
  - ✓ D^0 (cτ~123 μm)
  - ✓ D_s (cτ~150 μm)

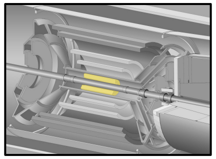




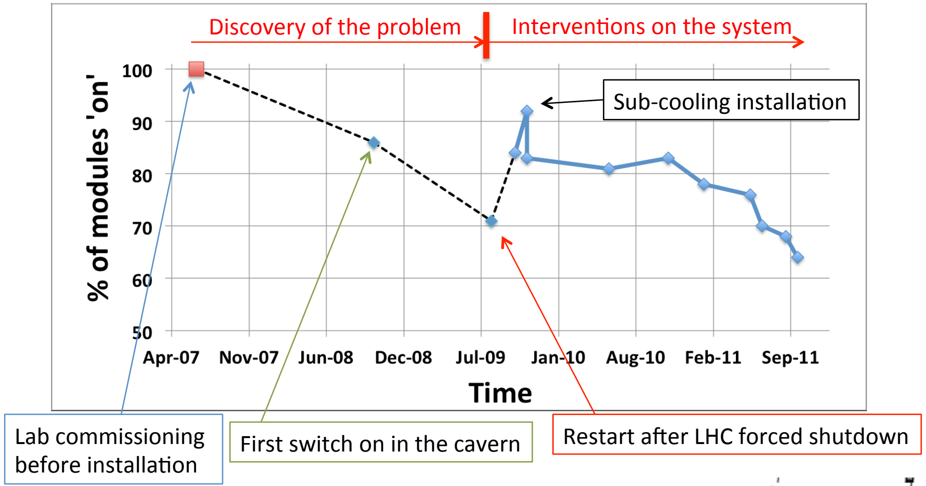


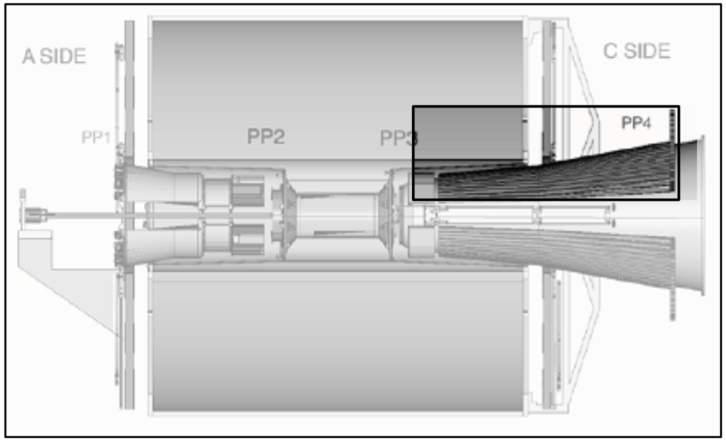
Operations from Run1 to Run2

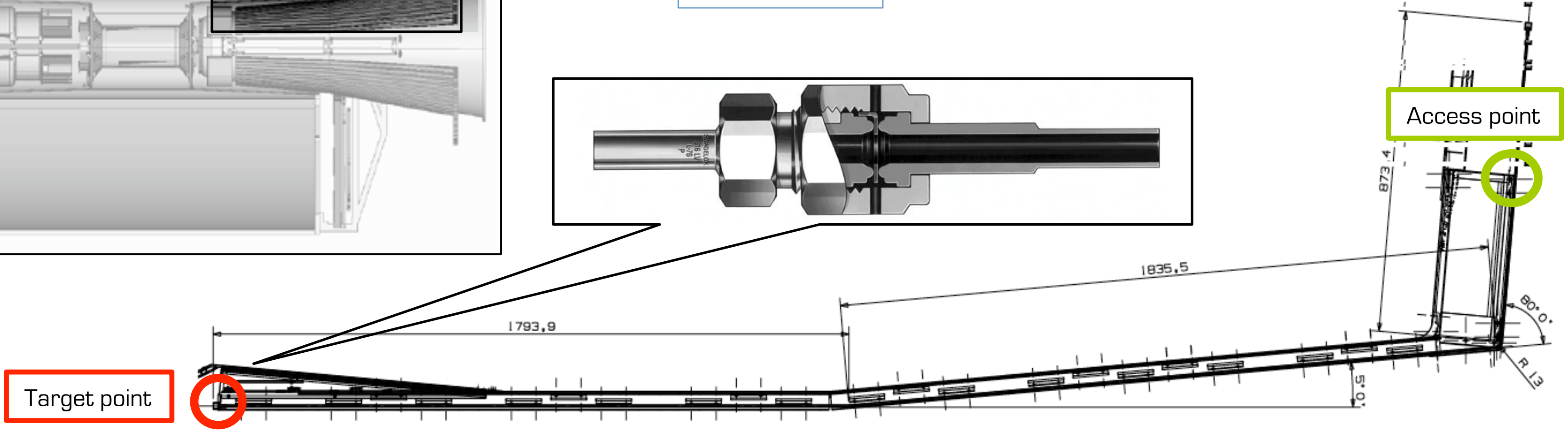
SPD – Clogged filters in the cooling lines



- Increasing number of half-staves affected by cooling problems
- Filters clogged: access possible only removing the TPC







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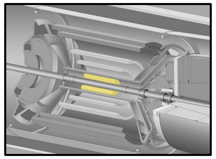
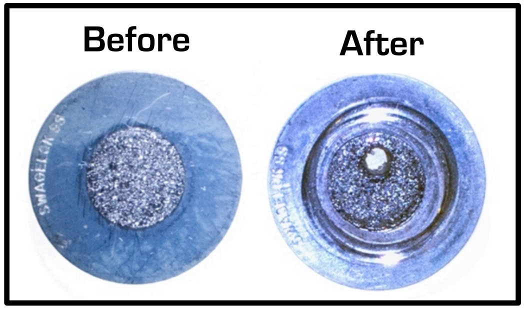
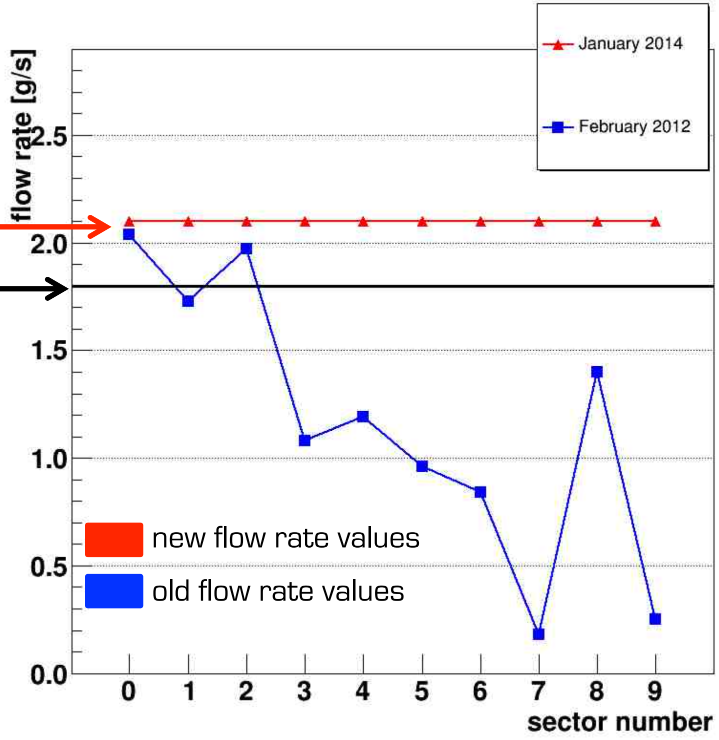


- Increasing number of half-staves affected by cooling problems
- Filters clogged: access possible only removing the TPC
- Solution → drilling campaign
  - ✓ From February 2012 to January 2014
- Moving to 100% cooling efficiency:
  - November 2011: 65/120 HSs (62.5%)
  - March 2013: 110/120 HSs (91.6%)



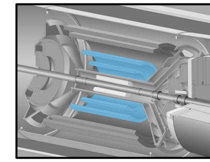
2.1 g/s common setpoint

1.8 g/s minimum value for total heat drain



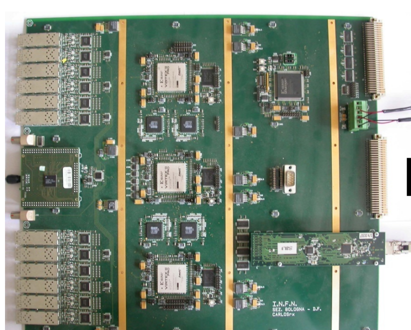
Operations from Run1 to Run2

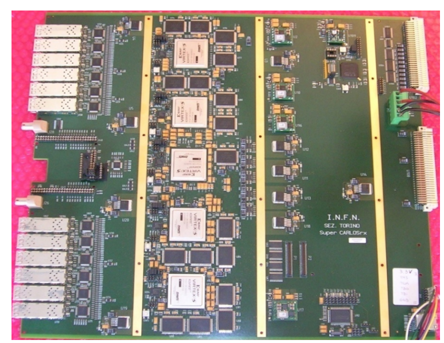
SDD – Upgrade of data concentrator cards



- The most frequent reason for the end of run comes from wrong common data header (cdh) created by the Front-end Electronics
- Resources in the data concentrator cards (CARLOSrx) saturated → no much room for adding new firmware features
- From CARLOSrx to SuperCARLOSrx
  - ✓ More computing power (5 Xilinx Virtex-5 FPGA)
  - ✓ More flexible and faster zero suppression and common mode noise subtraction on-board

CARLOSrx
- Production 2005-06
- 3 Xilinx VirtexII-PRO FPGAs

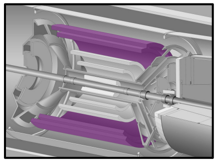




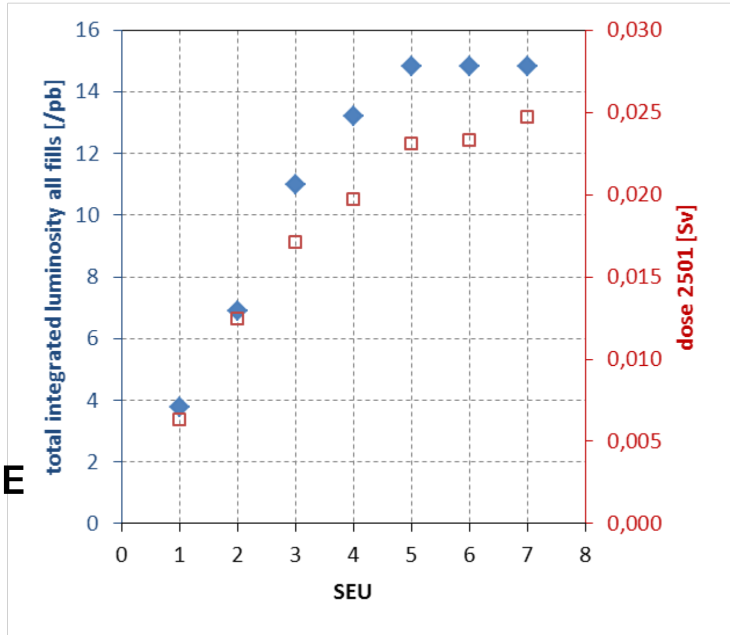
SuperCARLOSrx
- Production 2011
- 5 Xilinx VirtexI5 FPGAs

Operations from Run1 to Run2

SSD – SEU problem in the FEROM and LV board



- Seven Single Event Upset (SEU) observed during Run1
  - Front End ReadOut Module (FEROM)
    - ✓ performs offset correction and zero-suppression
    - ✓ located just outside the ALICE magnet
  - SEU statistics
    - ✓ in Run1: 4 in pp collisions + 3 in p-Pb collisions
    - ✓ estimated for Run2 (per day): 1 in pp, 0.04 in Pb—Pb
  - Possible solutions
    - ✓ Iron shielding: expensive, complicated and not efficient → **Discarded**
    - ✓ RadHard PROMs upgrade (radiation tolerant) → **DONE**
    - ✓ Firmware upgrade for faster recovery → **DONE**

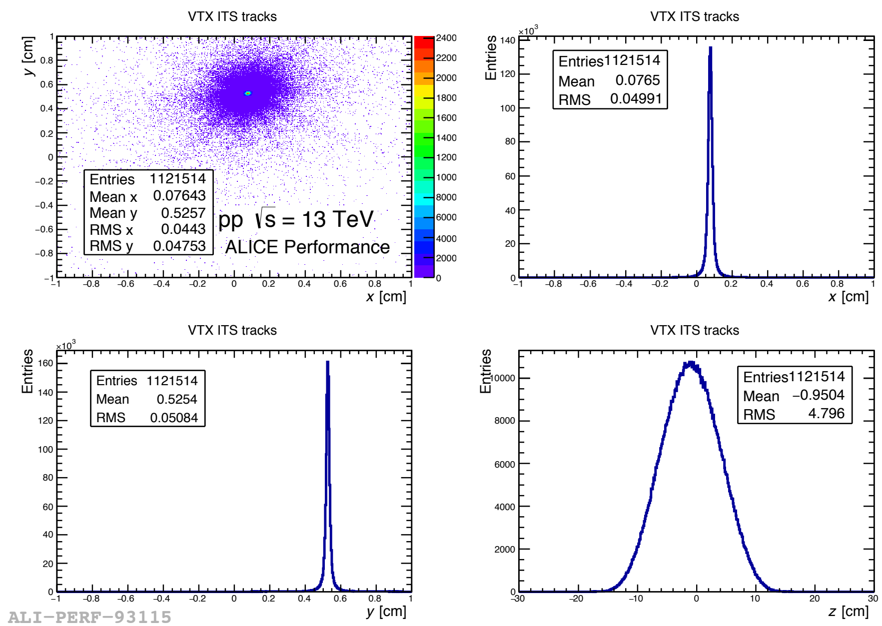


- All the LV boards have been substituted after a modification requested to CAEN in order to reduce the common mode noise

Operations from Run1 to Run2

Readiness for Run2

- Since January 2015 the three detectors underwent
  - ✓ cosmic rays campaign for alignment study
  - ✓ technical runs
  - ✓ LHC transfer line test
  - ✓ LHC quiet and non-quiet beam at 0.9 and 13 TeV
- Issues spotted during Run1 solved
  - SPD cooling plant → stable
  - SDD cdh error → disappeared
  - SSD SEU problem → not shown (to be verified with LHC beam at higher rate)
- Specific Detector Control System (DCS) and FEE firmware for the three detectors compliant with the recent improvements of the central system
- Actual modules status
  - SPD 107/120 half-staves
  - SDD 226/260 sensors
  - SSD 137/144 half-ladders

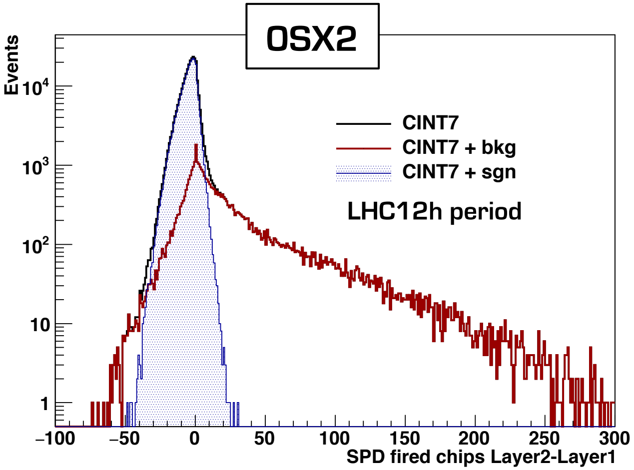


Vertex reconstructed with ITS (SPD+SSD only) standalone tracks
pp quiet beam, run 223270, on 20/05/2015 22:24
The displacement in y is due to the installation of the TRD modules; the apparatus is moving downward

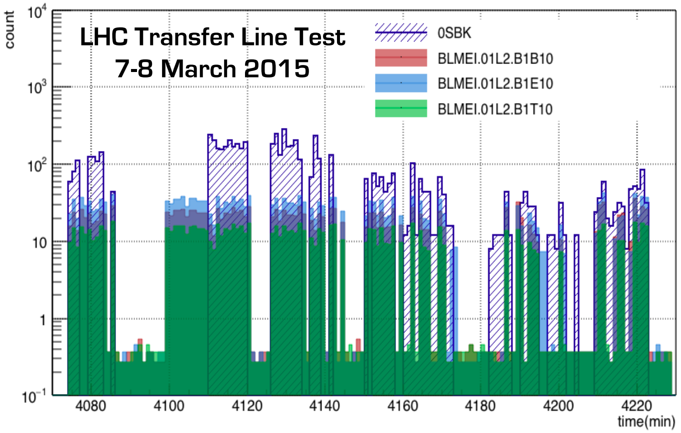
Operations from Run1 to Run2

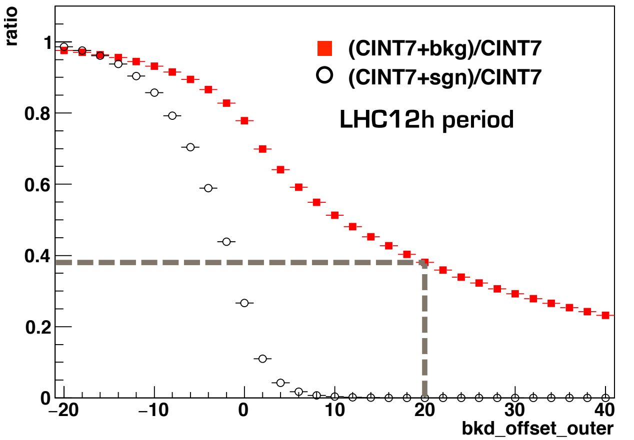
Readiness for Run2 – New functionality

- SPD as online background monitoring for Run2
  - ✓ OSX2: $\#FiredChips_{INNER\_LAYER} - \#FiredChips_{OUTER\_LAYER} > Threshold$
  - ✓ Bunch-Bunch collisions expected to have equal number of Fired Chips in the two layers → events distribution peaked around 0 fired chip difference in Layer1 – Layer2
  - ✓ Bunch-Gas collisions expected to have large difference in the number of Fired Chips in the two layers
- Recent study performed on data taken in 2012
  - ✓ applying a threshold in the difference between the number of fired chips in the two SPD layers we can efficiently separate signal and background
  - ✓ E.g. with a Threshold = 20 the background reduction is ~40% with negligible loss of BB events



- LHC Transfer Line Test (7-8 March)
  - ✓ beam quenched on the TDI → only background
  - ✓ checked a detailed correlation between BLM and OSX2





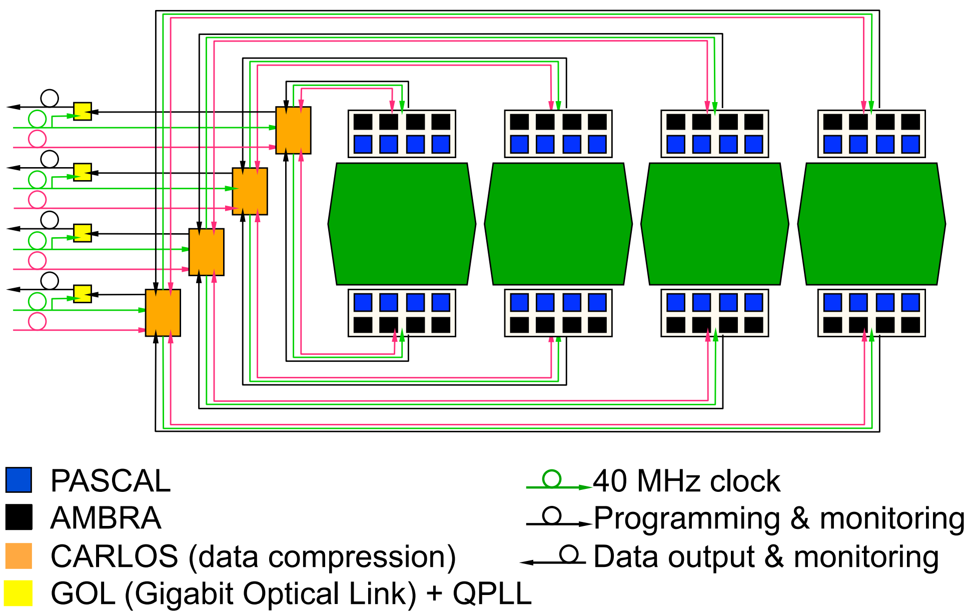
Summary

- ALICE Inner Tracking System has been in operation from 2010 to 2013 and participated in all the pp, p—Pb and Pb—Pb data taking
  - The three subsystems (SPD, SDD, and SSD) performed remarkably well and according to the specifications
- The performance is well in agreement with the design requirements and is stable with time
  - Standalone capability allows to track and identify charged particles with momenta down to 100 MeV/c
  - Particle identification performance allows for separation of pions, kaons and protons down to very low p_T
  - Impact parameter resolution on ~60 μm for tracks with p_T = 1 GeV/c allows the reconstruction of charmed secondary vertices
- Readiness for Run2
  - Issues spotted during Run1 solved
  - All the three detectors participated in the 2015 cosmic rays campaign and LHC quiet beams with success
  - Ready for Run2
- Stay Tuned! Upgrade is coming…
  - "The Upgrade of the Inner Tracking System of ALICE" presented today by Monika Kofarago

Backup

Backup

SDD – Readout architecture



PASCAL (64 channels)

- Preamplifier (τ ~ 40 ns, RC-CR2 shaping)
- Analog memory (64 × 256 cells)
- 32 10-bit linear ADC (1 every 2 channels)

AMBRA (64 channels)

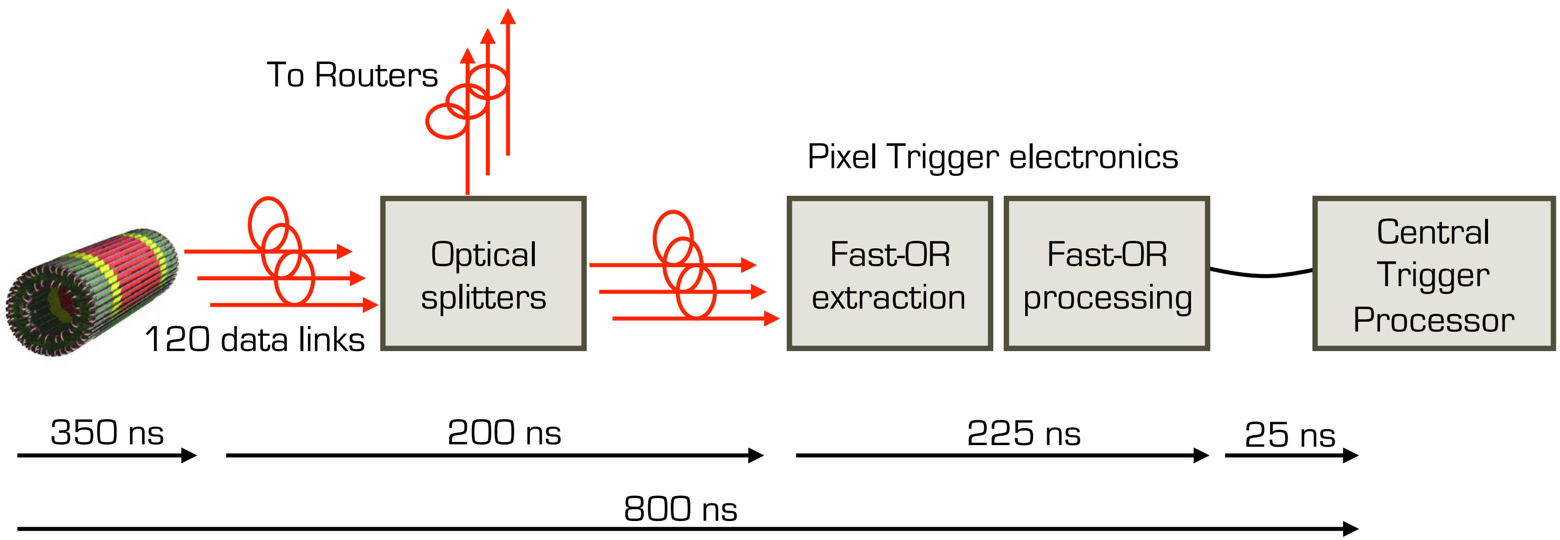
- Four 16 kB buffers
- Baseline equalization
- 10 to 8-bit compression

CARLOS (1 for 8 AMBRAs)

- Zero suppression and Compression of data from 1 SDD with a 2D – 2-Threshold algorithm (programmable parameters)
- Interface with AMBRAs, GOL and CARLOS-rx (FPGA based board, in counting room, which links to DDLs)
- FEE monitoring (SEU) time-multiplexed with data on the 16-bit output data bus
- Protections against radiation effects (parity check)

Backup

SPD – Trigger integration



- Fast-OR active on registration of at least 1 hit per readout chip
- Contribution to the first level of trigger in ALICE
  - ✓ IN: 1200 bits every 100 ns from the SPD to the Pixel Trigger
  - ✓ OUT: 10 programmable outputs based on Boolean logic propagated to CTP
- Maximum latency at CTP input = 800 ns → installed at 40 m from SPD