Upgrade of the Inner Tracking System of ALICE

with a focus on pixel sensor development

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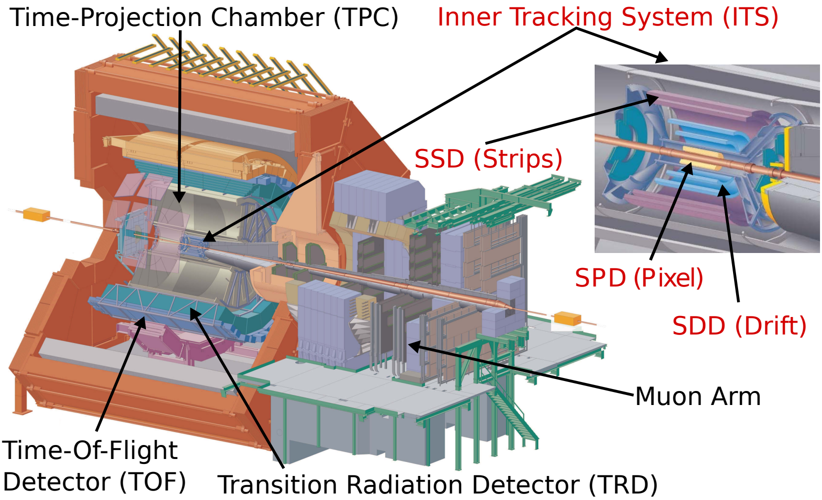
on behalf of the ALICE Collaboration

1st June 2015

24th International Workshop on Vertex Detectors

A Large Ion Collider Experiment (ALICE)



Talk by Domenico Colella on the current ITS on Monday morning

Upgrade of ALICE in the 2nd LHC long shutdown (2018/19)

Motivations and strategy:

- ALICE was designed to study the **quark-gluon plasma** formed in heavy ion collisions
- High precision measurements of **rare probes at low p_T**
  - cannot be selected by a hardware trigger
- Record large **minimum bias** samples
  - read out all collisions at the maximum LHC collision rate (50 kHz)
- **Integrated luminosity of 10 nb^{-1}** in Pb-Pb (plus pp and p-A data)
  - factor 100 in statistics compared to LHC Run 1 and 2 (2009 - 2018)

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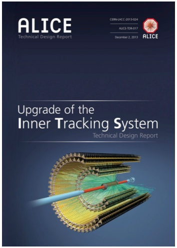
Upgrades:

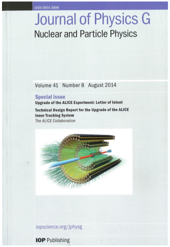
- New Inner Tracking System (ITS)
- New Muon Forward Tracker (MFT)
- Smaller beam pipe
- Online and offline system
- Electronics and readout of the Time-Projection Chamber (TPC)
- Readout electronics of several detectors

Design objectives for the upgrade of the ITS

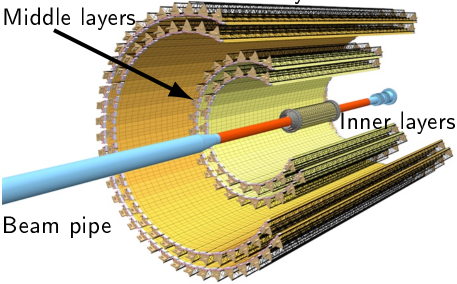
- Improve impact parameter resolution by a factor of 3(5) in r-φ(z) at $p_T = 500$ MeV/c
  - First layer closer to interaction point: 39 mm $\rightarrow$ 23 mm
  - Material budget: $\sim 1.14\%\ X_0 \rightarrow 0.3\%\ X_0$ for the three innermost layers
  - Pixel size: 50µm x 425µm $\rightarrow$ O(30µm x 30µm)
- Improve tracking efficiency and p_T resolution at low p_T
  - 6 layers $\rightarrow$ 7 layers
  - All layers pixel chips (instead of strip, drift and pixel layers)
- Fast readout (now limited to 1 kHz with full ITS)
  - Pb-Pb: $>$ 100 kHz
  - pp: several 10^5 Hz
- Fast insertion/removal for yearly maintenance



CERN-LHCC-2013-24



J. Phys. G(41) 087002



- 7 layers of pixel sensors ($r = 23 - 400$ mm)
- 10 m^2 of silicon with 12.5 Gpixels
- $|\eta| < 1.22$ for tracks from 90% of the most luminous region

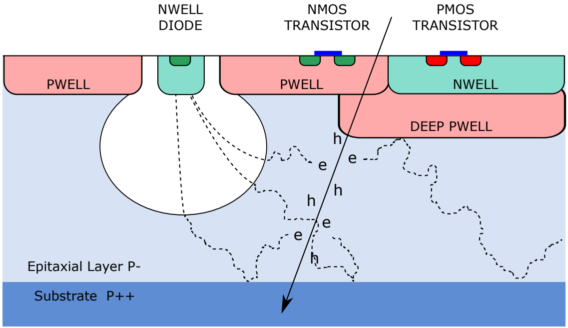
Parameter	**Inner barrel**	**Outer barrel**
Silicon thickness	50μm	
Spatial resolution	5μm	10μm
Power density	$<$ 300 mW/cm^2	$<$ 100 mW/cm^2
Event resolution	$<$ 30μs	
Detection efficiency	$>$ 99%	
Fake hit rate	$< 10^{-5}$ per event per pixel	
Average track density	15 - 35 cm^{-2}	0.1 - 1 cm^{-2}
TID radiation *	2700 krad	100 krad
NIEL radiation *	1.7x10^{13} 1 MeV n_{eq}/cm^2	10^{12} 1 MeV n_{eq}/cm^2

* Including a safety factor of 10

Technology choice

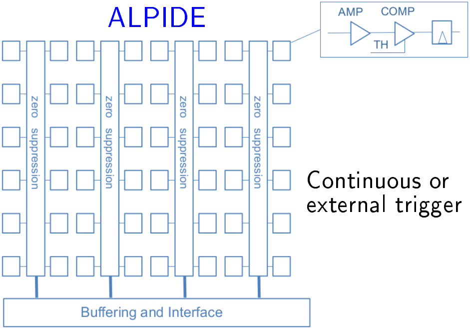
Monolithic **A**ctive **P**ixel **S**ensors using TowerJazz 0.18μm CMOS imaging process

- High-resistivity ($> 1\mathrm{k}\Omega$ cm) epitaxial layer on p-type substrate
- Quadruple well process: deep PWELL shields NWELL of PMOS transistors, allowing for full CMOS circuitry within active area
- Moderate reverse substrate biasing is possible, resulting in larger depletion volume around NWELL collection diode

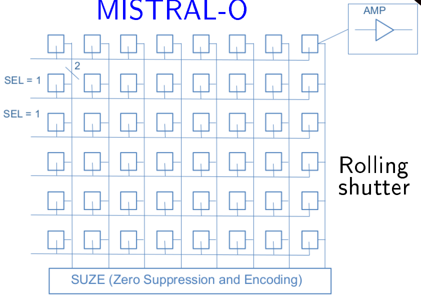


Chip architectures

ALPIDE



MISTRAL-O



ALPIDE:

- Readout: Data driven
- Pixel pitch: 28µm x 28µm
- Event time resolution: $\lesssim 2\mu s$
- Power consumption: 39 mW/cm^2
- Dead area: 1.1 mm x 30 mm

MISTRAL-O:

- Rolling shutter
- 36µm x 65µm
- $\sim 20\mu s$
- $80 - 90$ mW/cm^2
- 1.5 mm x 30 mm

- Baseline solution is the ALPIDE
- Both chips have the same dimensions, identical physical and electrical interfaces

Stages of the ALPIDE development

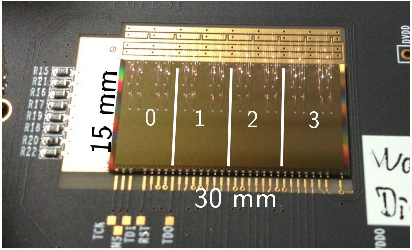
2012	Explorer-0
2013	Explorer-1 pALPIDEss-0
2014 May	pALPIDE-1 pALPIDEss-1 Investigator
2015 April	pALPIDE-2
2015 August	pALPIDE-3
2016 February	ALPIDE

Existing ALPIDE chip types:

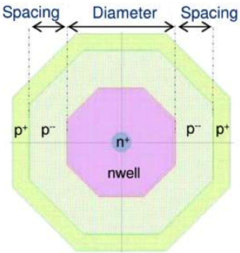
- **Explorer and Investigator:**
  Analog chip to study pixel geometry, starting material and sensitivity to radiation
- **pALPIDEss:**
  Small scale digital chip to study the priority encoder and the front-end electronics
- **pALPIDE-1:**
  Full scale chip to study system effects
- **pALPIDE-2:**
  Full scale chip which supports integration into module prototypes:
  New pad over logic geometry and support of Outer Barrel local data bus

Specification of the pALPIDE-1

- First prototype with final size (15 mm x 30 mm)
- 512 x 1024 pixels
- Pixels are 28μm x 28μm
- Digital readout with priority encoder
- Four sectors with different pixel layouts

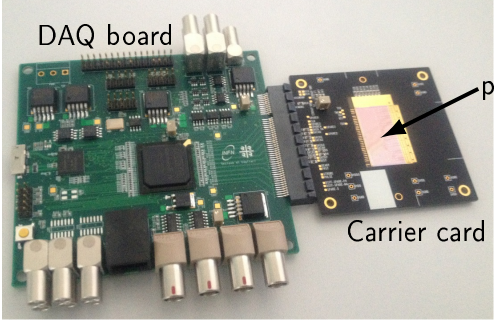


Sector	Nwell diameter	Spacing	Pwell opening	Reset
0	2μm	1μm	4μm	PMOS
1	2μm	2μm	6μm	PMOS
2	2μm	2μm	6μm	Diode
3	2μm	4μm	10μm	PMOS

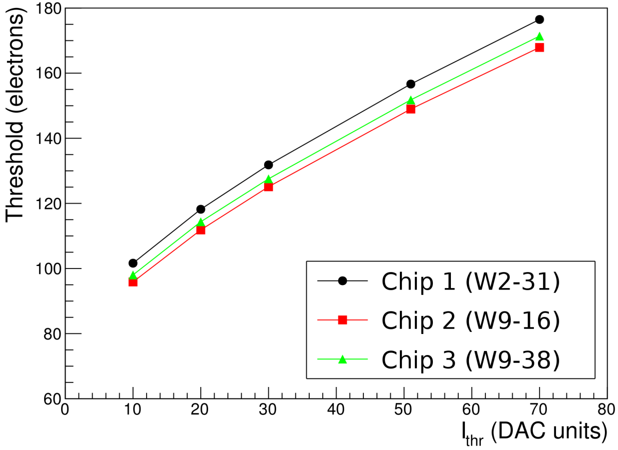


Characterization methods - laboratory

- Noise and threshold measurements
- Radioactive source measurements
- Noise occupancy measurements
- Several setups:
  CERN, France, Italy, Russia, South Korea, Thailand



Input charge threshold measurements



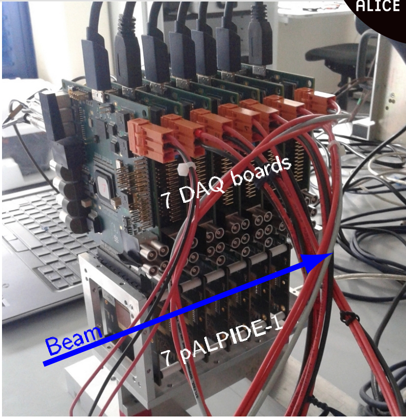
$V_{BB} = -3$ V
Sector 2

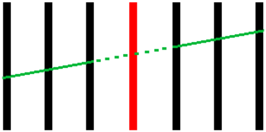
- Input charge threshold increases as function of I_{thr}
- Threshold spread between pixels: 20 - 50 electrons
- Results are from one sector $\longrightarrow$ fourth of the final chip size

Test beam

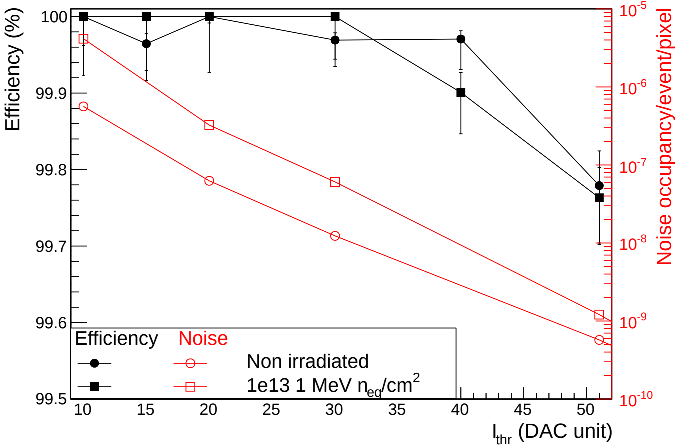
- Tracking is done by a stack of 7 layers of pALPIDE-1
- Readout and analysis is done using the EUDAQ/EUTelescope framework *
- Several campaigns from 60 MeV to 120 GeV (PS, SPS, DESY, BTF, PAL)
- Measurement of detection efficiency and spatial resolution

*https://eutelescope.web.cern.ch



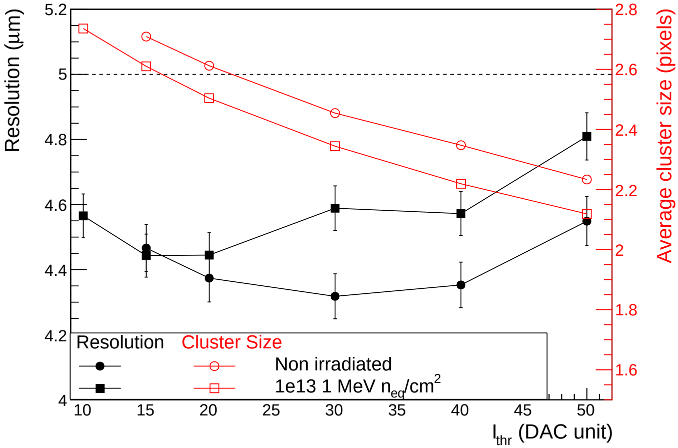


Device Under Test



- 20 most noisy pixels masked
- Wide operating range with efficiency above 99% and noise occupancy below 10^{-5}/event/pixel
- Slight increase in noise occupancy after irradiation

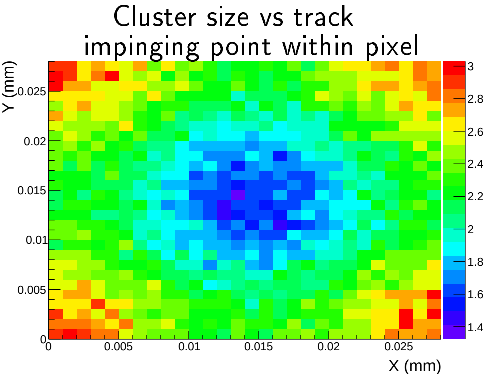
$V_{BB} = -3$ V
Sector 2
W9-16, W5-25



$V_{BB} = -3$ V
Sector 2
W2-31, W2-12

- Wide operating range with resolution below 5µm
- Resolution becomes slightly worse after irradiation

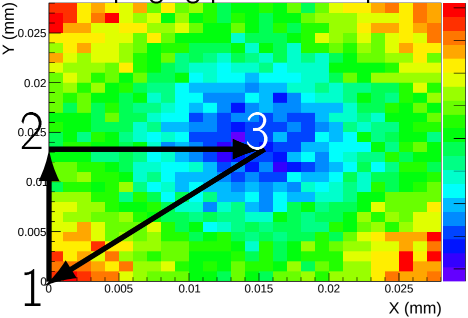
Dependency of cluster size on track impinging point



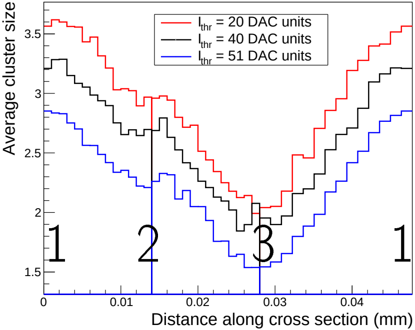
$V_{BB} = 0$ V
Sector 2
W2-25

Dependency of cluster size on track impinging point

Cluster size vs track impinging point within pixel



Cross section

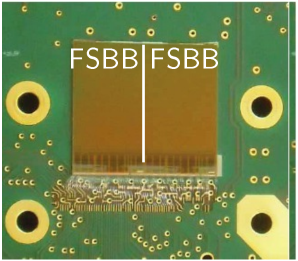


- Clusters size changes with track impinging point as expected from charge sharing

$V_{BB} = 0$ V
Sector 2
W2-25

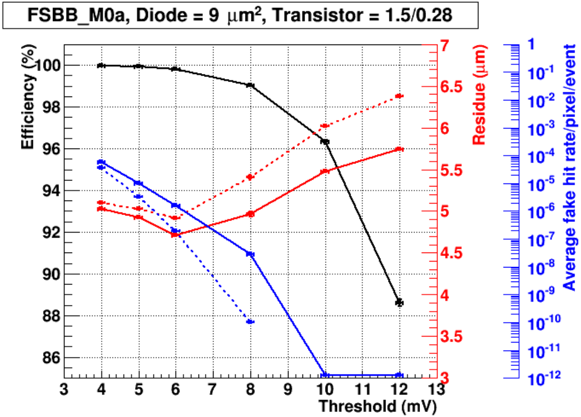
MISTRAL FSBB

- First Full Scale Building Block (FSBB)
- Sensitive area: $13.7 \times 9.2\text{mm}^2$ ($\sim$ third of the final chip size)
- Staggered pixels of $22 \times 33\mu\text{m}^2$
- In-pixel pre-amplification and clamping with 6 metal layers
- 416×416 of Columns x Row of pixels ended by discriminator (8-cols with analogue output)
- Double-row readout at 160 MHz clock frequency resulting in 40μs integration time



MISTRAL-O

- Being optimized for the outer layers
  - Target requirements on the spatial resolution: $\sim 10\mu$m
  - Target requirements on power consumption: $< 100\text{mW/cm}^2$
- Staggered pixels of $36 \times 65\mu\text{m}^2$
- 20μs integration time

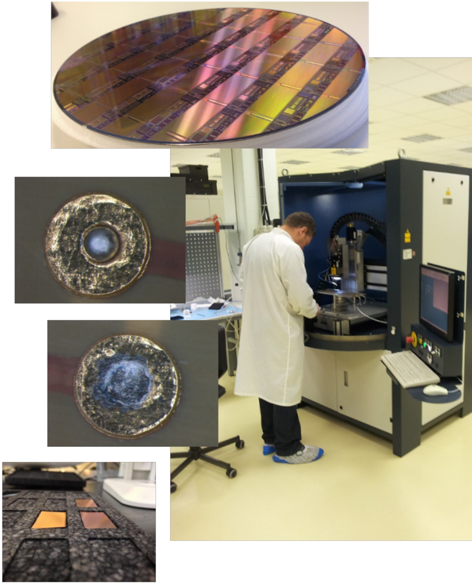


For more information:
Talk by Michael Deveaux on Friday

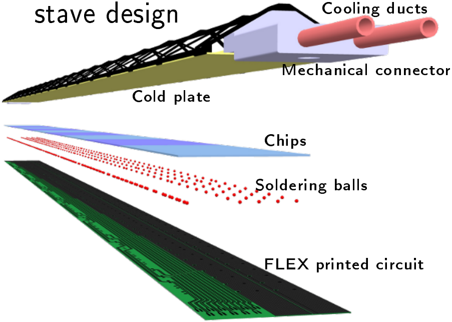
- Large operational margin: 5.0 mV $\leq$ Thr $\leq$ 8.0 mV
- Fake hit rate averaged over 11 sensors
- Fake hit rate drops by O(10) by masking the 20 noisiest pixel
- Tracking resolution is $(4.7 \pm 0.1)\mu$m (U) and $(4.9 \pm 0.1)\mu$m (V) at Thr= 6 mV

Other aspects of the project

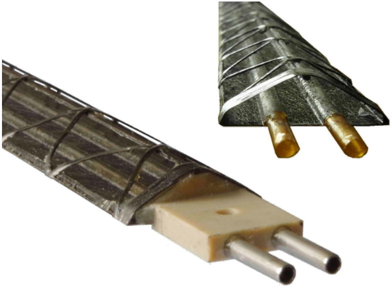
- Inner barrel prototypes and testing
- Outer barrel prototypes and testing
- Cooling
- Assembly machine
- Readout electronics
- Sensor post processing
- Chip transport
- Laser soldering
- Mass testing



Inner barrel stave design

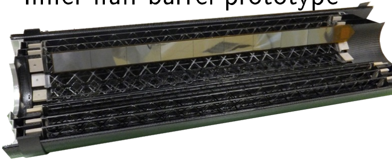


Inner barrel stave prototypes



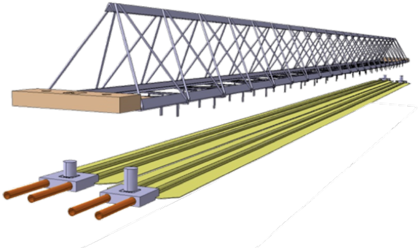
- Material budget: $\sim 0.3\%\ X_0$
- Detector operated at room temperature
- Coolant: H_2O
- Chips are laser soldered to FLEX printed circuit

Inner half barrel prototype

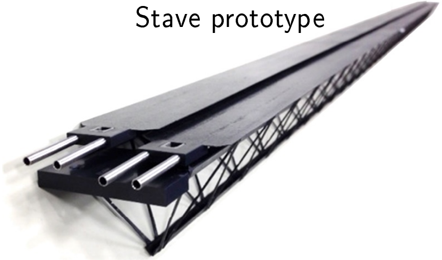


Outer barrel

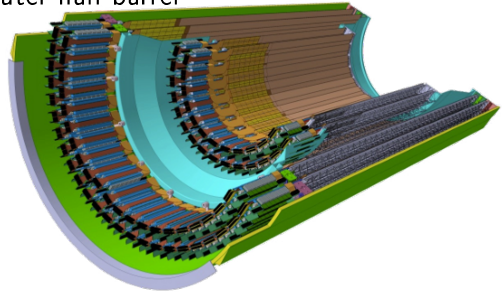
Stave design



Stave prototype



Outer half barrel



- Material budget: $\sim 1\%\ X_0$
- Two half staves grouped into one stave

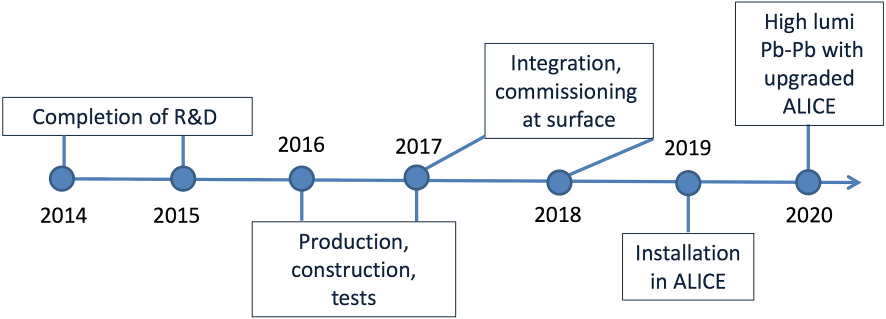
Summary and outlook

- The Inner Tracking System of ALICE will be replaced during the second long shut down of the LHC (2018/19)
- Impact parameter and tracking resolution and p_T resolution at low p_T will improve significantly
- 7 layers of monolithic pixel sensors will be used
- First full scale prototypes show good performance and large margin of operation
- All aspects of the R&D are close to completion and all specifications are possible to meet
- Project is advancing according to schedule

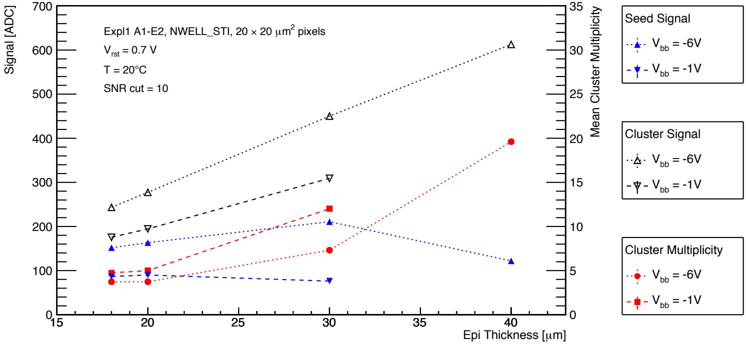
Thank you for your attention!

BACKUP

Timeline


Completion of R&D
2016
2017
Integration, commissioning at surface
2019
High lumi Pb-Pb with upgraded ALICE
2014
2015
2018
2020
Production, construction, tests
Installation in ALICE

20 × 20 μm² pixels:

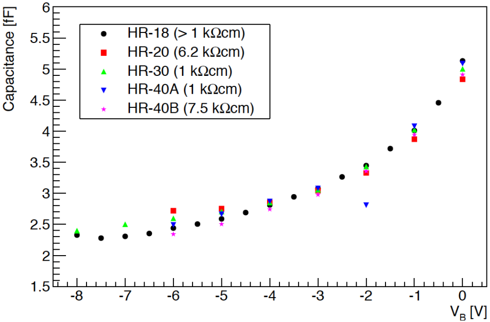


- Cluster charge increases linearly with epi-layer thickness
- Cluster size increases with epi-layer thickness
- Optimum epi-layer thickness depends on the applied reverse substrate bias

Starting material - resistivity

NWELL diode output signal = Q/C

- Minimize spread of charge over many pixels
- Minimize capacitance:
  - Small diode surface
  - Large depletion volume

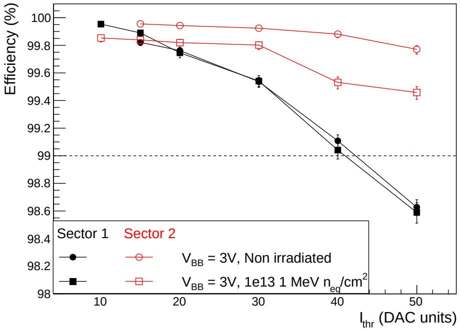


- Pixel input capacitance decreases with increasing reverse substrate bias
- Minor influence of epi-layer resistivity for current pixel layout

Effects of irradiation on the different sectors of the pALPIDE-1

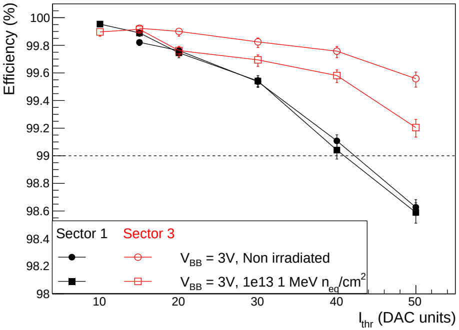
Effect of reset method

- Sector 1: PMOS reset
- Sector 2: Diode reset



Effect of spacing

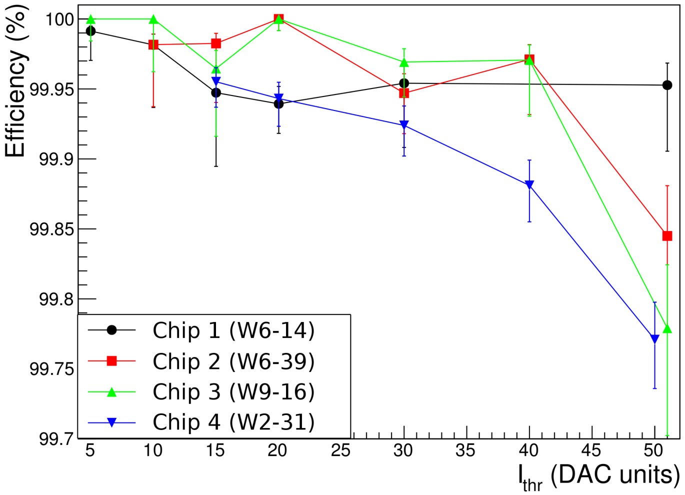
- Sector 1: 2µm
- Sector 3: 4µm



- Diode reset seems to show better performance before and after irradiation
- Diode reset seems to be more effected by irradiation
- Larger spacing seems beneficial

$V_{BB} = -3$ V
W2-31, W2-12

Chip to chip fluctuations



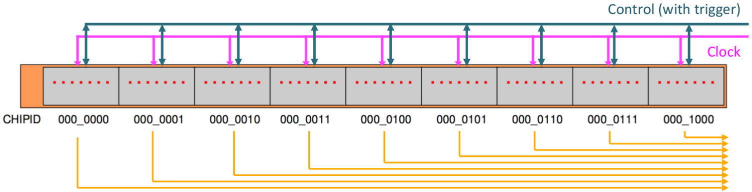
$V_{BB} = -3$ V
Sector 2

- Chip to chip fluctuations are within statistical fluctuations

Readout

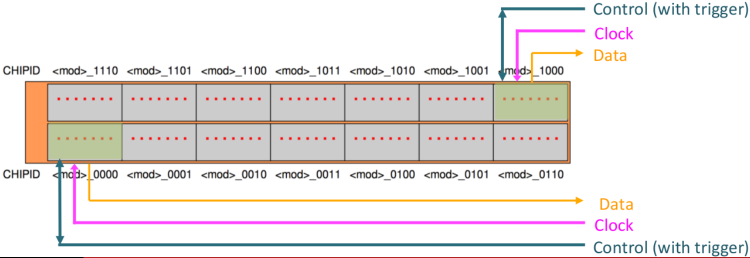
Inner layers:

- 9 independent sensors (each reads/drives its own data line)



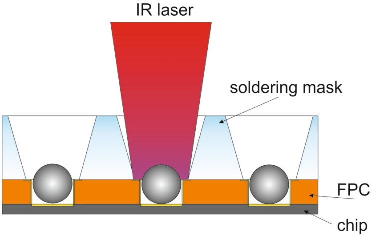
Mid/outer layers:

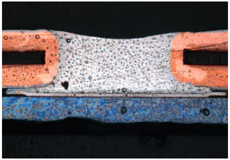
- 2 symmetric group of 1 master and 6 slave chips
- Only the master accesses the data/control lines

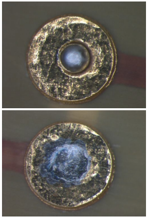


Laser soldering

- Interconnection of pixel chip with flexible printed circuit
- Both mechanical and electrical connection

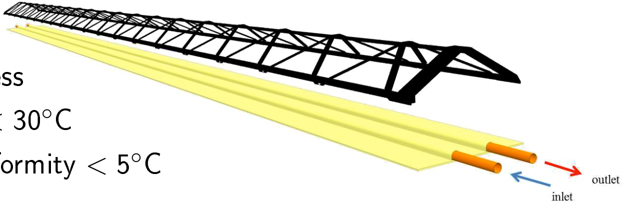




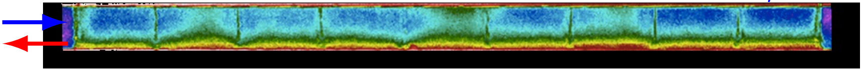


Cooling

- Coolant: H_2O, leak-less
- Sensor temperature $< 30°C$
- Temperature non-uniformity $< 5°C$

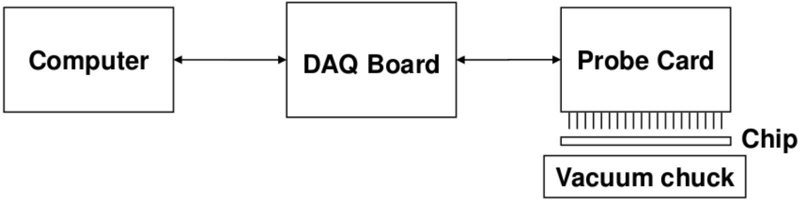


$T_{in} = 15.8°C$ Min $T_{pixel} = 16.5°C$

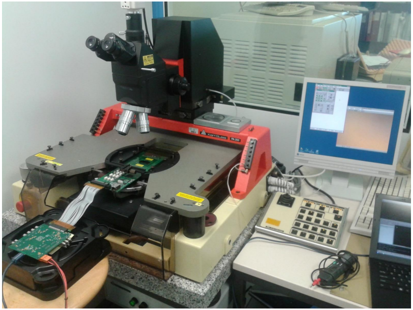


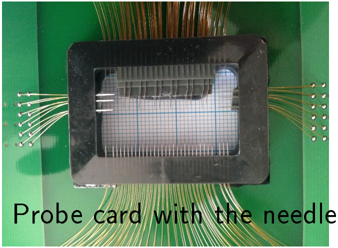
$T_{out} = 16.6°C$ Max $T_{pixel} = 18.5°C$

Plans for mass testing

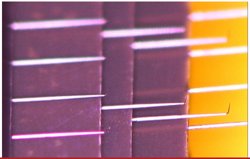


Probe station prototype



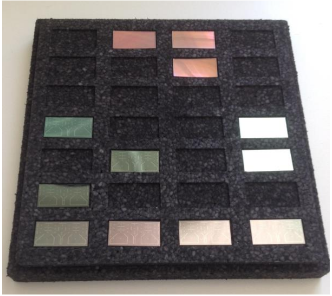


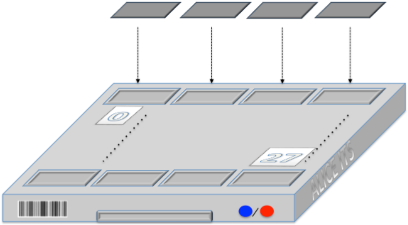
Probe card with the needles



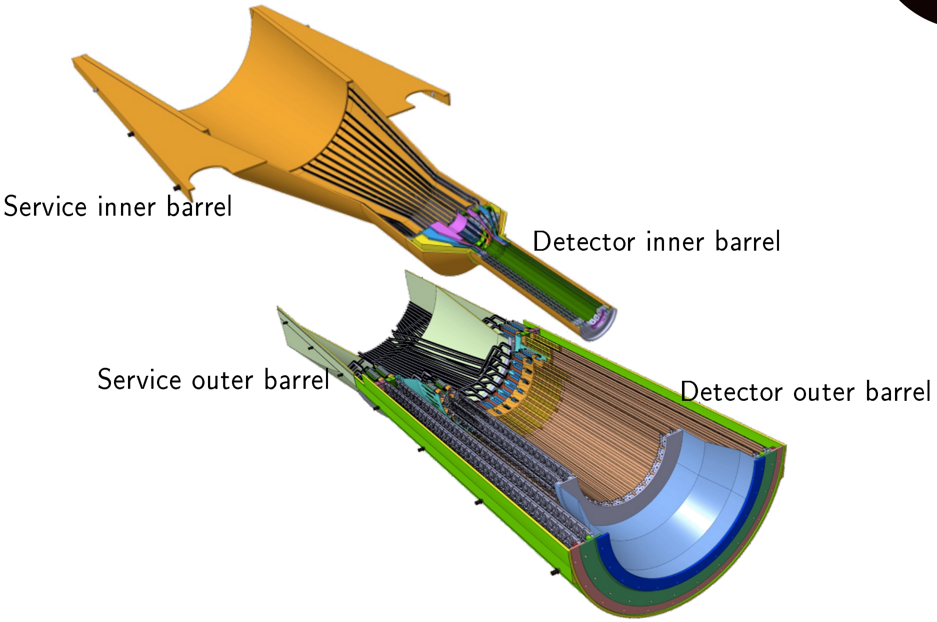
Chip transport

- Assembly will take place in many parts of the word ⟶ safe transport method needed
- Transport test from CERN to Pusan (South Korea) and back
- Visual inspection in both places
- Measurement of temperature, acceleration and humidity during the trip
- Chips are back to CERN ⟶ No visual damage



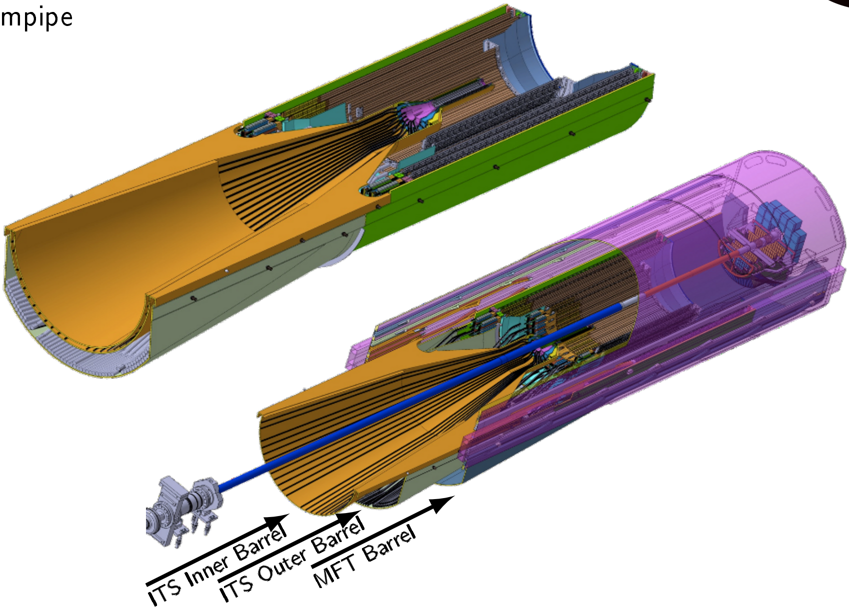


Service barrel



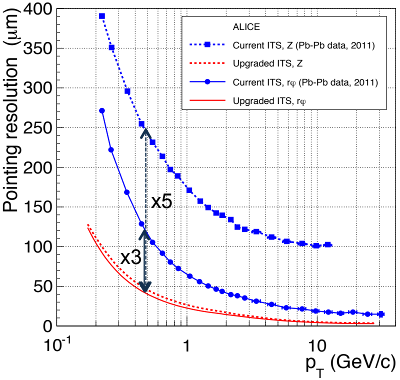
Installation

Independent insertion of ITS Inner and Outer half barrel along the beampipe

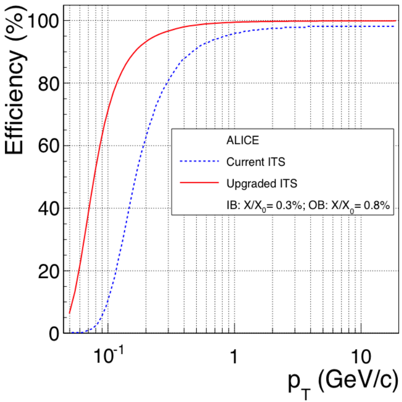


Physics simulations

Impact parameter resolution

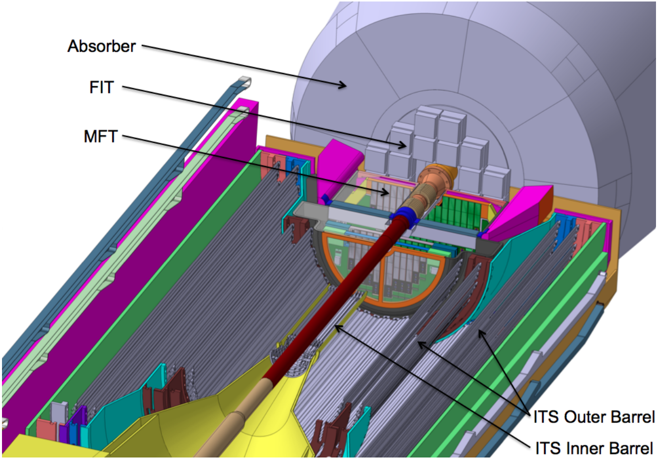


Tracking efficiency (ITS standalone)



Muon Forward Tracker - goal

- Study QGP physics at forward rapidity in ALICE
- Vertexing for the ALICE Muon Spectrometer (MS) at forward rapidity



Muon Forward Tracker - specifications

- 5 detection disks of silicon pixel sensors O(25 μm x 25 μm)
- 0.6% of X_0 per disk
- TID < 400 krad, NEIL $< 6 \times 10^{12}$ 1 MeV n_{eq}/cm^2 (safety factor of 10)

⇓

Same chip will be used as for the ITS

- Disk 0 at $z = -460$ mm, $R_{in} = 25$ mm (limited by the beam-pipe radius)
- Disk 4 at $z = -768$ mm (limited by FIT and the frontal absorber)