HR-CMOS: Status of Fully-Depleted Monolithic Active Pixel Sensors

Steve Worm
Rutherford Appleton Laboratory

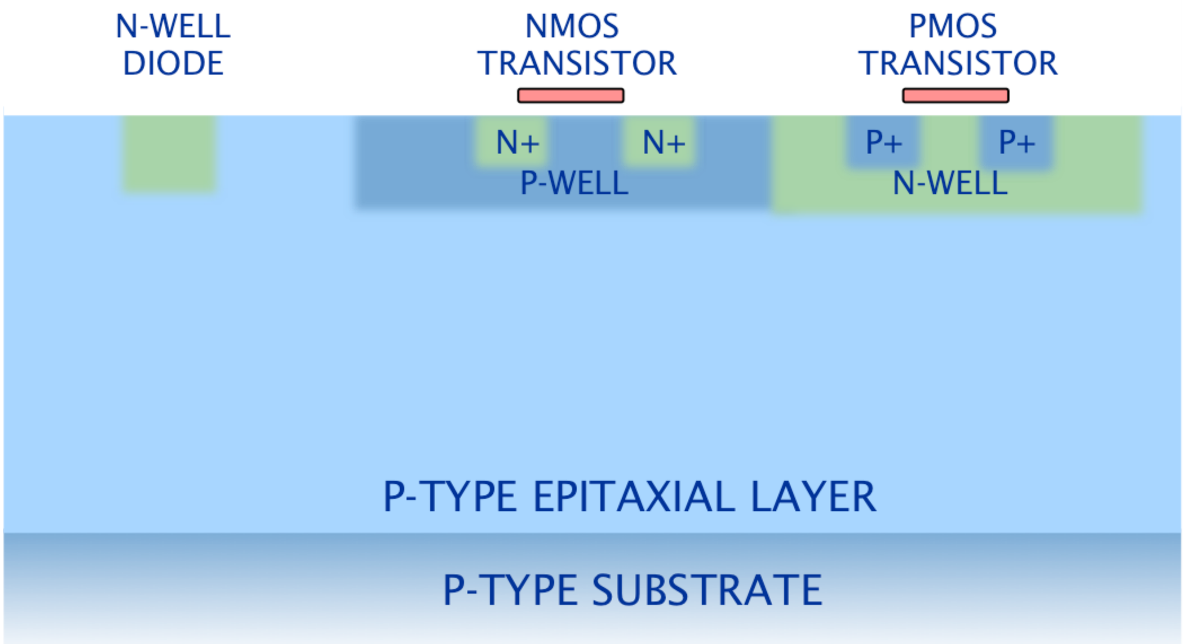
VERTEX 2015: Santa Fe, USA

Outline

- CMOS pixels for particle physics: MAPS
- Deep implants and high-resistivity epitaxial layers
- Working sensors: TPAC, Fortis, Cherwell...
- Latest submission: HR-CHESS
- Plans for the future

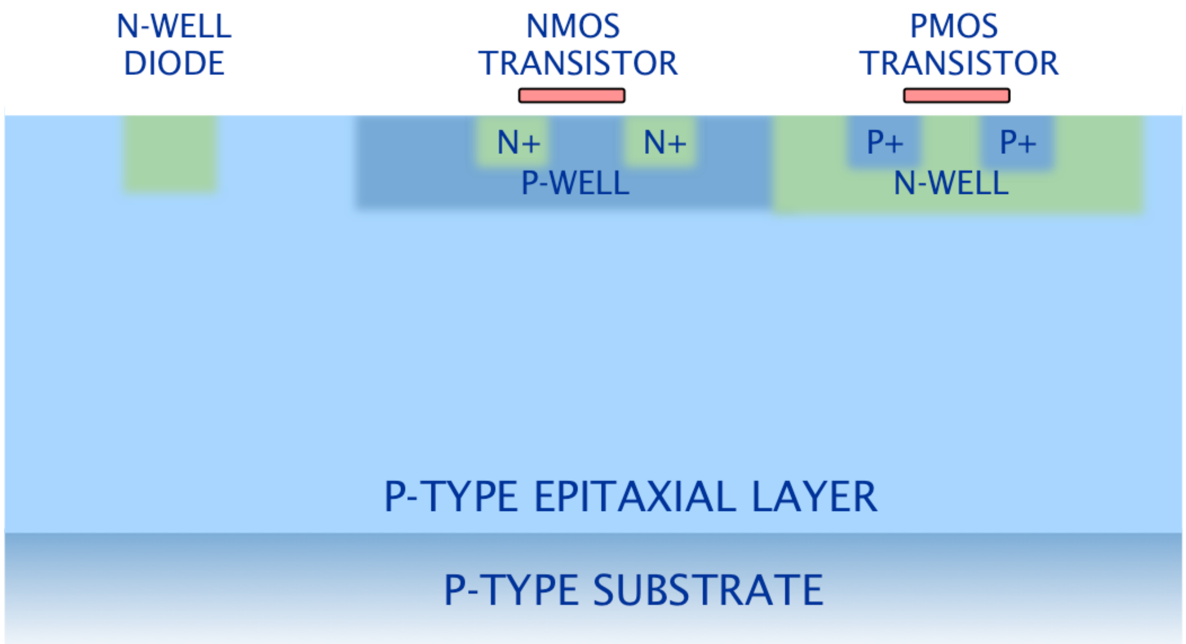
Monolithic Active Pixels for Particle Physics

- MAPS being actively developed for Particle Physics applications
  - ✓ leverage camera technology; lots of nice design features and flexibility
  - ✓ Small, high resolution "intelligent" pixels



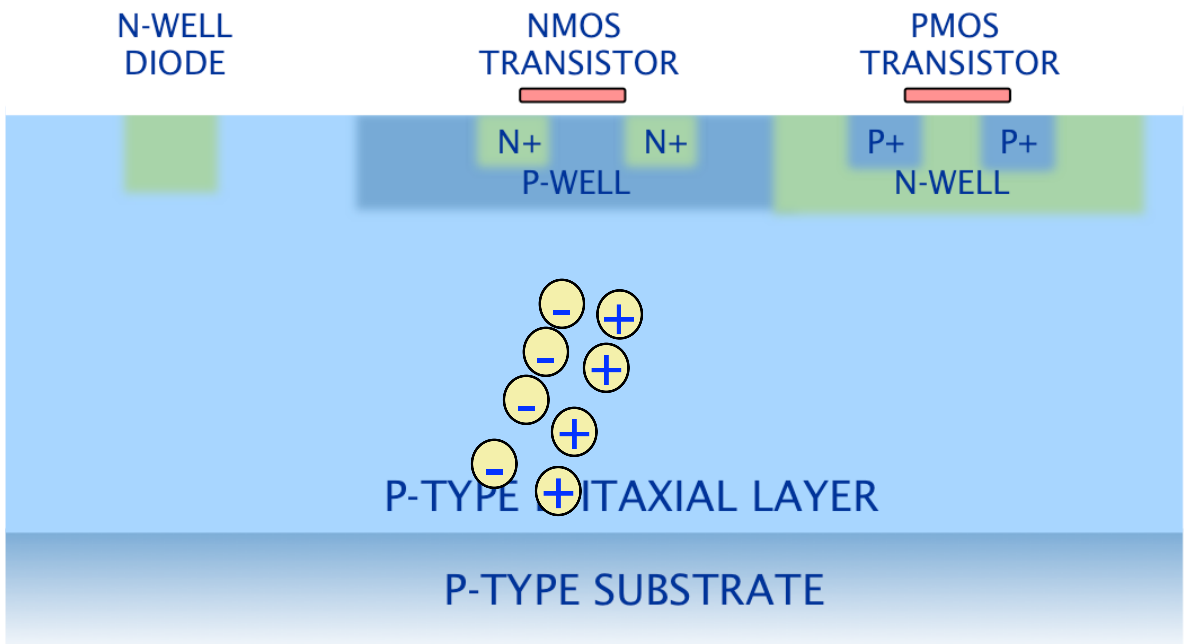
Monolithic Active Pixels for Particle Physics

- MAPS being actively developed for Particle Physics applications
  - ✓ leverage camera technology; lots of nice design features and flexibility
  - ✓ Small, high resolution "intelligent" pixels
  - x First efforts: relatively slow readout & rad soft (for LHC), parasitic collection



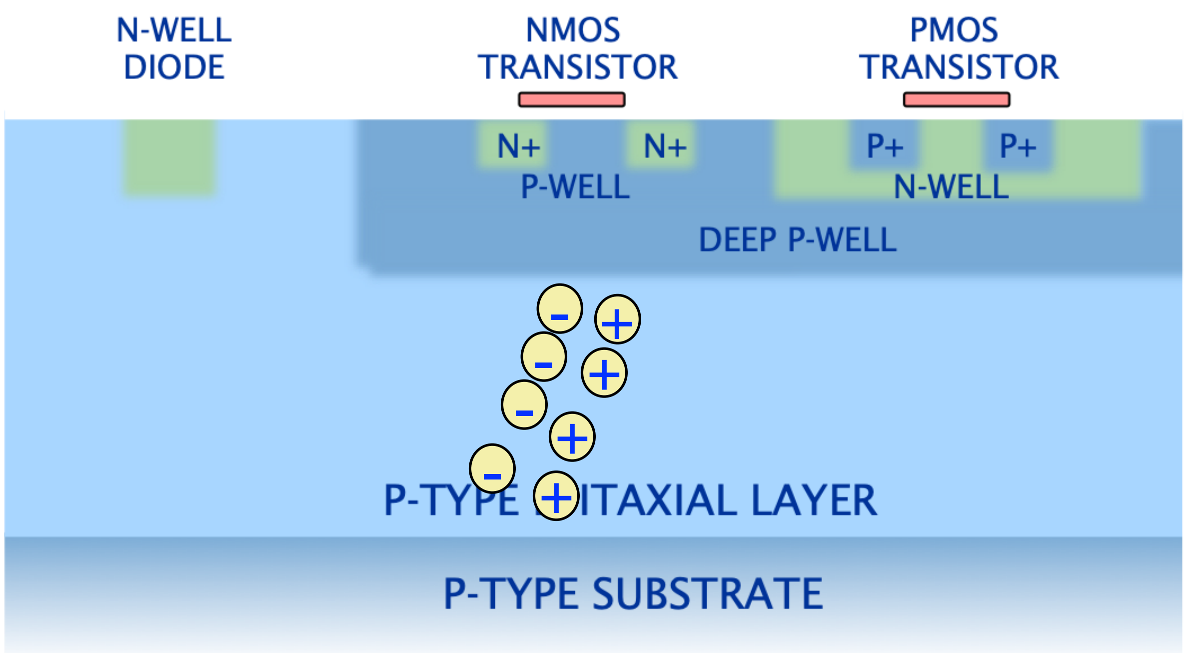
Monolithic Active Pixels for Particle Physics

- MAPS being actively developed for Particle Physics applications
  - ✓ leverage camera technology; lots of nice design features and flexibility
  - ✓ Small, high resolution “intelligent” pixels
  - x First efforts: relatively slow readout & rad soft (for LHC), parasitic collection



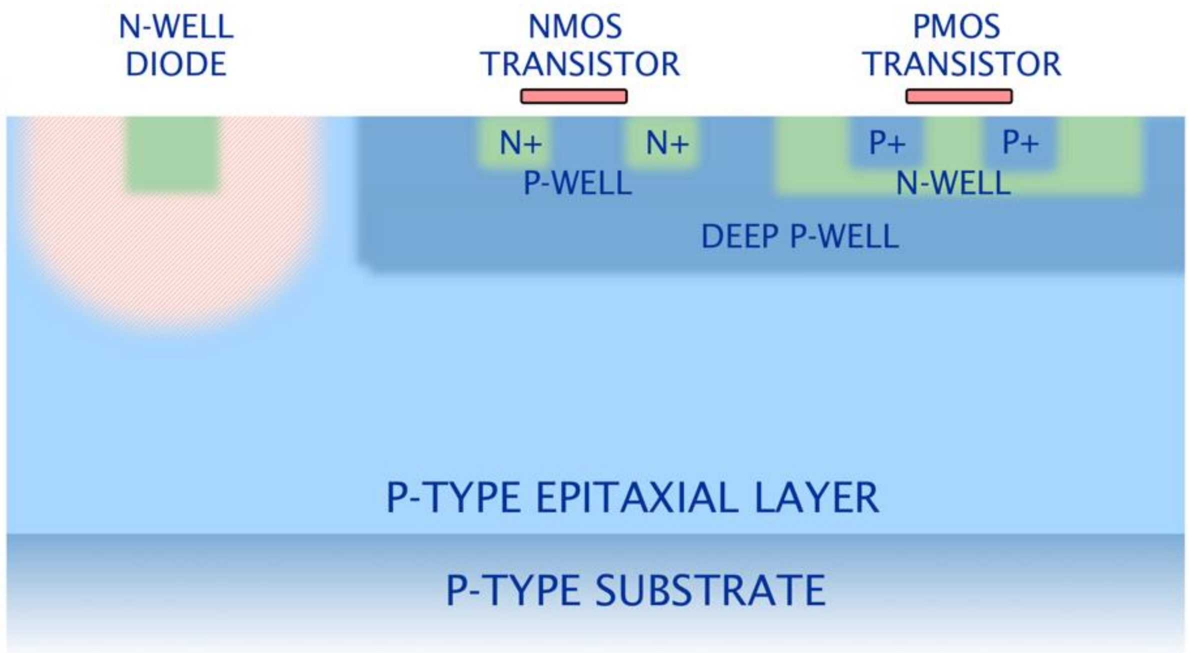
Deep-Well MAPS

- MAPS being actively developed for Particle Physics applications
  - ✓ leverage camera technology; lots of nice design features and flexibility
  - ✓ Small, high resolution "intelligent" pixels
  - x First efforts: relatively slow readout & rad soft (for LHC), parasitic collection
- Deep p-well: full CMOS design



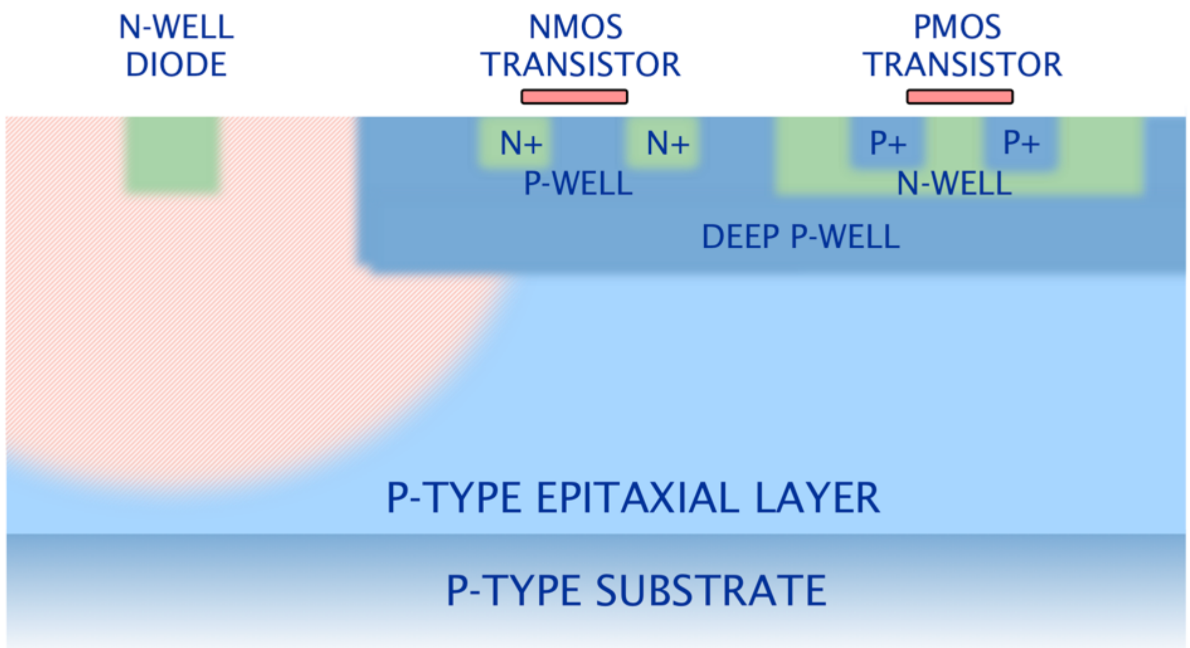
Deep-Well MAPS with HR Epitaxial Layer

- MAPS being actively developed for Particle Physics applications
  - ✓ leverage camera technology; lots of nice design features and flexibility
  - ✓ Small, high resolution “intelligent” pixels
  - x First efforts: relatively slow readout & rad soft (for LHC), parasitic collection
- High-resistivity epitaxial layer: fast charge collection, rad hard



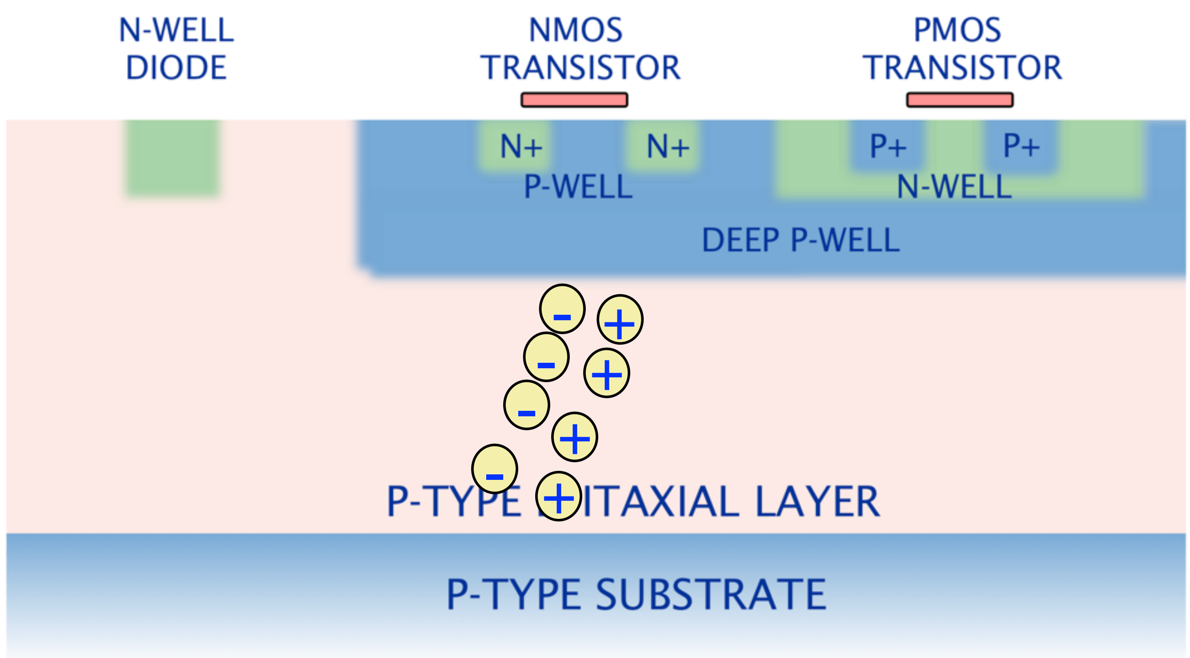
Deep-Well MAPS with HR Epitaxial Layer

- MAPS being actively developed for Particle Physics applications
  - ✓ leverage camera technology; lots of nice design features and flexibility
  - ✓ Small, high resolution “intelligent” pixels
  - x First efforts: relatively slow readout & rad soft (for LHC), parasitic collection
- High-resistivity epitaxial layer: fast charge collection, rad hard



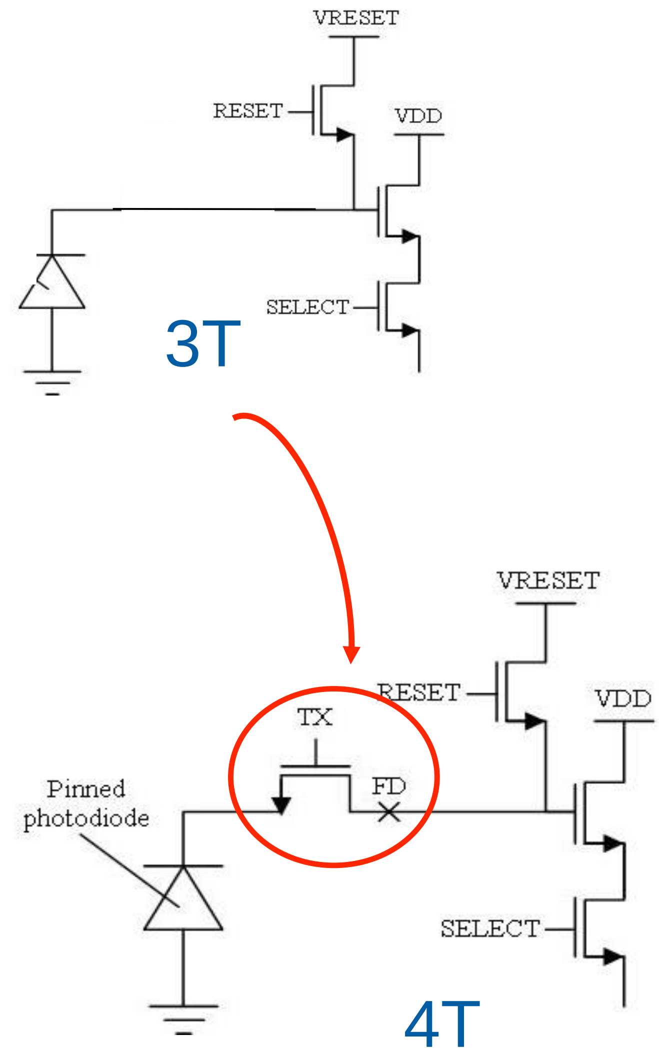
Deep-Well MAPS with HR Epitaxial Layer

- MAPS being actively developed for Particle Physics applications
  - ✓ leverage camera technology; lots of nice design features and flexibility
  - ✓ Small, high resolution “intelligent” pixels
  - x First efforts: relatively slow readout & rad soft (for LHC), parasitic collection
- High-resistivity epitaxial layer: fast charge collection, rad hard



Deep-Well CMOS Imagers

- Standard CMOS (Imager) Process
  - e.g. 180 nm; 6 metal layers
  - Precision passive components (R/C)
  - Low leakage diodes
  - Thick epitaxial layers (e.g. 12-18 µm)
  - 4T (or more) structures
  - Stitching options
- Added features
  - Additional deep implant; n- or p-well
  - Custom epi (e.g. high-resistivity, 25 µm or more)
- Benefits
  - Faster charge collection (drift, not diffusion)
  - Reduced charge spread
  - Increased Radiation hardness



HR-CMOS Features

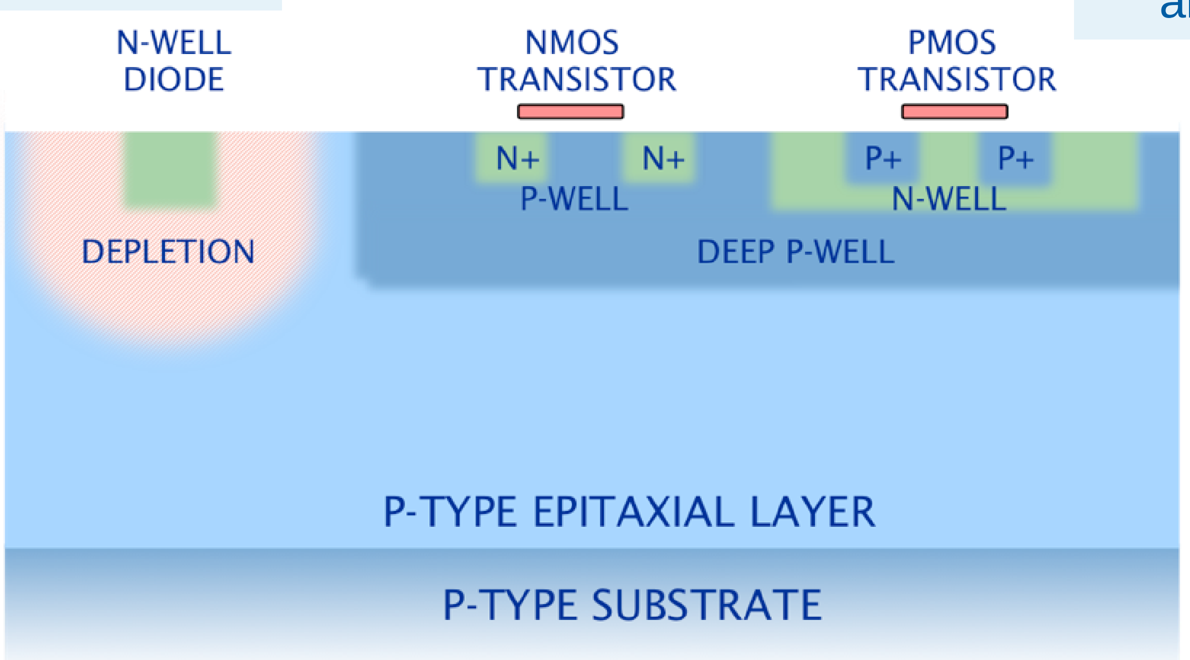
HR-CMOS: High-resistivity epitaxial layer, low-voltage bias, charge collection by drift, faster, rad hard

Thin sensitive layer: shorter collection times, less multiple scattering & charge capture

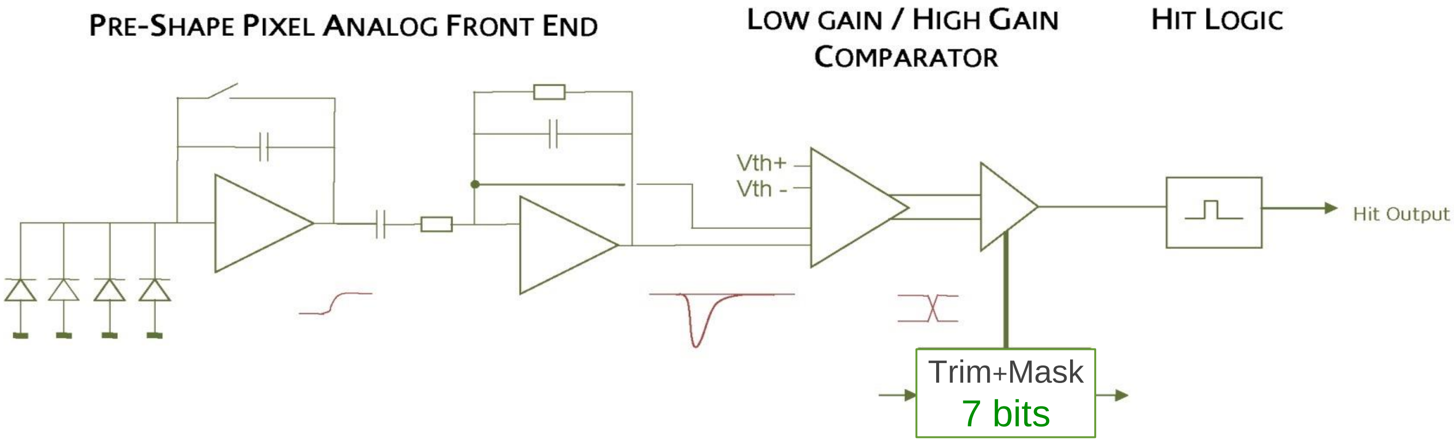
Guard rings: improve resistance to radiation damage

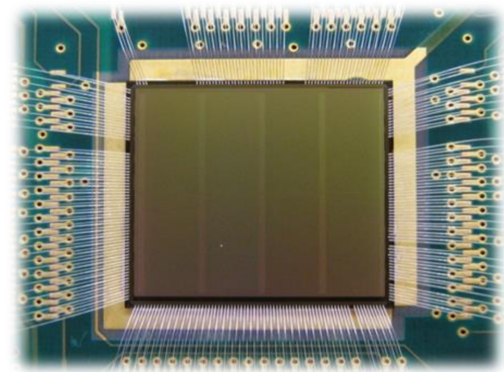
High-resistivity epitaxial layer: improved signal to noise

Deep p-well: enhanced charge collection, allows full CMOS

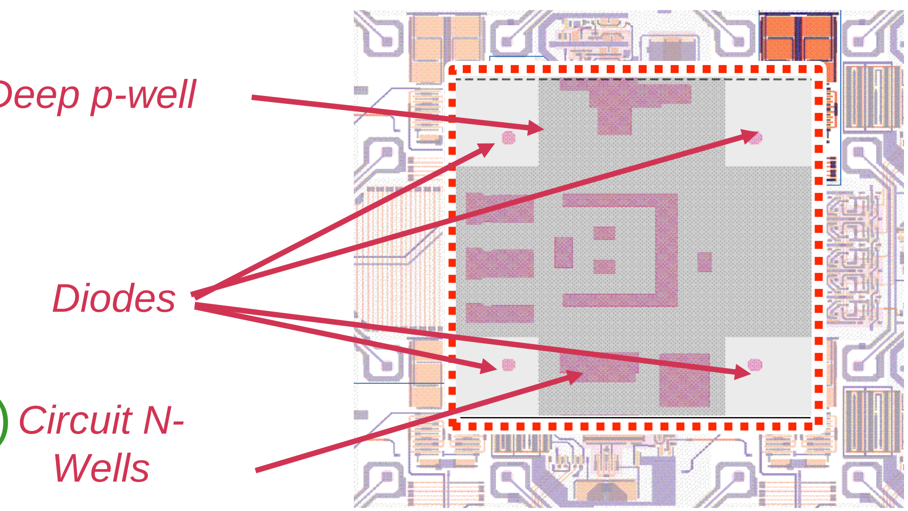


TPAC: Sensor for a Digital ECAL





- Digital ECAL Particle Counter
  - 28224 pixels , 50 x 50 μm^2
  - 8.2 million transistors
  - Sensitive area 79.4 mm^2
- Data readout
  - Record hit locations & timestamps
  - On-chip sparsification
  - 30 bit parallel data output (slow <5Mhz)

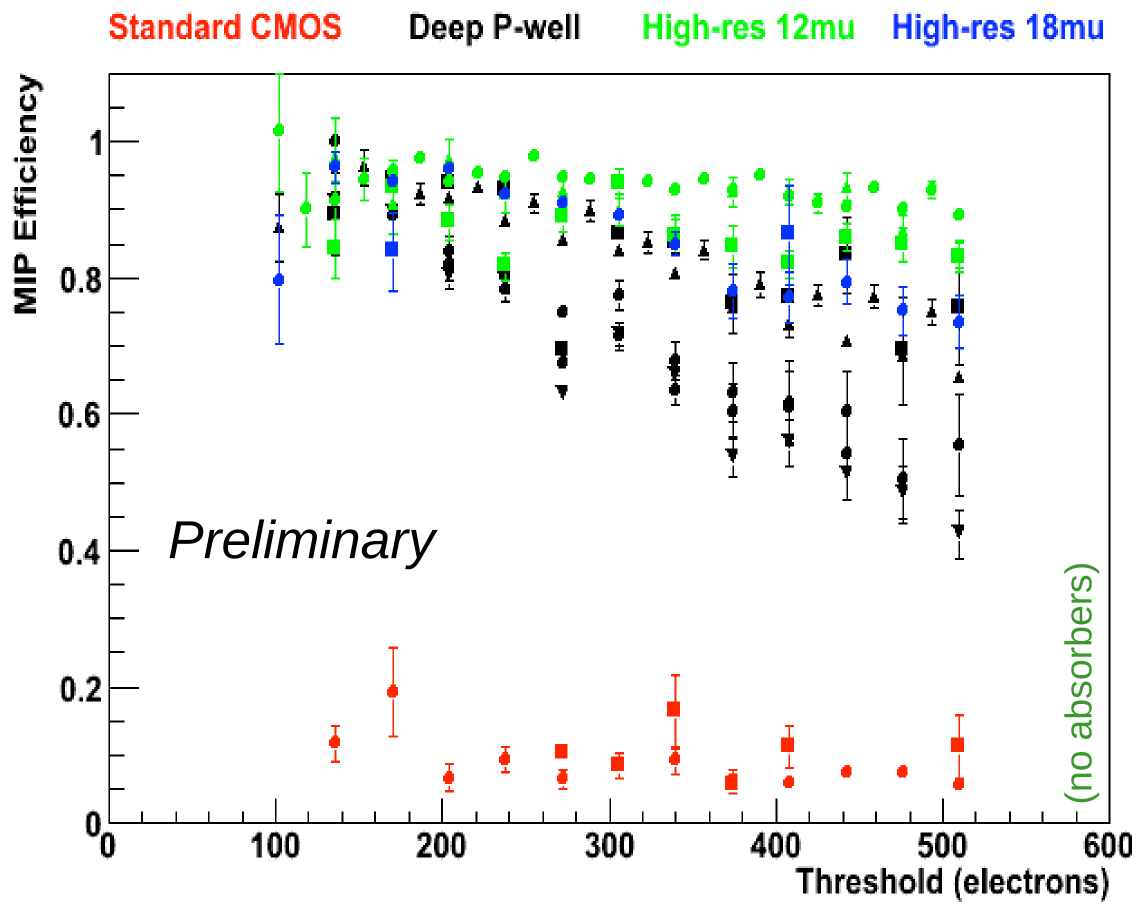


TPAC: Testbeam Results

Standard CMOS: use of in-pixel PMOS transistors means low efficiency

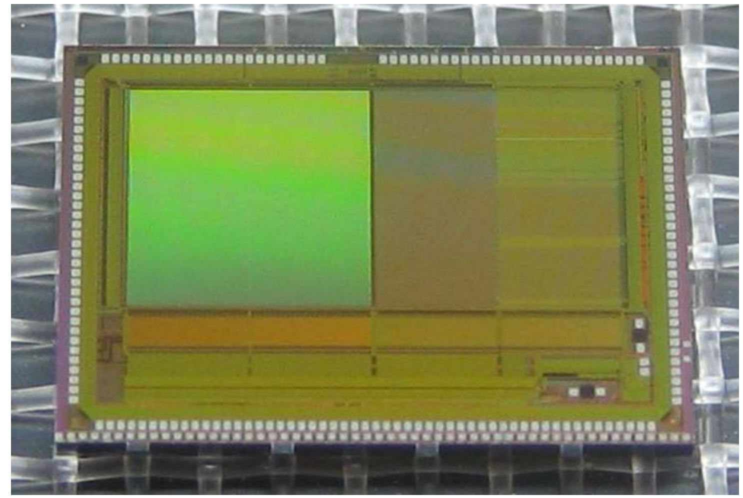
Deep P-well: shields N-wells and raises efficiency by factor ~5

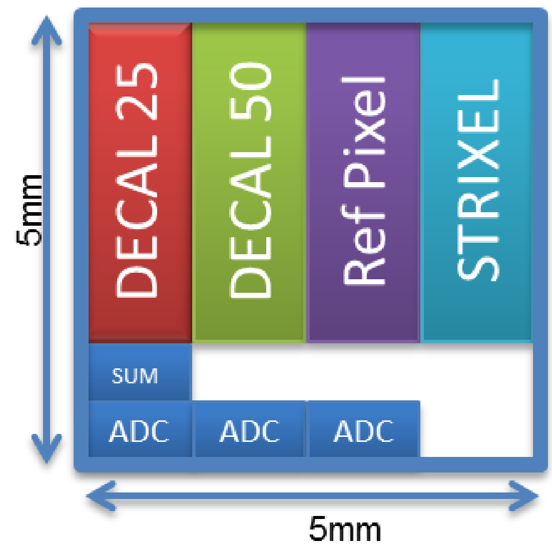
High-resistivity epi: adding this makes further improvement with resulting efficiency close to 100%



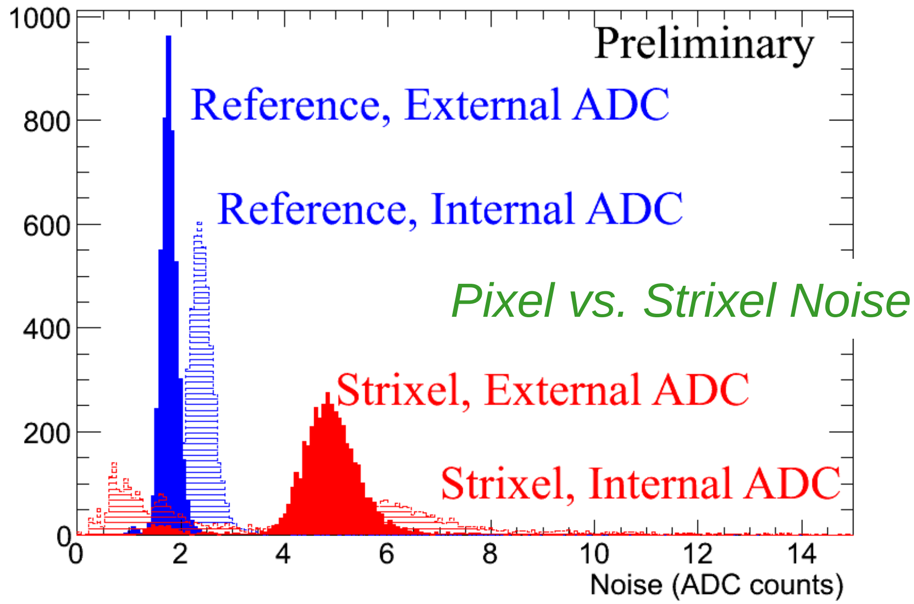
Cherwell

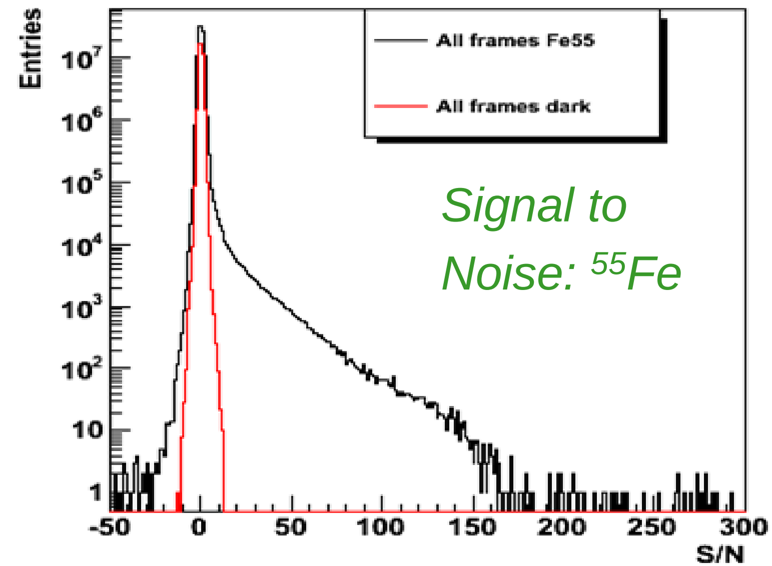
- HR-CMOS MAPS for tracking/calorimetry
  - Brings together full 4T pixels, deep p-implant, high resistivity epitaxial later
  - Variants with in-pixel CDS, global shutter
  - 25 and 50 μm pitch, strixel arrays
- Summary of Cherwell1 results
  - Signal to noise > 100
  - Noise ~8 e-
  - Hit efficiency > 99.7%
  - Hit resolution ~3.7 μm
  - Pedestals and noise consistent across pixels
  - In-pixel electronics results still to be done
- Three generations: Cherwell 2 & 3 candidates for ALICE pixels

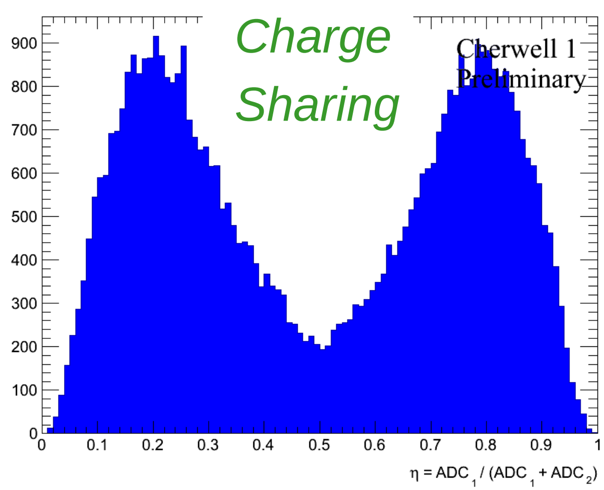


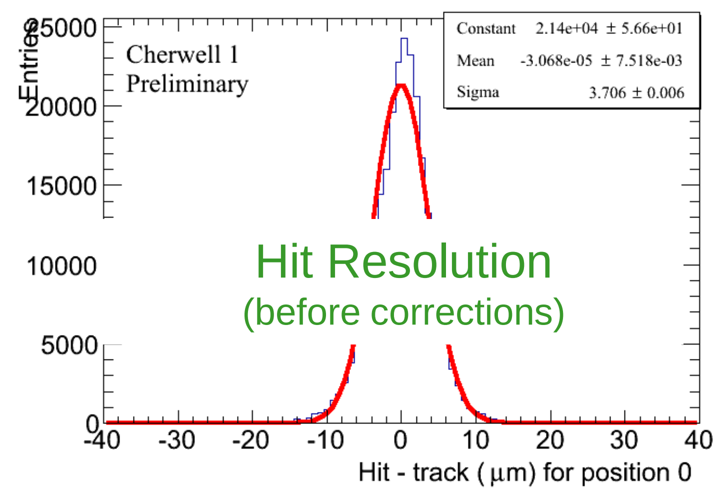


Cherwell: Preliminary Results



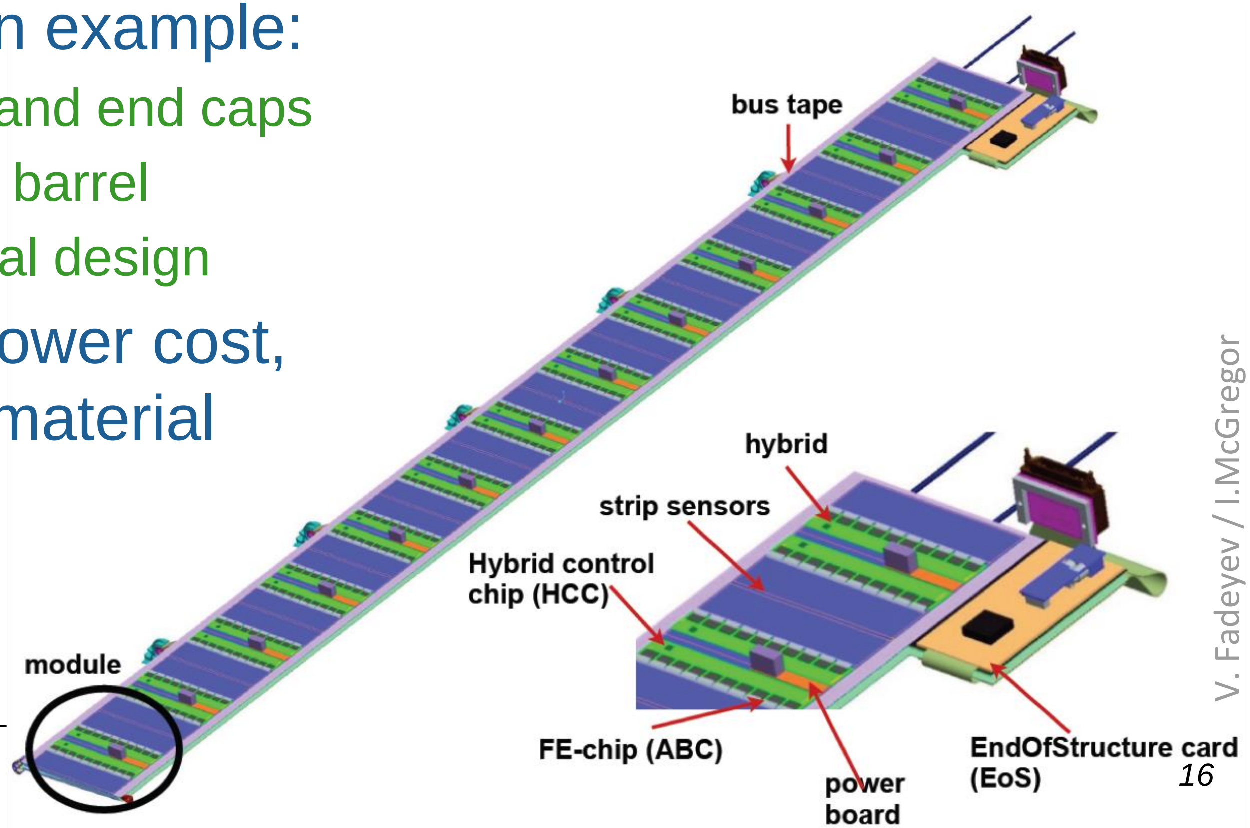






HR-CMOS @ LHC

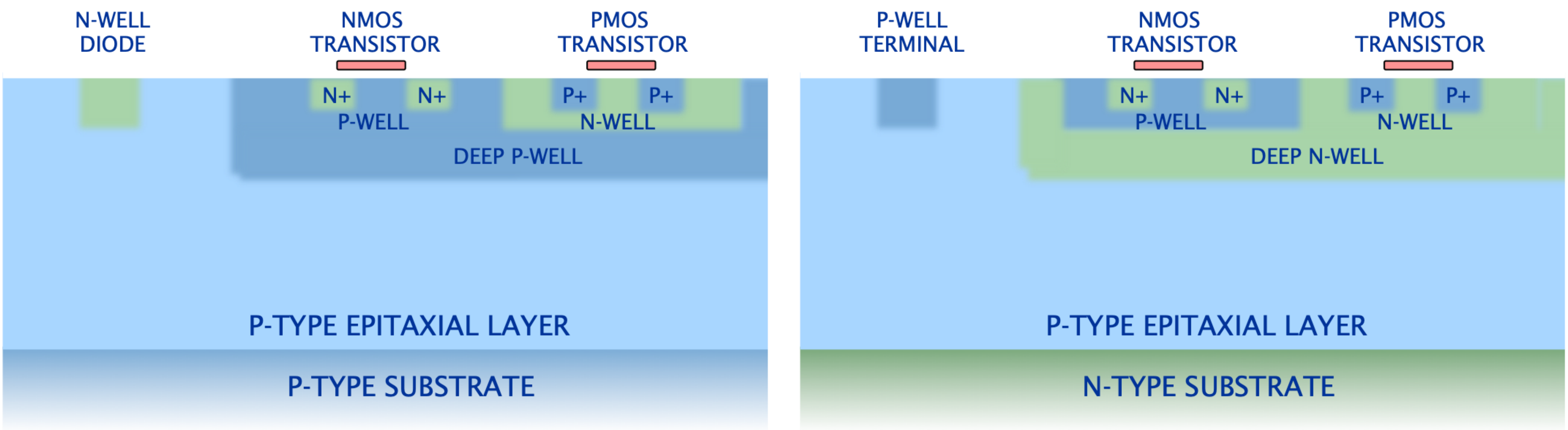
- CMOS pixels studied for LHC upgrades; pixel and strip detectors
  - HR-CMOS most promising for tracker upgrades as a “sensor replacement”
  - On-chip: sensing elements, amplifiers/comparators with pixel sensors
  - Off-chip: digital processing, trigger pipeline, command I/O with readout ASIC
  - Keep the existing readout chain, but still need bump bonding
- ATLAS strip tracker as an example:
  - ~200 m^2 silicon in barrels and end caps
  - stave/module structure for barrel
  - 10 x 10 cm^2 sensor nominal design
- CMOS has potential for lower cost, faster construction, less material



V. Fadeyev / I.McGregor

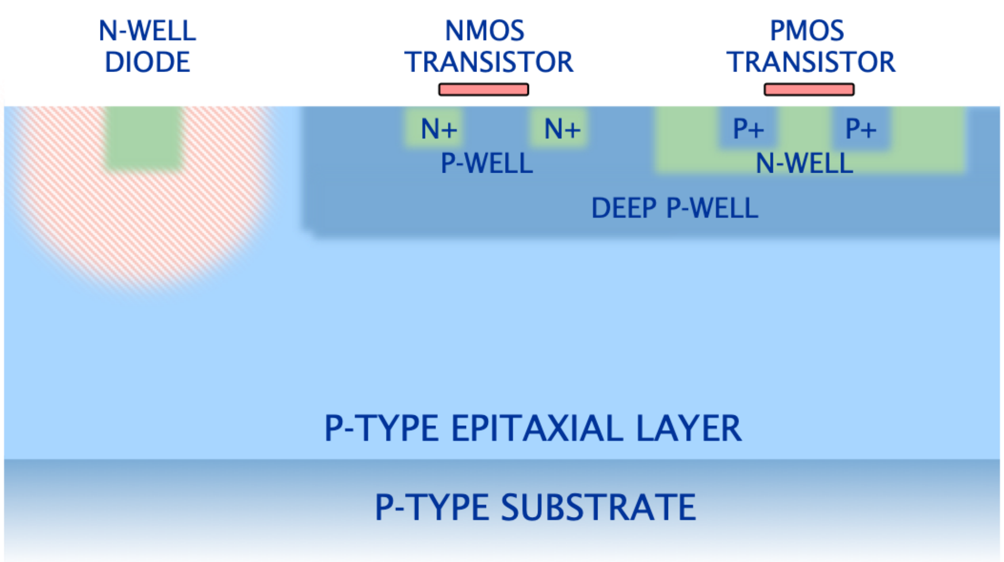
HR-CHESS Project

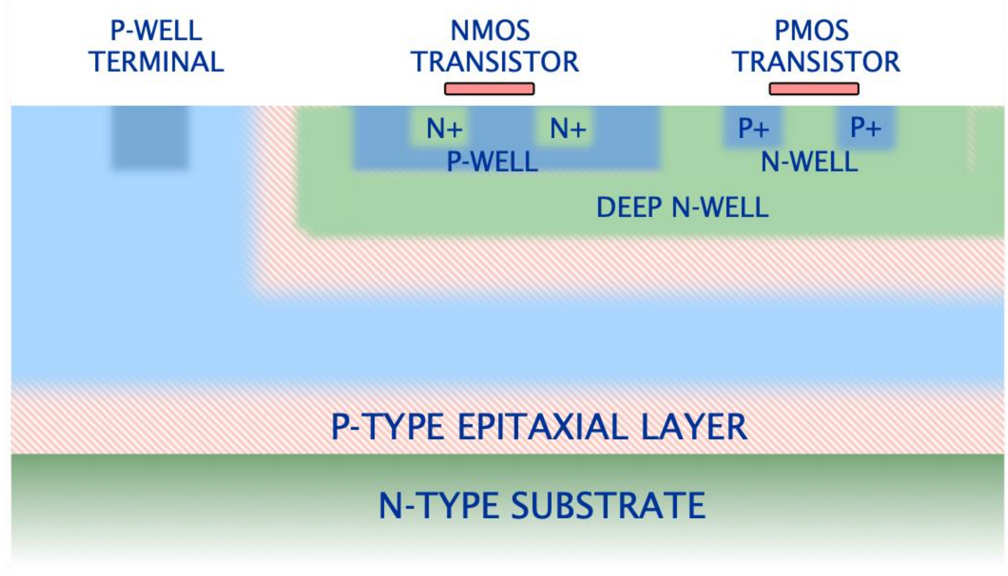
- Over-depleted epi for charge transport by drift rather than diffusion
- Many variants and epitaxial thicknesses explored
  - p-type epitaxial on n-type substrate (PonN)
  - p-type epitaxial on p-type substrate (PonP)



HR-CHESS Project

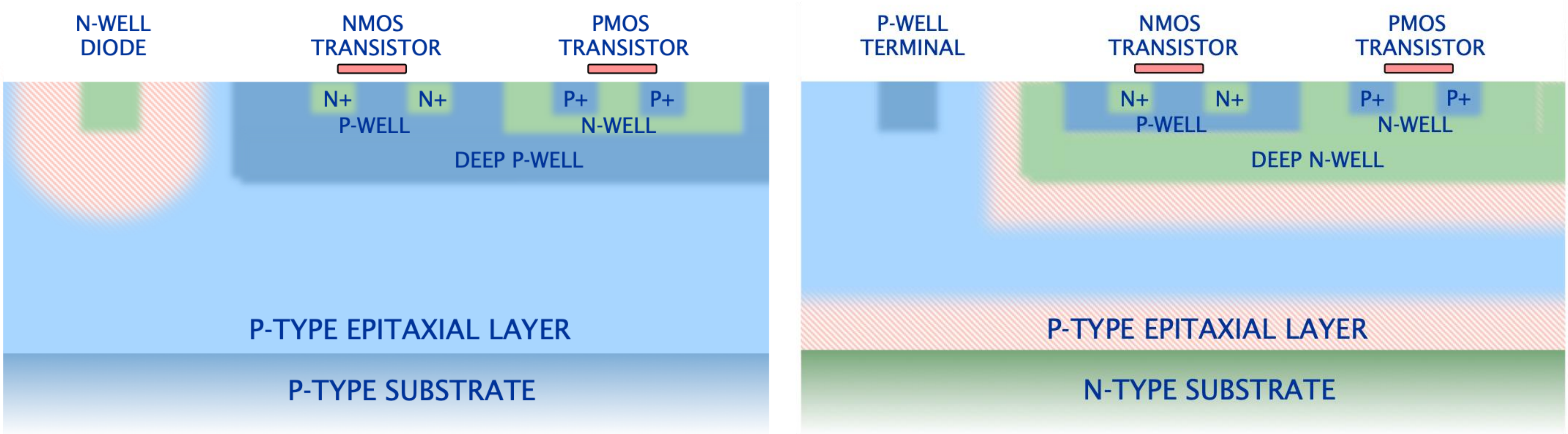
- Over-depleted epi for charge transport by drift rather than diffusion
- Many variants and epitaxial thicknesses explored
  - p-type epitaxial on n-type substrate (PonN)
  - p-type epitaxial on p-type substrate (PonP)





HR-CHESS Project

- Over-depleted epi for charge transport by drift rather than diffusion
- Many variants and epitaxial thicknesses explored
  - p-type epitaxial on n-type substrate (PonN)
  - p-type epitaxial on p-type substrate (PonP)



Goals: high-radiation tolerance > ~100 Mrad, high speed with 90% of charge collected in < ~20 ns, low voltage depletion (10-20V)

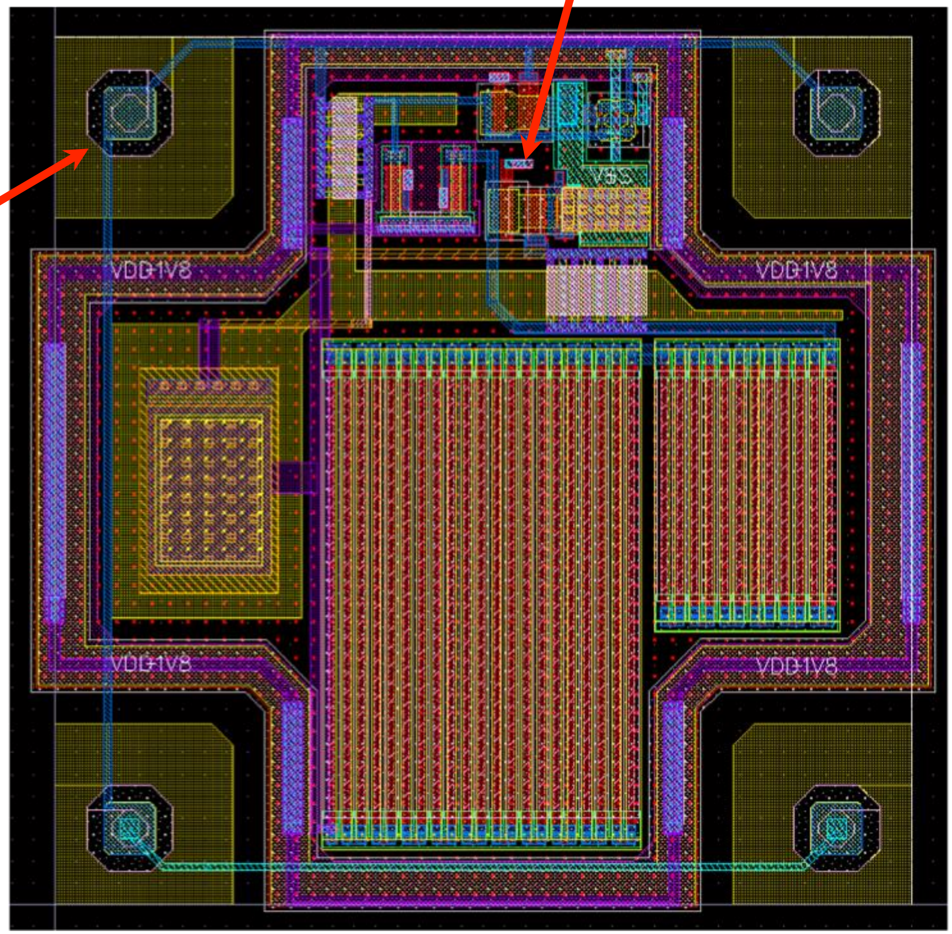
HR-CHESS Project

- Test devices from MPW coming out now
- First structures for testing pixel response (minimal ancillary logic)
- Lots of variants and structures to test:
  - 40µm x(40, 80, 200, 400, 800)µm pixels
  - Different epitaxial layer thicknesses, resistivities
- Development team:
  - Design: D. Das, R. Turchetta
  - Physicists: J. Doepke, S. McMahon, G. Villani, F. Wilson, S. Worm
  - Simulation: RAL+Glasgow
  - Testing: open to all

HR-CHESS: PonN 40x40 μm^2

Electronics in deep N-well

Collecting Cathodes (x4)

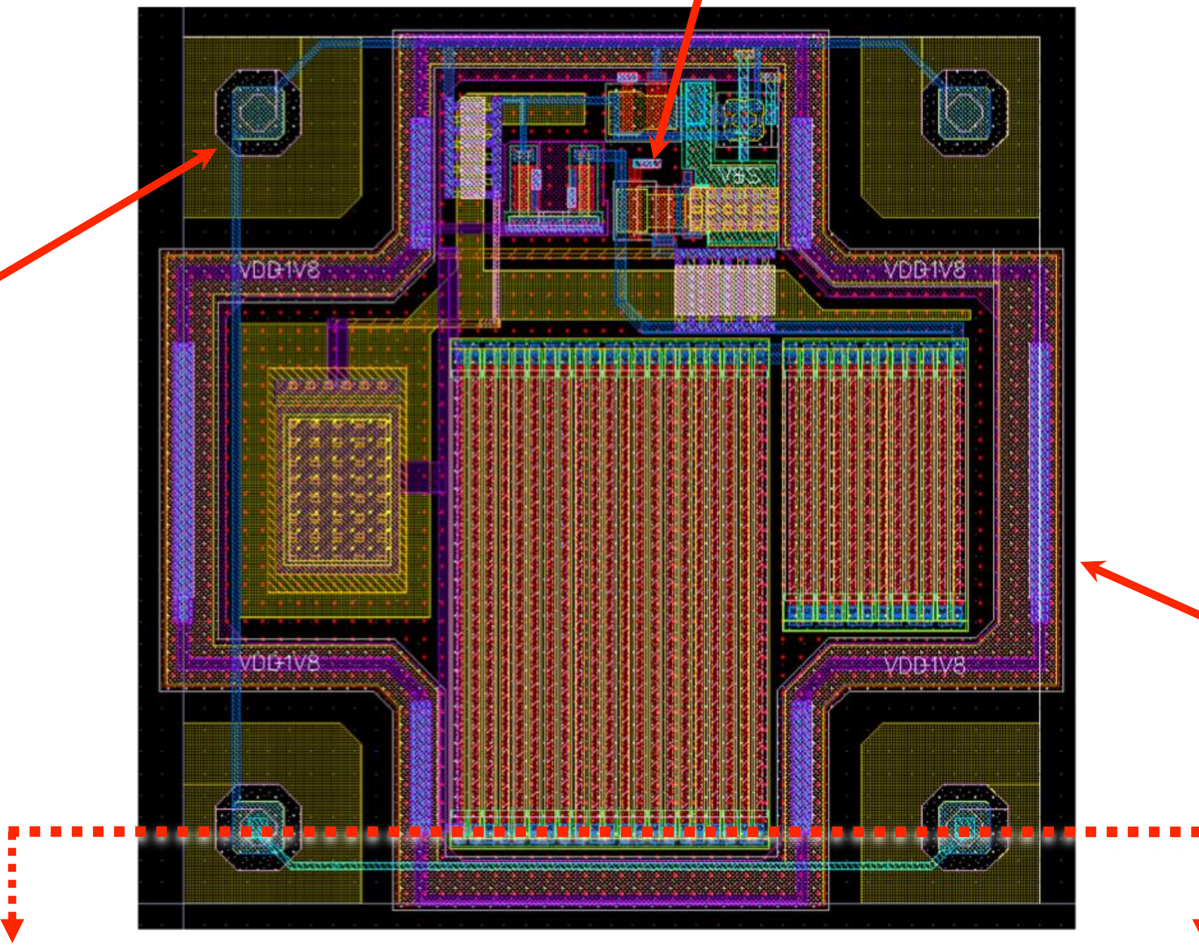


N-well isolation ring

HR-CHESS: PonN 40x40 μm^2

Electronics in deep N-well

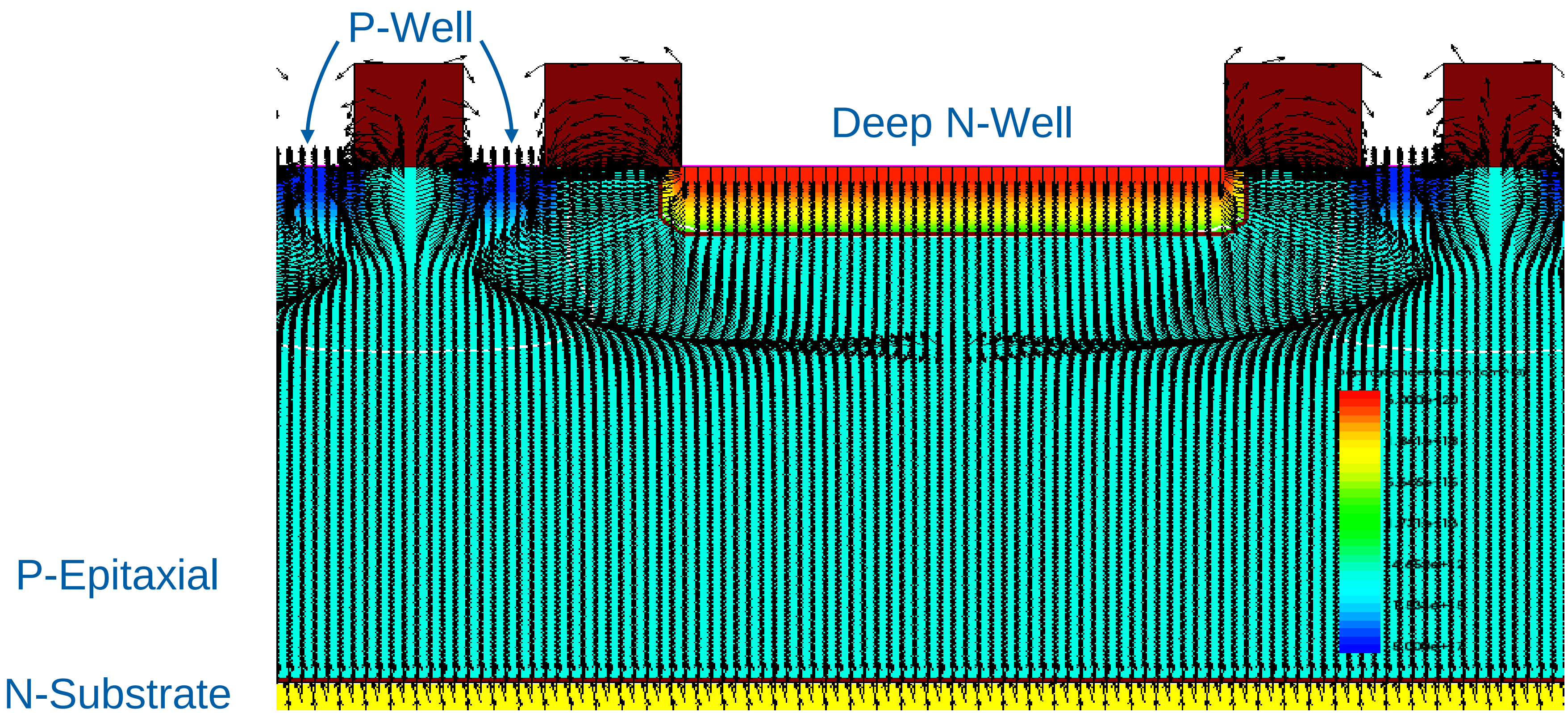
Collecting Cathodes (x4)



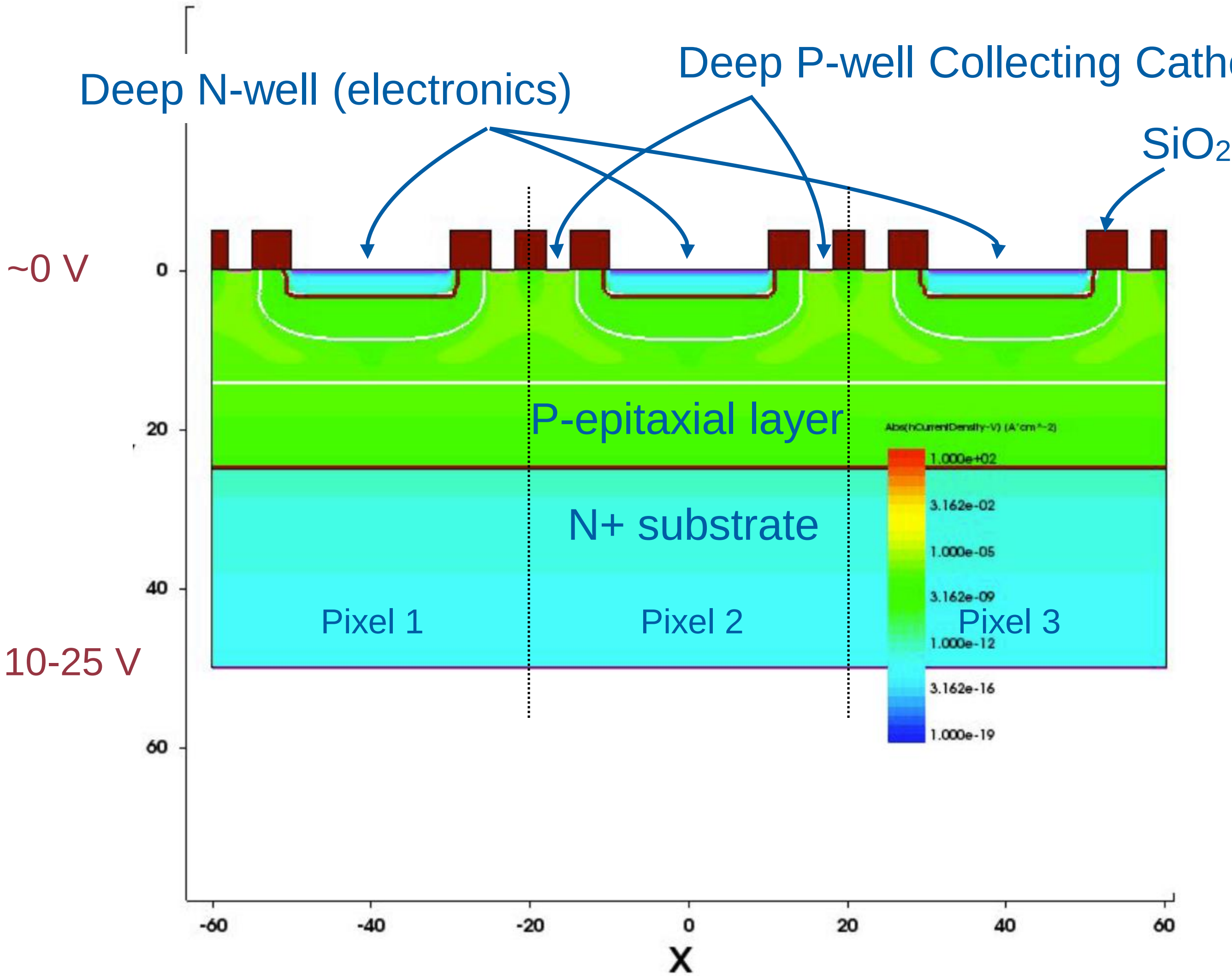
N-well isolation ring

HR-CHESS: E-Field Simulation

- Simulation to test back bias, confirm no charge gets stuck
- Now optimising for different resistivities, geometries, trapping...



HR-CHESS: Layout

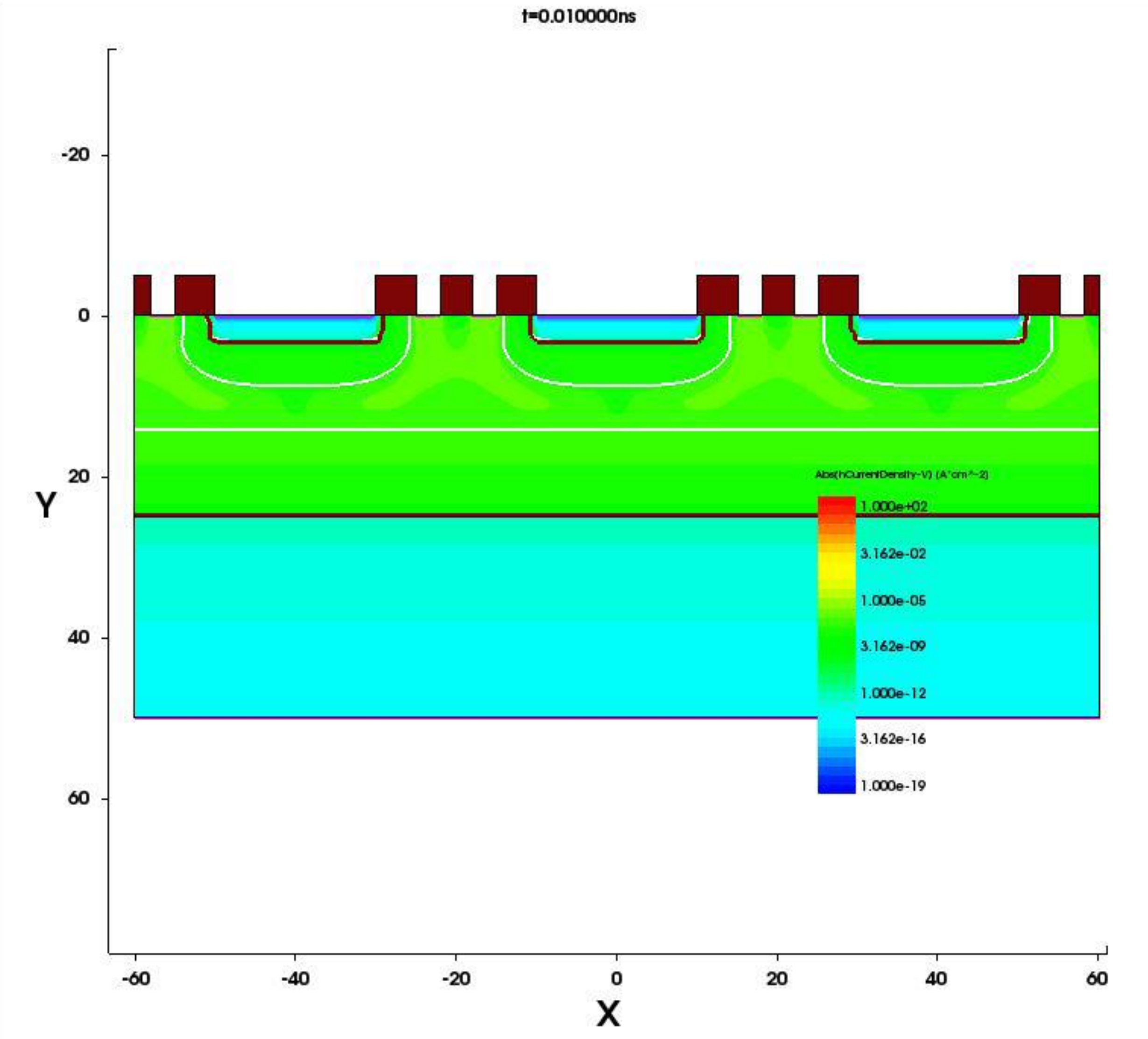


Basic Layout: Based on previous successful pixels (e.g. PIMMS)

Simulation: Studied electric field versus configuration and implant details

Bias: Surface structures set between 0-1.8V, substrate around 10-25V

HR-CHESS: Charge Drift for PonN

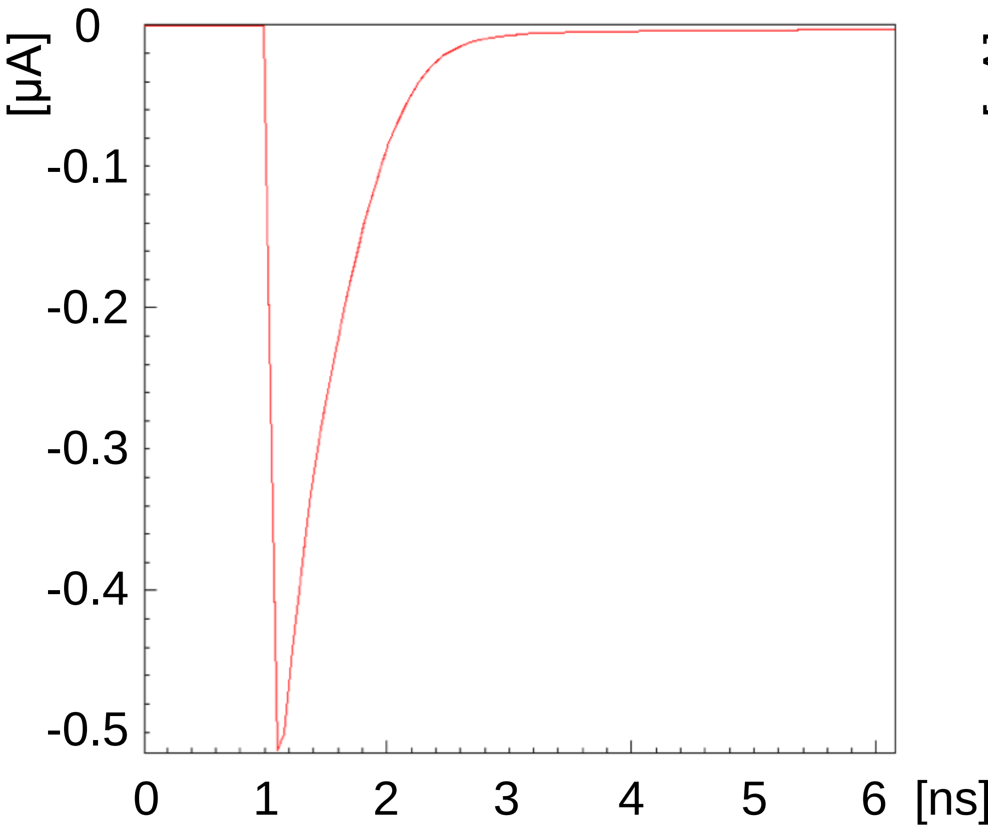


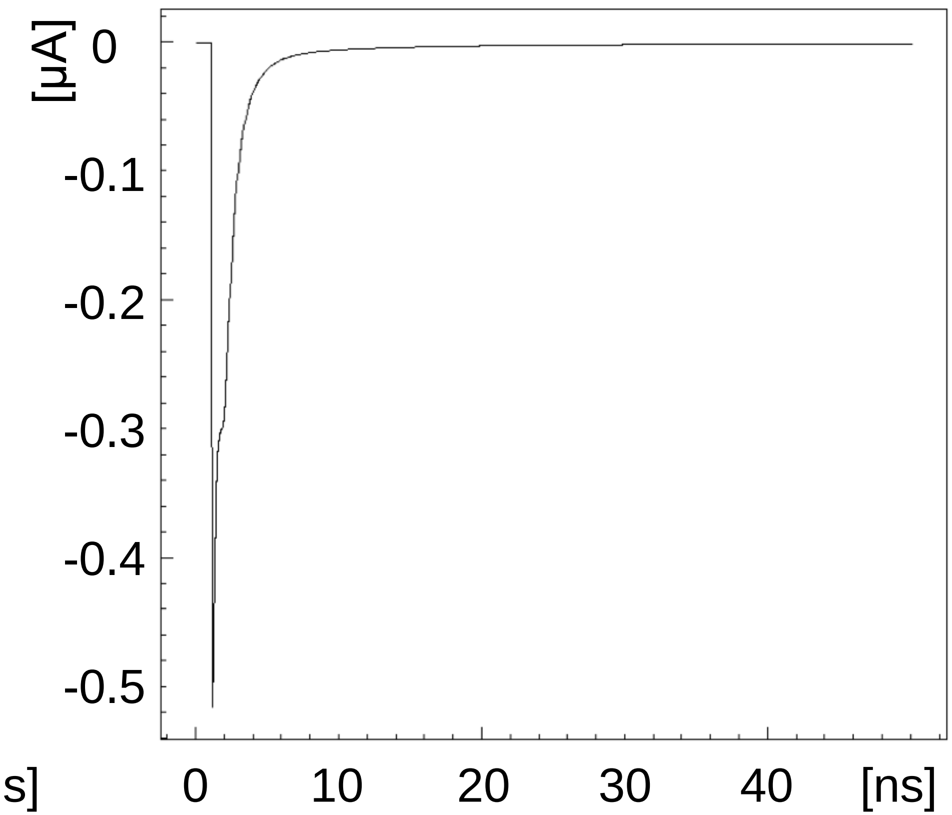
Setup: Perpendicular track through middle of sensor

Timing: Shows current density distribution between 0-27 ns

Result: Majority of charge arrives within a few ns. Charge does not get trapped under pixel.

HR-CHESS: Current Simulation for PonN





15 V backbias, at diode (20μm)

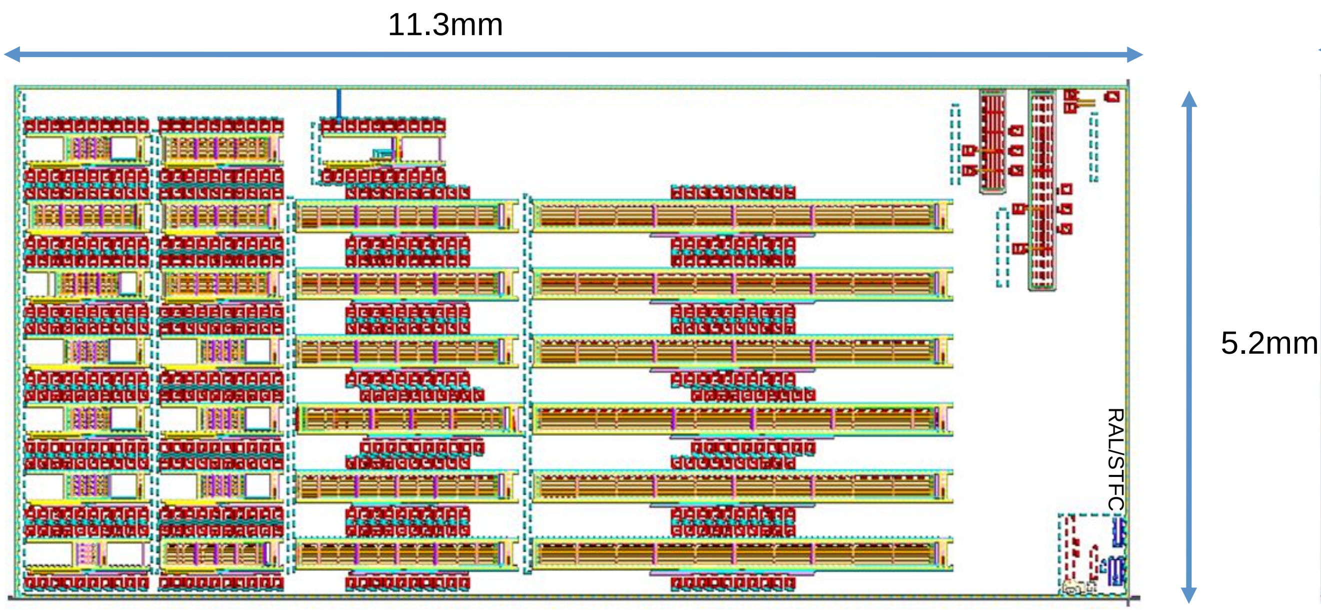
fast charge collection for nominal conditions (close to diode)

10 V backbias, 10 μm from diode

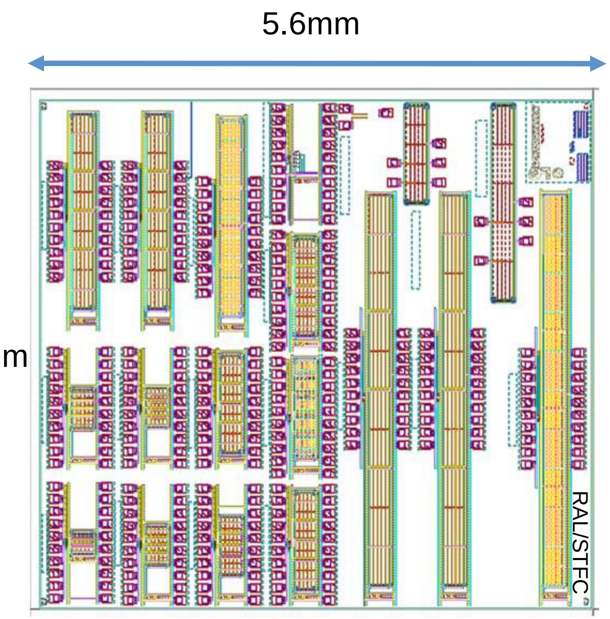
good charge collection for less optimal conditions also

HR-CHESS Project

PonN: 30 variants



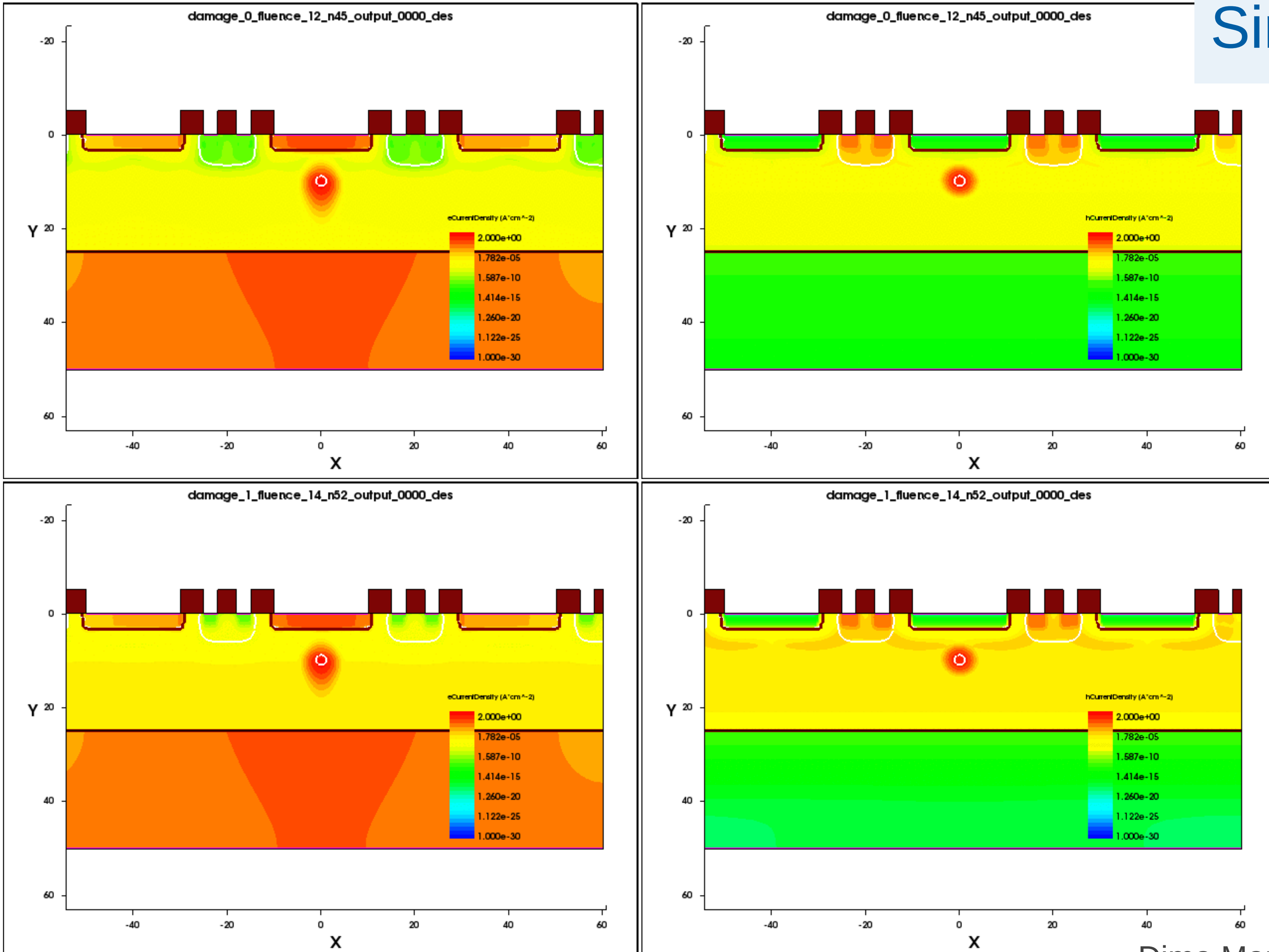
PonP: 19 variants



PonN Simulation

electrons

holes



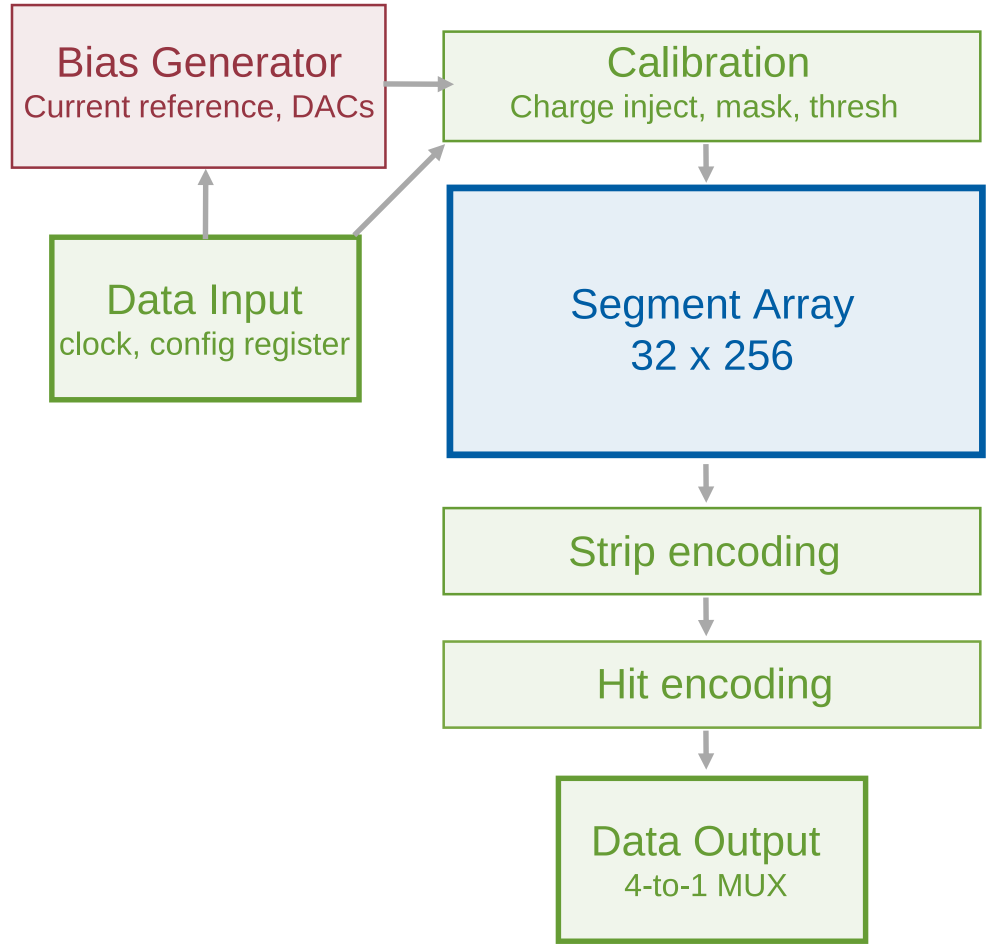
no RAD damage

1e14 damage

Dima Maneuski, Glasgow

Plans for HR-CHESS2

	Requirement
Segment size	800 µm x 40 µm
Array	32 segments x 256 strips
Sensor size	25.6 mm x 10.24 mm
Hits to be readout	8 hits@40MHz per 128 strip (max 8 hits/cm^2/25ns) 4.16 Gbits/s
Signal (e- per MIP)	2000 (25 µm thickness)
Noise in e- RMS	< 30
Radiation Hardness	100 Mrad TID; 10^{15} n_{eq}/cm^2
Power Budget	0.02 W/cm^2 (6 µW/pixel)

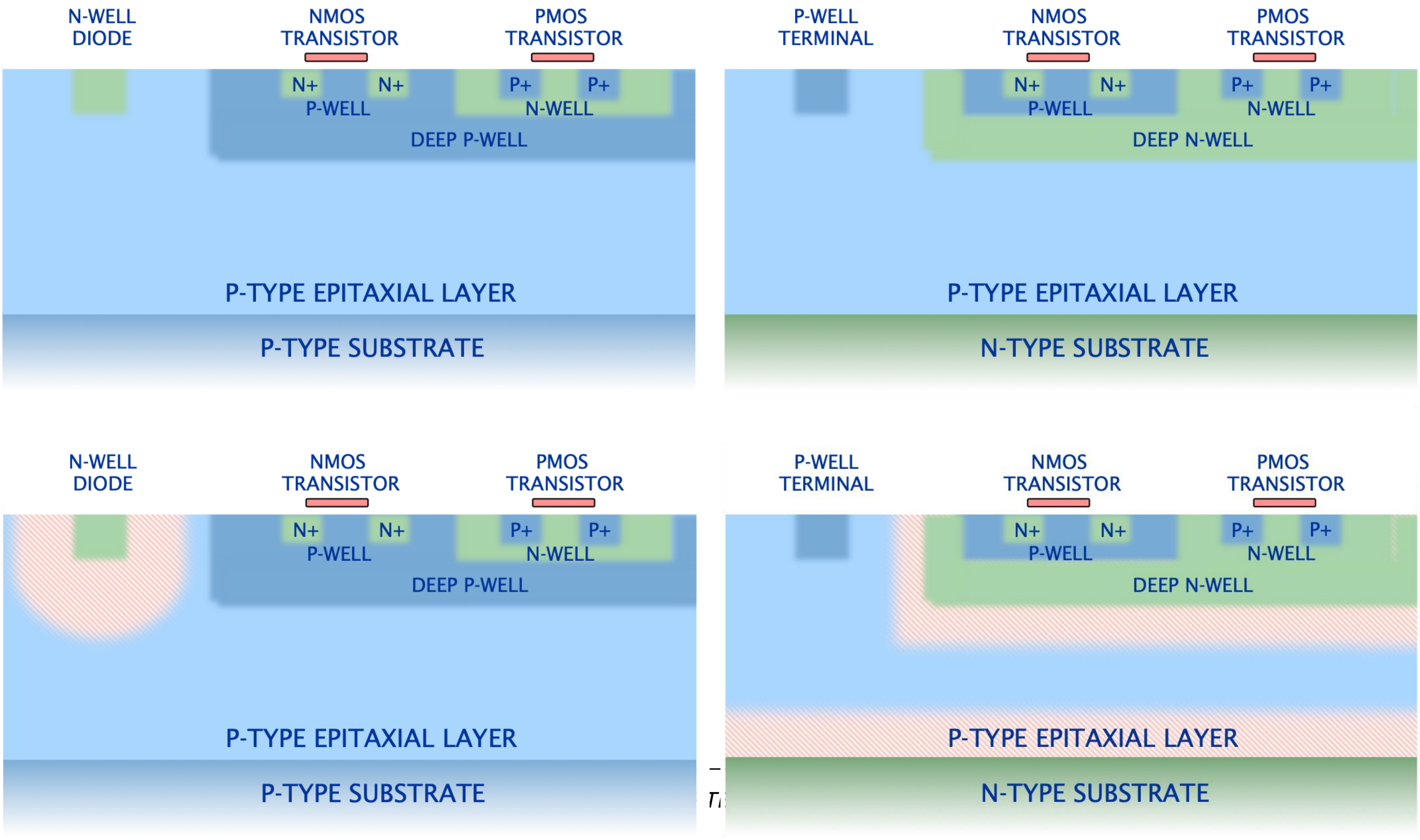


HR-CHESS2: Architectural submission following ATLAS upgrade readout specs

Conclusions

- CMOS pixels have *huge potential* for particle physics
- Deep implants and high-resistivity epitaxial layers can be used to make the most of the technology: *HR-CMOS*
- Many working examples and a new chips back soon: *HR-CHESS*
- Assuming success, architectural submission is next: (*Engineering run, anyone?)*

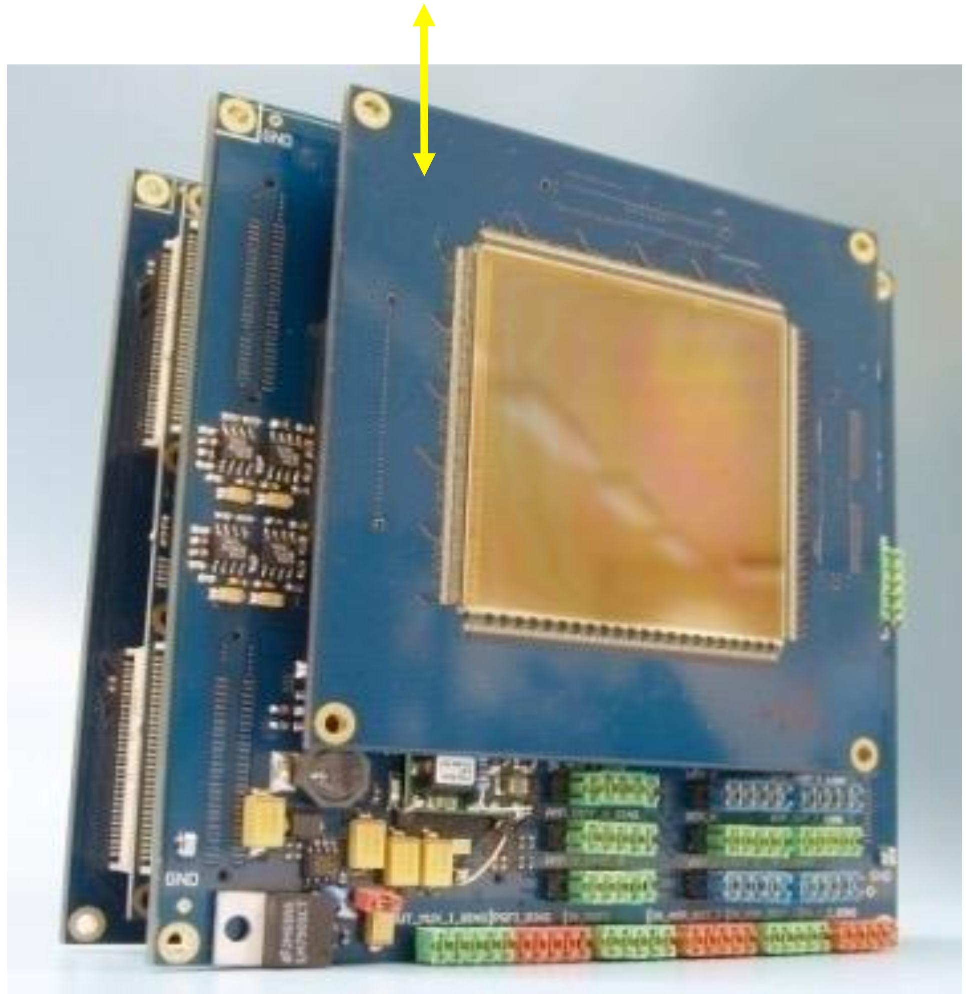
HR-CMOS: PonP and PonN Structures



Stitched Sensors

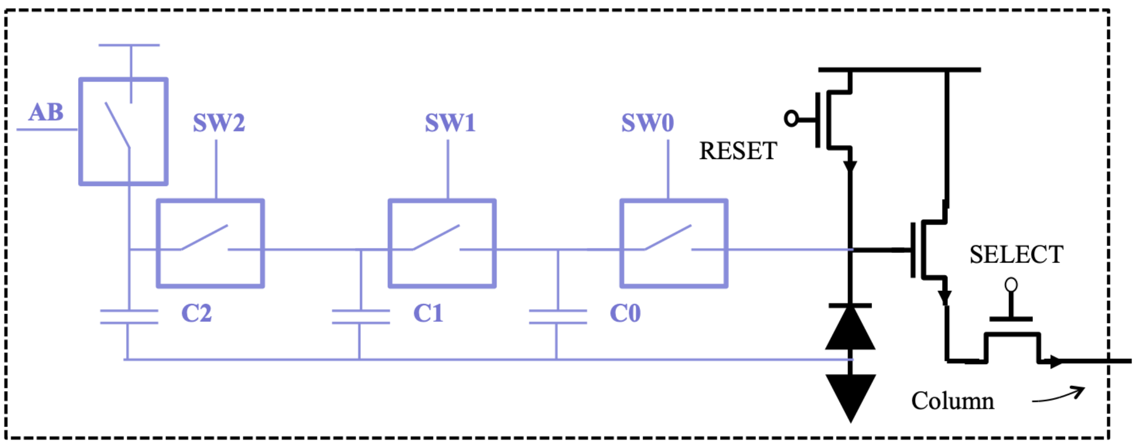
Standard CMOS limited to reticle ~2.5 x 2.5 cm²

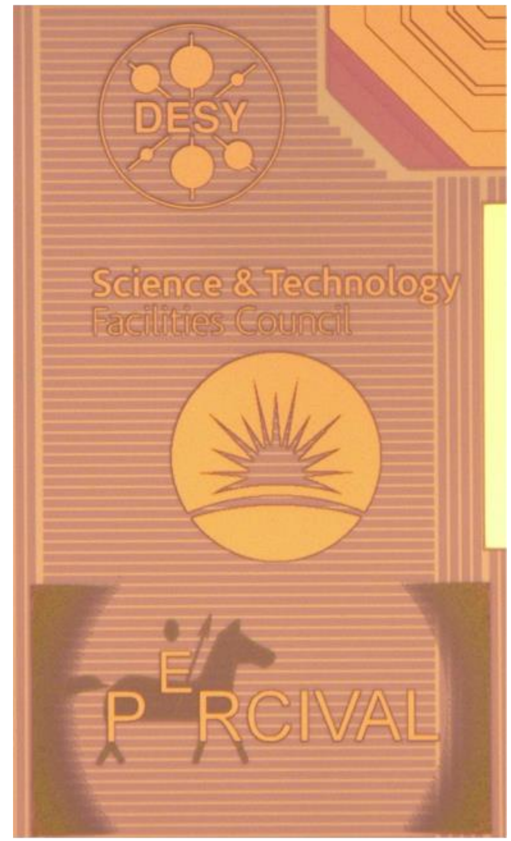
- Stitching relatively established for CIS
  - Stitching offered by many foundries
  - Allows wafer-scale sensors
- Example Sensor
  - Lassena (for imaging)
  - Designed at RAL
  - 5.4 x 5.4 cm²



Percival

- Percival: Pixelated Energy Resolving CMOS Imager, Versatile and Large
  – Wafer-scale CMOS imager sensor for low-energy X-ray detection
  – Low noise (<15 e- RMS), HDR (>10Me- full well), large pixel (25 µm)
  – Final goal of stitched, wafer-scale sensor
  – Multiple (7) ADCs per column
  – High-speed serialiser (500Mbit/sec)
- Brings together all the pieces: deep implant, thick high-resistivity epi, stitching, high speed...





CHESS2 Architecture Demo Chip Block Diagram