Developments in CMOS for strip detectors

H. Grabas for the CHESS collaboration

Glasgow – JSI – Oxford – RAL – Ljubljana University
HV-CMOS for strips

- HV

External amplifier

Drift

Full depletion

STRIP Baseline

- HV

In strip amplifier

Deep nwell

STRIP HVCMOS

VERTEX

2
Demonstrator: CHESS-1

• Multiple active and passive HVCMOS pixel matrices
  o Allows to measure capacitance/resistance
  o Response signal, even for low signals (i.e. real particles)

• Large array to allow for charge deposition measurement (depletion depth, 2x2[mm] in size)

• Small passive array to support edge-TCT (Laser)

• Component array to study radiation defects in transistors/caps/diodes
CHESS1 results

• Leakage at 100V is:
  o 0.15nA/strip before IR
  o 6.4nA /strip after IR (100MRad gamma)

• 45 x 800µm pixels capacitance:
  o 400fF at 100V

• Amplifier noise:
  o ~80 to 100 e- of noise
CHESS1 charge collection

Sr-90 electrons, mean charge, 25 ns shaping

- Large drop of collected charge after 5e15 n/cm²
  - Initial acceptor removal finished
  - Depleted region narrows because of radiation induced defects

Evolution of $N_{\text{eff}}$ with fluence:

$$N_{\text{eff}} = N_{\text{eff0}} - N_c \cdot \left(1 - \exp(-c \cdot \Phi_{eq})\right) + g \cdot \Phi_{eq}$$

- Acceptor removal
- Radiation introduced deep acceptors (stable damage): $g \sim 0.02 \text{ cm}^{-1}$
Towards CHESS2

• CHESS-2 will be the second demonstrator for both HR & HV-CMOS for strip sensor R&D.
• CHESS1 and HV_Strip1 have proven that HV_CMOS can be used for Strip detector.
• CHESS-2 is meant to demonstrate that HR & HV_CMOS can cope with the physics at HL-LHC.
• CHESS-2 will integrate full length strips + readout.
• Design done in collaboration with UCSC, SLAC and Ivan Peric.
• Slides are for HV-CMOS but a CHESS-2 equivalent will be submitted as well in the HR-CMOS process by Renato, following the same specifications.
Strip detector hit occupancy

Consistent with simulation by Nick Edwards:

<table>
<thead>
<tr>
<th>Layer</th>
<th>68% Clusters</th>
<th>95% Clusters</th>
<th>99% Clusters</th>
<th>68% Hits</th>
<th>95% Hits</th>
<th>99% Hits</th>
</tr>
</thead>
<tbody>
<tr>
<td>Layer 0</td>
<td>1</td>
<td>2</td>
<td>4</td>
<td>3</td>
<td>8</td>
<td>17</td>
</tr>
<tr>
<td>Layer 1</td>
<td>1</td>
<td>2</td>
<td>4</td>
<td>3</td>
<td>8</td>
<td>17</td>
</tr>
<tr>
<td>Layer 2</td>
<td>1</td>
<td>2</td>
<td>4</td>
<td>3</td>
<td>8</td>
<td>16</td>
</tr>
<tr>
<td>Layer 3</td>
<td>1</td>
<td>2</td>
<td>4</td>
<td>3</td>
<td>8</td>
<td>16</td>
</tr>
<tr>
<td>Layer 4</td>
<td>1</td>
<td>2</td>
<td>4</td>
<td>3</td>
<td>9</td>
<td>19</td>
</tr>
</tbody>
</table>

Table 1: Number of hits/clusters corresponding to the 95% and 99% quantiles of the distribution of hits/clusters per SCT chip in $t\bar{t}$ events with $\mu = 140$. Chips with zero hits/clusters are not included in the calculation.
## Strip detector hit encoding

- 1% average occupancy of the detector is not an issue.
- **No de-randomizer in the sensor.**
- Need to be able to cope with bursts of ~20 hits in the detector.
- Contrary to the Baseline Sensor, we cannot retain all the hits in the CHESS detector.
- Need to encode strips hits.
- Need to minimize number of wirebonds.
- Can send 8 words at 320MHz per 25ns bunch crossing (no buffering in chip).

<table>
<thead>
<tr>
<th>Nb of strips in group</th>
<th>Wirebonds needed</th>
<th>Wirebonds per strip</th>
<th>Max. number of hits @320MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>512</td>
<td>$5 + 1 + 9 = 15$</td>
<td>0.03</td>
<td>8</td>
</tr>
<tr>
<td>256</td>
<td>$(5 + 1 + 8) \times 2 = 24$</td>
<td>0.045</td>
<td>16</td>
</tr>
<tr>
<td>128</td>
<td>$(5 + 1 + 7) \times 4 = 52$</td>
<td>0.1</td>
<td>32</td>
</tr>
<tr>
<td>64</td>
<td>$(5 + 1 + 6) \times 8 = 96$</td>
<td>0.18</td>
<td>64</td>
</tr>
</tbody>
</table>

- We are going to 128 strips group retaining 8 hit for each group.
Single strip hit selection

- Simulation by Marco Battaglia shows that double hit in $\zeta$ direction is highly suppressed.
  - $\sim 2 \times 10^{-3}$ probability
- Will be investigated in the high pile-up environment (should be ok given the low occupancy).
## Baseline to HV-CMOS

<table>
<thead>
<tr>
<th></th>
<th>Baseline</th>
<th>HV-CMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Number of strip</strong></td>
<td>256 (for comparable area)</td>
<td>512</td>
</tr>
<tr>
<td><strong>Strip pitch</strong></td>
<td>75 µm</td>
<td>40 µm</td>
</tr>
<tr>
<td><strong>Strip segmentation</strong></td>
<td>None</td>
<td>32</td>
</tr>
<tr>
<td><strong>Segment length</strong></td>
<td></td>
<td>800 µm</td>
</tr>
<tr>
<td><strong>Number of sensor</strong></td>
<td>2 (stereo)</td>
<td>1 (can be thinned)</td>
</tr>
<tr>
<td><strong>Output signal</strong></td>
<td>Analog</td>
<td>Encoded Digital</td>
</tr>
<tr>
<td><strong>Max. nb. of hits</strong></td>
<td>256/ b. crossing</td>
<td>32/ b. crossing</td>
</tr>
<tr>
<td><strong>Nb. of wirebonds</strong></td>
<td>1/strip</td>
<td>0.1/strip</td>
</tr>
</tbody>
</table>
Sensor dimension

• Ideally we would like a 20mm x 25mm sensor (to be compatible with the baseline Strip sensor).

• Can’t do a monolithic 20mm x 25mm due to reticle size
• 1mm of periphery
CHESS-2 main architecture

• Design done between UCSC, SLAC & with Ivan Periç.
• Engineering run 20, 80, 200 Ohm bulk resistivity
• Pixels without discriminator have smaller detector capacitance. But there might be analog cross-talk going to the edge.
• 50 & 30% diode fraction
Pixel amplifier

- Most probable value for MIP is ~1500e at 120V for a 20 Ohm substrate.
- Landau distribution significant values start ~700e (20Ohms).
- For a 32 segment strip, we require threshold to noise of 5 to 1.
- Requires below 25ns peaking time (LHC bunch rate).
- Note: Signal to noise is improved for higher resistivity substrate.
Details of the pixels

- Active amplifier and threshold trimming in each pixel.
- Discriminator front and trimming in pixel
- Full discriminator in pixel or periphery.
- Latches and encoding logic at the periphery.

Capabilities:
- Hot pixels masking.
- Injection of calibration signal.
- 4bit threshold trimming.
Pixel schematic from I. Peric and E. Vilella

Sensor bias

Diode

Coupling

Regulated Low-pass Cascode $\Delta V \sim 85 \text{ mV}$

Amplifier

Feedback

AmpOut

SFOut (connected to FB) r.t. $\sim 23 \text{ ns}$
**Amplifier simulation**

- New amplifier design by Eva Vilella and Ivan Peric
- Fast: \(~10\text{ns risetime}\)
- SNR = 10 for 700e
- Power 30\(\mu\text{W/pixel, 0.5W per sensor.}\)
Comparator output [1]

• The sensor is 2.5cm long
• The lines are very coupled and very capacitive:
  - 32 lines 0.6\(\mu\)m spacing
  - 2.5cm long
  - Up to 1pF capacitance to other metals (gnd).

• Full in pixel comparator with digital output:
  - Digital output – no worries about crosstalk
  - Bigger layout – added detector capacitance
Comparator output [2]

• The lines are very coupled and very capacitive:
  o 32 lines 0.6µm spacing
  o 2.5cm long
  o 1pF capacitance to other metal (gnd) maximum.

• Partial in pixel comparator (less added capacitance):
  o Current output – less cross-talk expected
  o Higher mismatch on the comparator.
Strip Hit Encoding

• Single hit in the strip
  - Encoded position of the first hit

• Double or multiple hits in the strip
  - Encoded position of the first hit + Flag

• The first hit in the strip is encoded on **5bits**
• Additional hit **Flag** is raised in case of multiple hits.
• **Flag** provides loose information on the position of the additional hits.
• During strip encoding an internal bit is also raised when the strip is hit.
Hit encoding

Group of 8 strips

Sum of hit = 010

More than 8 hits
Hit encoding

Group of 8 strips

Sum of hit = 010 + 010

Sum across 16 groups of 8 strips

More than 8 hits

1
1
1
1

1
1
1
1

1
1
1
1

Sum = 010

More than 8 hits
Hit encoding

Group of 8 strips

Sum of hit = 010 + 010

Sum across 16 groups of 8 strips

hit carry

hit

store = 010

overflow

More than 8 hits

VERTEX
Hit encoding

Group of 8 strips

Sum of hit = 010 + 010

More than 8 hits

Sum across 16 groups of 8 strips
Output data format

32 segments = 5bits + 7 bits

127 strip = 7bits

127 strips

5 +1 bits
Strip & Flag

7 bits
127 group

Output Pads

2x 13 pads + 2 synch
SACI – SLAC ASIC Control Interface

Serial Interface with handshake protocol
5 Signals
- 3 shared: saciClk, saciCmd, saciRsp.
- 1 dedicated select line per slave: saciSelL.
- 1 Reset Line (RstL) can be shared with the ASIC Global Reset.

- Operated between 0V and 3.3V
- Allows multiple SACI on same bus (parallel mode).

Layout

VERTEX
SLAC ASIC Control Interface (SACI)

SACI cmd (serial signal):

- SET (1bit)
- RW (1bit)
- CMD (7bit)
- ADDR (12bit)
- DATA (32bit)

ASIC internal Signals

Write/Read DATA bus

SACI clk, SACI cmd, SACI resp, SACI sel, rst

Signals from PADS

VERTEX
SACI - Signals

SACIclk
SACIselL
SACIcmd
SACIrsp
SACIrstL

SACIcmd (serial signal):
- SET (1bit)
- RW (1bit)
- CMD (7bit)
- ADDR (12bit)
- DATA (32bit)

SACIrsp (serial signal):
- SET (1bit)
- RW (1bit)
- CMD (7bit)
- ADDR (12bit)

Write Mode
Read Mode
The ASIC decoded the command last 4 bits. Any given command longer than 4 bits will be interpreted as a 4 bit command.
Encoding Read-Out scheme – Overview

Strip Encoding Output

4 groups of 13 rows
8 bits shift-registers

8 bits

25ns Multiplexing

Digital Multiplexer

3.125ns Period Clock (320MHz)

VERTEX
**LVDS Driver – Simulated Performance**

*Schematic simulated at all condition (wo, wz, ws, wp) at room*

<table>
<thead>
<tr>
<th>Specs</th>
<th>Typical</th>
<th>Min</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>Differential Output Voltage (( @ R_{LOAD} =100\Omega ))</td>
<td>600mV</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Common Mode</td>
<td>1.2V</td>
<td>0.5</td>
<td>2.8</td>
</tr>
<tr>
<td>Current</td>
<td>3mA</td>
<td>0.2mA</td>
<td>3.5mA*</td>
</tr>
<tr>
<td>Speed</td>
<td>320MHz</td>
<td></td>
<td>500MHz</td>
</tr>
<tr>
<td>Supply</td>
<td>3.3V</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

*Can meet standard LVDS requirements.*
## CHESS-2 specification

<table>
<thead>
<tr>
<th>Specification</th>
<th>Details</th>
</tr>
</thead>
<tbody>
<tr>
<td>Size of the chip</td>
<td>0.6cm x 2.5cm</td>
</tr>
<tr>
<td>Pixel size</td>
<td>40µm x ~800µm</td>
</tr>
<tr>
<td>Number of strips</td>
<td>127</td>
</tr>
<tr>
<td>Number of pixels per strip</td>
<td>32</td>
</tr>
<tr>
<td>Readout speed</td>
<td>320MHz</td>
</tr>
<tr>
<td>Output buffers</td>
<td>LVDS with tunable signal amplitude</td>
</tr>
<tr>
<td>Maximum number of hit per strip</td>
<td>1 + overflow flag</td>
</tr>
<tr>
<td>Maximum number of hits in strip array</td>
<td>8</td>
</tr>
<tr>
<td>Size of data output</td>
<td>13 bits</td>
</tr>
<tr>
<td>Format of data output</td>
<td>5 + 1+ 7 bits</td>
</tr>
<tr>
<td>Latency</td>
<td>Fixed latency</td>
</tr>
</tbody>
</table>
Summary

• A huge amount of knowledge has been accumulated from CHESS-1 & HV_Strip1
• Physics simulation seems to indicate that 128 strip grouping retaining 8 hits should meet occupancy requirements.
• More simulation would still need to be done including pile-up and harsh conditions in layer 1 and endcaps.
• Design in progress for submission end of June.
• HV & HR are collaborating for this new submission following the specs (https://twiki.cern.ch/twiki/bin/viewauth/Atlas/CHESSStripTestChip).
• Engineering run scheduled with res. from 20 to 200ohms.