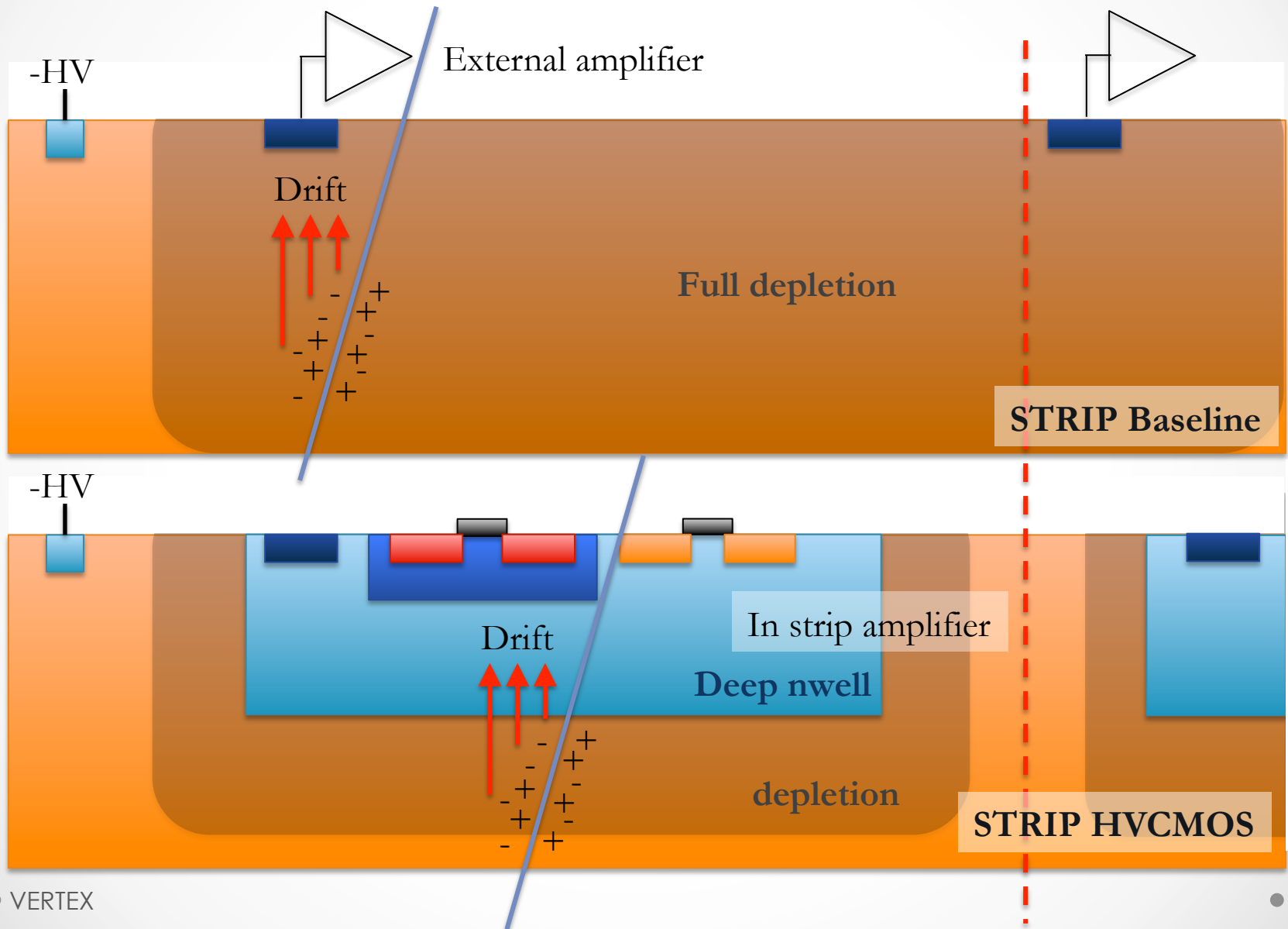# Developments in CMOS for strip detectors

H. Grabas for the CHESS collaboration

UCSC – SLAC – KIT - ANL – Cambridge Geneva – Glasgow – JSI – Oxford – RAL – Ljubljana University

HV-CMOS for strips

External amplifier

-HV

Drift

Full depletion

STRIP Baseline

-HV

Drift

In strip amplifier
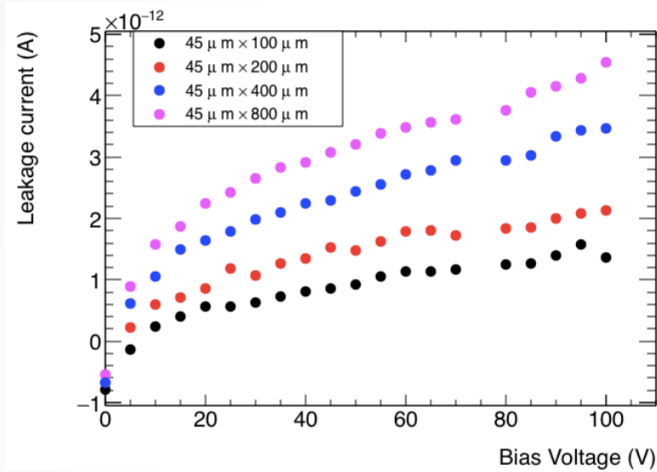
Deep nwell

depletion

STRIP HVCMOS

Demonstrator: CHESS-1

- Multiple active and passive HVCMOS pixel matrices

  o Allows to measure capacitance/ resistance

  o Response signal, even for low signals (i.e. real particles)

- Large array to allow for charge deposition measurement (depletion depth, 2x2[mm] in size)

- Small passive array to support edge-TCT (Laser)

- Component array to study radiation defects in transistors/caps/diodes
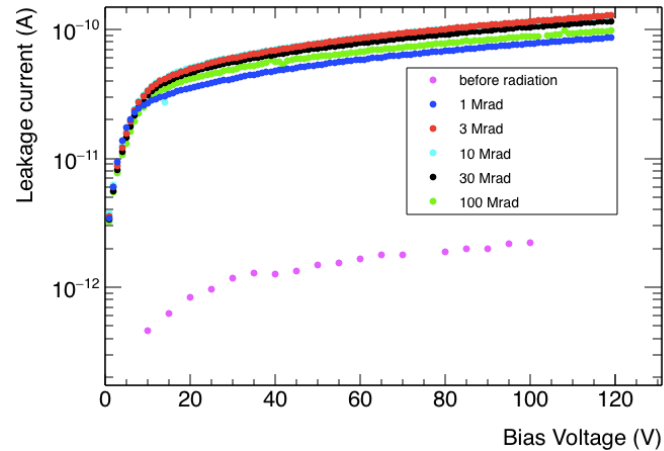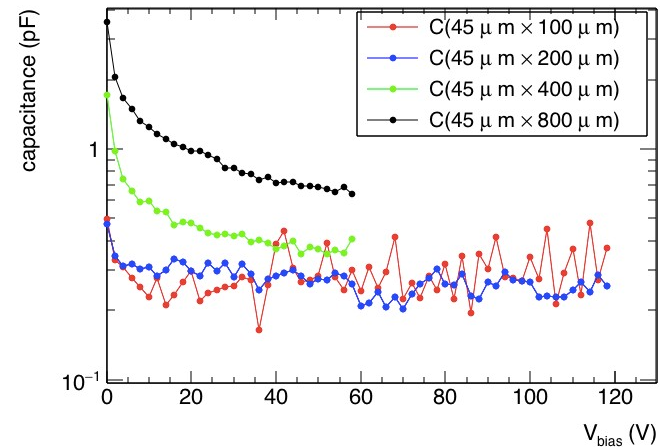

1000.00μm
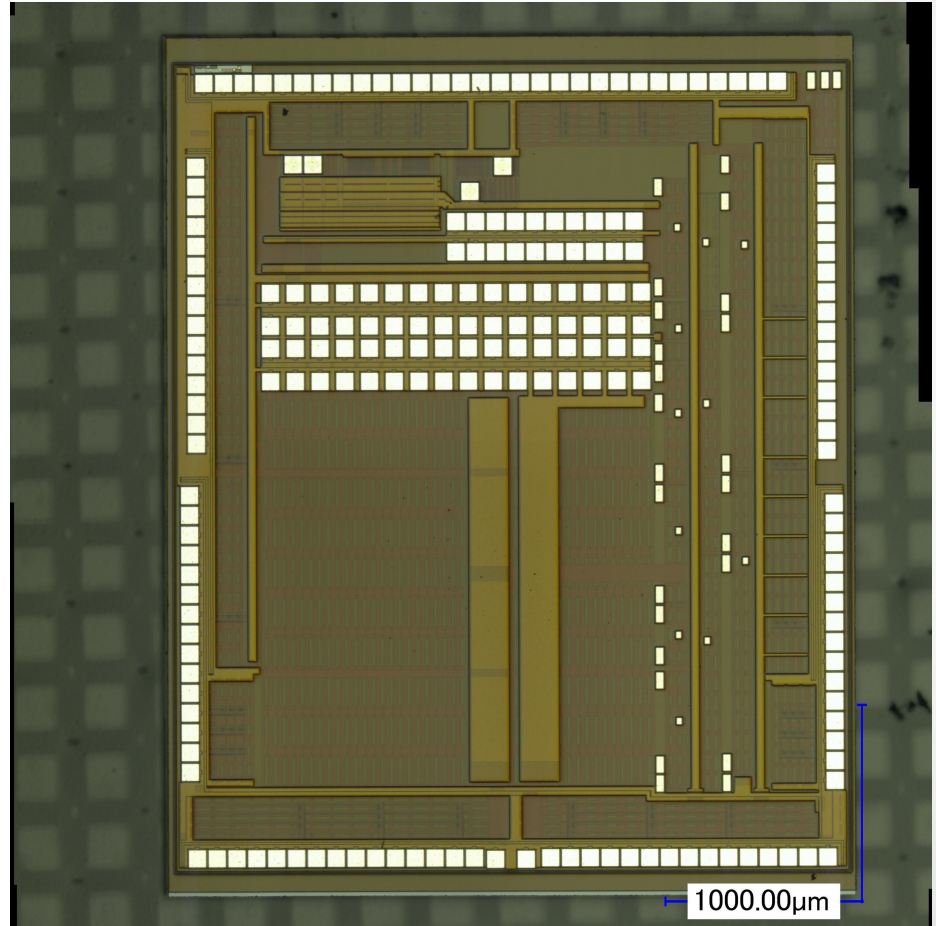
CHESS1 results

- Leakage at 100V is:
  - 0.15nA/strip before IR 6.4nA /strip after IR (100MRad gamma)
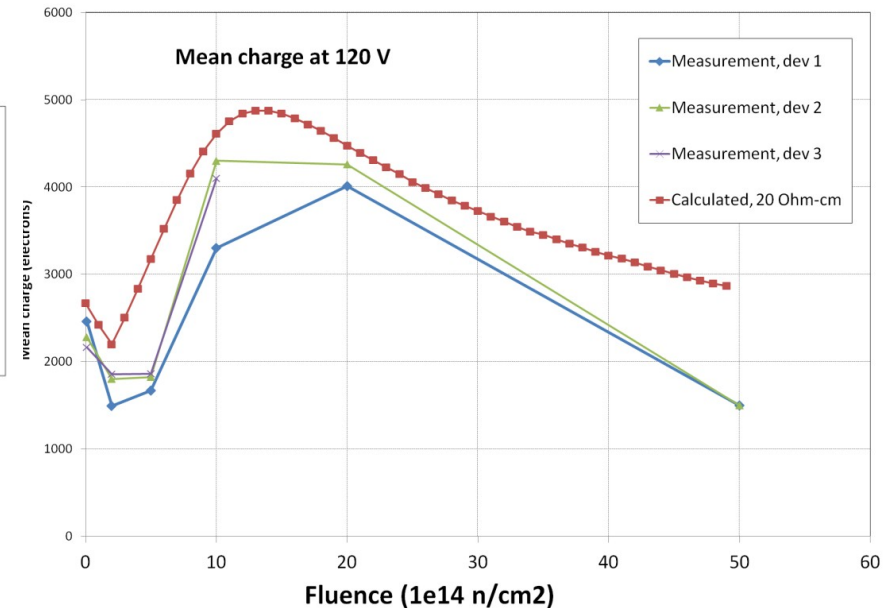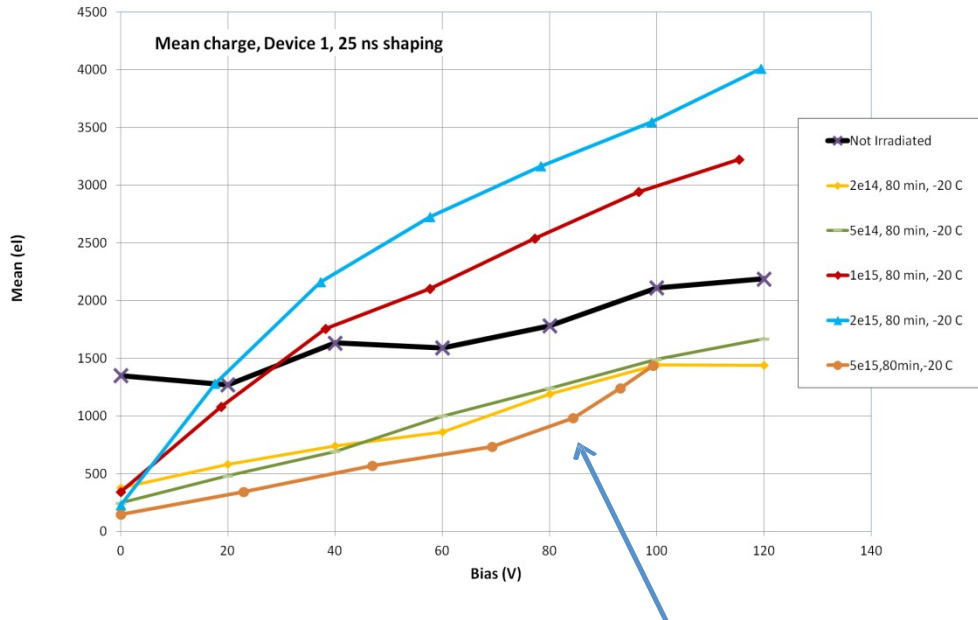

- 45 x 800μm pixels capacitance:
  - 400fF at 100V

- Amplifier noise:
  - ~80 to 100 e- of noise

CHESS1 charge collection

Sr-90 electrons, mean charge, 25 ns shaping

Mean charge, Device 1, 25 ns shaping

Legend:
- Not Irradiated
- 2e14, 80 min, -20 C
- 5e14, 80 min, -20 C
- 1e15, 80 min, -20 C
- 2e15, 80 min, -20 C
- 5e15,80min,-20 C

Mean charge at 120 V

Legend:
- Measurement, dev 1
- Measurement, dev 2
- Measurement, dev 3
- Calculated, 20 Ohm-cm

❑ Large drop of collected charge after 5e15 n/cm²
- ▪ Initial acceptor removal finished
- ▪ Depleted region narrows because of radiation induced defects

Evolution of N_{eff} with fluence:

$$N_{eff} = N_{eff\,0} - N_c \cdot (1 - \exp(-c \cdot \Phi_{eq})) + g \cdot \Phi_{eq}$$

acceptor removal

Radiation introduced deep acceptors (stable damage): $g \sim 0.02$ cm^{-1}

Initial concentration

Towards CHESS2

- CHESS-2 will the second demonstrators for both HR & HV-CMOS for strip sensor R&D.

- CHESS1 and HV_Strip1 have proven that HV_CMOS can be used for Strip detector

- CHESS-2 is meant to demonstrate that HR & HV_CMOS can cope with the physics at HL-LHC.

- CHESS-2 will integrate full length strips + readout.

- Design done in collaboration with UCSC, SLAC and Ivan Peric.

- Slides are for HV-CMOS but a CHESS-2 equivalent will be submitted as well in the HR-CMOS process by Renato, following the same specifications.
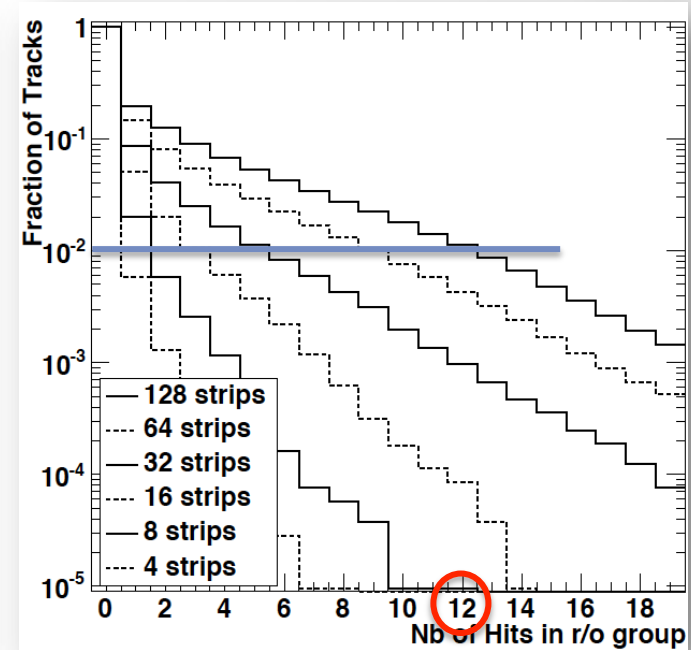
Strip detector hit occupancy

Sim. Marco Battaglia
[high pT H → bb jets]
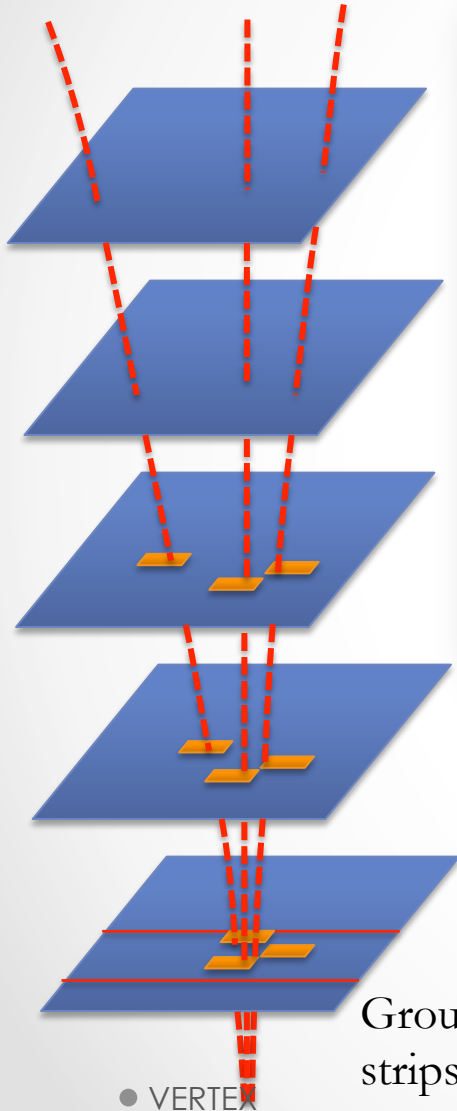
First strip layer
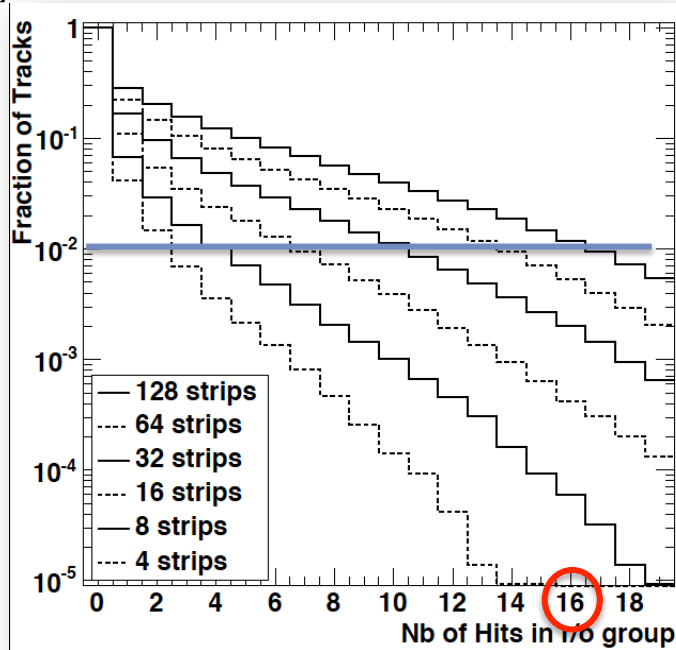
Fifth strip layer

Consistent with simulation by Nick Edwards:

Groups of strips

● VERTEX

Layer	68% Clusters	95% Clusters	99% Clusters	68% Hits	95% Hits	99% Hits
Layer 0	1	2	4	3	8	17
Layer 1	1	2	4	3	8	17
Layer 2	1	2	4	3	8	16
Layer 3	1	2	4	3	8	16
Layer 4	1	2	4	3	9	19

Table 1: Number of hits/clusters corresponding to the 95% and 99% quantiles of the distribution of hits/clusters per SCT chip in $t\bar{t}$ events with $\mu = 140$. Chips with zero hits/clusters are not included in the calculation.

Strip detector hit encoding

- 1% average occupancy of the detector is not an issue.
- **No de-randomizer in the sensor.**
- Need to be able to cope with bursts of ~20 hits in the detector.
- Contrary to the Baseline Sensor, we cannot retain all the hits in the CHESS detector.
- Need to encode strips hits.
- Need to minimize number of wirebonds.
- Can send 8 words at 320MHz per 25ns bunch crossing (no buffering in chip).

Nb of strips in group	Wirebonds needed	Wirebonds per strip	Max. number of hits @320MHz
512	5 + 1 + 9 = 15	0.03	8
256	(5 + 1 + 8) x 2 = 24	0.045	16
128	(5 + 1 + 7) x 4 = 52	0.1	32
64	(5 + 1 + 6) x 8 = 96	0.18	64

- We are going to 128 strips group retaining 8 hit for each group.

Single strip hit selection

- Simulation by Marco Battaglia shows that double hit in z direction his highly suppressed.
  - ○ ~2.10^{-3} probability
- Will be investigated in the high pile-up environment (should be ok given the low occupancy).
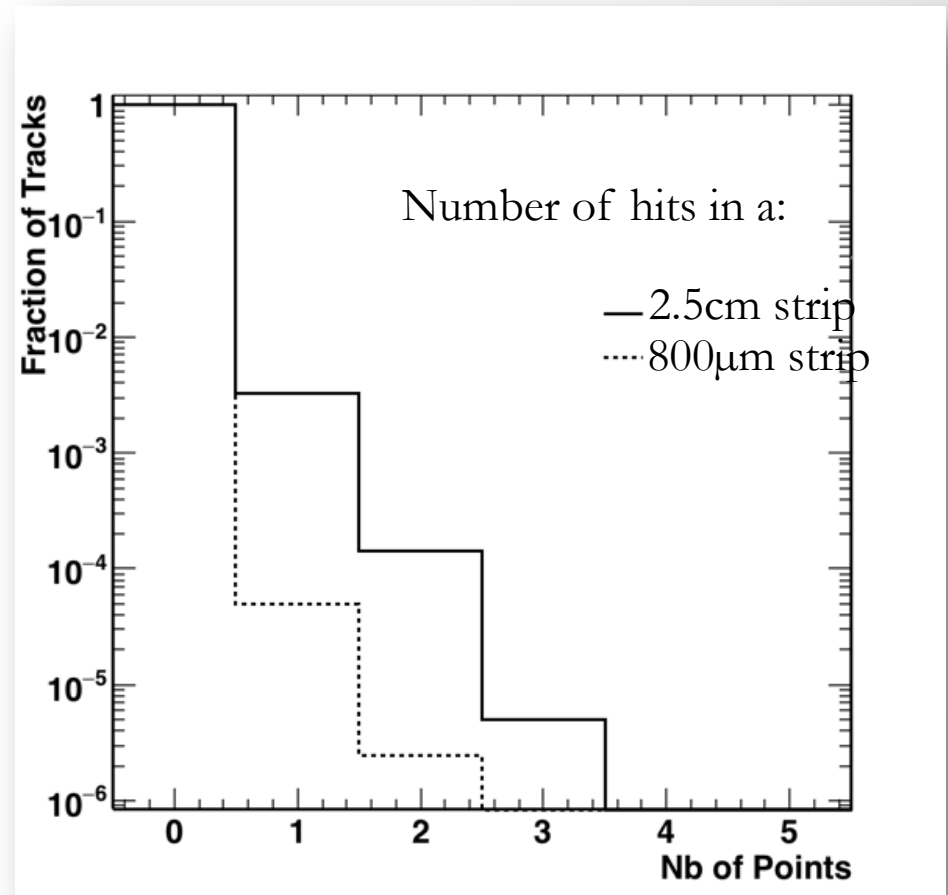
Baseline to HV-CMOS

Baseline	
Number of strip	256 (for comparable area)
Strip pitch	75μm
Strip segmentation	None
Number of sensor	2 (stereo)
Output signal	Analog
Max. nb. of hits	256/ b. crossing
Nb. of wirebonds	1/strip

| HV-CMOS	
Number of strips	512
Strip pitch	40μm
Strip segmentation	32
Segment length	800μm
Number of sensor	**1 (can be thinned)**
Output signal	Encoded Digital
Max. nb. Of hits	32/ b. crossing
Nb. of wirebonds	**0.1/strip**

Sensor dimension

- Ideally we would like a 20mm x 25mm sensor (to be compatible with the baseline Strip sensor).
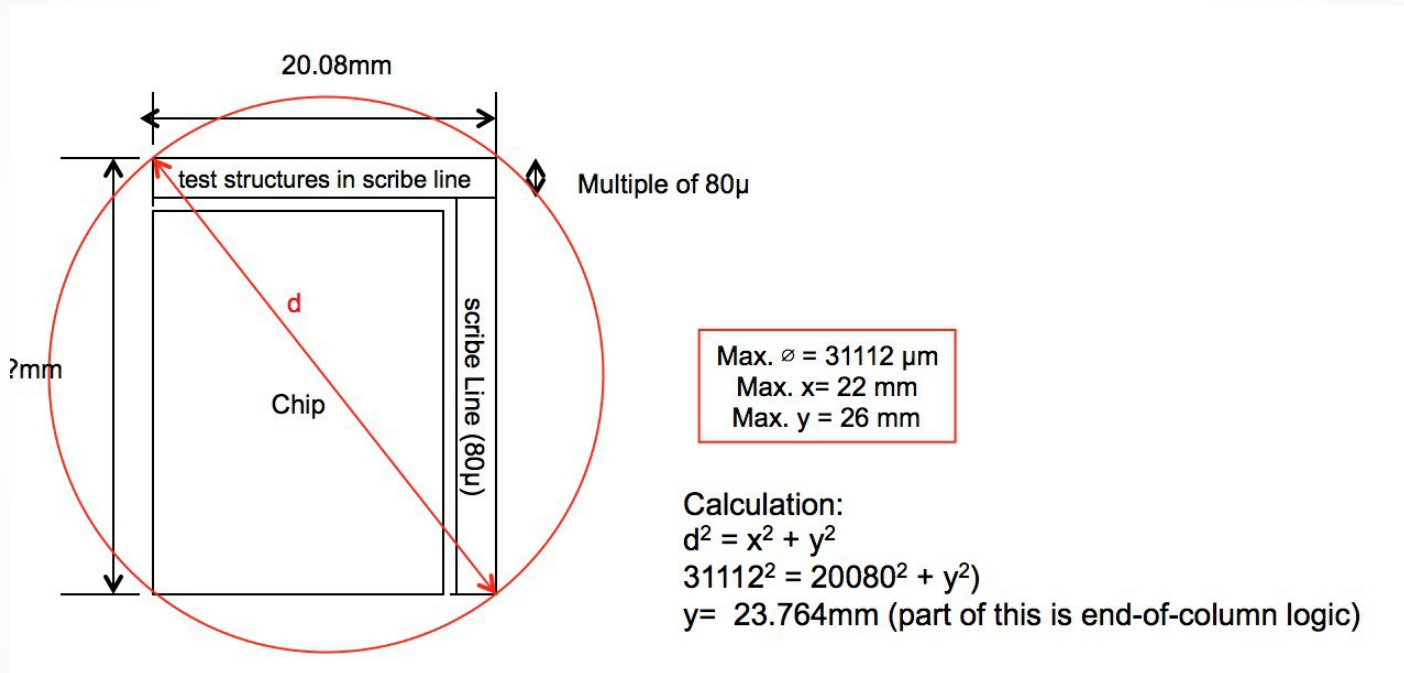
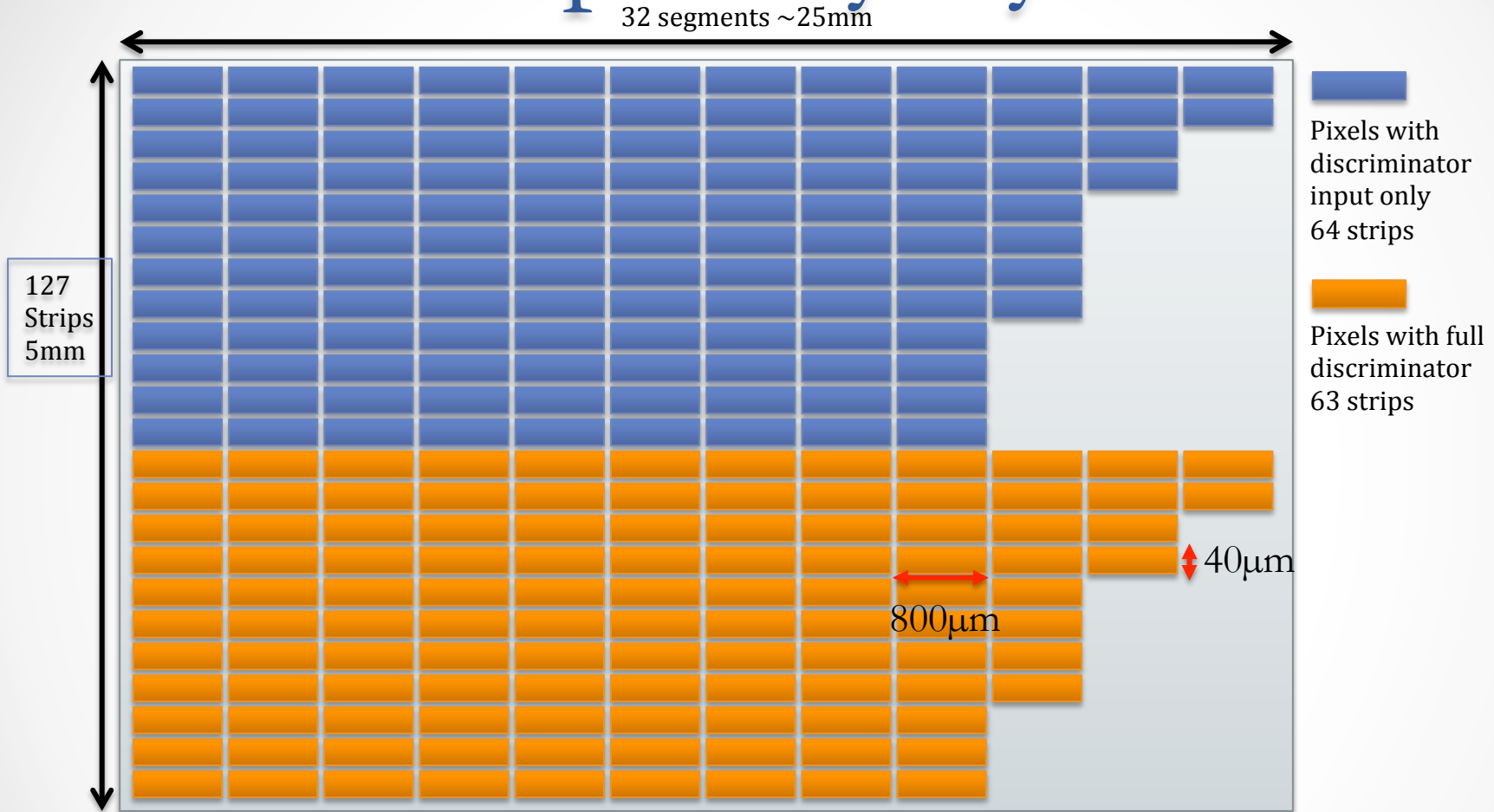- Can't do a monolithic 20mm x 25mm due to reticle size
- 1mm of periphery

CHESS-2 main architecture

Strips ~24mm   Periphery 1mm
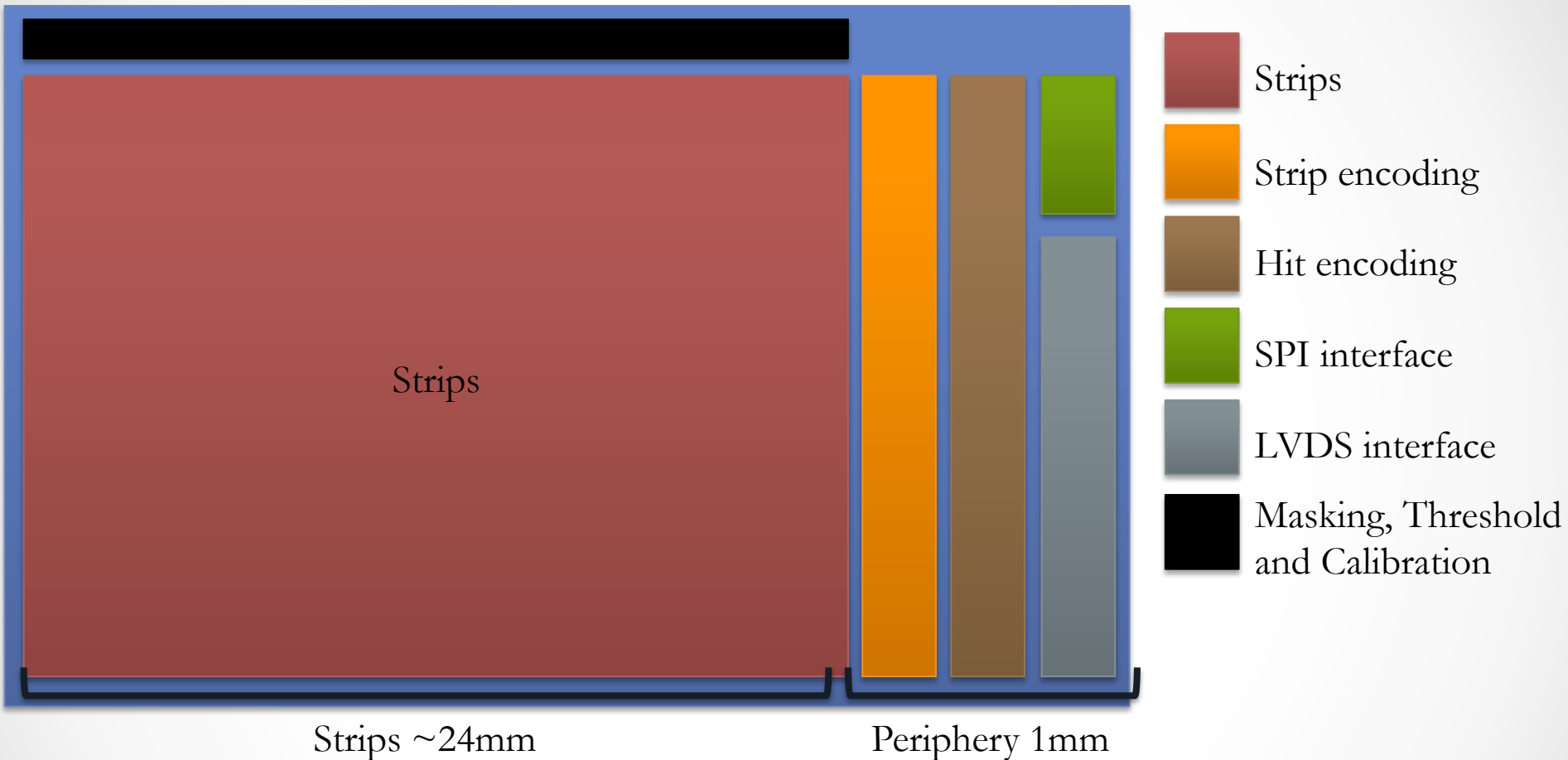
- Design done between UCSC, SLAC & with Ivan Perič.
- Engineering run 20, 80, 200 Ohm bulk resistivity

Strip array layout

32 segments ~25mm

127 Strips 5mm

Pixels with discriminator input only 64 strips

Pixels with full discriminator 63 strips

40μm

800μm

- Pixels without discriminator have smaller detector capacitance. But there might be analog cross-talk going to the edge.
- 50 & 30% diode fraction

Pixel amplifier

- Most probable value for MIP is ~1500e at 120V for a 20 Ohm substrate.

- Landau distribution significant values start ~700e (20Ohms).

- For a 32 segment strip, we require threshold to noise of 5 to 1.

- Requires below 25ns peaking time (LHC bunch rate).

- Note: Signal to noise is improved for higher resistivity substrate.

-HV

3.3V

Drift

Deep nwell

depletion

- - +
- - +
- + + -
- + + -
- + - +
- + -
- - +

p sub
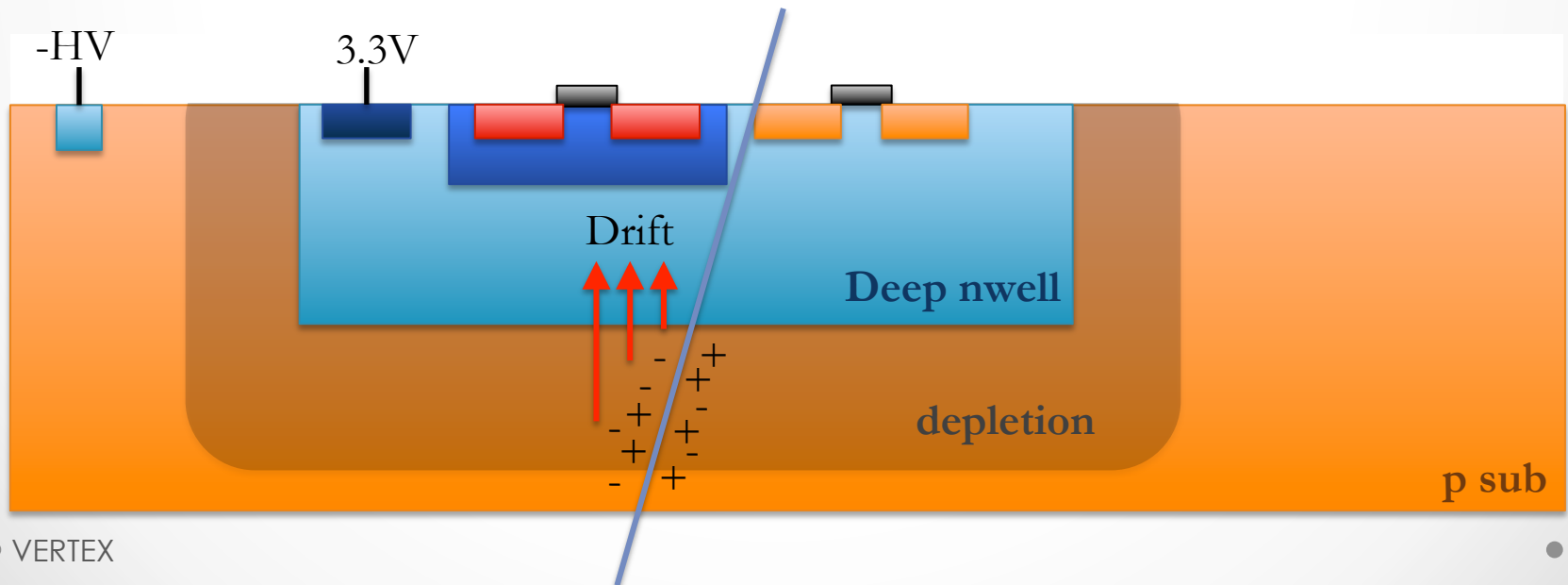
Details of the pixels

- Active amplifier and threshold trimming in each pixel.
- Discriminator front and trimming in pixel
- Full discriminator in pixel or periphery.
- Latches and encoding logic at the periphery.
- Capabilities:
  o Hot pixels masking.
  o Injection of calibration signal.
  o 4bit threshold trimming.

In pixel   Pixel or periphery   Periphery
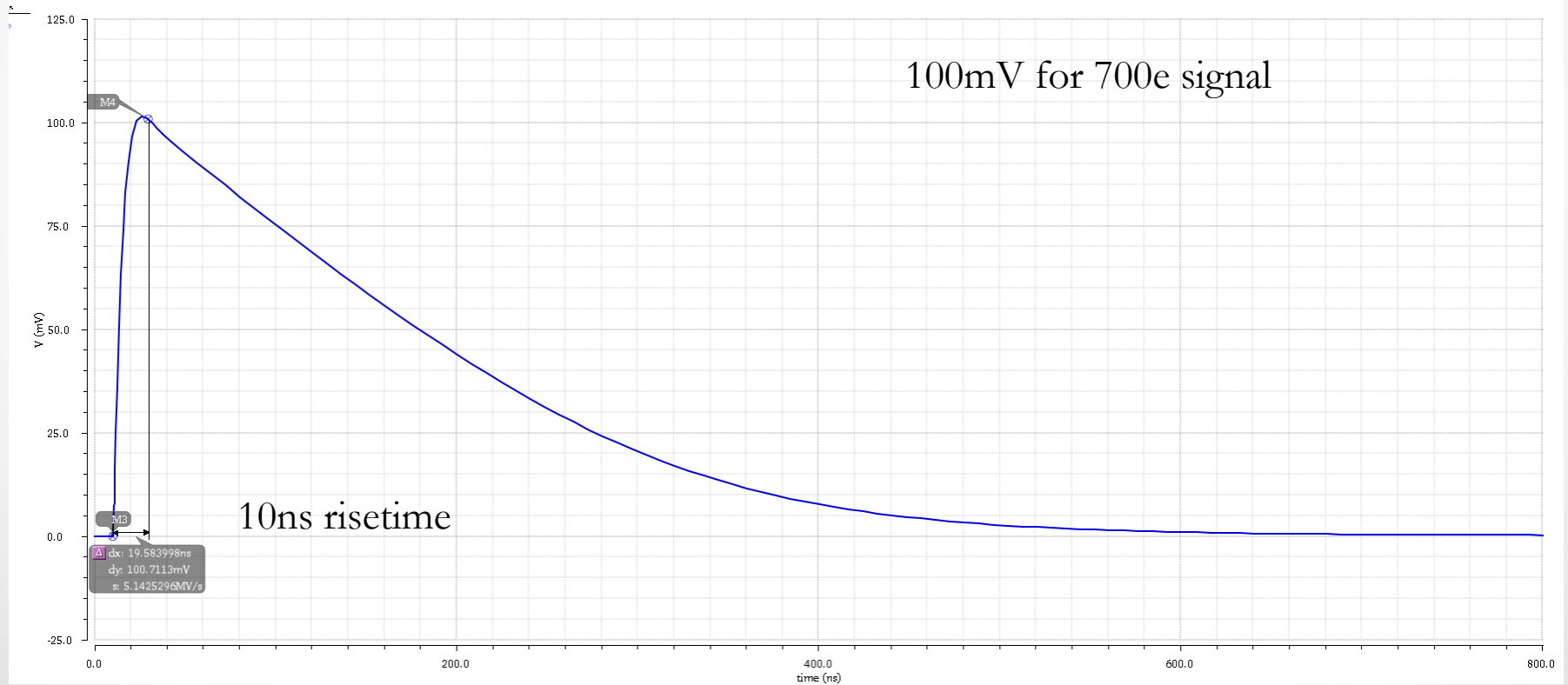
Cal.

Amplifier

Discri.

Latch

25ns Ck

Threshold trimming
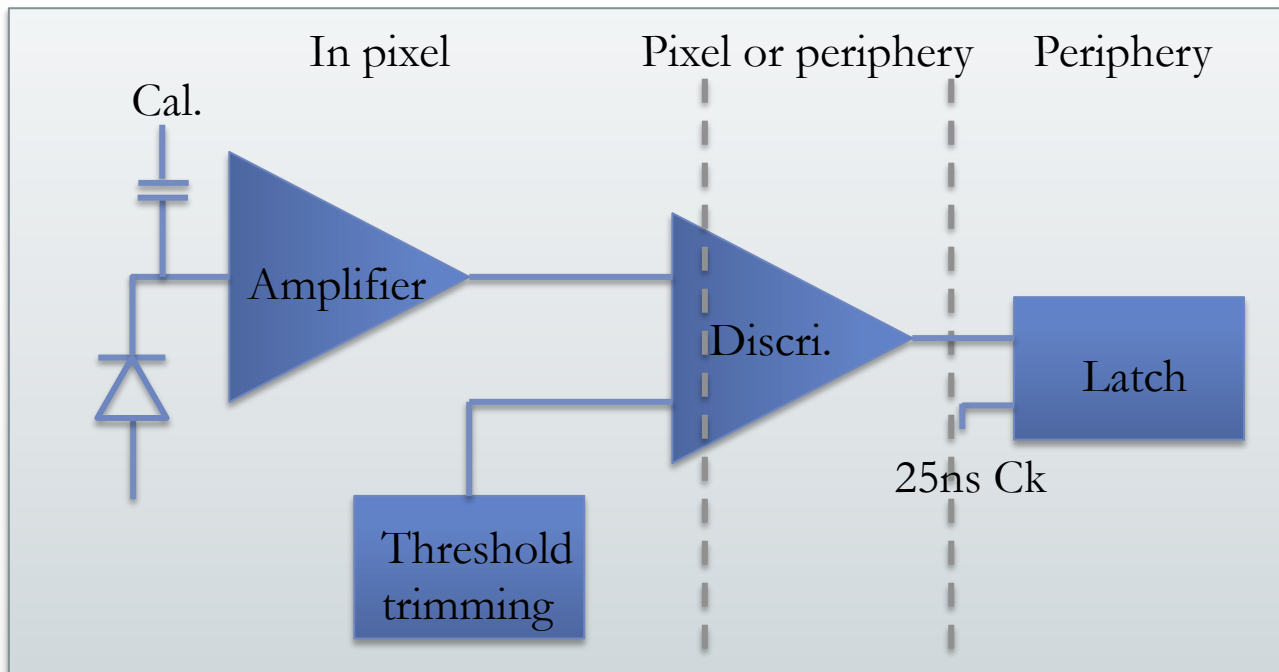
Pixel schematic from I. Peric and E. Vilella
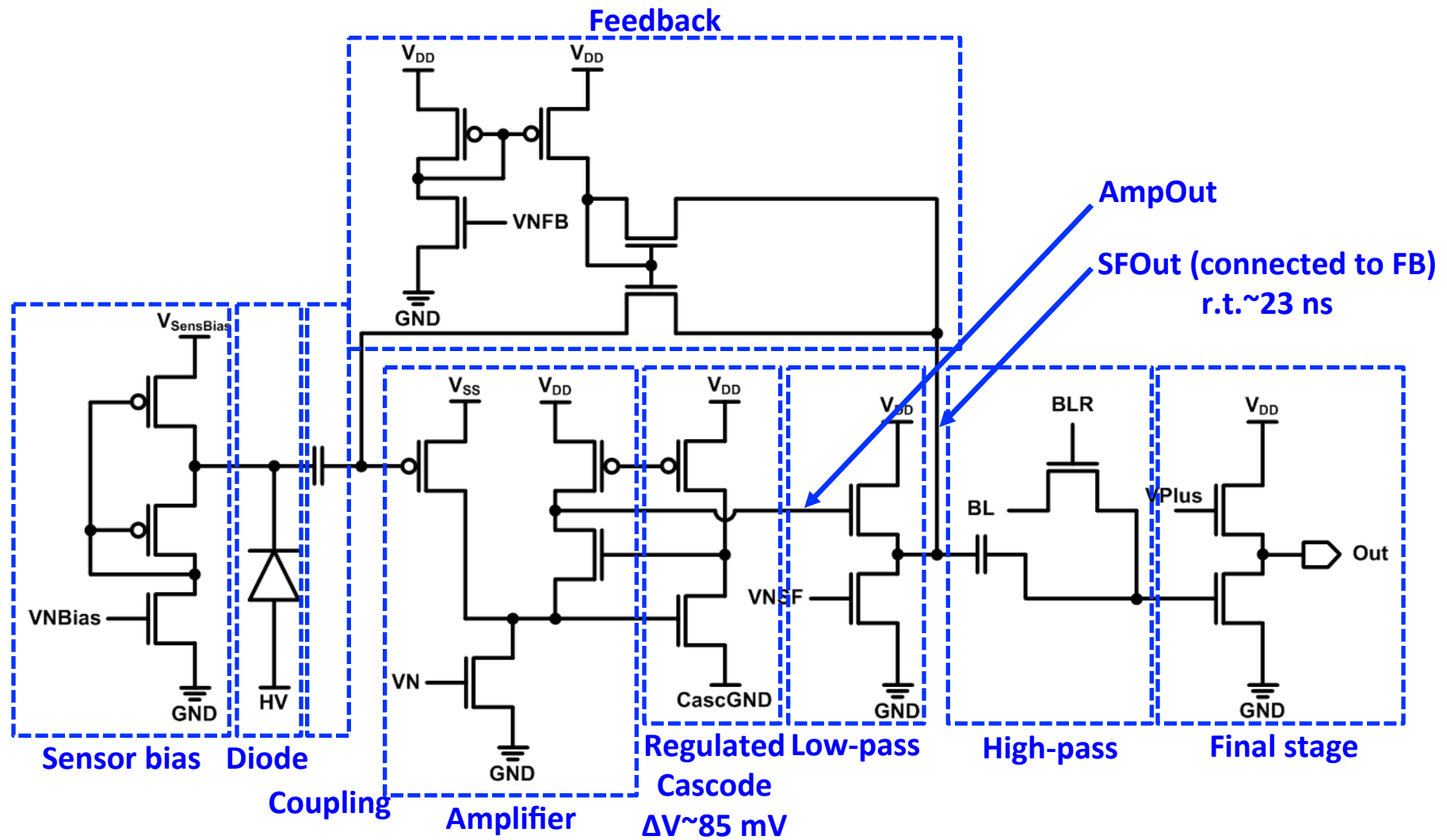
Amplifier simulation

- New amplifier design by Eva Vilella and Ivan Peric
- Fast: ~10ns risetime
- SNR = 10 for 700e
- Power 30µW/pixel, 0.5W per sensor.


100mV for 700e signal

10ns risetime

Comparator output [1]

- The sensor is 2.5cm long

- The lines are very coupled and very capacitive:
  - 32 lines 0.6μm spacing
  - 2.5cm long
  - Up to 1pF capacitance to other metals (gnd).

- Full in pixel comparator with digital output:
  - Digital output – no worries about crosstalk
  - Bigger layout – added detector capacitance
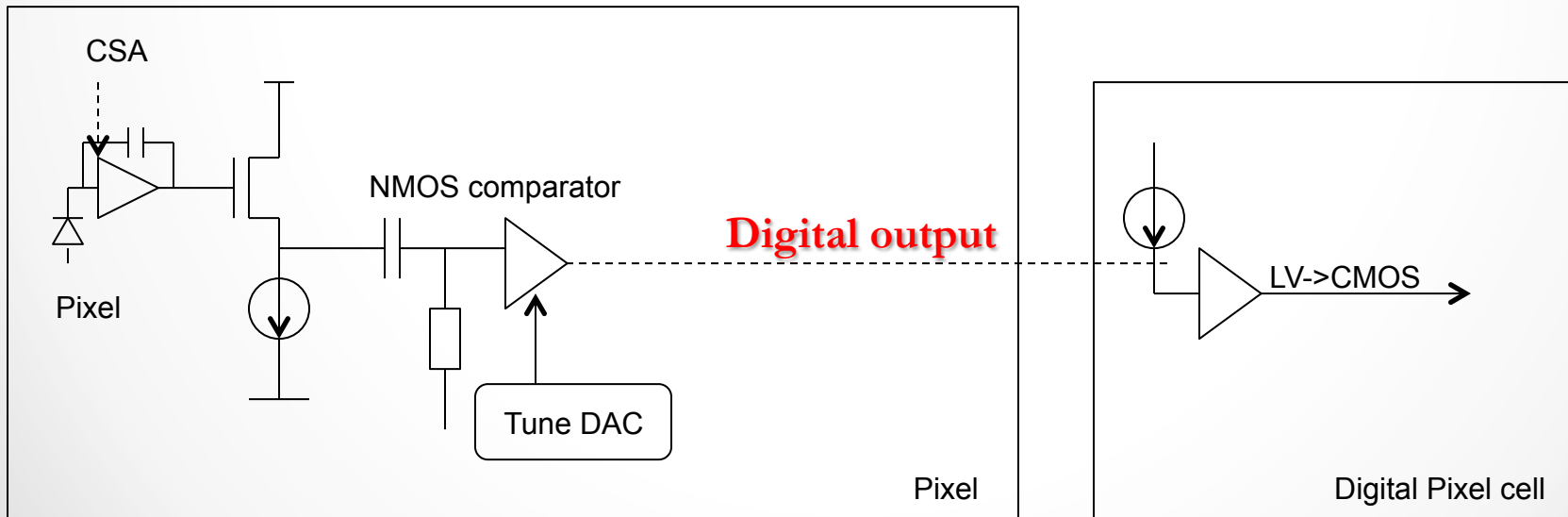
Comparator output [2]

- The lines are very coupled and very capacitive:
  o 32 lines 0.6μm spacing
  o 2.5cm long
  o 1pF capacitance to other metal (gnd) maximum.

- Partial in pixel comparator (less added capacitance):
  o Current output – less cross-talk expected
  o Higher mismatch on the comparator.
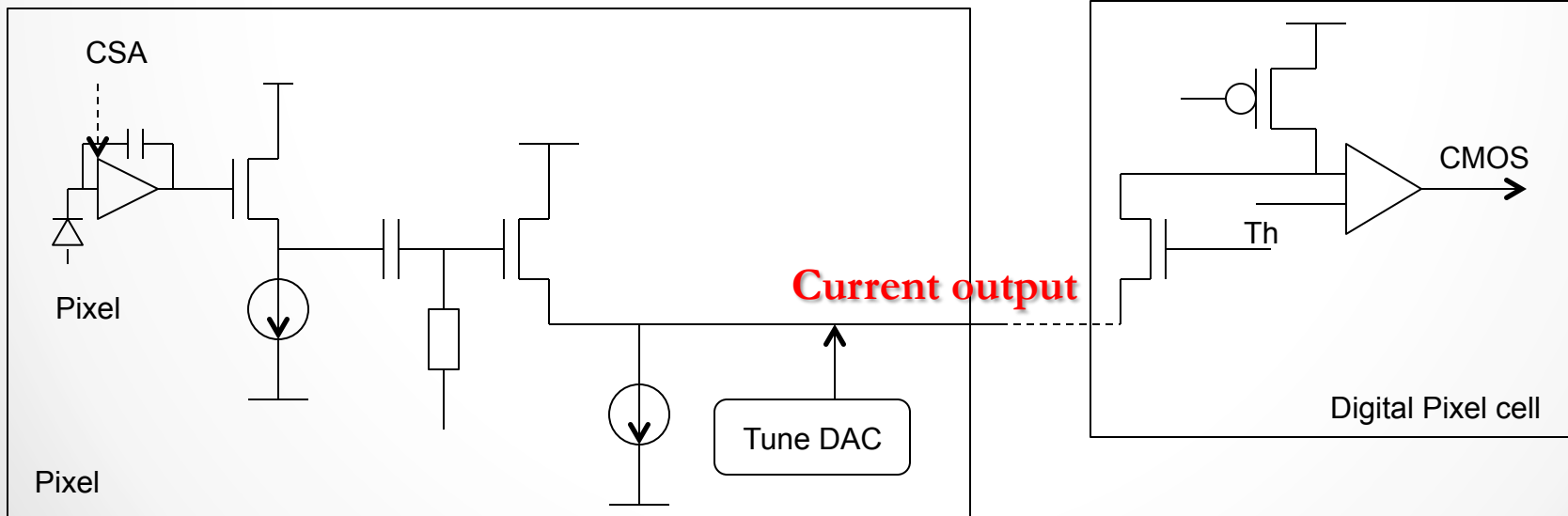
Strip Hit Encoding

- Single hit in the strip

  o Encoded position of the first hit

  0b00111

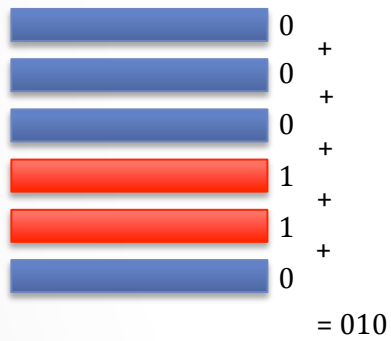- Double or multiple hits in the strip

  o Encoded position of the first hit + Flag

  0b00111 +

- The first hit in the strip is encoded on **5bits**

- Additional hit **Flag** is raised in case of multiple hits.

- **Flag** provides loose information on the position of the additional hits.

- During strip encoding an internal bit is also raised when the strip is hit.

Hit encoding

hit

1	+
0	+
0	+
0	+
1	+
0	

Group of
8 strips

Sum of hit = 010

0	+
0	+
0	+
1	+
1	+
0	

= 010

More than 8 hits

1	
1	+
1	+
1	

Hit encoding

Sum across 16
groups of 8 strips

hit

000

Group of
8 strips

1 +
0 +
0 +
0 +
1 +
0

sum

Sum of hit = 010 +   010

0 +
0 +
0 +
1 +
1 +
0

= 010 +   100

More than 8 hits

⋮

1
1 +
1 +
1

Hit encoding

Sum across 16 groups of 8 strips

Group of 8 strips

hit

hit carry

Sum of hit = 010 +

= 010 +
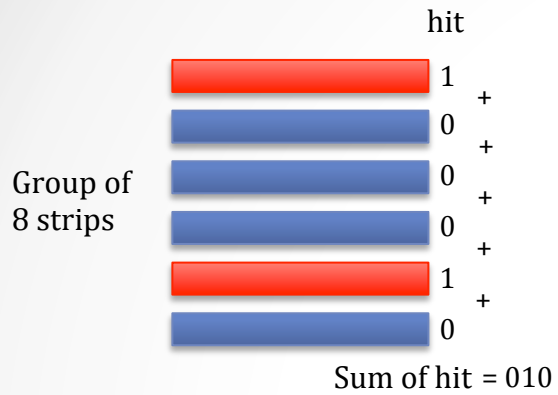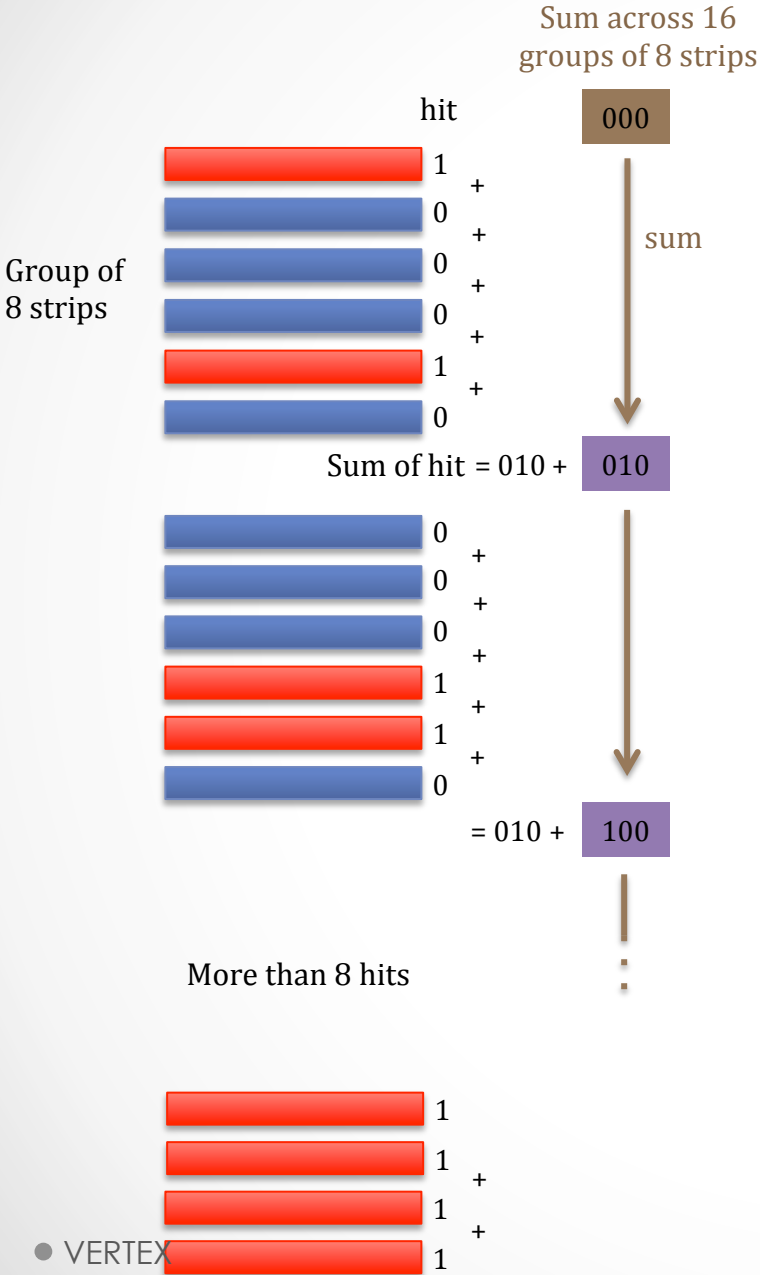
More than 8 hits

overflow

Hit encoding
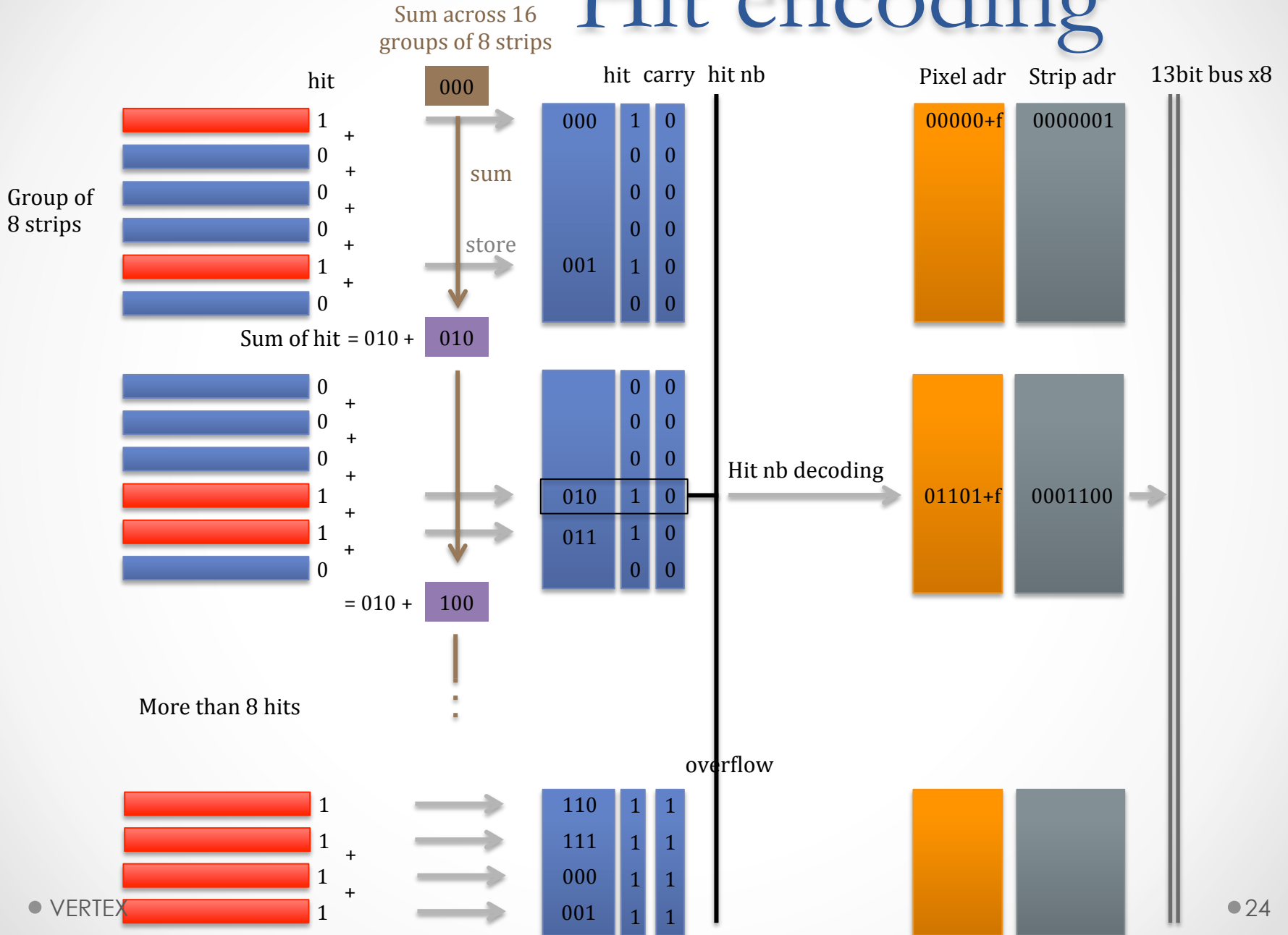
Output data format

127 strip = 7bits

32 segments = 5bits +
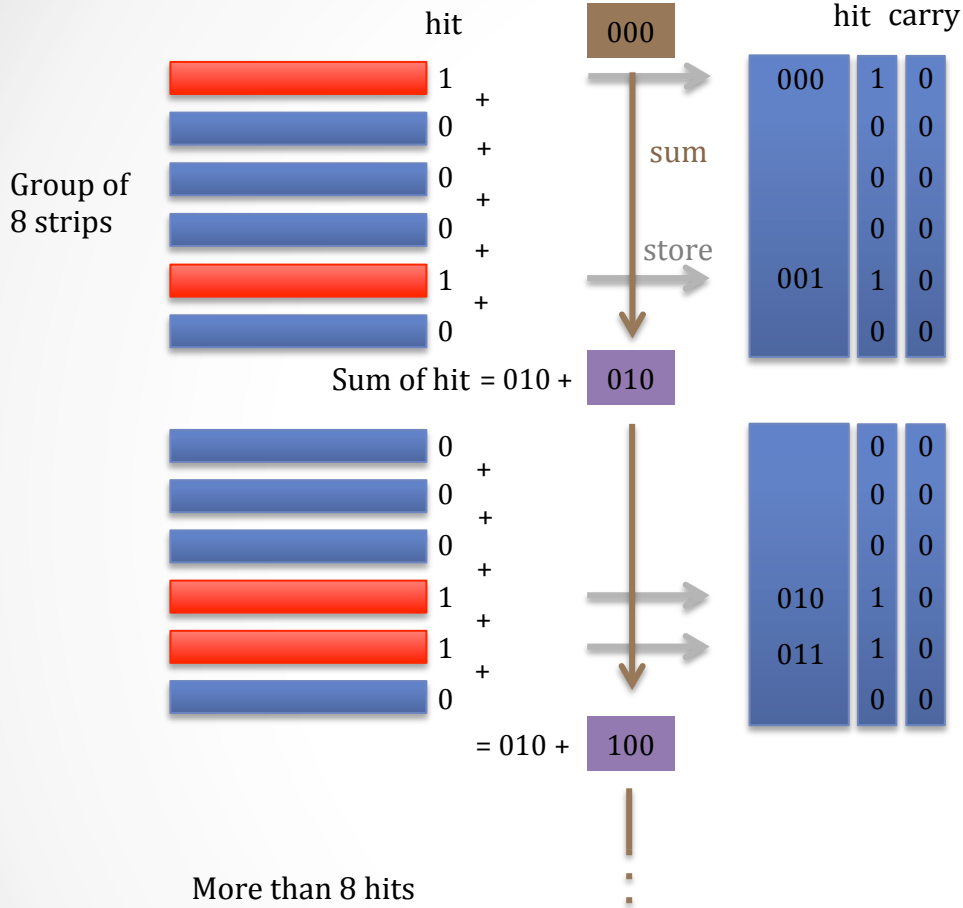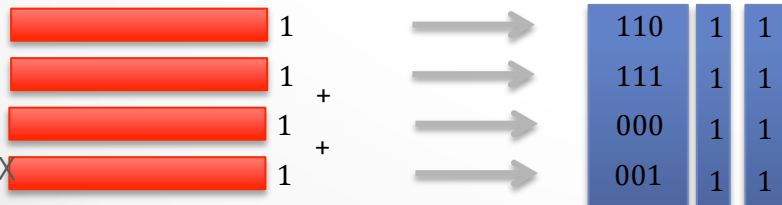
Output Pads

5 +1 bits	7 bits
1 0 1 1 0 0 | 1 0 1 0 1 0 0	
Strip & Flag	127 group

127 strips

2x 13 pads + 2 synch
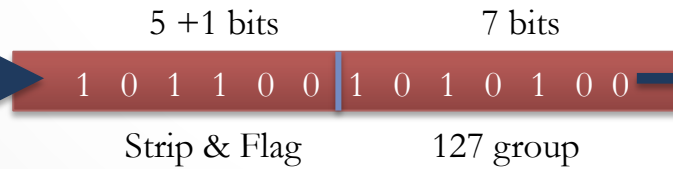
SACI – SLAC ASIC Control Interface
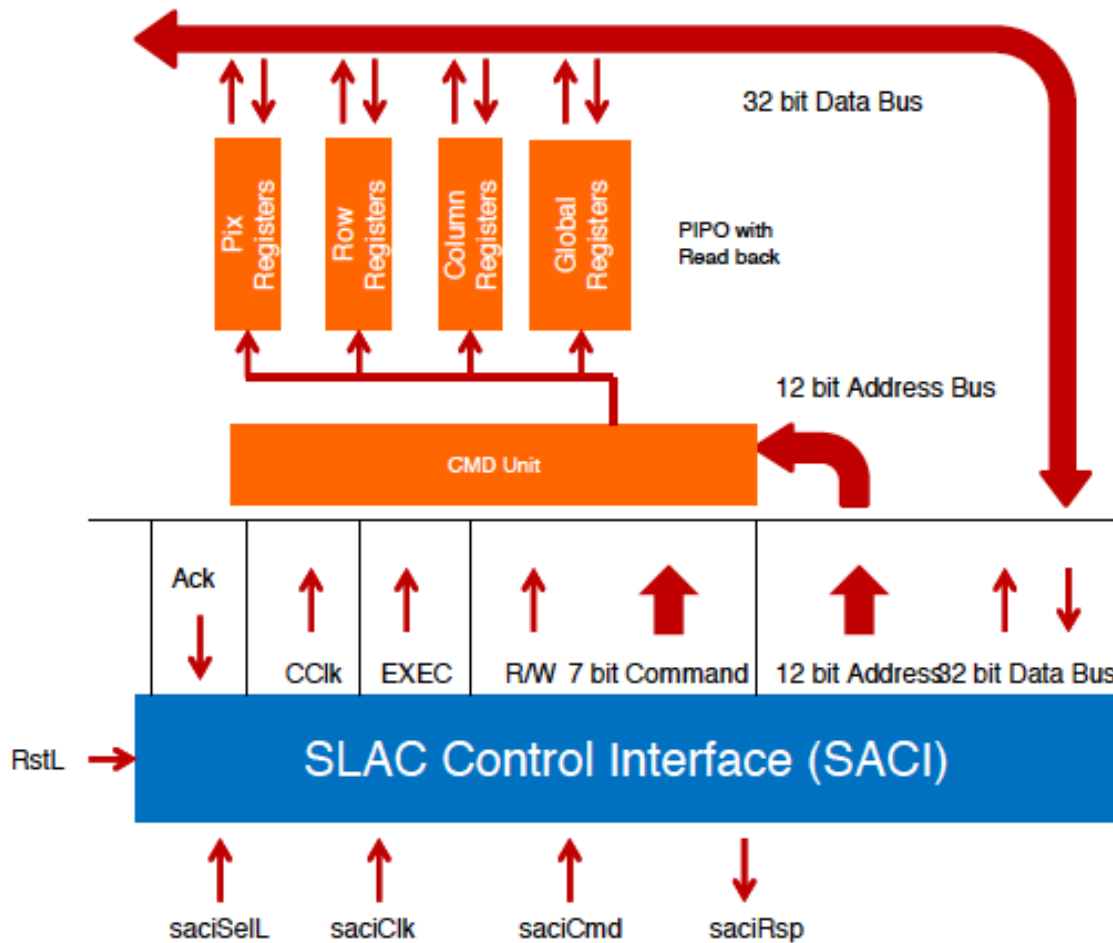
Serial Interface with handshake protocol

5 Signals

- 3 shared: *saciClk, saciCmd, saciRsp.*
- 1 dedicated select line per slave: *saciSelL.*
- 1 Reset Line (*RstL*) can be shared with the ASIC Global Reset.

- Operated between 0V and 3.3V
- Allows multiple SACI on same bus (parallel mode).
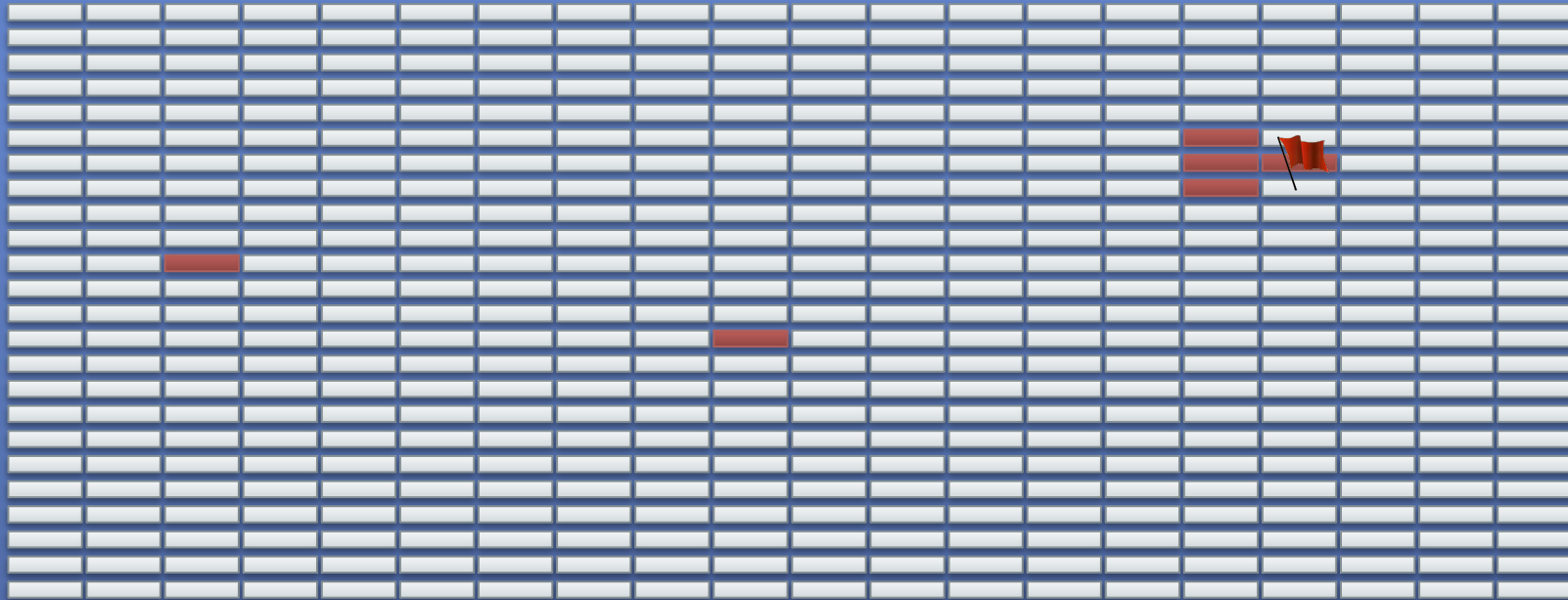
Layout

650μm

170μm

32 bit Data Bus

Pix Registers

Row Registers

Column Registers

Global Registers

PIPO with Read back

12 bit Address Bus

CMD Unit

Ack

CClk EXEC R/W 7 bit Command 12 bit Address 32 bit Data Bus

RstL

SLAC Control Interface (SACI)

saciSelL   saciClk   saciCmd   saciRsp

3

VERTEX
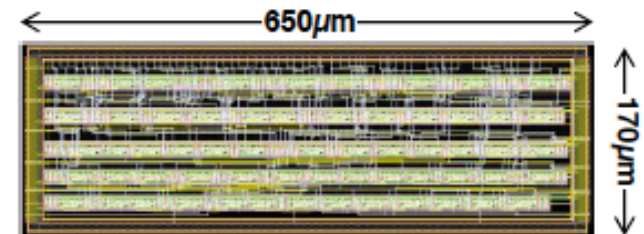
SLAC ASIC Control Interface (SACI)

SACIcmd (serial signal):

SET (1bit)	RW (1bit)	CMD (7bit)	ADDR (12bit)	DATA (32bit)
1	R/W	CMD	ADDR	DATA

ASIC internal Signals

Write/Read DATA bus

CMD, ack, exec

ADDRESS
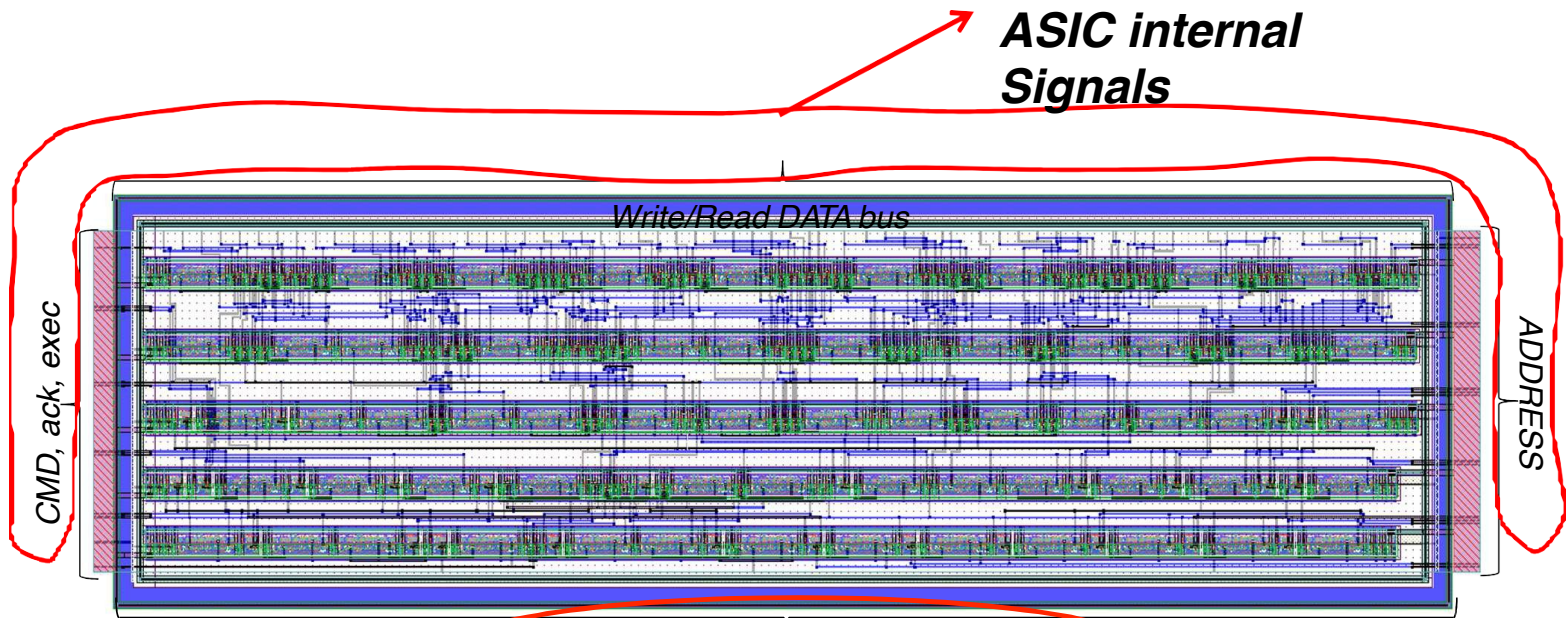
SACIclk, SACIcmd, SACIrsp, SACIsel,rst

Signals from PADS

SACI - Signals
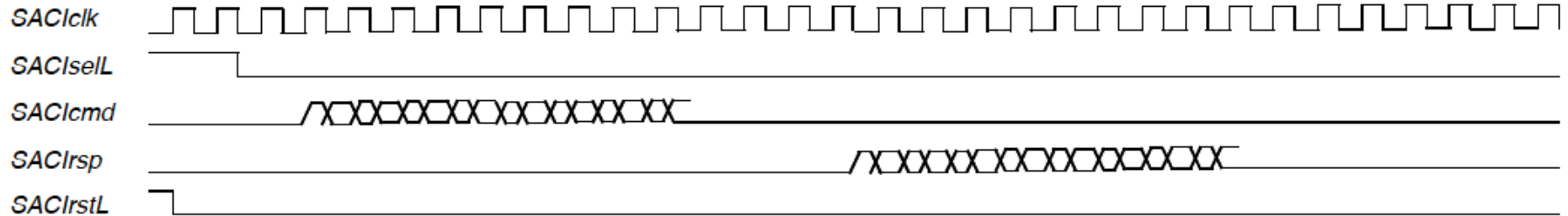
SACIcmd (serial signal):

SET (1bit)	RW (1bit)	CMD (7bit)	ADDR (12bit)	DATA (32bit)
1	$\overline{\text{R}}$/W	CMD	ADDR	DATA

SACIrsp (serial signal):

SET (1bit)	RW (1bit)	CMD (7bit)	ADDR (12bit)	DATA (32bit)	
1	1	CMD	ADDR		Write Mode
1	0	CMD	ADDR	DATA	Read Mode

5

SACI - Commands

SET (1bit)	RW (1bit)	CMD (7bit)	ADDR (12bit)	DATA (32bit)
1	RW		ADDR	DATA

RW	CMD		Function Clock Cycle
0/1	tbd	Read/Write Global Register	
1	tbd	Write Matrix	
0/1	tbd	Read/Write Pixel	

- The ASIC decoded the command last 4 bits. Any given command longer than 4 bits will be interpreted as a 4 bit command.

8

Encoding Read-Out scheme – Overview

Strip Encoding Output

4 groups of 13 rows
8 bits shift-registers

13 rows

8 bits

13

13

13

13

13

13

13

25ns Multiplexing

Digital Multiplexer

3.125ns Period Clock (320MHz)
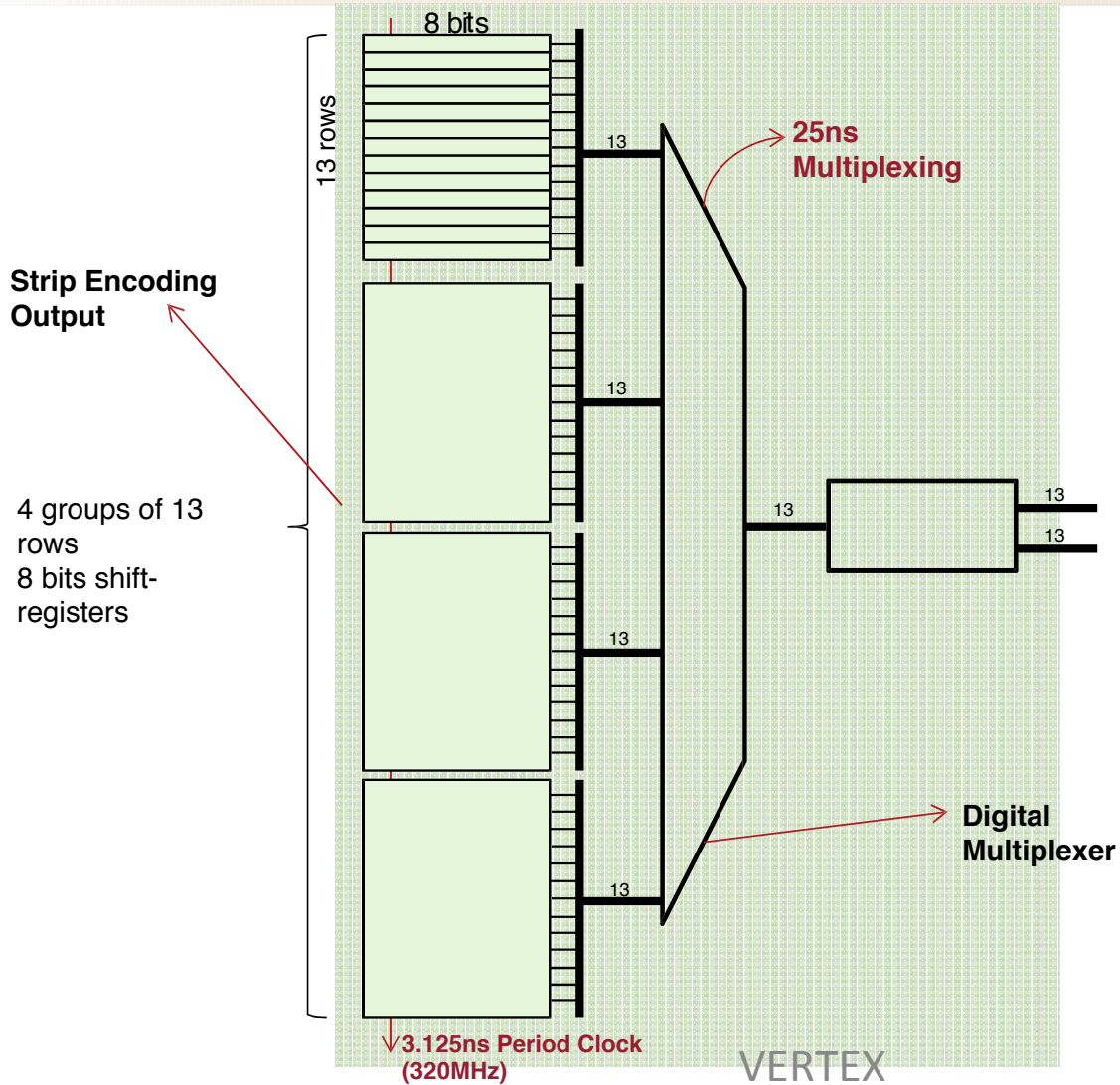
LVDS Driver – Simulated Performance

Schematic simulated at all condition (wo,wz,ws,wp) at room

Specs	Typical	Min	Max
Differential Output Voltage (@ R_{LOAD} =100Ω)	600mV		
Output Common Mode	1.2V	0.5	2.8
Current	3mA	0.2mA	3.5mA*
Speed	320MHz		500MHz
Supply	3.3V		

***Can meet standard LVDS requirements.**

14

CHESS-2 specification

	Specifications
Size of the chip	0.6cm x 2.5cm
Pixel size	40μm x ~800μm
Number of strips	127
Number of pixels per strip	32
Readout speed	320MHz
Output buffers	LVDS with tunable signal amplitude
Maximum number of hit per strip	1 + overflow flag
Maximum number of hits in strip array	8
Size of data output	13 bits
Format of data output	5 + 1+ 7 bits
Latency	Fixed latency

Summary

- A huge amount of knowledge has been accumulated from CHESS-1 & HV_Strip1

- Physics simulation seems to indicate that 128 strip grouping retaining 8 hits should meet occupancy requirements.

- More simulation would still need to be done including pile-up and harsh conditions in layer 1 and endcaps.

- Design in progress for submission end of June.

- HV & HR are collaborating for this new submission following the specs (https://twiki.cern.ch/twiki/bin/viewauth/Atlas/CHESSStripTestChip).

- Engineering run scheduled with res. from 20 to 200ohms.