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VELOPIX: A high rate pixel ASIC for the LHCb VELO upgrade

The LHCb Vertex Detector (VELO) will be upgraded in 2018 along with the other subsystems of LHCb in order to enable full detector readout at 40 MHz. LHCb will run without a hardware trigger and all data will be fed directly to the software triggering algorithms in the CPU farm. The upgraded VELO is a lightweight silicon hybrid pixel detector with 55 um square pixels, operating in vacuum in close proximity to the LHC beams. The readout will be provided by a dedicated front end ASIC, dubbed VeloPix, matched to the LHCb luminosity requirements. The occupancy across the chip is very non uniform, and the radiation levels reach an integrated 400 MRad over the lifetime of the detector in the most irradiated regions. VeloPix is a binary pixel chip with a matrix of 256 x 256 pixels, covering an area of 2 cmˆ2. It is designed in a 130 nm CMOS technology, and is closely related to the Timepix3, from the Medipix family of ASICs. The principal challenge that the chip has to meet is a hit rate of up to 900 Mhits/s/ASIC, resulting in a data rate of more than 16 Gbit/s. Combining pixels into groups of 2x4 super-pixels enables the use of shared logic and a reduction of bandwidth due to combined address and timestamp information. The pixel hits are combined with other simultaneous hits in the same super-pixel, timestamped, and immediately driven off-chip via custom designed 5.12 Gbit/s serialisers. The analog front end must be sufficiently fast to accurately timestamp the data, with a small enough dead time to minimise data loss in the most occupied regions of the chip. The power consumption of the analog front end is about 5 uW per pixel, and the total power consumption of the ASIC is less than 2 W. An extensive testbeam and lab test campaign is underway in order to characterise prototype upgrade VELO sensors and simultaneously study the performance of the Timepix3 chip in a high track rate environment. These measurements provide valuable input to the VeloPix project. The VeloPix ASIC design is nearing completion and the chip is expected to be submitted in the autumn. The current status of the ASIC design, performance simulations and prototyping will be described, along with recent lab and testbeam results.

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