







LHCb Upstream Tracker Upgrade

Jianchun Wang For The LHCb UT Group

Vertex 2015 Santa Fe, May 31-June 5, 2015





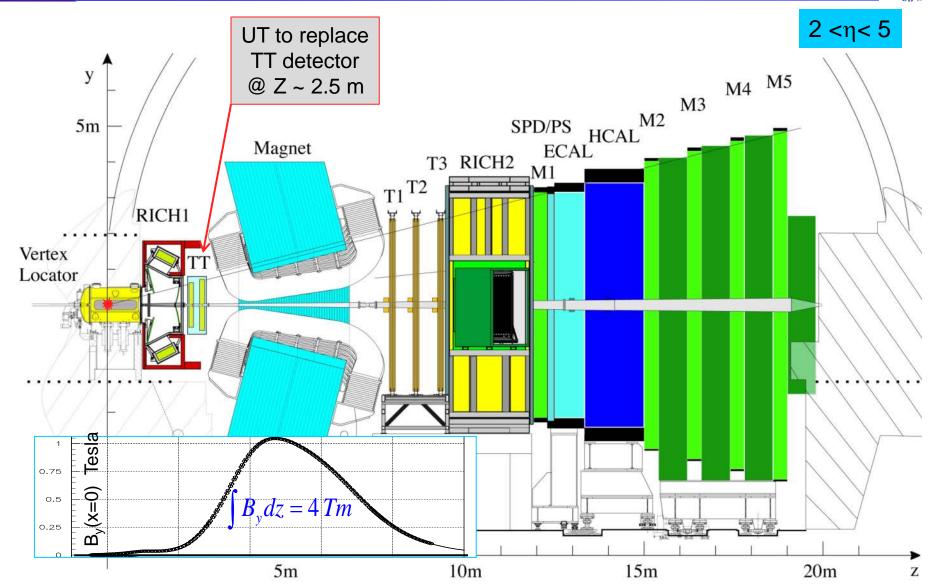






UT In The LHCb



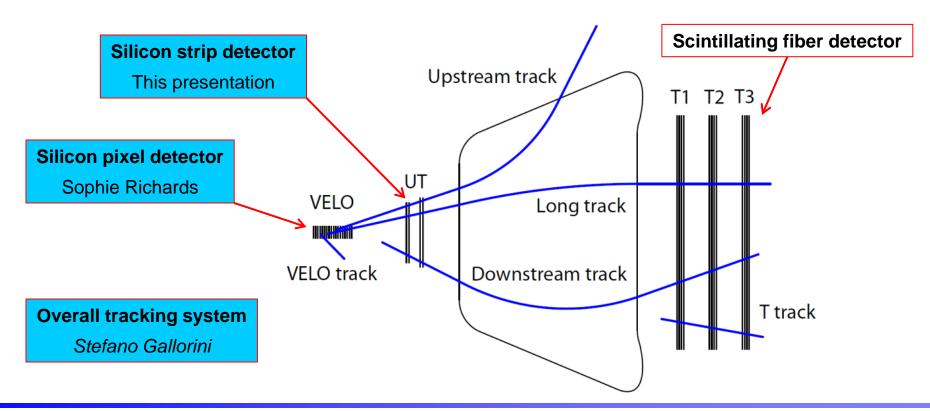




Upgrade Of The LHCb Tracking System



- The LHCb upgrade extend the physics reach by
 - Running at higher luminosity: L = 2x10³³ cm⁻² s⁻¹.
 - Reading out events at 40 MHz, & using full software trigger to increase trigger efficiency.
- ☐ All 3 tracking detectors are to be upgraded: Velo, UT, SciFi.



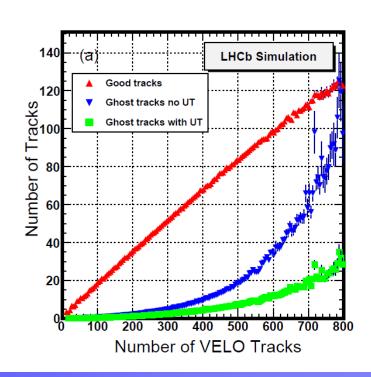


The UT Upgrade



- UT (Upstream Tracker) is to replace the TT detector:
 - Silicon strip sensors of finer granularity to cope with increased particle density.
 - Improved coverage at small polar angles.
 - Signal processing & digitization in sensor proximity at 40 MHz rate.
 - Improved radiation hardness for at least 50 fb⁻¹ data collection.

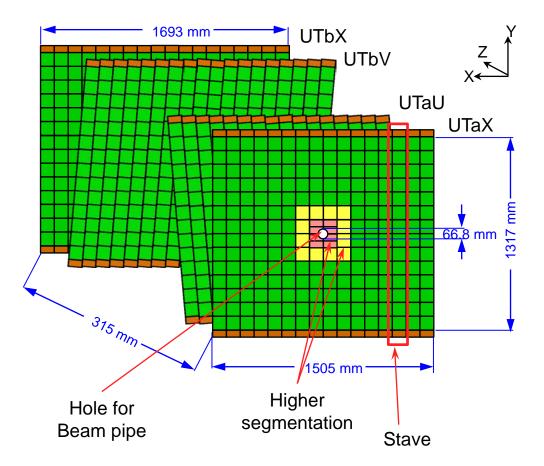
- UT in the LHCb tracking system
 - Provide fast estimates of momentum in the software trigger.
 - Increase reconstruction efficiency of long lived particles: e.g. $K_s^0 \to \pi^+\pi^-$, $\Lambda \to p\pi^-$.





The UT Detector System





- 4 planes constructed using "staves" with silicon on both sides, partially overlapping in X direction to ensure 100% coverage.
- Measuring XUVX coordinates.
- ☐ Higher segmentation in the region surrounding the beam pipe.
- Inner detectors with circular cuts to maximize acceptance.
- □ Basic mechanical unit "stave", total 68 UT staves.



UT Constituents To Be Discussed



Main constituents of UT detector are introduced in the order that follows signal data flow:

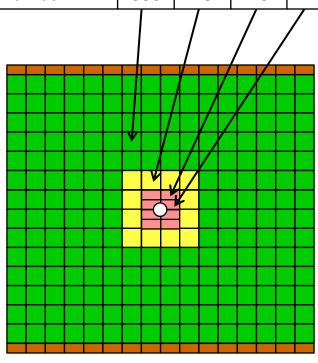
- 1) Silicon sensor,
- 2) SALT ASIC,
- 3) Flex cable,
- 4) Readout electronics,
- 5) Mechanical & cooling.



Silicon Sensors



Sensor				
	A	В	С	D
Pitch (μm)	~190	~95	~95	~95
Length (mm)	~100	~100	~50	~50
Strips/sensor	512	1024	1024	1024
Number	888	48	16	16



- Four different types of sensor.
- Sensor size: ~100×100 mm² (A & B), half length (C & D).
- Strip pitch: ~190 & 95 μm.
- Guard rings: 800 μm
- Thickness: 250 μm (maybe 320 μm for A)
- ♦ Wafer resistivity 3-5 KΩ•cm.
- n+-in-p technology (maybe p+-in-n for A).
- Sensor backside is passivated, & sensor is biased from front-side HV contact.
- Outer sensors (Type A) have much larger pitch than that of FE ASIC (~80 μm). Pitch adapters are needed, embedded or off sensor.



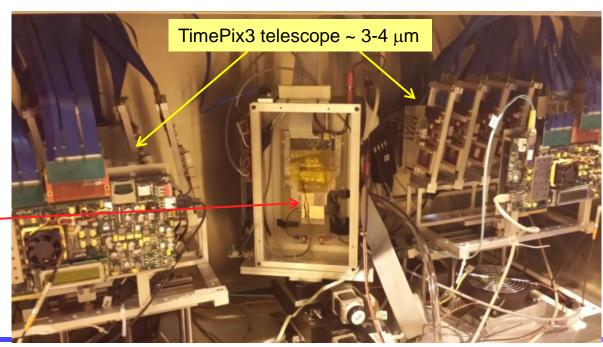
Sensor R&D - Phase I





- Mini-sensors ~1.1×1.1 cm²
- Both n+-in-p & p+-in-n types
- Strip pitch 80 μm.
- Different guard ring structure near circular cut.
- ❖ Inner-most sensors need to sustain ~5×10¹⁴ 1-MeV n_{eq}/cm² fluence for 50 fb⁻¹ running.
- Sensors were exposed to up to ~4×10¹⁴ n_{eq}/cm² at Mass. General Hospital in June 2014, and tested in a 180 GeV proton beam at CERN in Oct. 2014.

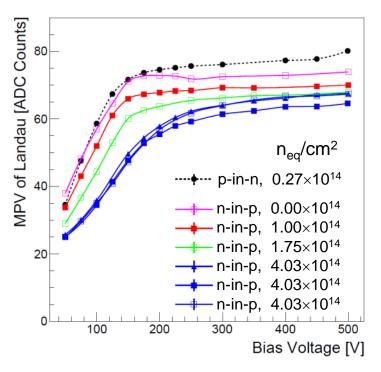
Mini sensors are read out by Beetle chips-& Alibava DAQ system

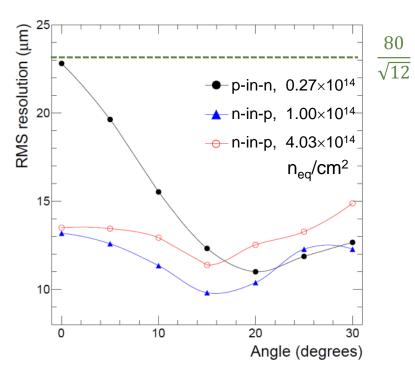




Phase-I Sensor Test Beam Results





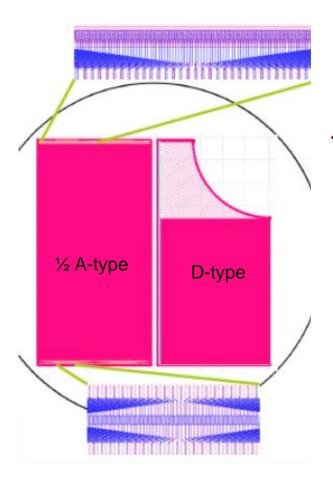


- For the n⁺-in-p sensors, there is a gradual loss in total charge collected with increased radiation dose.
- * All sensors reach plateaued @ 300-400V, S/N rate >~ 15. They should be efficient after 50 fb⁻¹ running (5×10^{14} n_{eq}/cm²).
- More charge sharing at normal incidence for irradiated n⁺-in-p sensors.



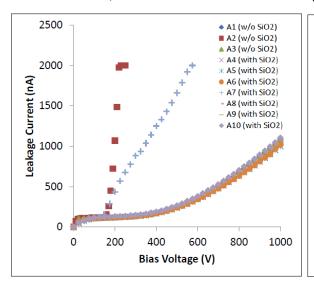
Sensor R&D Phase II

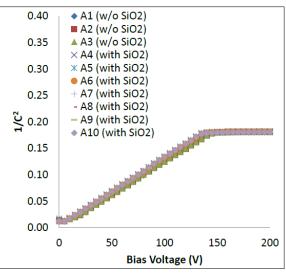




- What do we need to assess:
 - Functionalities of detectors (type D) with circular cut.
 - Performance of built-in pitch adapter for type A sensors.
 - In parallel glass pitch adapters to implement "external pitch adapter" solution in hand (produced by CNM)
 - Evaluation of these devices will allow us to fix sensor sizes & constrain hybrid sizes.

IV, CV for ½ A sensors (D sensors are similar).







Test Beam In Summer 2015

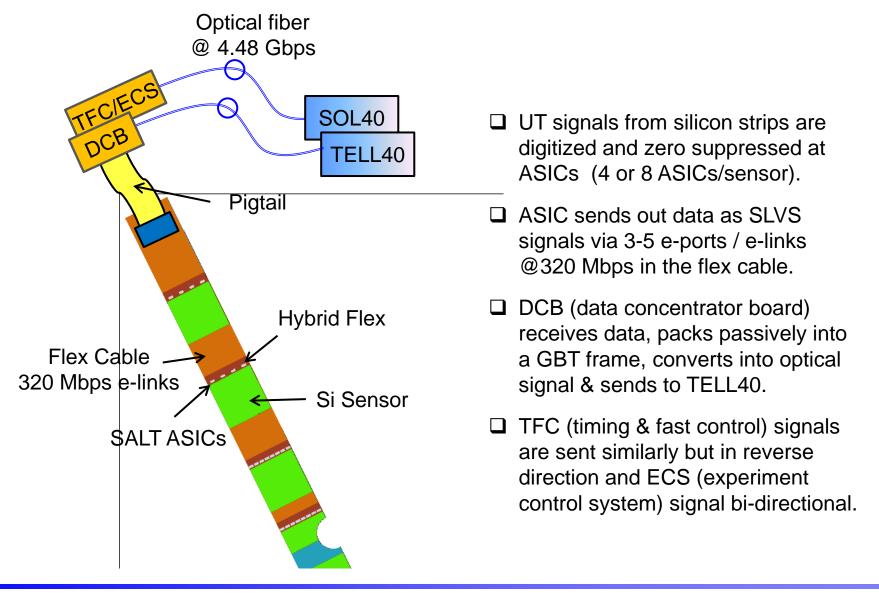


- Phase II prototype sensors were irradiated at CERN in May, and will be tested soon.
 - Type A sensors radiation dose ~1 MRad.
 - Type D sensors exposed to $\sim 5 \times 10^{14} \text{ n}_{eq}/\text{cm}^2$ (40 MRad).
- The irradiated sensors and un-irradiated reference sensors will be tested in proton beam at CERN this July.
- We want to learn:
 - Will the embedded pitch adapter work properly after 1 MRad irradiation?
 - Performance of type D sensor near the cutout.
 - Validate backside passivation and biasing scheme.
- As type A sensors ~92% of all sensors, we plan to submit RFQ of type A in August and start production if the performance is satisfactory.



UT Signal Readout Chain

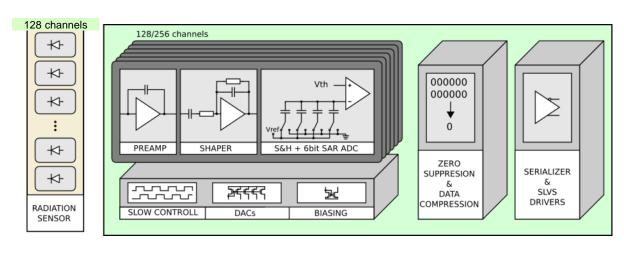






Front End ASIC - SALT

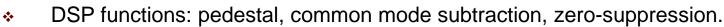




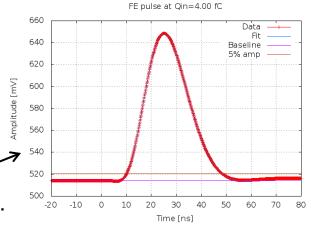
SALT – custom design for UT.

Preamp-shaper prototype

- CMOS 130 nm technology (IBM, TSMC).
- 128 channels, per channel preamplifier & 6-bit ADC.
- Sensor capacitance 5-20 pF, AC coupled.
- Dynamic range ~ 30 ke, both input signal polarities.
- Noise: ENC ~ 1000 e @ 10 pF + 50 e / pF.
- Pulse shape: T_{peak} < 25 ns, short tail ~5% @ 25ns+T_{peak}.



- Serialization & data transmission via 320 Mbps e-ports.
- Power consumption < 6 mW / channel.</p>

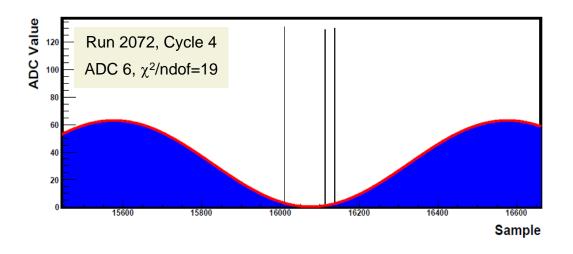




Radiation Test Of SAR ADC



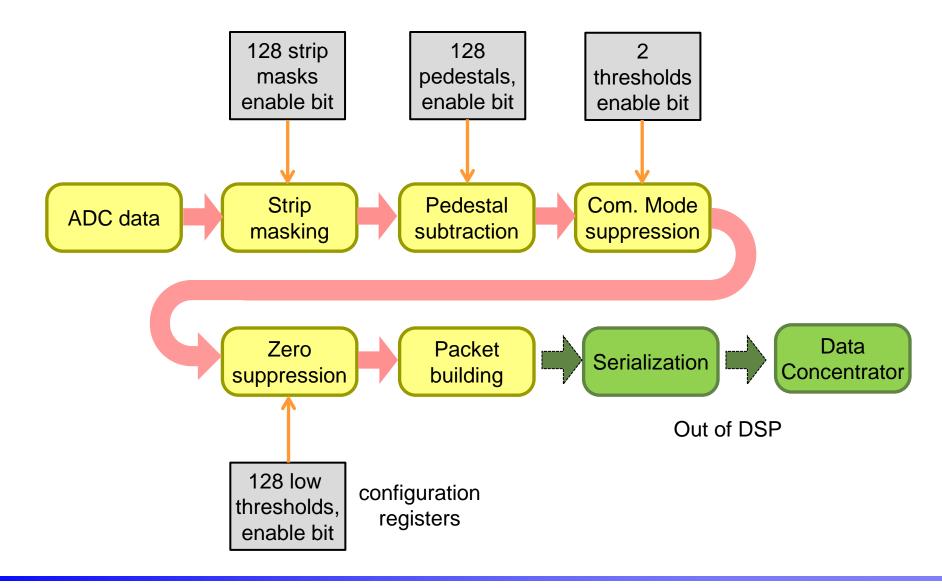
- SALT chip uses 6-bit SAR (successive-approximation-register) ADC, which is more susceptible to SEUs.
- A prototype 8-channel ADC (from IBM) was tested in 226 & 60 MeV proton beams at MGH in June 2014.
- Beam intensity: radiation level from ~ LHCb running to ×1000 to boost statistics.
- A 40 KHz sine wave signal was injected & digitized at 40 Msps. A SEU sample can be identified by comparing measurement against expectation from fit.
- A few SEU candidates were observed from 2x10⁸ samples. ⇒ Whole UT system has ~7x10⁻⁶ SEU channels per bunch crossing in LHCb nominal running.





SALT DSP Flow Chart







SALT ASIC Plan



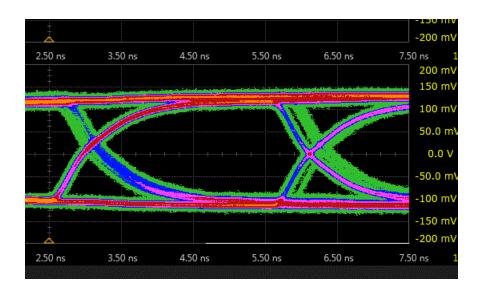
- Performance of SALT prototype functional blocks (by IBM) with separate analog and digital functions meet the specifications.
- SALT8 prototype ASICs from TSMC were delivered this April, which has 8 input channels and full digital functions.
- The ASICs are currently under test to verify functionalities & performance. Radiation tests for SEU rate & TID effect are in plan.
- The ASICs will also be used in UT electronics slice tests to validate the whole readout chain.
- The next submission will be 128-channel ASIC with full digital functions (Nov 2015).



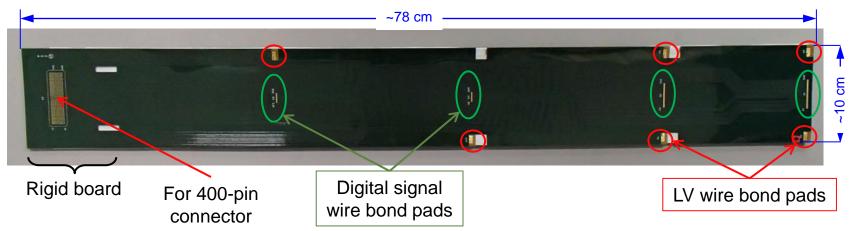
Flex Cables



- 4 flex cables per stave for digital signals (up to ~240/cable), LV & HV powers.
- Requirements:
 - Signal integrity.
 - Low material budget.
 - LV round trip drop < 0.5 V (for ~2.5A).
- 1st iteration cables made, single pair signal quality OK, low yield in production.
- 2nd generation design is submitted and will be produced at CERN.



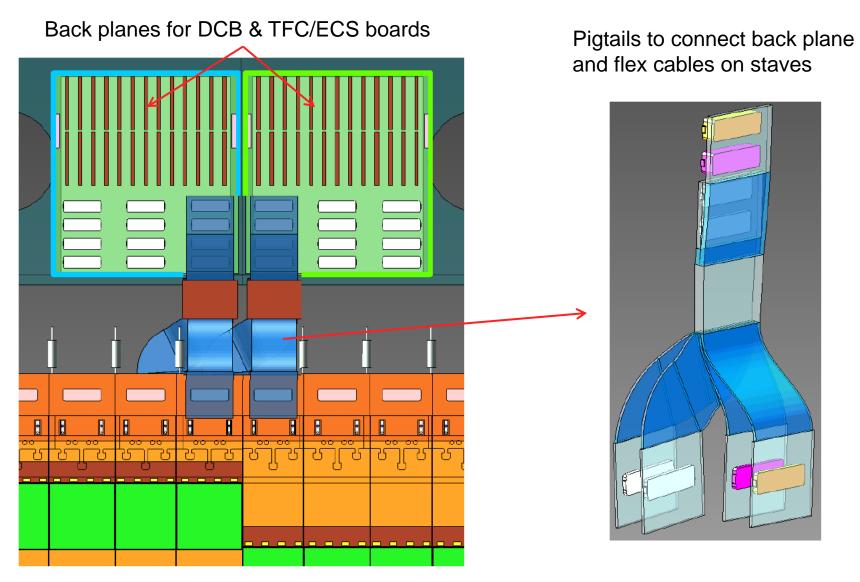
1st iteration cable





End of Stave Volume

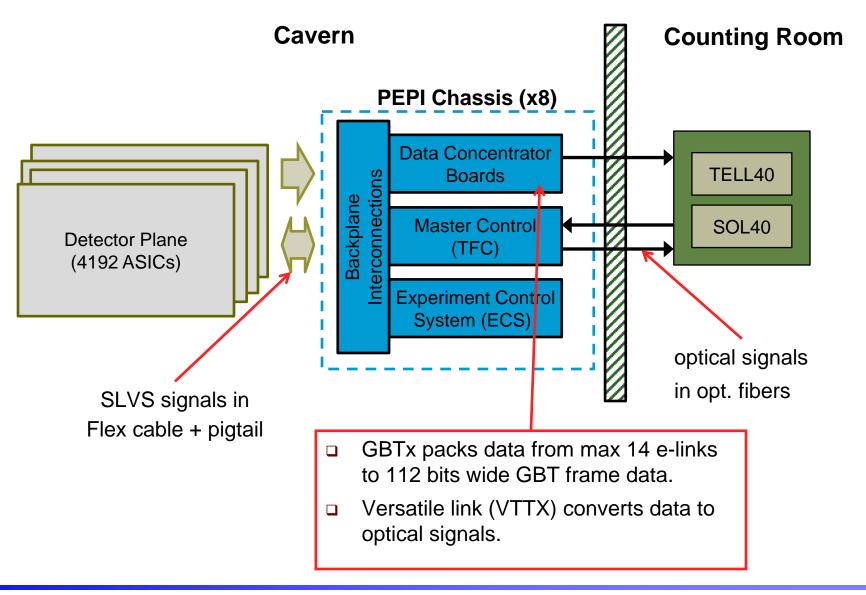






Readout Electronics

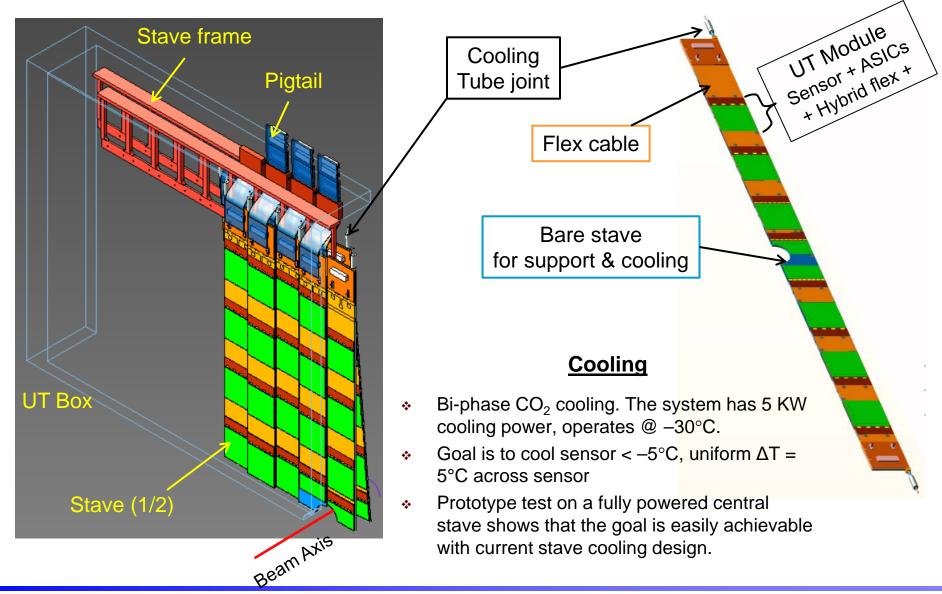






UT Mechanics And Cooling

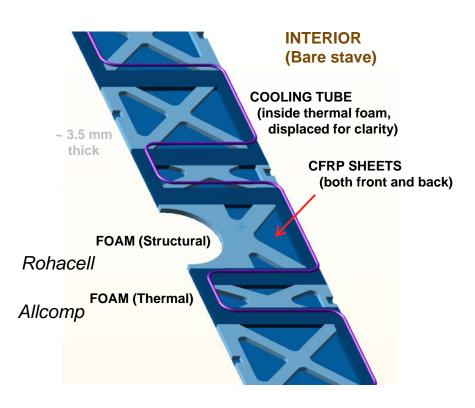


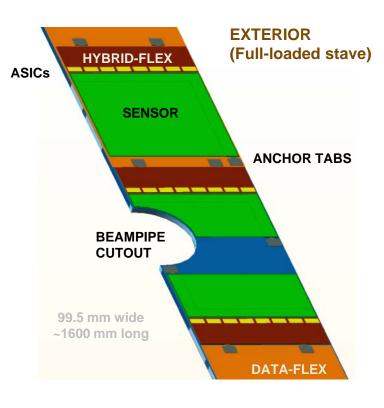




UT Stave







- 2 CFRP (Carbon fiber reinforce polymer) face sheets attached to foam core, forming a sandwich structure, all epoxy construction.
- Ti cooling tube is embedded in the thermal foam: 2.275 mm OD, 135 um wall.
- Cooling tube in "snake" shape to make run under all ASICs.



Recent Tests of Stave Components



Thermflow T725 epoxy

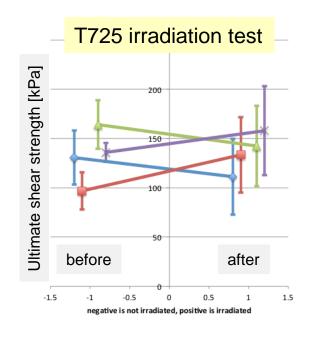
- Reworkable epoxy (phase changing thermal interface material) for module to stave.
- Measured ultimate shear strength, before & after irradiation (40 MRad) - OK.
- Tested in low-temp no change.

Ti tube fittings

- Braze (AgCu) vs epoxy (Araldit 2011 / Armstrong A12).
- Pressure-tested samples before & after irradiation (100 kRad) OK to 150 bar
- □ Low-temp tests in progress

Rohacell structural foam

- Measured ultimate tensile strength & ultimate shear strength.
- Irradiated to 40 MRad, to be tested
- □ Low-temp tests in progress





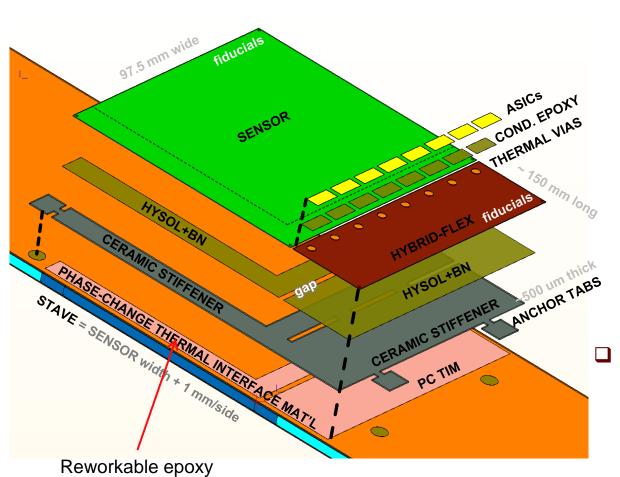


UT Module (Exploded View)



Sensor: -5° C, $\Delta T = 5^{\circ}$ C

Bias: up to 500 V



Requirement:

- Provide connection between ASICs & flex cable.
- Protect wire bonds during testing and handling.
- Maximize heat transfer from ASICs to stave, minimize heat transfer to sensor.
- Isolate sensor bias from stave facings (ground).
- Stiffener CTE match to Si. Not to over-constrain sensor, allows for bow.

Design options:

- Hybrid flex + Pyrolytic BN ceramic stiffener (500 μm).
- \circ AIN ceramics (250 $\mu m)$ + multilayer printed traces.



Summary



- UT is silicon strip tracker to replace the TT detector in the LHCb upgrade. It has better granularity, front end electronics in sensor proximity, & taking data at 40 MHz rate.
- R&D work is in advanced stage and will transit to construction in a staged manner starting with "bare stave" assembly.
- Preproduction of Si sensor will start soon, first the type A sensor (majority of detector coverage).
- An active program of test beam studies of subsystems with increasing complexity will validate all the aspects of the design. Focus in year 2015 is on irradiated detectors.
- UT installation will start in Jan 2019.





Backup Slides

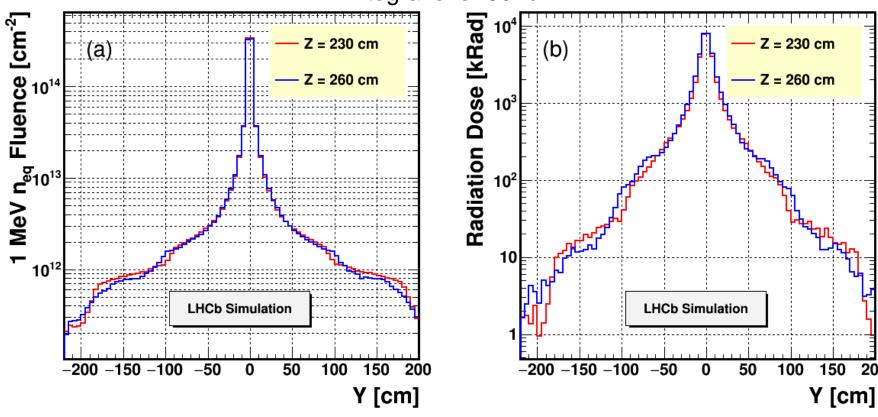
06/01/2015



Radiation Constraint





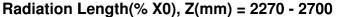


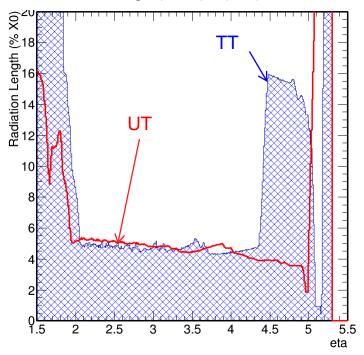
- \bullet Sensor closest to beam: ~ 40 MRad, or ~ 5x10¹⁴ n_{eq}/cm² fluence.
- ❖ Sensor cooled to −5°C, bias voltage up to 500 V.
- Closest readout ASIC: ~ 20 MRad.



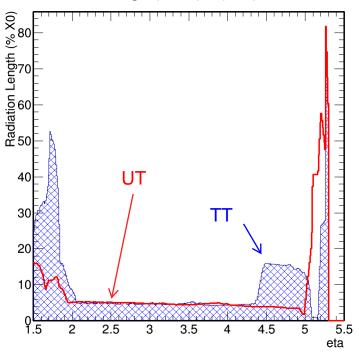
Radiation Length Plots







Radiation Length(% X0), Z(mm) = 2270 - 2700



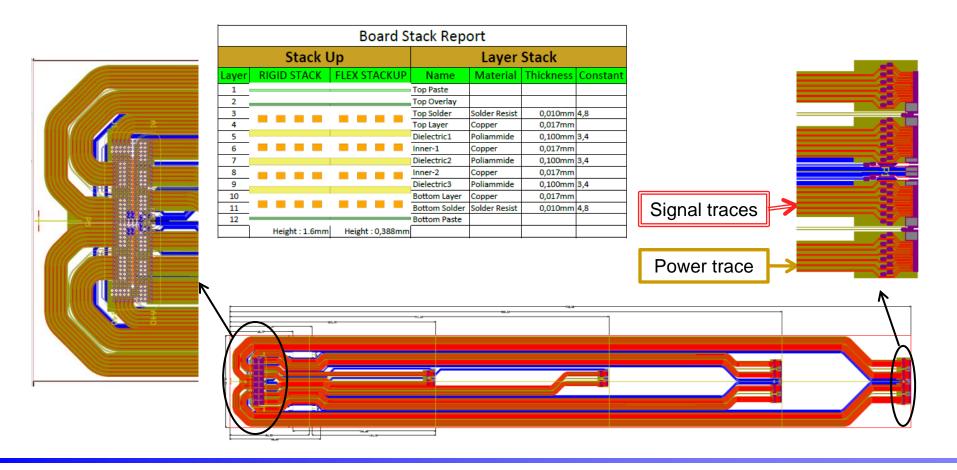
- ➤ Radiation length between Z=2270-2700 mm, including 0.14% X₀ of air, 0.34% of UT box.
- The total radiation length between $2<\eta<4.9$ in the new UT release (2) is 4.6% X_0 . RL per UT plane is 1.02% X_0 .
- Beam jacket is from the current best design. The overall $\int RL \cdot d\eta = 7.02\% X_0$ in this design, slightly smaller than 7.49% X_0 in the TT design. More importantly, it occupies much smaller angle $(\eta>5)$, instead of $(4.4 < \eta < 5)$ where tracks are used in physics study.



Flex Cables – 2nd Iteration



- The 2nd generation design is submitted and will be produced at CERN.
- 4 conductive layers: 2 for signals, 1 for LV power, 1 for test purpose.
- Signal traces run on top of power traces all the way for better impedance uniformity.

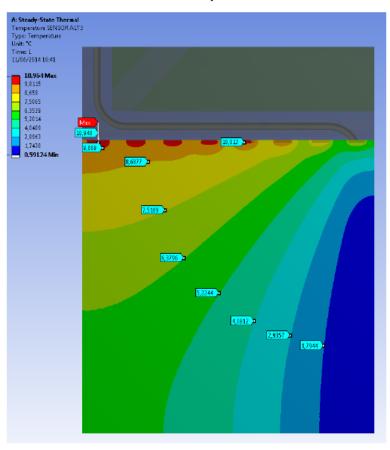




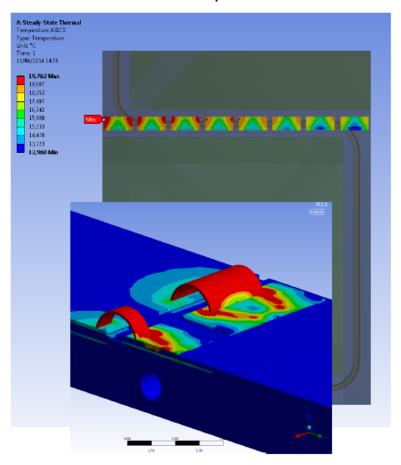
Thermal Simulation



sensor temperature



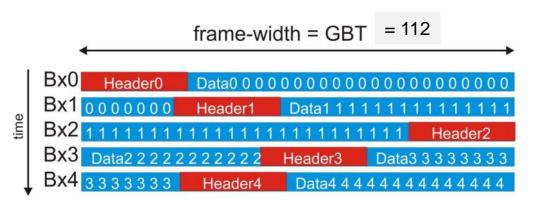
ASICs temperature





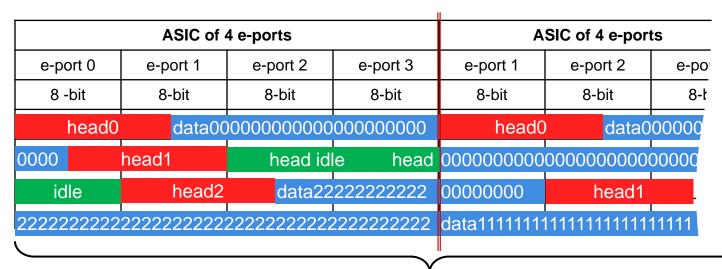
UT GBT Sub-Frame Format





From "Electronics Architecture of the LHCb Upgrade" http://cds.cern.ch/record/1340939

UT ASICs are independent. E-ports within an ASIC send data coherently. Each ASIC data form its own GBT sub-frame.



Up to 14 e-ports per GBTx

06/01/2015