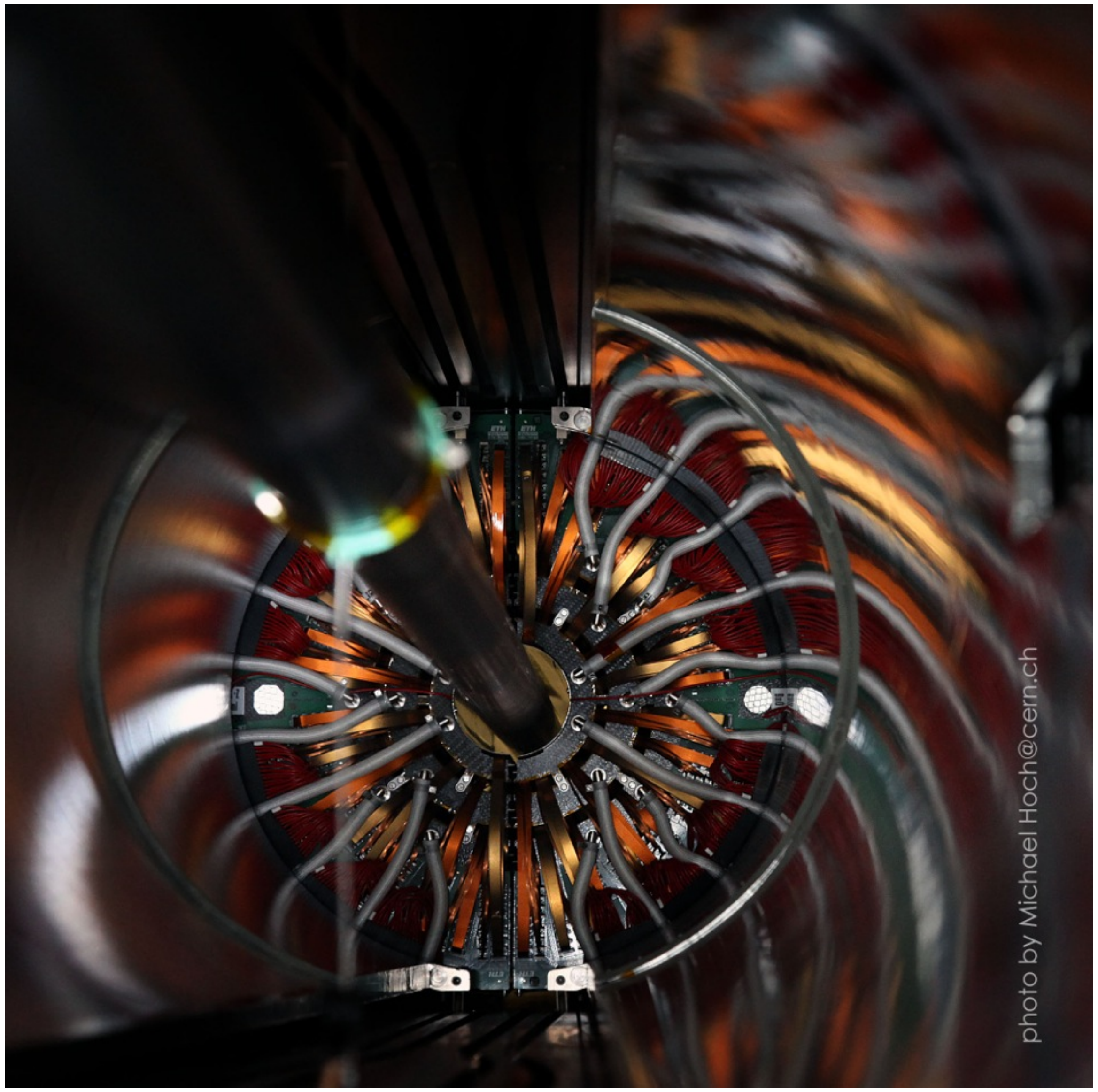
University of Zurich[UZH]
Physik-Institut

CMS Inner Detector

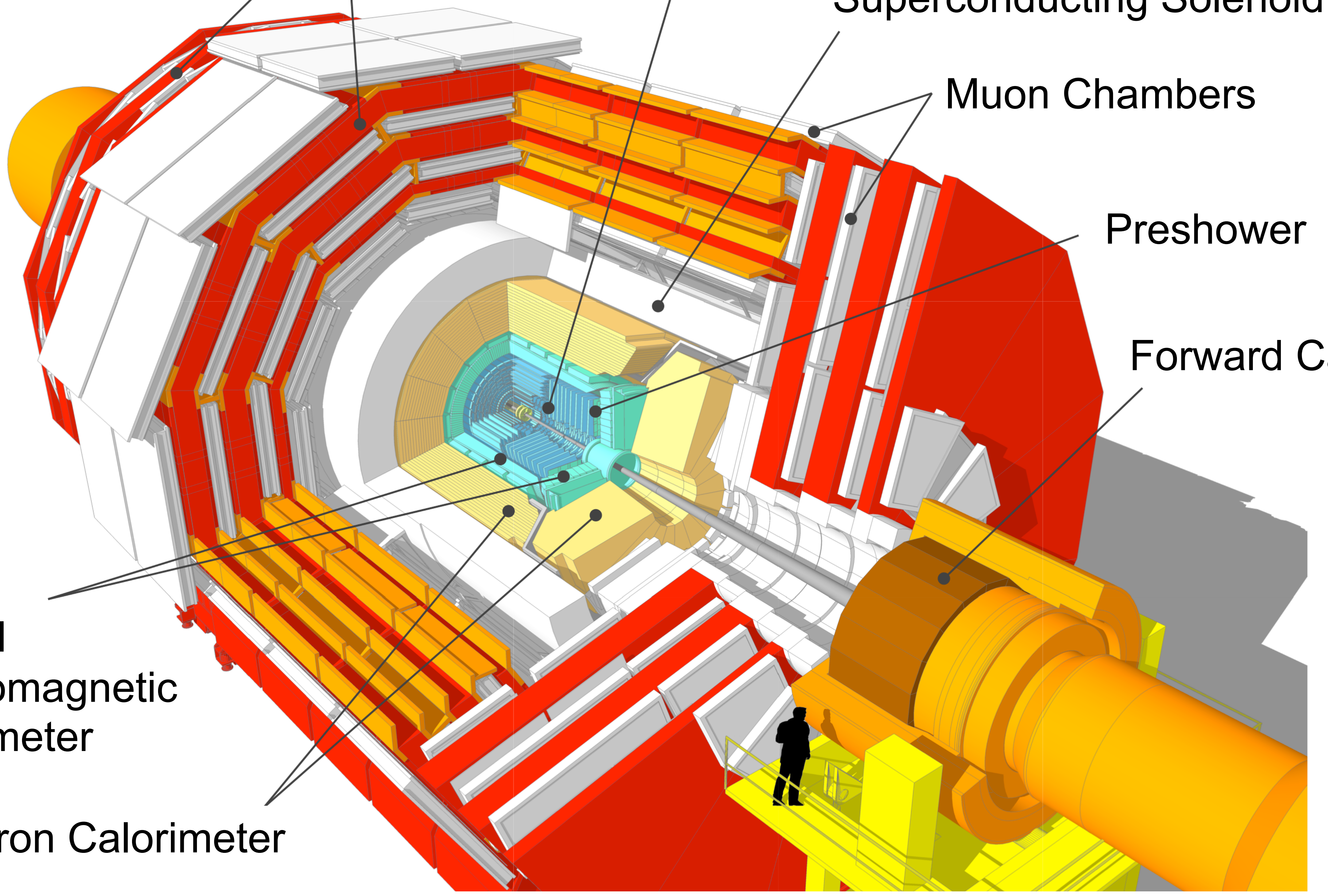
The Run 1 to Run 2 transition, and first experience of Run 2



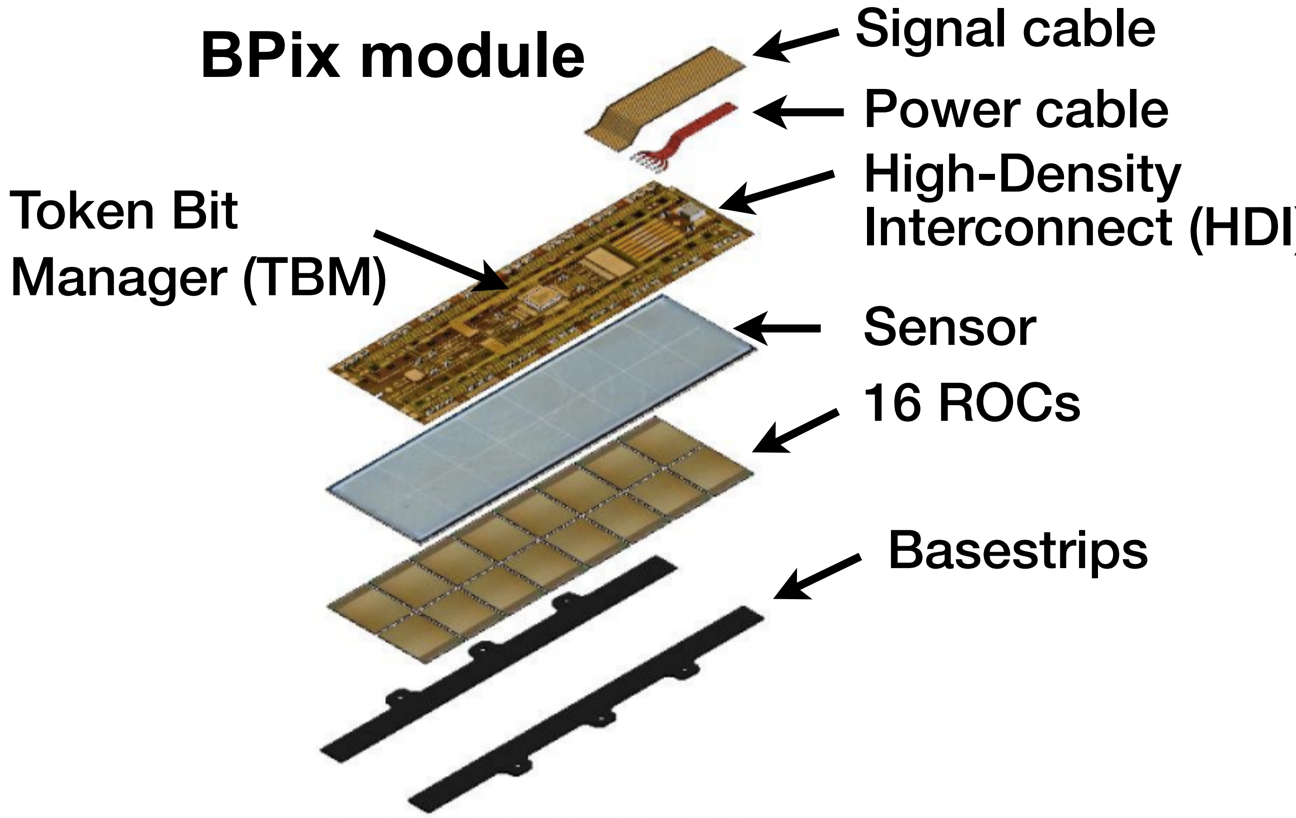
Clemens Lange (UZH)
on behalf of the CMS collaboration
VERTEX 2015
Santa Fe, New Mexico, USA
1st June 2015

CMS Detector

Weight: 14,000 tonnes
Diameter: 15 m
Length: 28.7 m

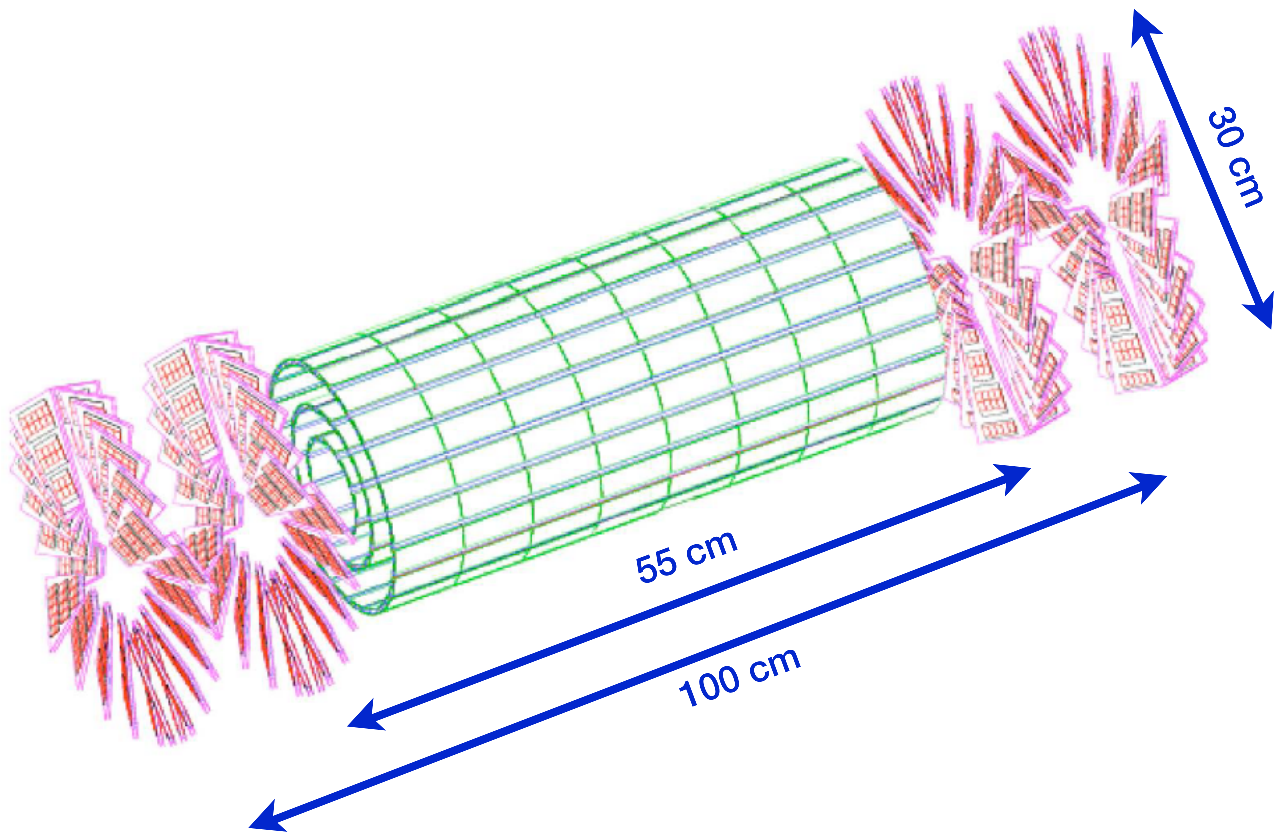


CMS Pixel Detector



basic properties:

- 3 barrel layers (BPix)
  - radii of 4.3, 7.2, and 11 cm
  - 48 million pixels, area of 0.78 m^2
- 2 endcap pixel disks at each side (FPix)
  - 18 million pixels, area of 0.28 m^2

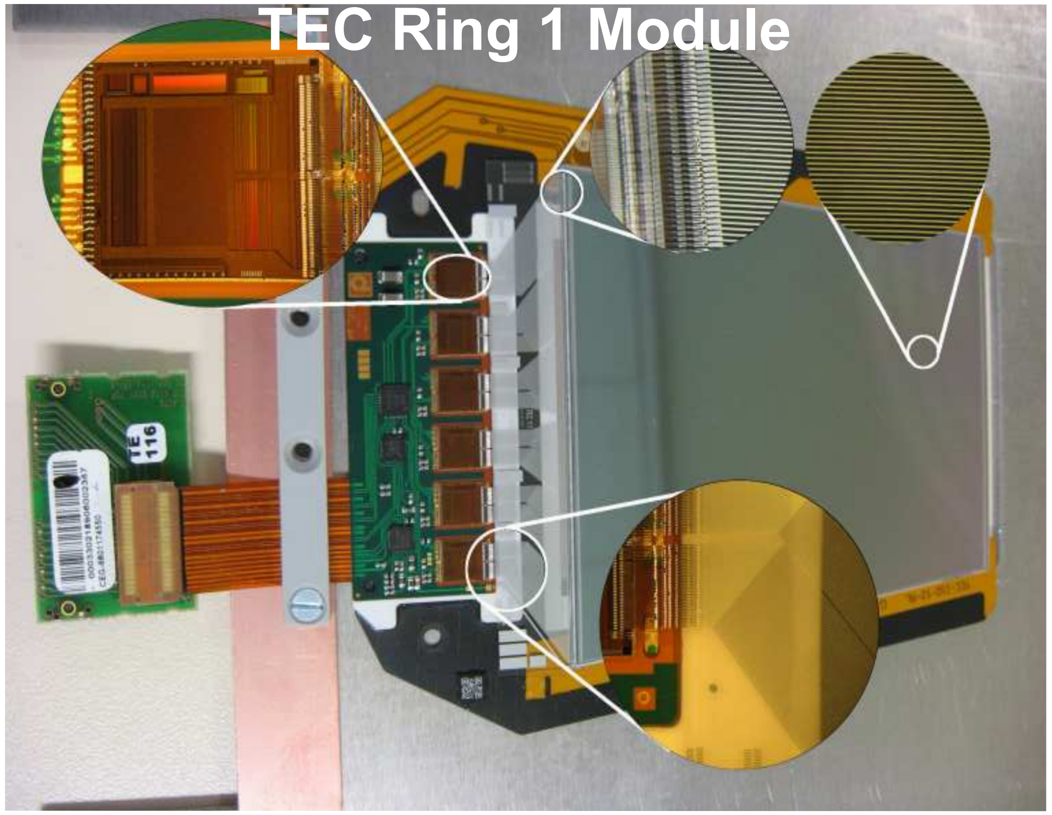


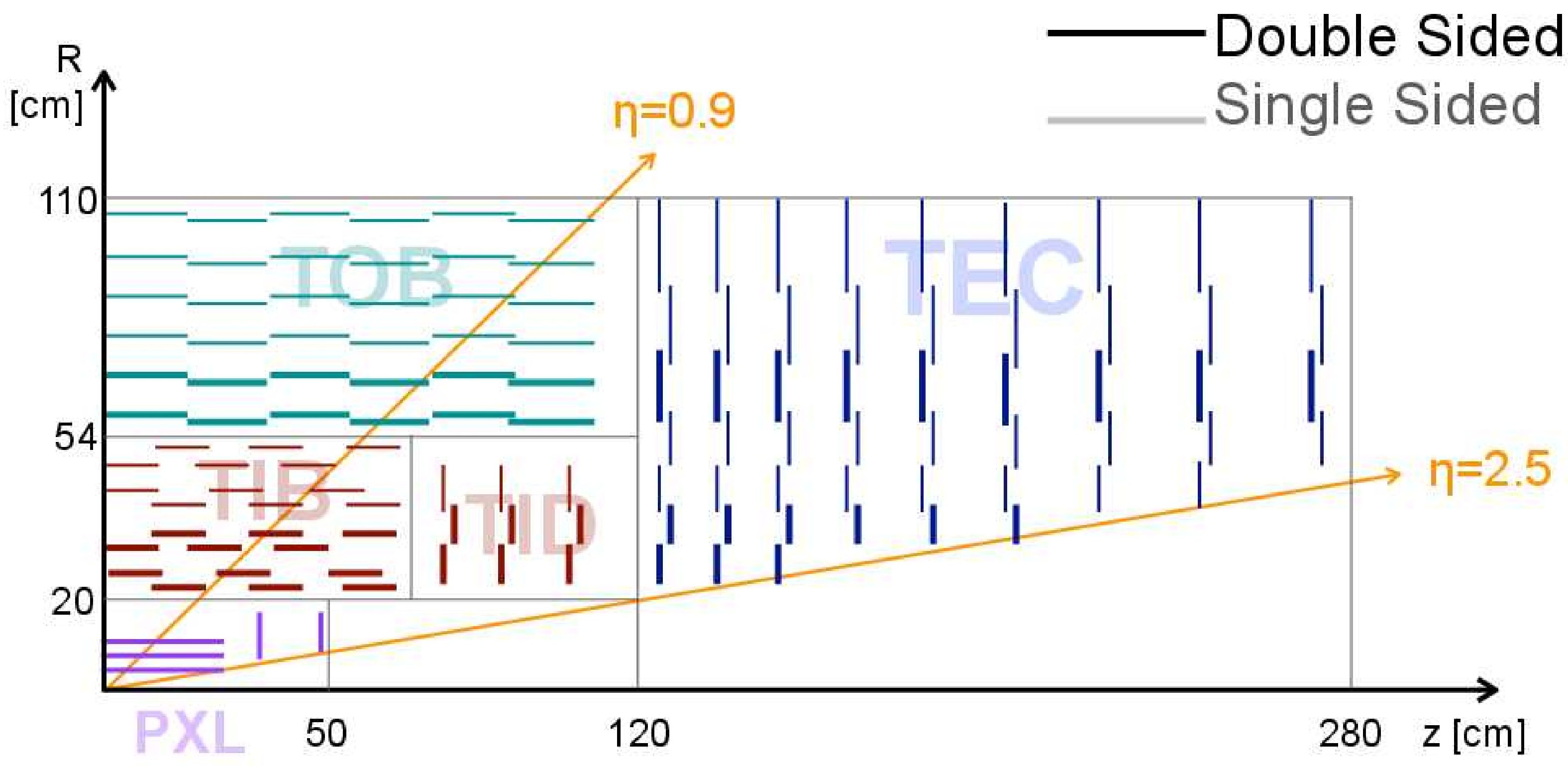
- BPix: 768 modules
- FPix: 192 panels
- pixel size: 100 x 150 μm (250 μm sensor thickness)
- 1 ROC serves a 52 x 80 array of pixels
- sensor: n+ implant in n bulk
- ~66 million readout channels in total

CMS Silicon Strip Tracker

basic properties:

- 10 layers in barrel region
  - 4 Inner Barrel (TIB), 6 Outer Barrel (TOB)
- 9+3 discs in the inner disks (TID) and endcaps (TEC)
- active area 200 m^2
- ~9.6 million electronic channels

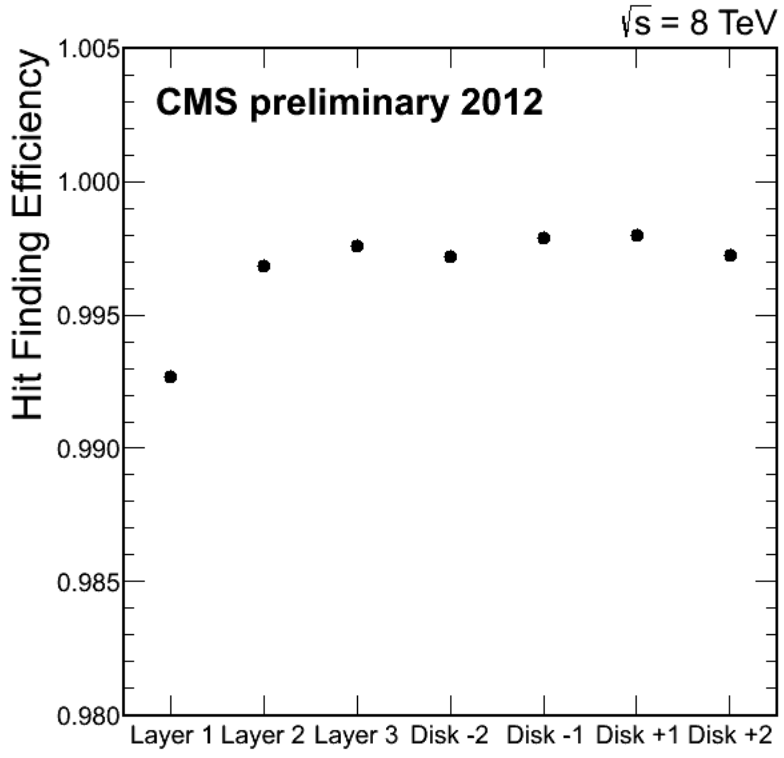


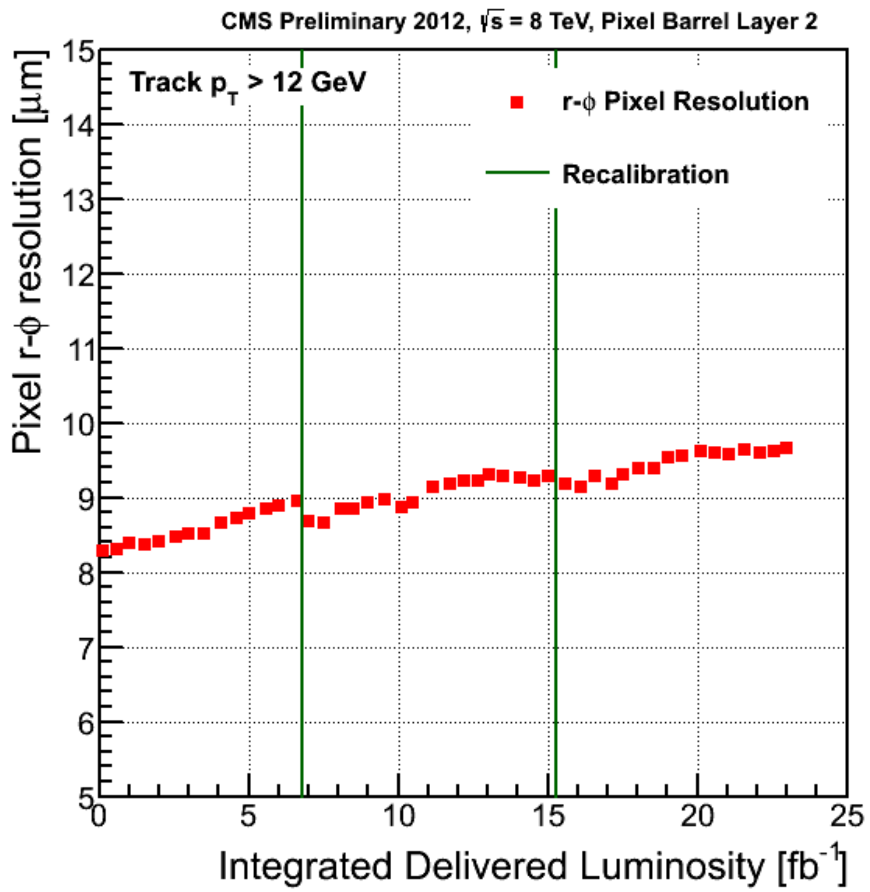


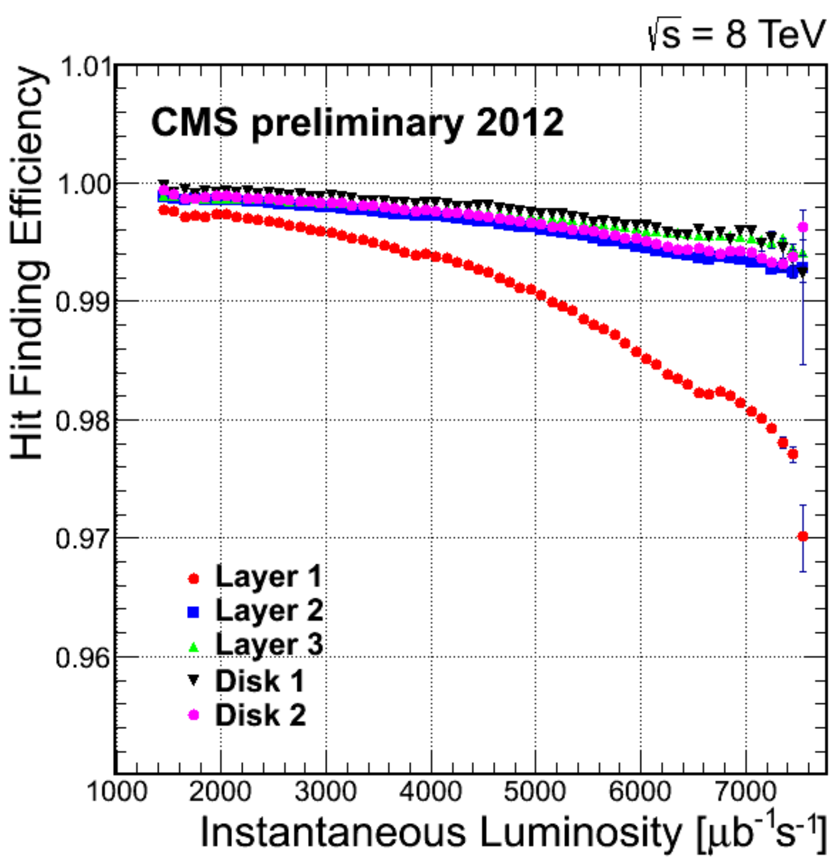
- p^+-in-n silicon sensors
- 320 µm and 500 µm thick
- 512-768 strips
- strip pitch 83-205 µm

Performance of the Pixel Detector in Run 1

- hit efficiency above 99% for all working ROCs
- dynamic inefficiency observed with increasing instantaneous luminosity:
  - higher occupancy increases probability of ROC buffer overflow
- measured r-φ resolution < 10 µm at the end of Run 1

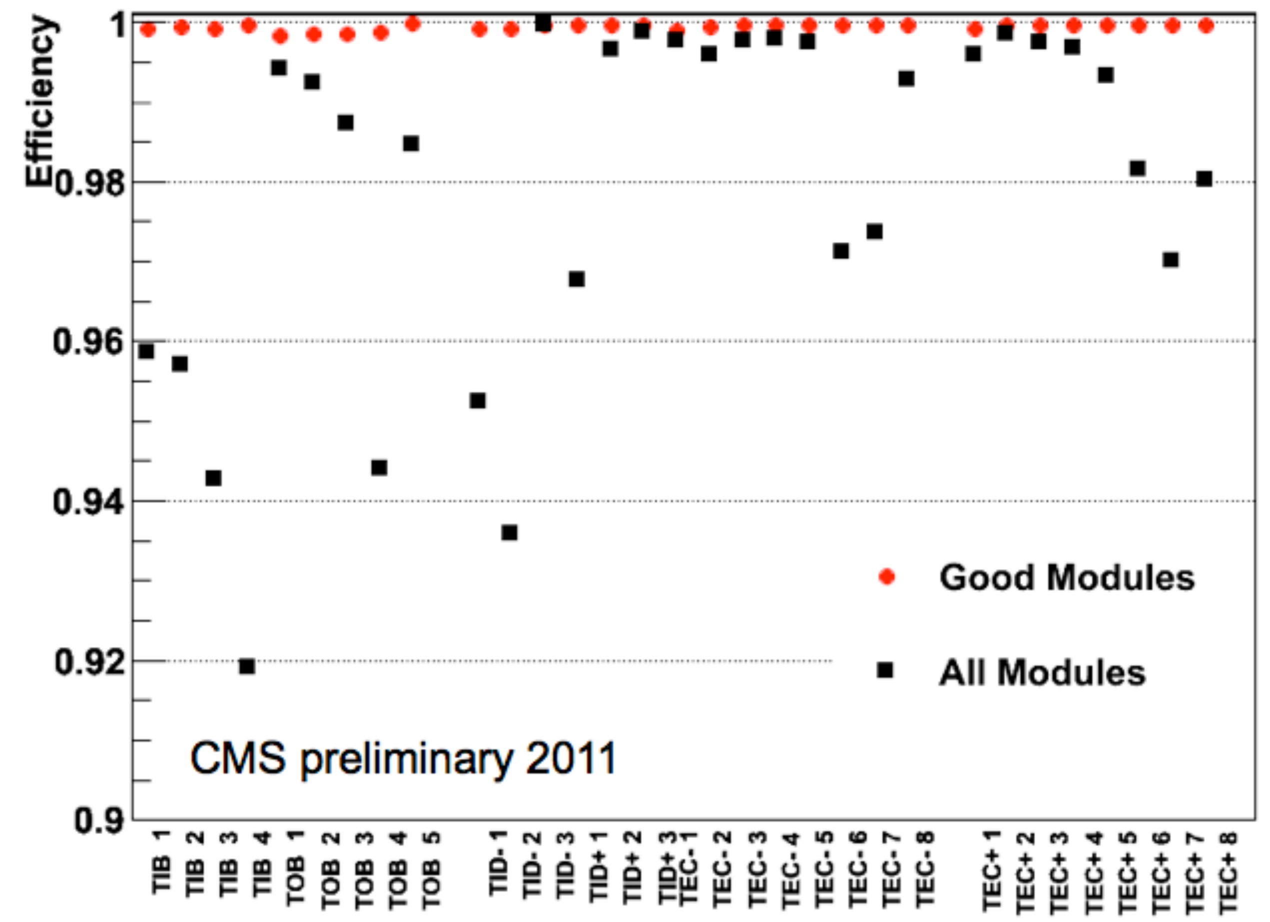


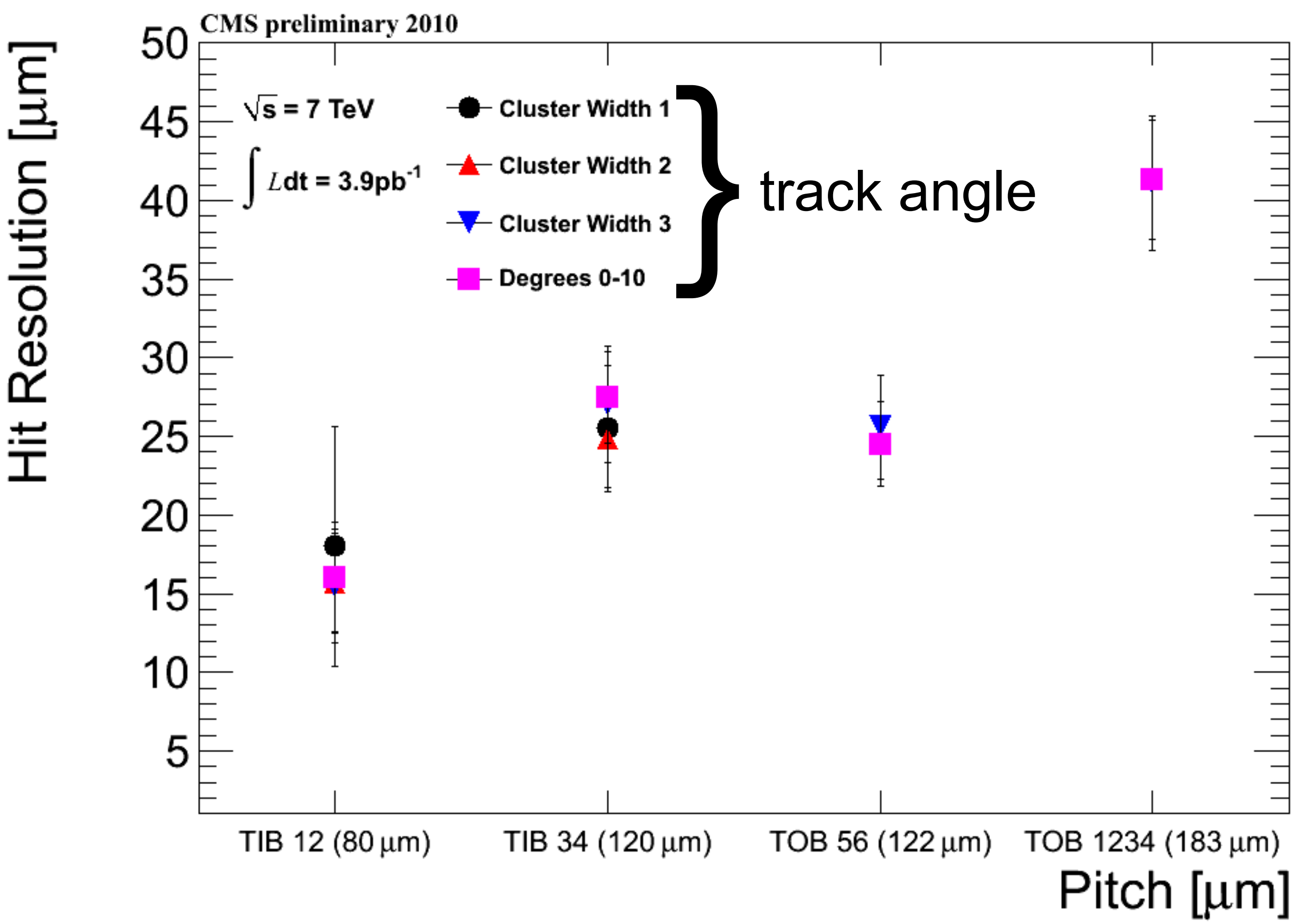




Performance of the Strips Tracker in Run 1

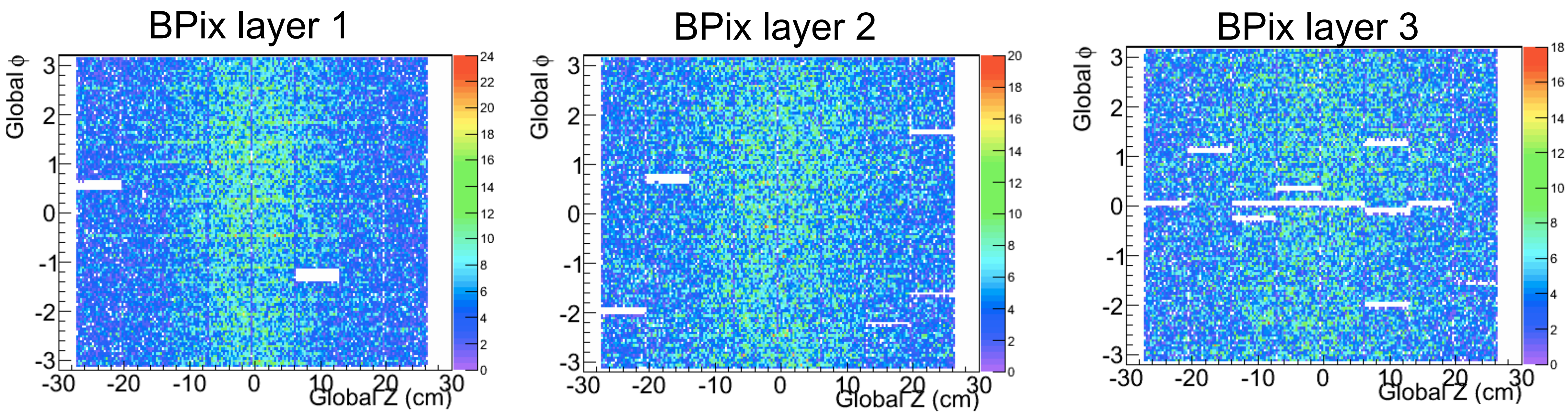
- hit efficiency considering all modules: variations down to 92%
- for good modules: > 99%



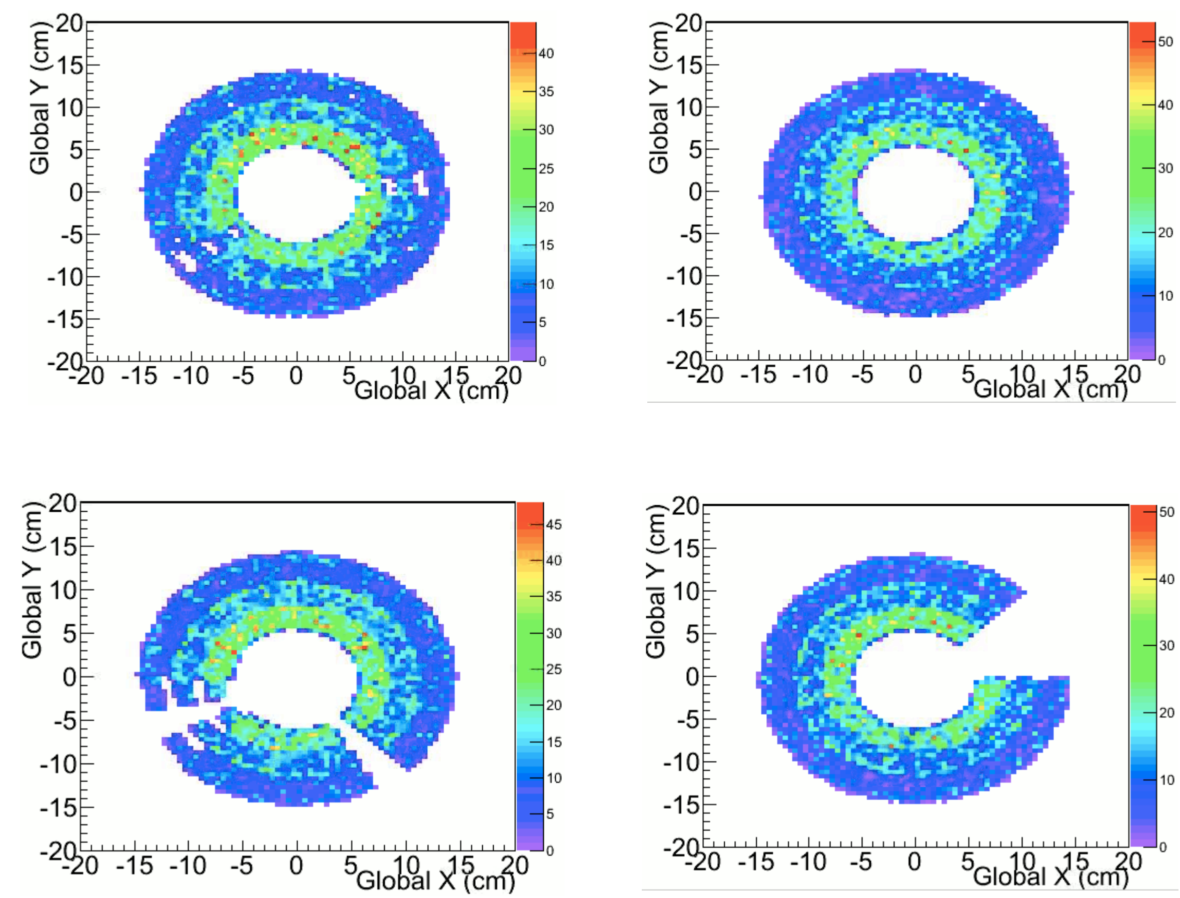


- hit resolution: 16-42 μm depending on pitch

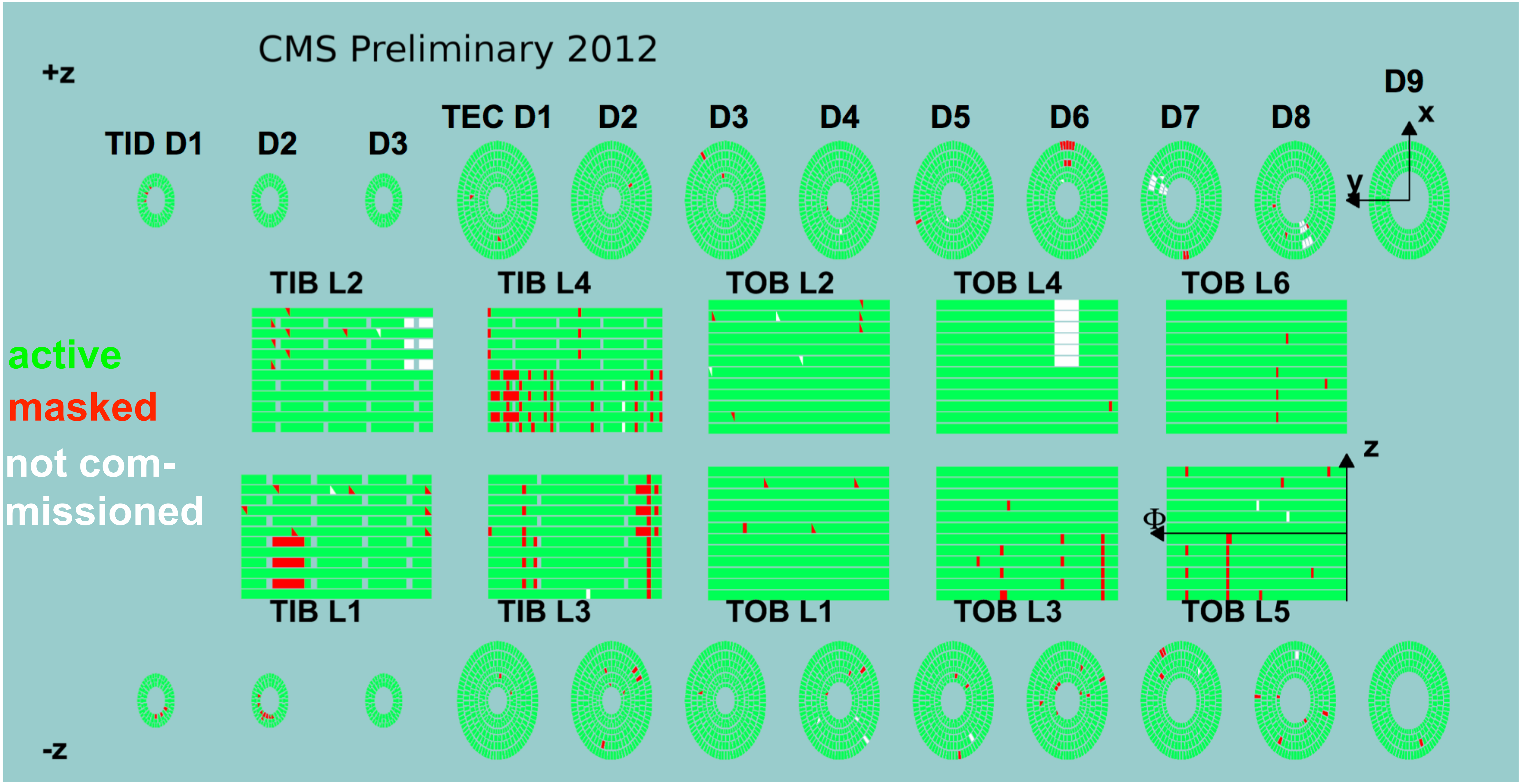
Status of Pixel Detector after Run 1



- BPix: ~2.3% of all channels not operational:
  - broken wirebond connections between ROC and HDI, and laser and AOH
  - modules with old ROC design
- FPix: ~7.8% non-operational:
  - slow channels: long rise time in analog readout, pixel address misreading, miscounting of ROCs and events
  - broken optical readout



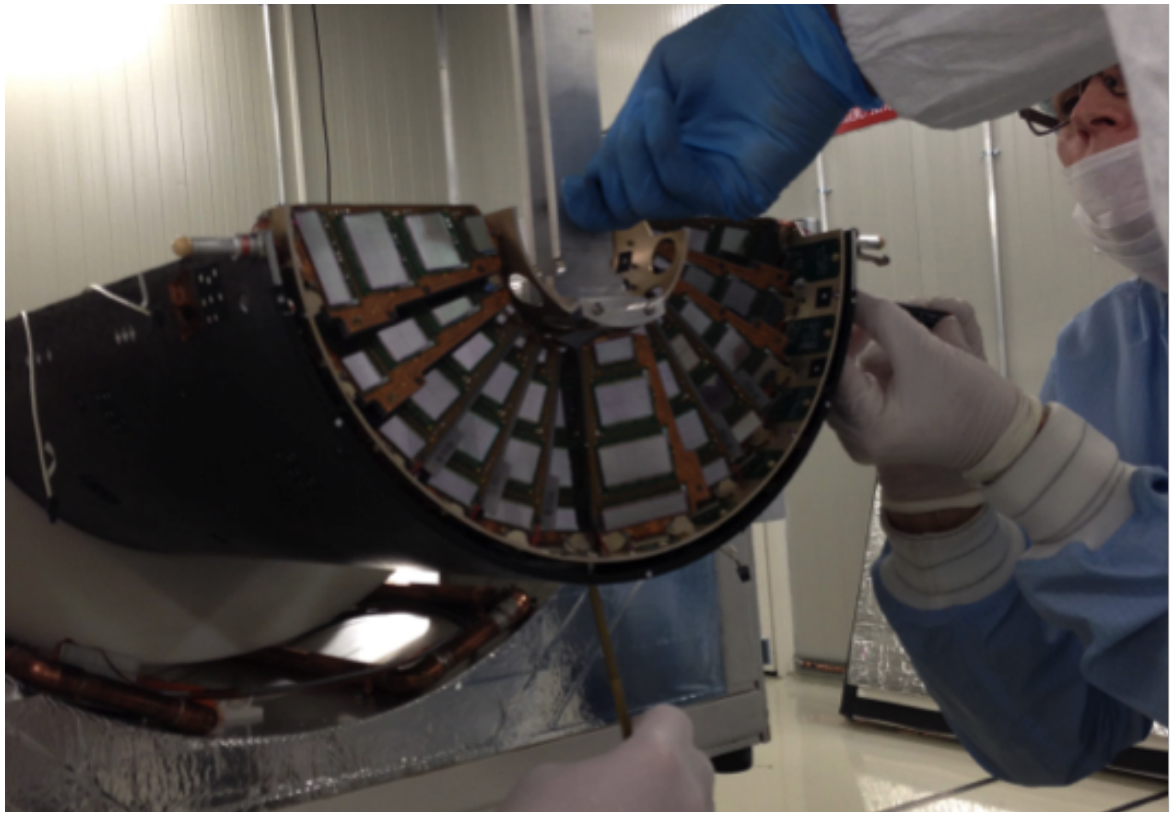
Status of Strips Tracker after Run 1

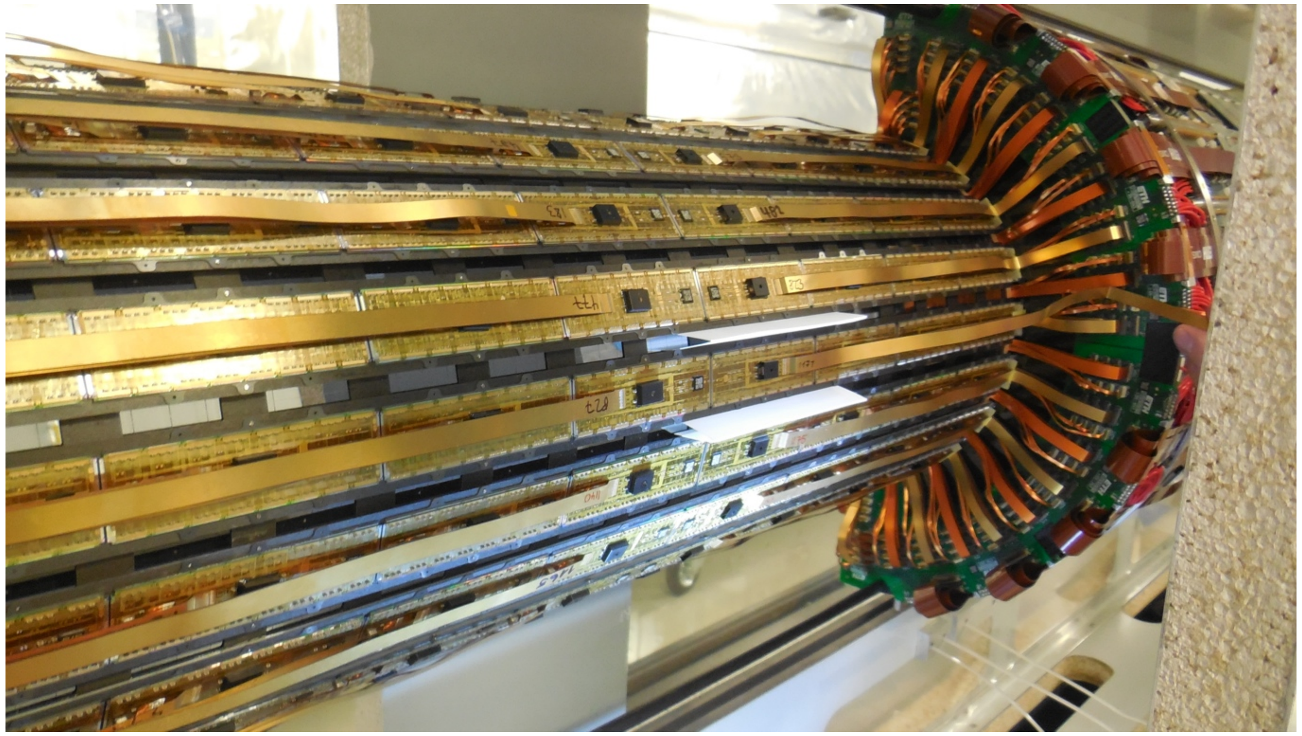


- 2.4% of strips tracker not active:
  - control ring shorts/missing, HV line shorts/open, fibres…

Repair of Pixel Detector on Surface

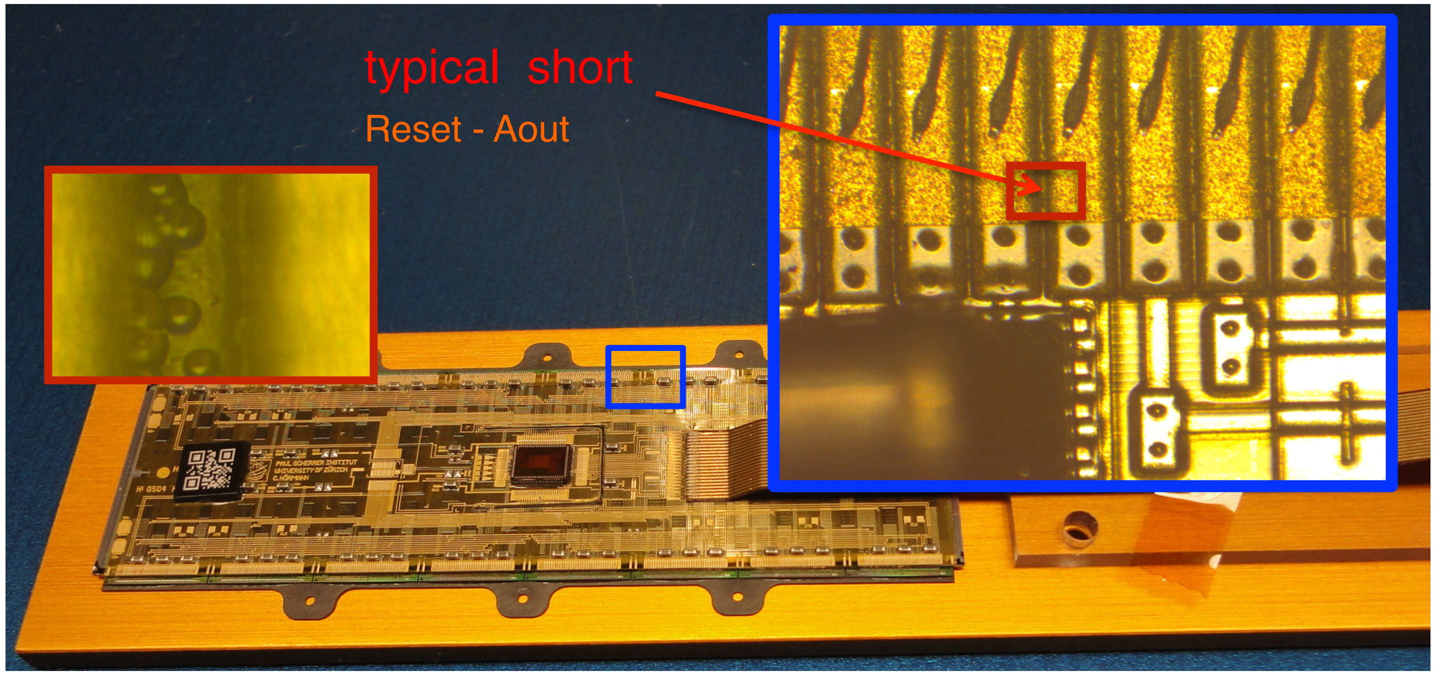
- pixel detector extracted from CMS in summer 2013
- FPix: 99.9% operational after repairs, issues fixed:
  - misaligned flex cables (46% of faulty channels)
  - unplugged analog electrical-to-optical converters (AOHs) - 40% of faulty channels
  - problematic panels (14%)
- BPix: replace only layer 3 outer shell (52% of faulty channels)
  - other layers and inner shell of layer 3 considered too risky to touch
  - 2 not fully operational AOHs replaced (so far workaround allowed data taking)
  - about 99% operational

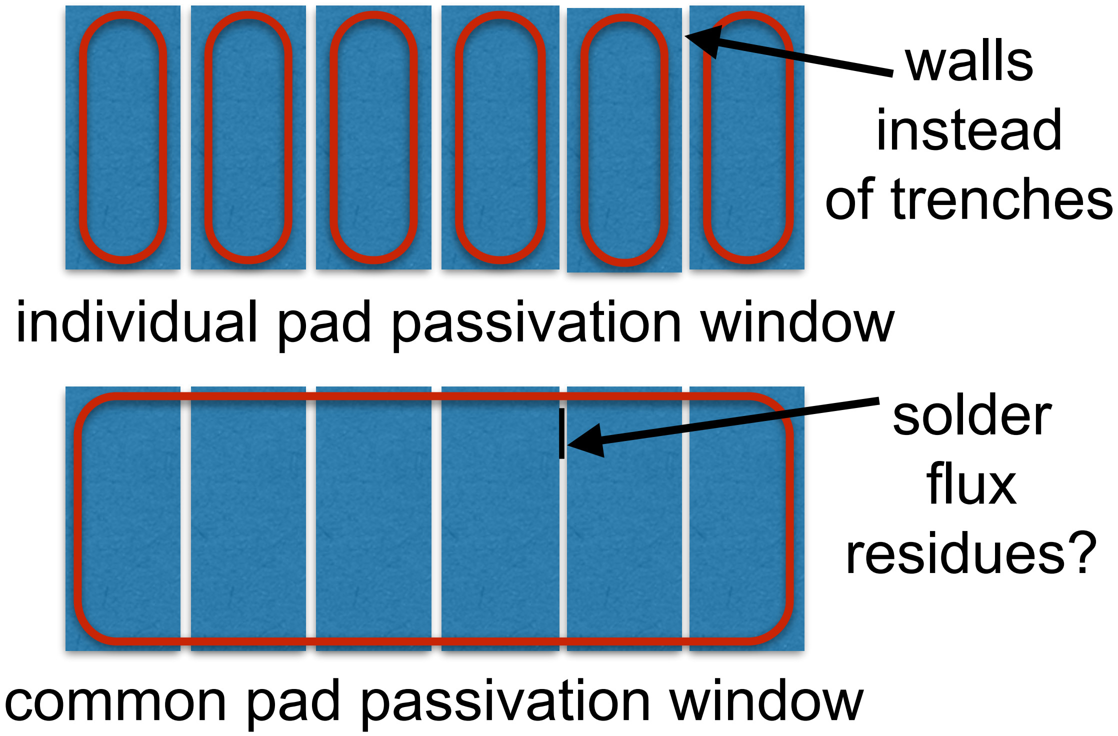




Barrel Pixel Detector Quadrant Failure

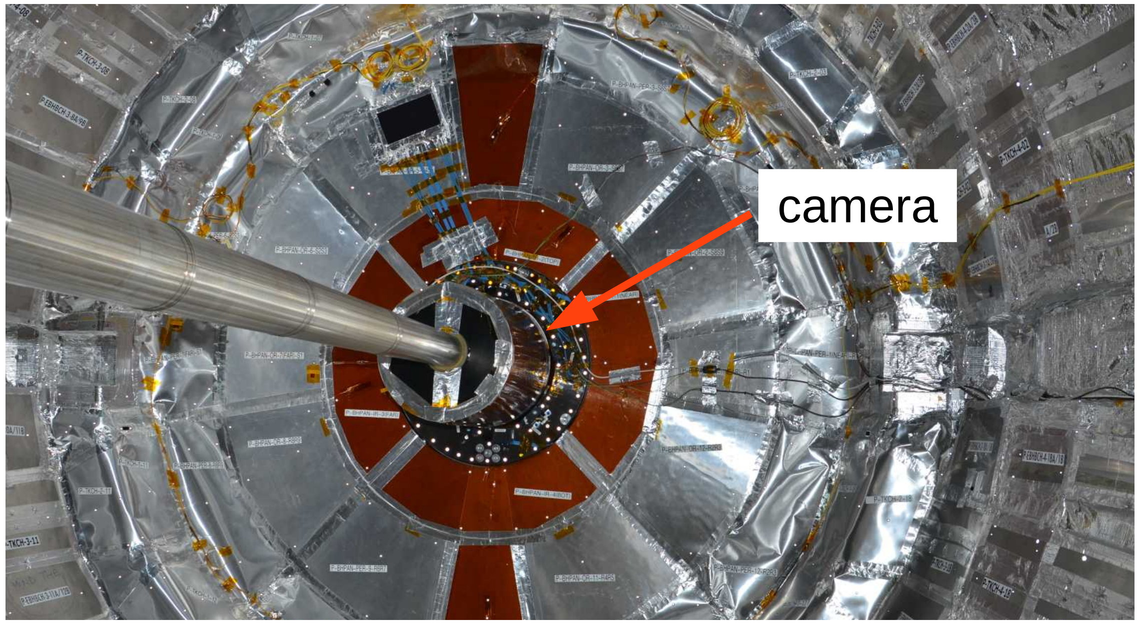
- in mid-August 2014, after having repaired a BPix module, tests of a quadrant show serious damage ➜ 55 modules not working anymore
- shorts found at ROC between two pins (mostly close to SMD components)
- multiple shorted modules also TBM pads and cable pads
- shorts suspected to be caused by humidity due to condensation in cooling box
- detector repaired (40 new modules, 19 repaired) at PSI within 3 months thanks to availability of spare components, expertise, and good manufacturer relations

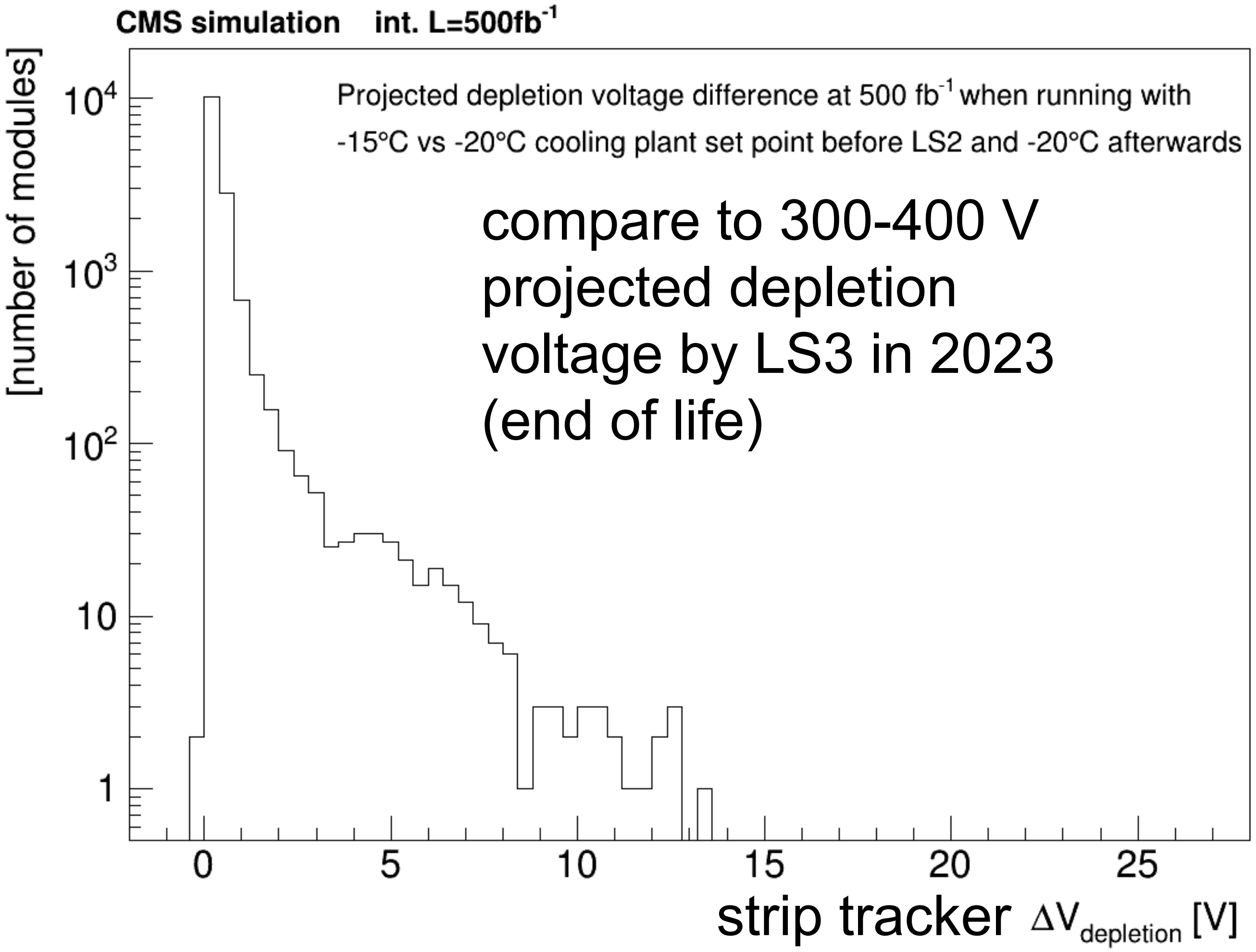




Operating at design temperatures

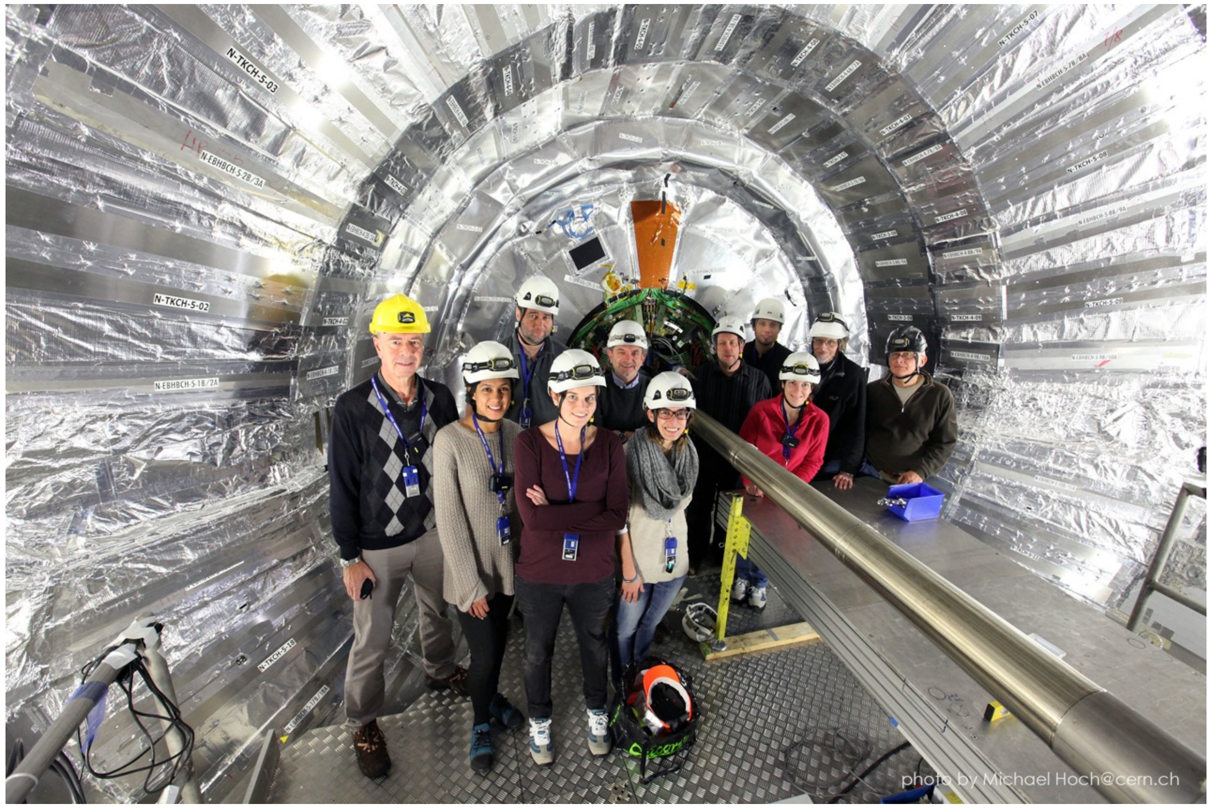
- tracking detectors were designed to operate at low temperatures from the beginning (-20°C for pixel)
  - reduce sensor leakage currents (~50% lower every 8°C)
  - prevent reverse annealing (would require too high depletion voltage at some point)
- dew points in tracker bulkhead and service channels not low enough
  - imperfect sealing
- long shutdown (LS) 1 used to improve sealing, insulation, C_6F_{14} cooling and dry gas plants
- could now run at -20°C
- decision to run at -15°C (-10°C for pixels) - safe until LS2 in 2018 ($\mathscr{L}$ ~ 150 fb^{-1})

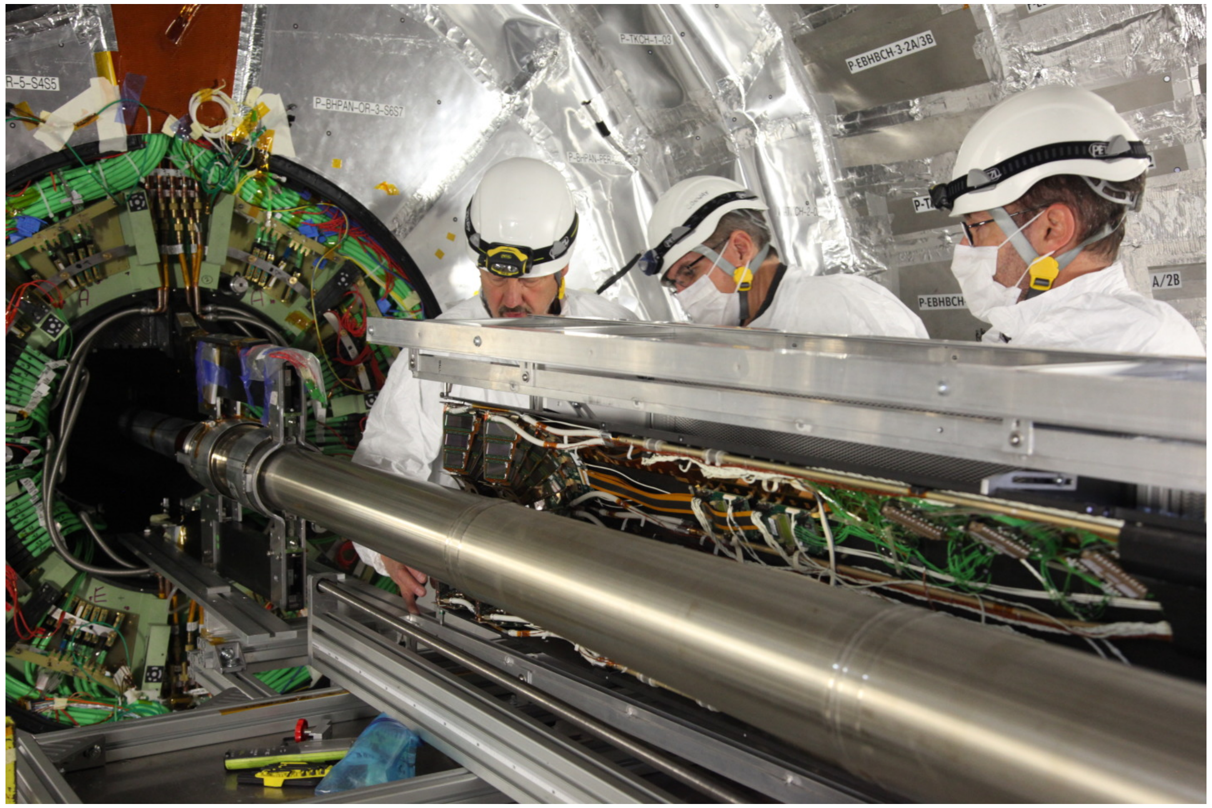




Re-insertion of the Pixel Detector

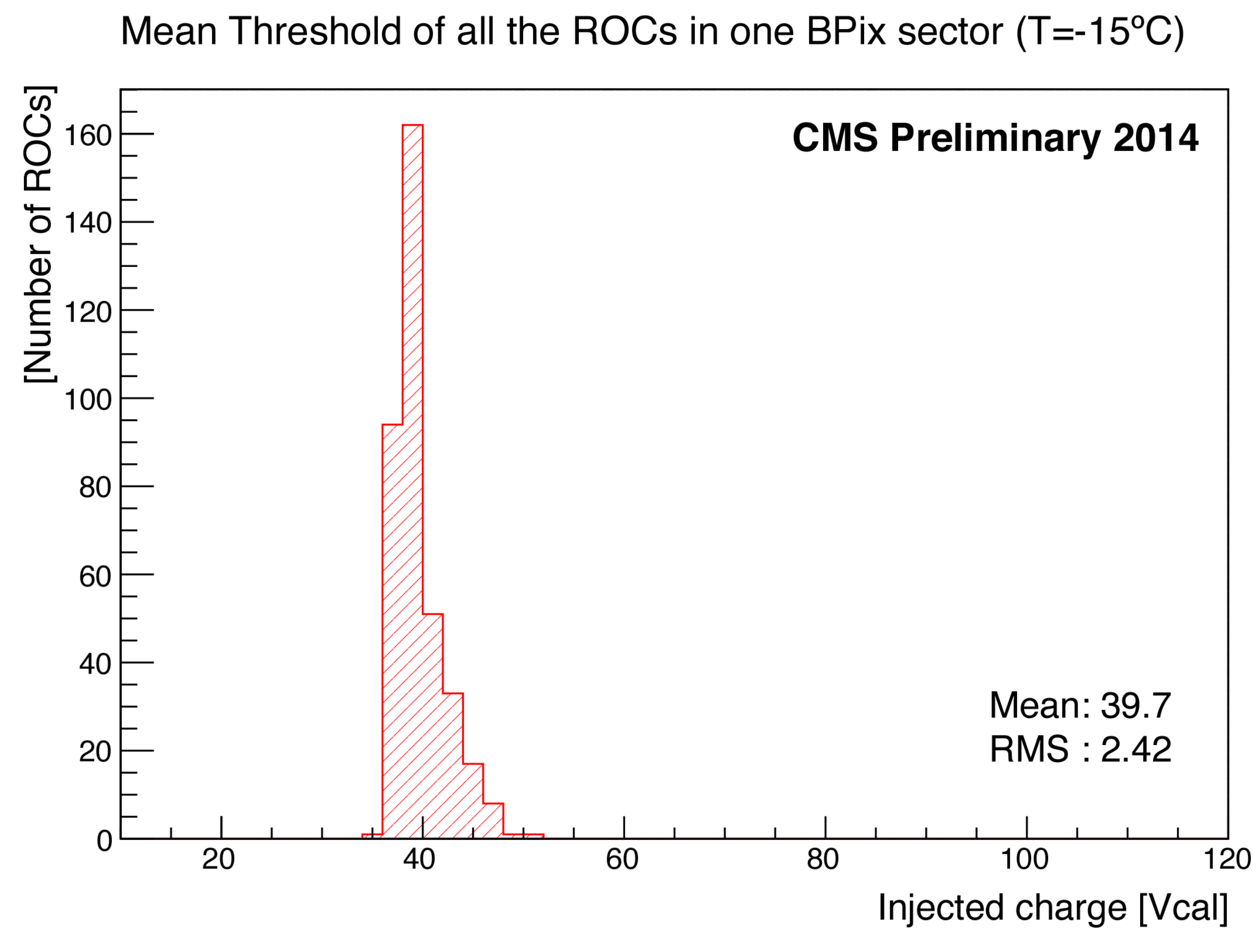
- BPix installed into CMS on 8th December 2014 (3 months later than planned)
  - centered w.r.t. new beampipe
- one day later:
  - cooling loops connected
  - Power cables + fibers connected
  - first attempt to power on and check one sector the same day
- 3 days for detector checkout at +16°C
- FPix installation on 13th December
- similar procedure as for BPix
- pilot system for Phase 1 upgrade installed (see B. Akgun's talk)
- most work finished before Christmas





Re-commissioning of the Pixel Detector

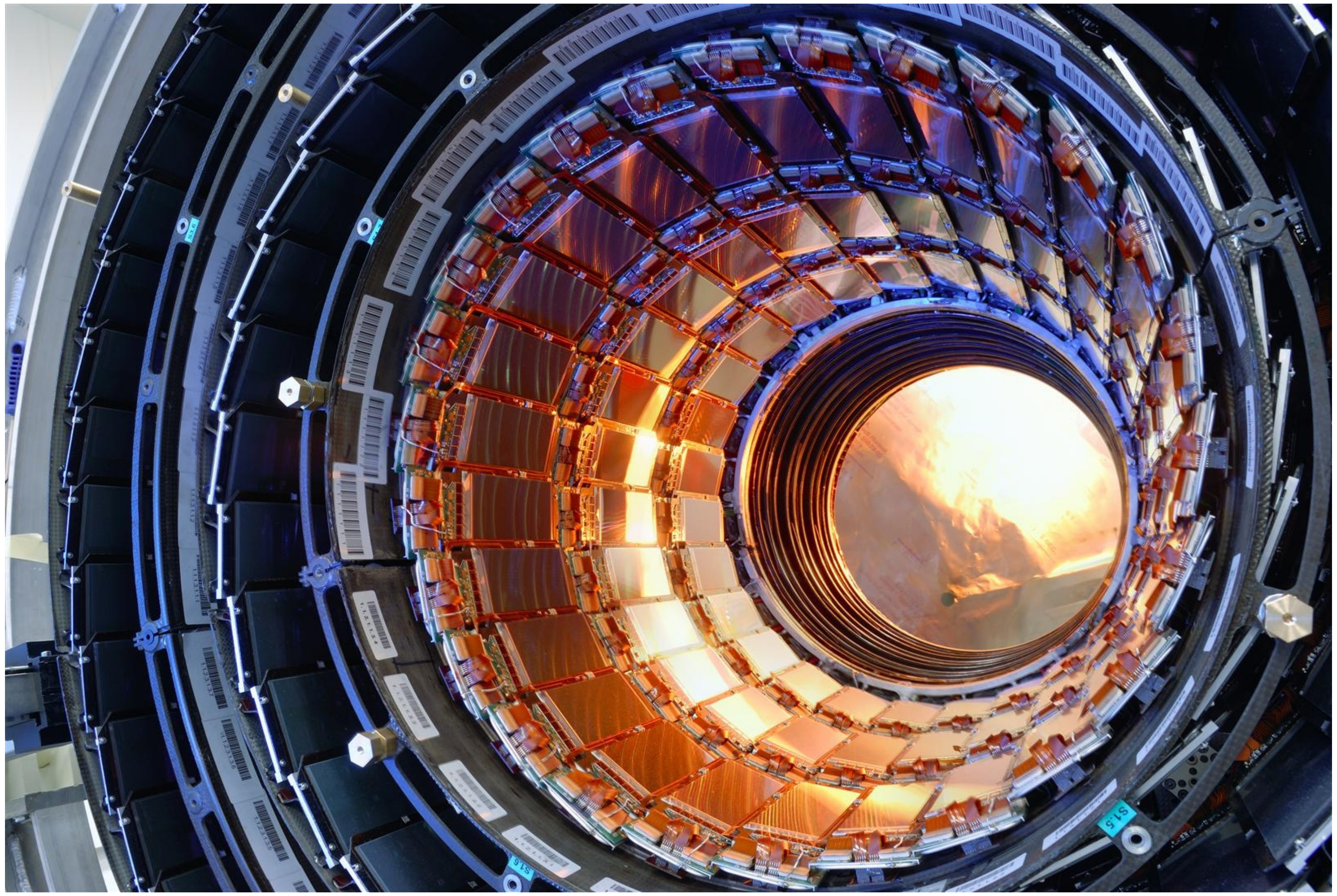
- pixel detector was re-commissioned in January 2015 within ~2 weeks
  - exercised and improved during LS1
  - basic set of calibrations
  - analog voltage for ROC (Vana) calibration
  - pixel comparator threshold calibration
  - pulse height optimisation
  - gain calibration
- switch to new trigger and timing control system
- tracker bulkheads closed on 29th January
- BPix: ~1% disabled channels
- FPix: 0.04% dead channels



Vcal: digital-to-analog amplitude unit corresponding to about 65.5 electrons (offset -414 electrons)

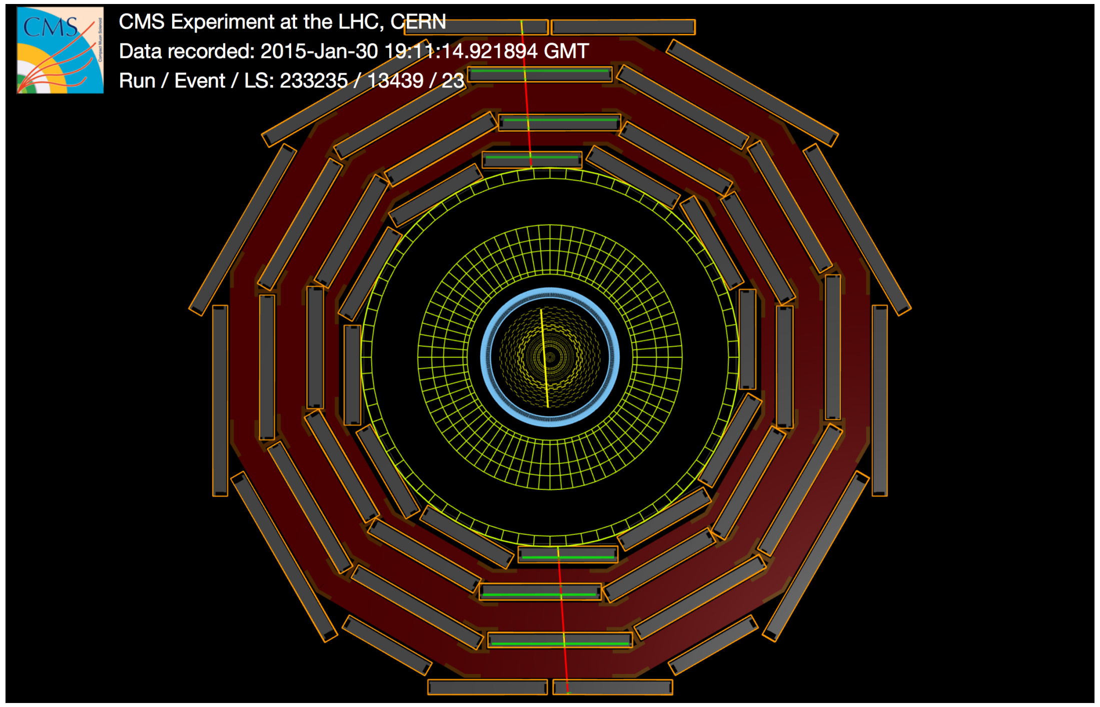
Re-commissioning of the Strips Tracker

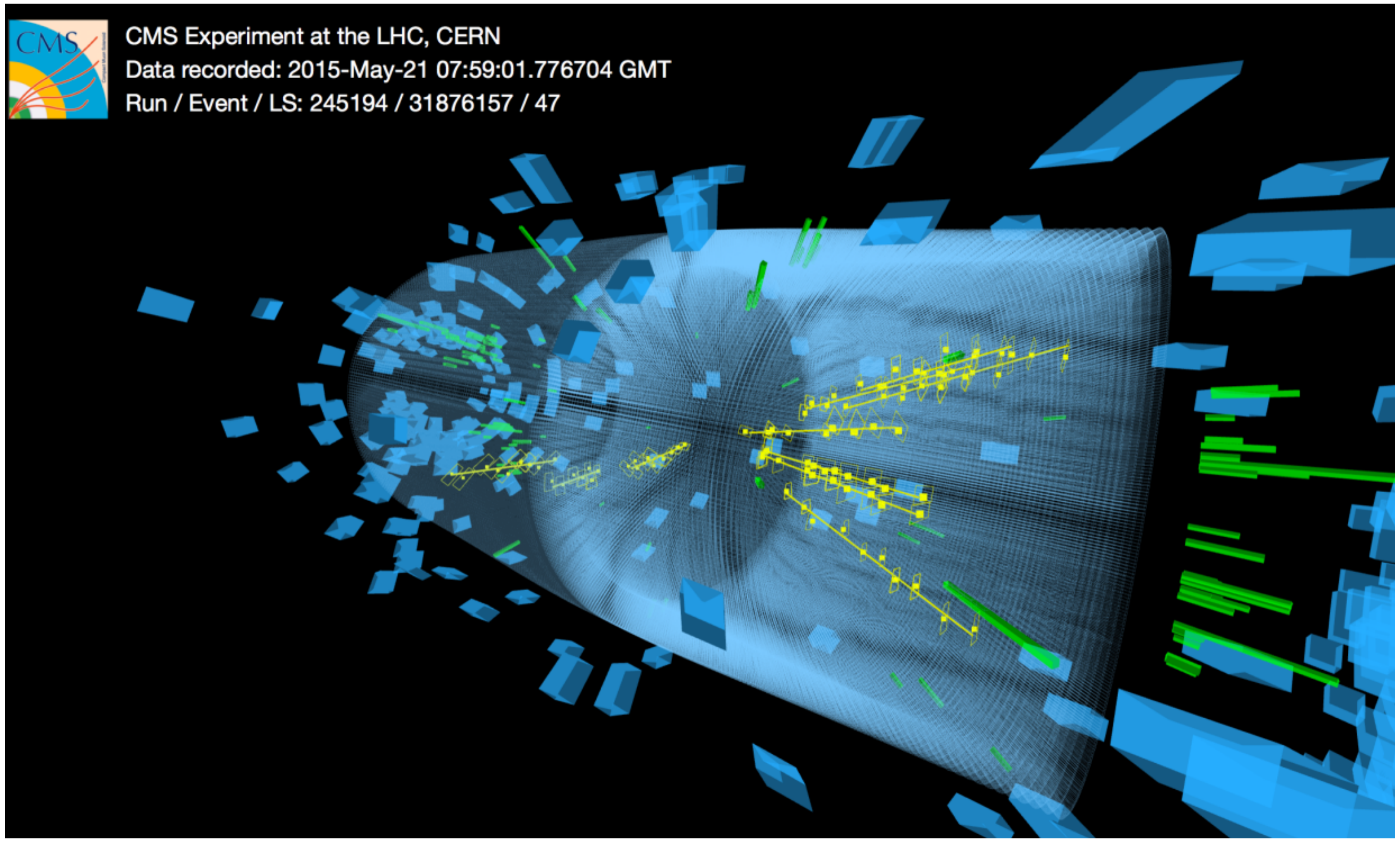
- a lot of work went into establishing the cooling system
- no repairs during LS1, 97.5% of modules operational at beginning of Run 2
- new software to commission detector
- new computing infrastructure, several software and firmware upgrades
- successfully commissioned and operating smoothly



Data-taking in 2015

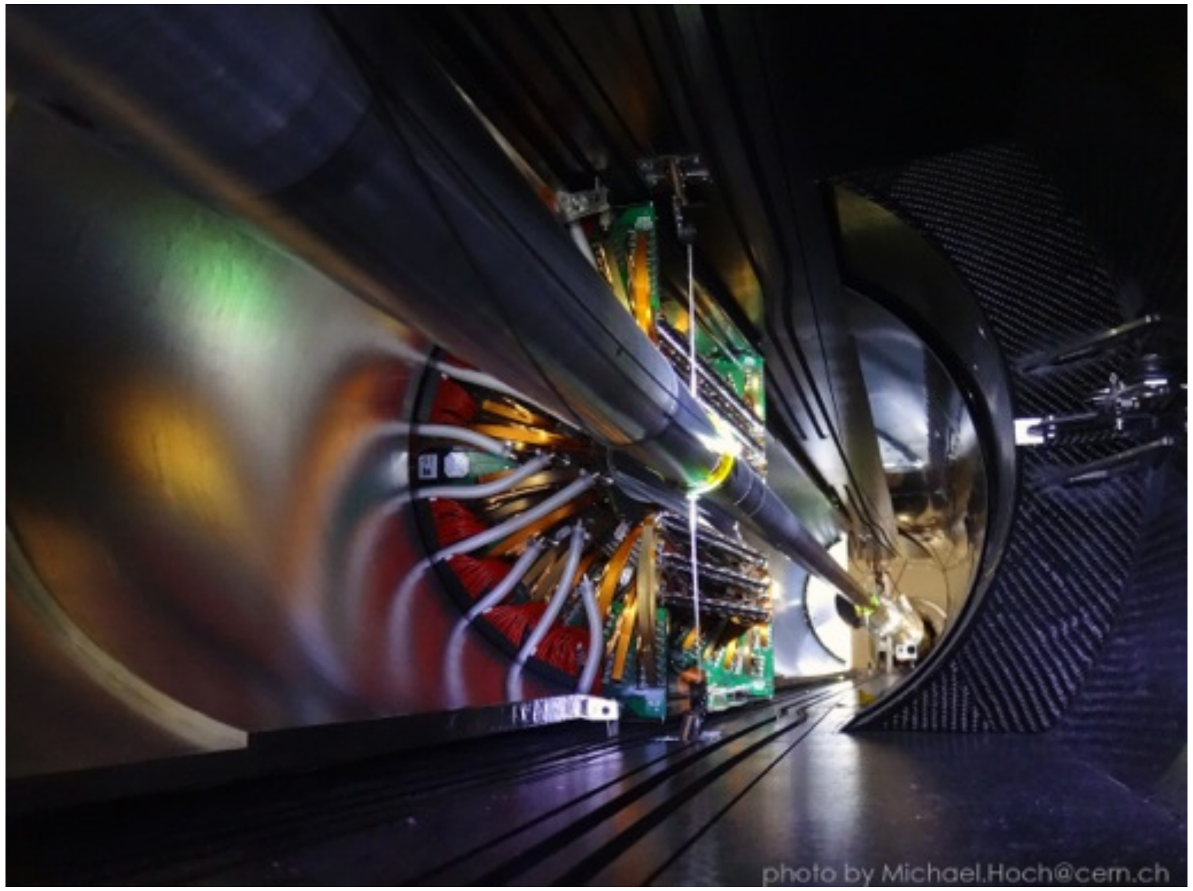
- CRUZET (Cosmic RUn at ZEro Tesla) started on 10th February
  - timing scans (internal and with respect to global)
  - noisy pixels masked (< 0.1%)
  - 420 hours of cosmics recorded
- CRAFT (Cosmic Run At Four Tesla) started on 19th March
  - recorded 3 million cosmics events (1.8 million tracks)
- 20th May: first LHC test collisions at 13 TeV centre-of-mass energy
  - pixel detector off since beams not declared as stable
  - strips tracker taking data





Conclusions and summary

- first long shutdown of LHC lies behind us
- time has been used
  - to repair the pixel detector to 99% operationality
  - to significantly improve cooling of tracking detectors
  - and for several other things…
- both pixel detector and strips tracker are ready for the challenges of LHC Run 2



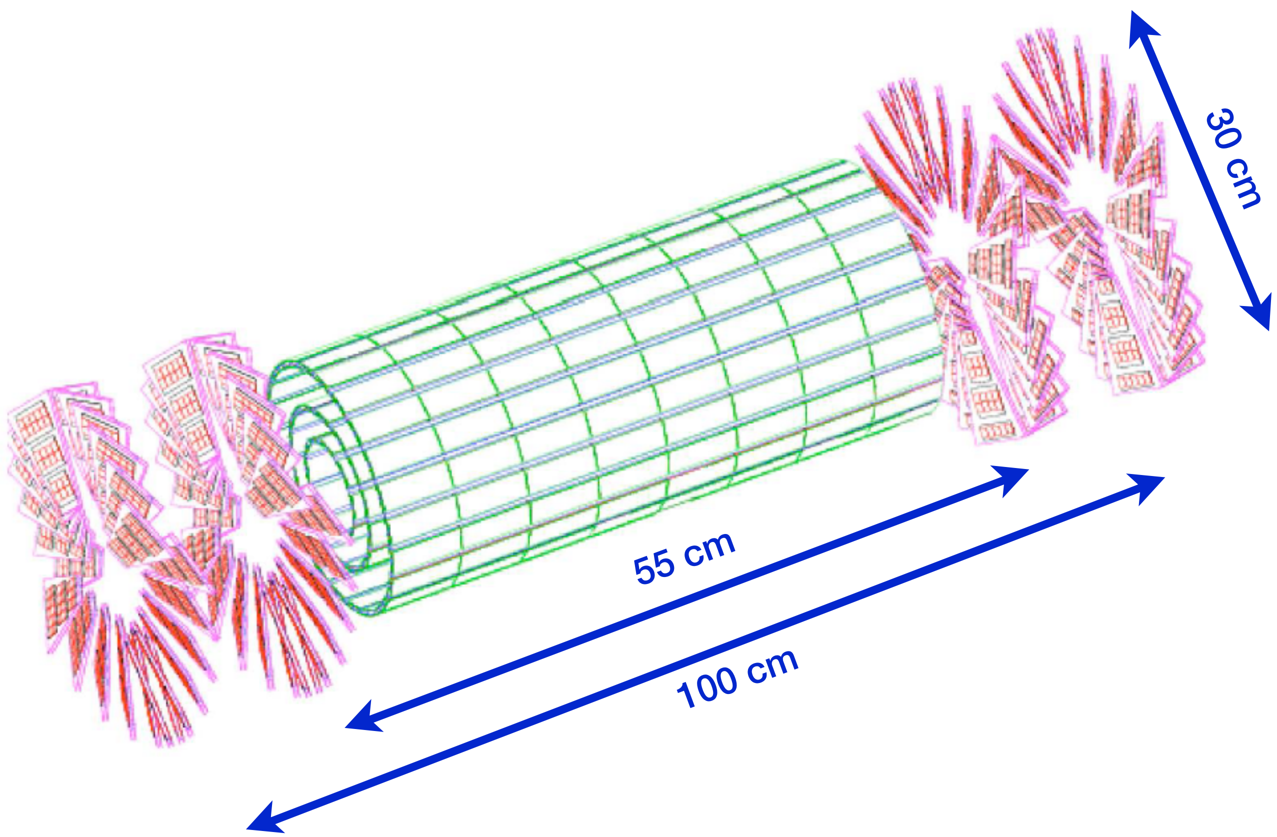
backup

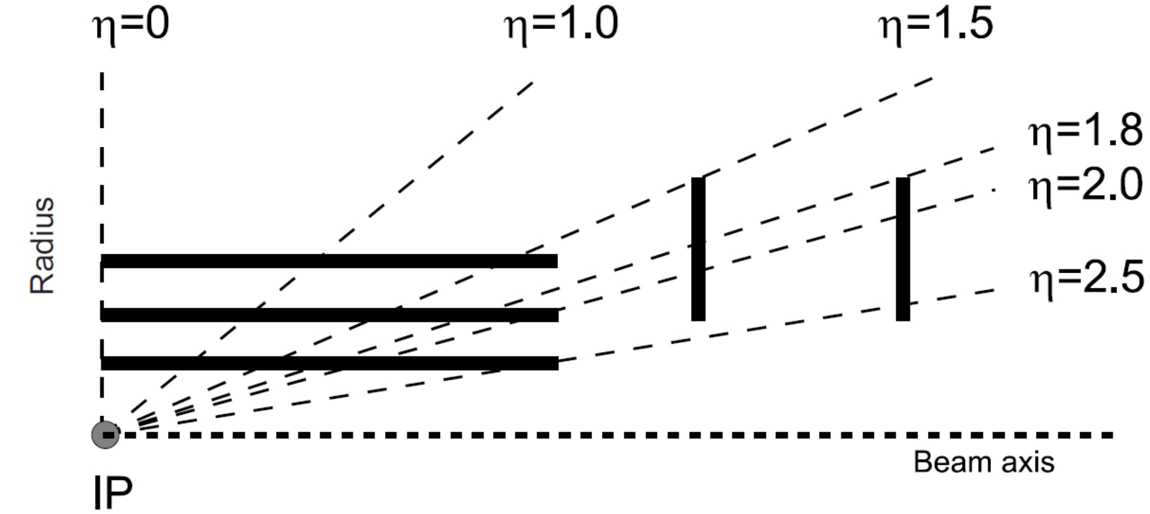
additional information

CMS Pixel Detector

<u>design requirements:</u>

- position resolution in rϕ < 15 μm
- ~3 hits for central part of CMS detector
- time resolution < 25 ns
- hit detection efficiency > 97%



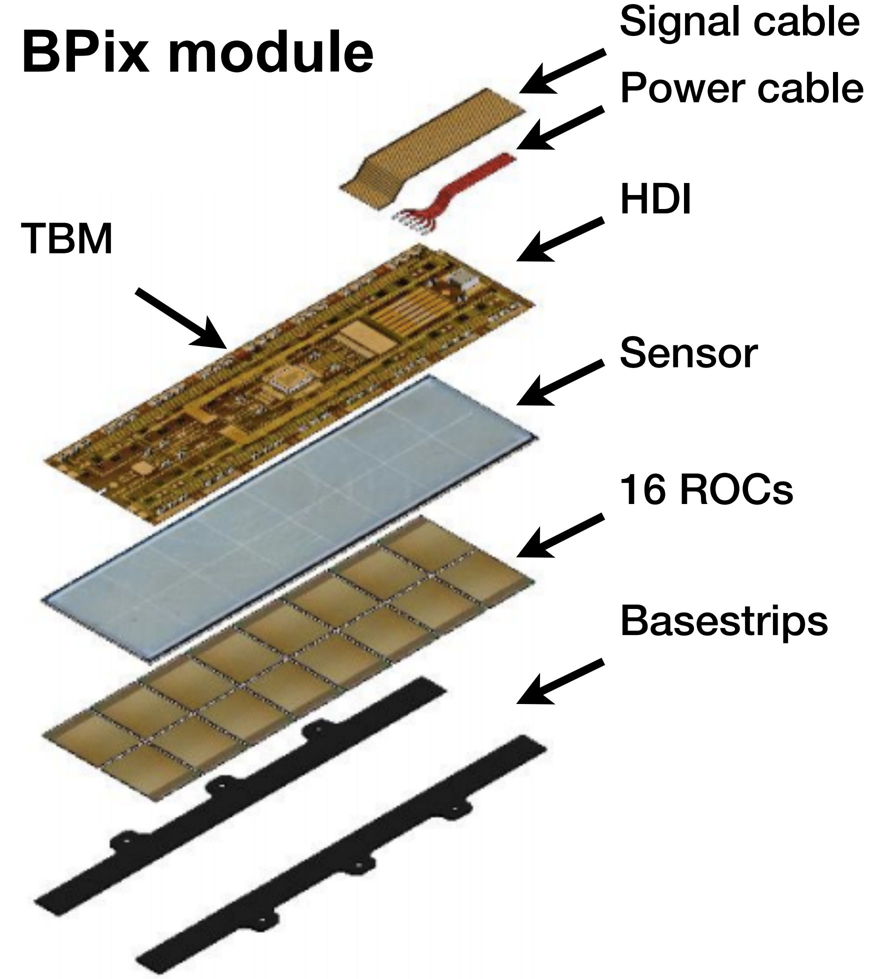


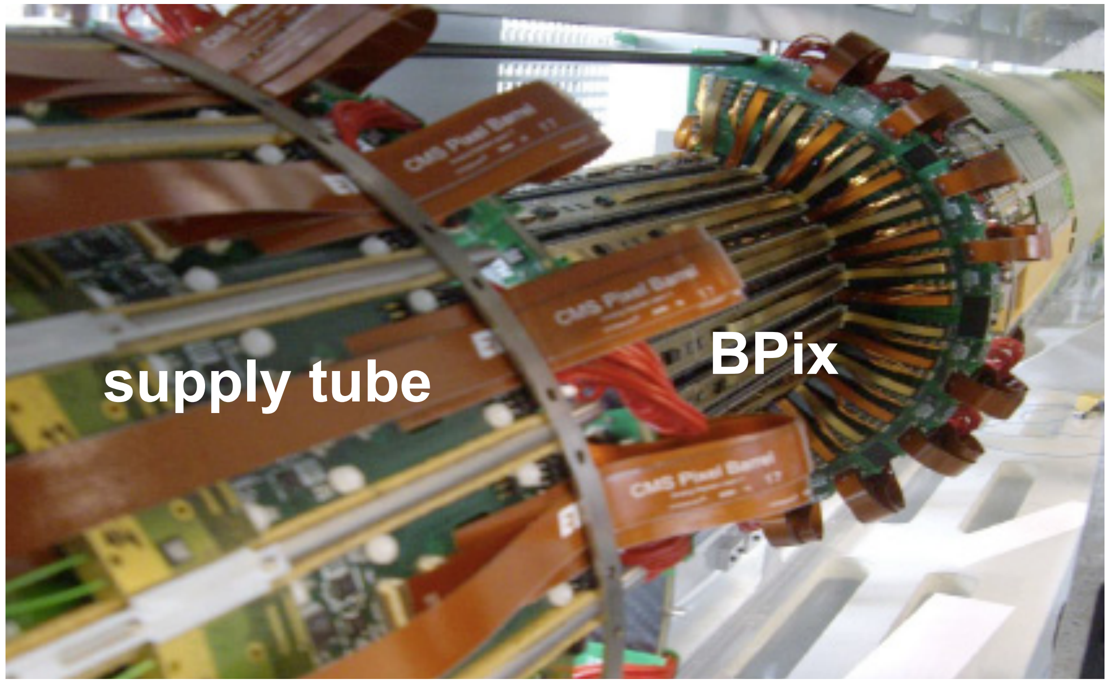
<u>basic properties:</u>

- 3 barrel layers (BPix)
  - radii of 4.3, 7.2, and 11 cm
  - 48 million pixels, area of 0.78 m^2
- 2 endcap pixel disks at each side (FPix)
  - longitudinal distance from centre of detector: $|z|$ = 34.5 and 46.5 cm
  - 18 million pixels, area of 0.28 m^2
- 3 hit system for $|\eta| < 2.1$ (2 hits up to $|\eta| < 2.5$)

CMS Pixel Modules

- BPix: 768 modules (672 full, 96 half modules), segmented into 11520 readout chips (ROCs)
- FPix: 192 panels, 4320 ROCs
- pixel size: 100 x 150 µm (250 µm sensor thickness)
- 1 ROC serves a 52 x 80 array of pixels
- sensor:
  - n+ implant in n bulk
  - bump-bonded to ROCs
- Token Bit Manager (TBM) located on High Density Interconnect (HDI)
  - distributes clock and trigger to ROCs
  - manages ROC controls and readout
- Analog Opto-Hybrids (AOH), cooling, power, readout boards etc. on supply tube

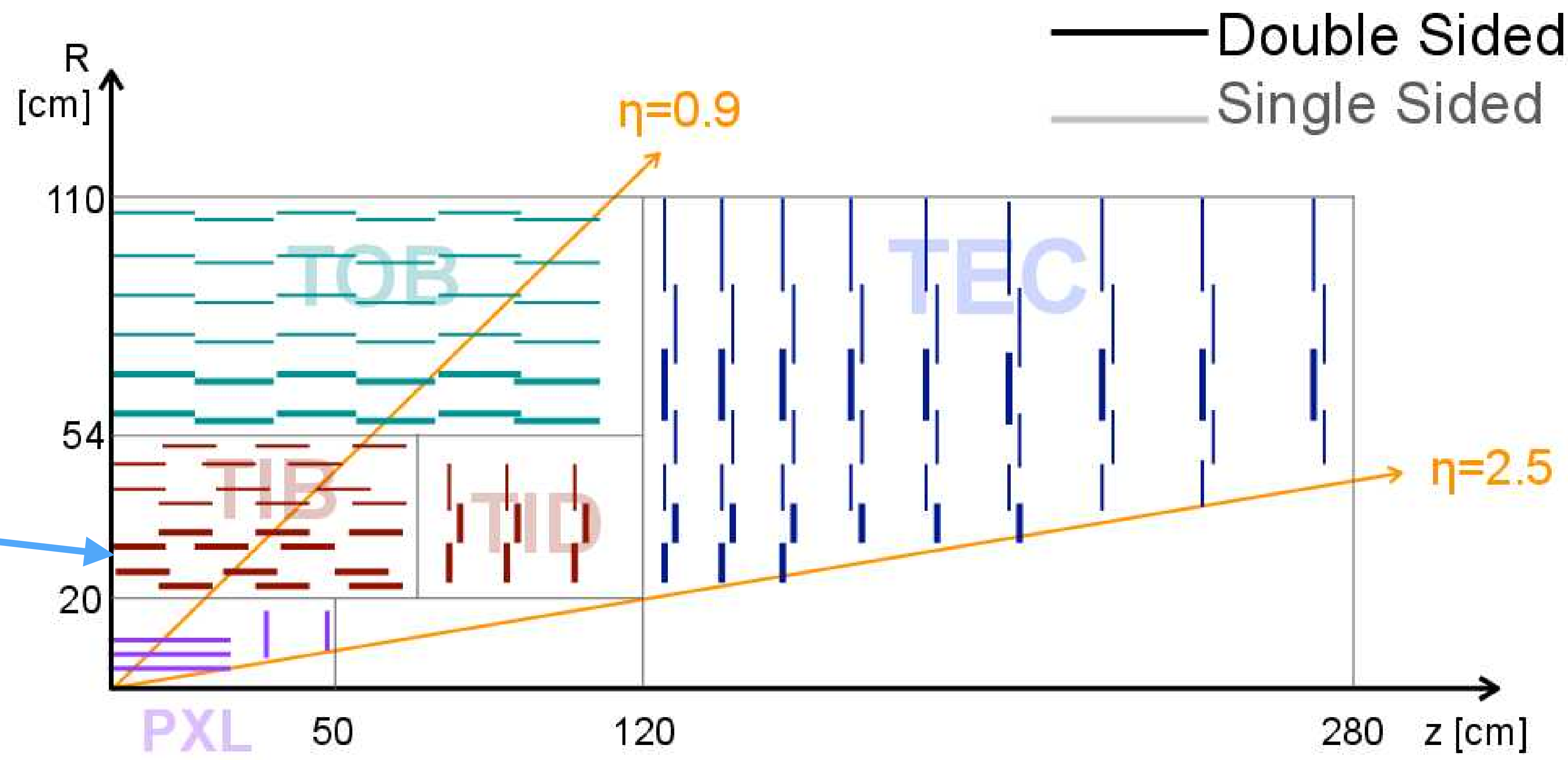




CMS Silicon Strip Tracker

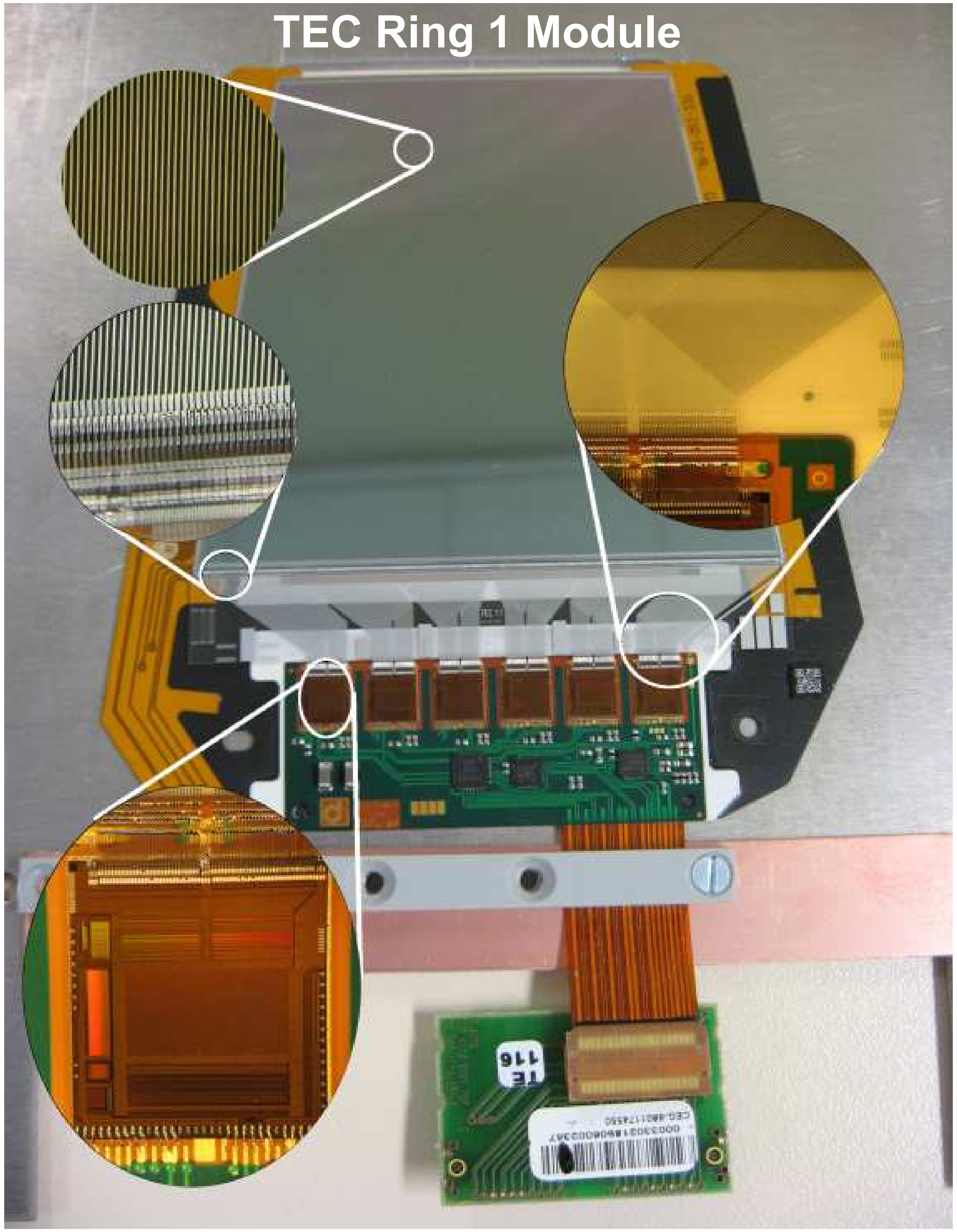
- 10 layers in barrel region
  - 4 Inner Barrel (TIB), 6 Outer Barrel (TOB)
- 9+3 discs in the inner disks (TID) and endcaps (TEC)
- largest and first 'all-silicon' central tracker ever built:
  - active area 200 m^2, length: 5 m, diameter: 2.5 m
- ~9.6 million electronic channels

stereo modules (two modules with 150 mrad stereo angle)



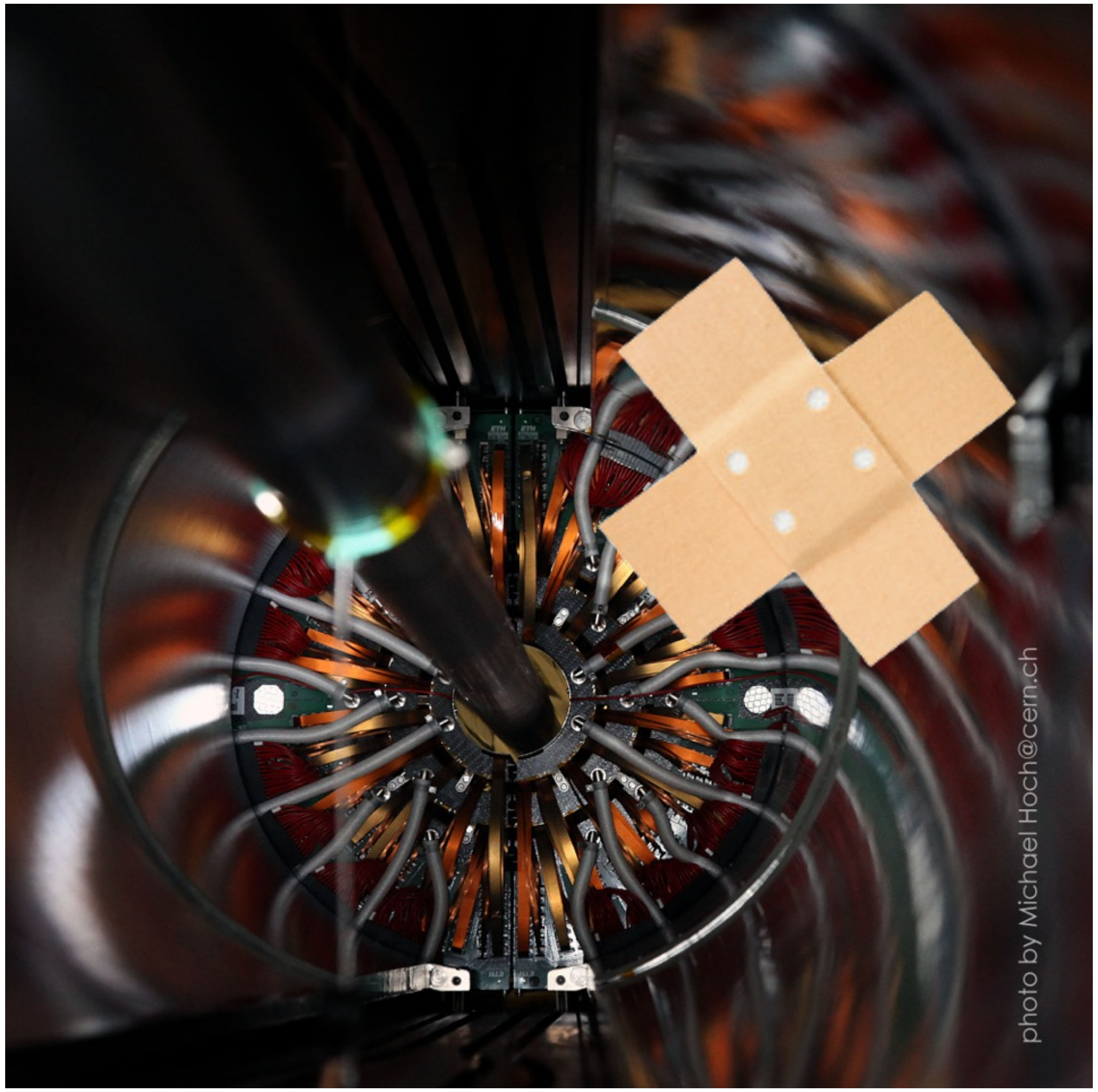
CMS Strip Modules

- p^+-in-n silicon sensors
- 320 µm and 500 µm thick
- 512-768 strips
- strip pitch 83-205 µm
- analog readout: 4-6 APV25 chips with two readout modes:
  - peak: robust timing, low noise, mostly for cosmics
  - deconvolution: fast (shorter signal), more noise, mostly for collisions
- electronics on hybrid
- optical links for data transfer



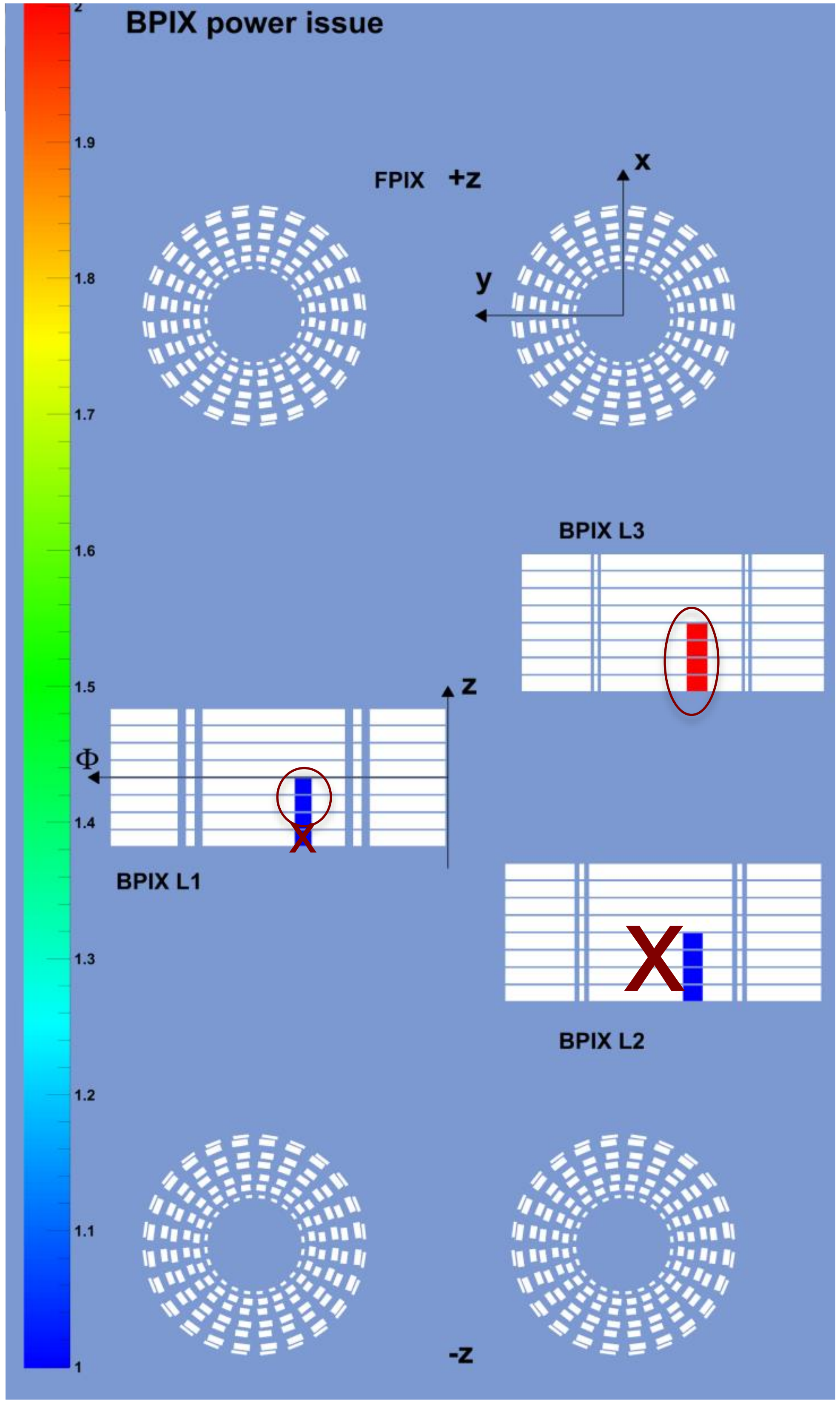
Pixel health (1)

- BPix: 88 permanently disabled ROCs, namely
  - 40 ROCs because of different problems in 4 modules
  - 16 ROCs because of no high-voltage for 2 modules
  - 32 ROCs because of no hits (HV problem) in two modules
  - in total ~1% disabled channels
- FPix: 1 dead ROC, some double columns
  - in total 0.04% dead channels



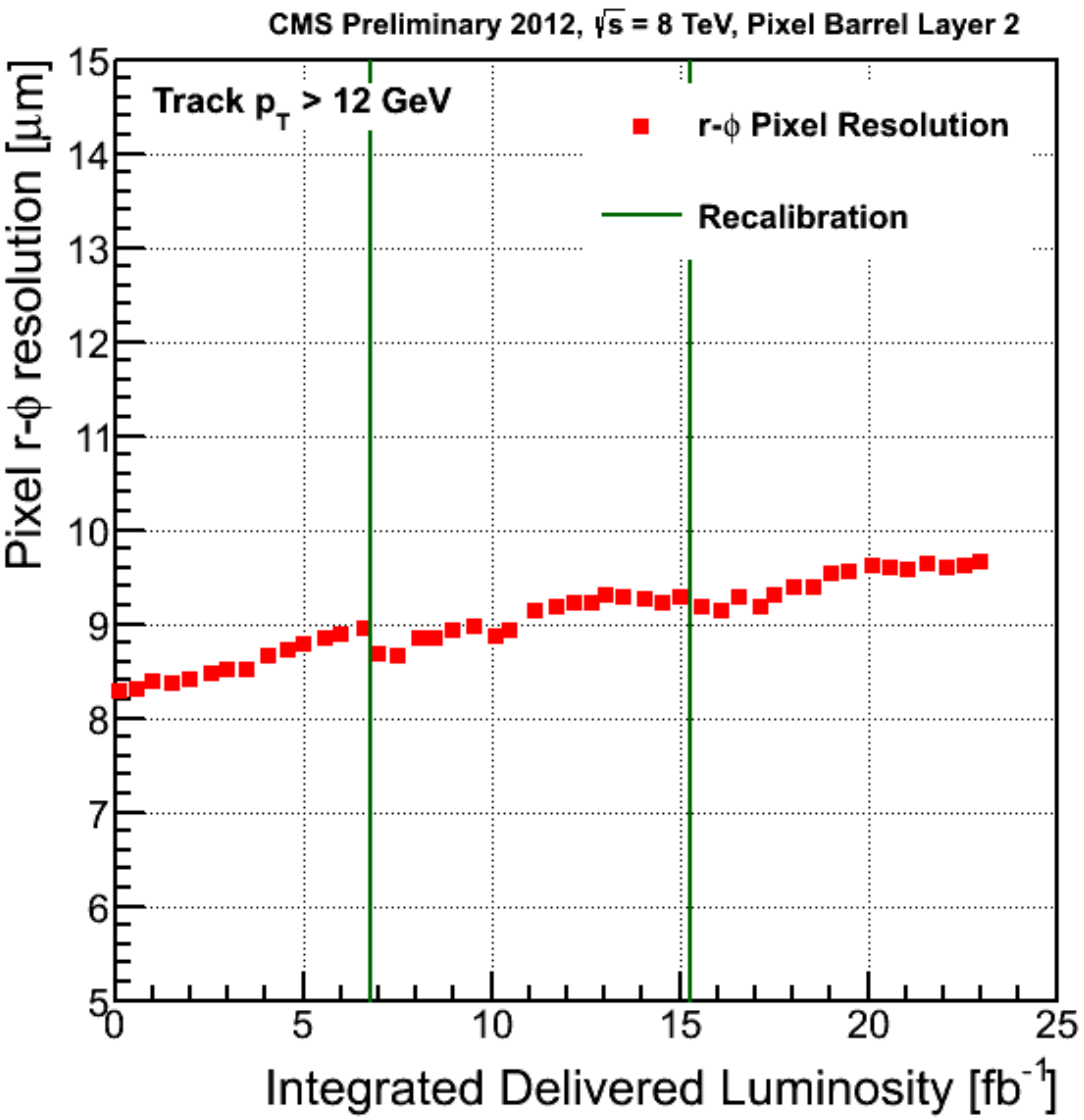
Pixel health (2)

- currently biggest problem: BmO sector 3, layers 1+2 (~1.6% of BPix, ~22.5° in ϕ):
  - configuring front-end leads to under-voltage of control power supply
  - Delay25 gets reset, but not PLL
  - problem only observed in presence of B-field
  - cosmics with magnet were taken with layer 3 powered only
  - several weeks spent investigating the problem, but still no solution found
  - currently best option: full layer 3 (12 modules) + 3 (out of 4) modules of layer 1
  - will also try again to increase current limit for control power supply to prevent under-voltage



Pixel bias voltage increase

- BPix bias voltage increased from 150V to 200V - FPix to remain at 300V
  - loss of position resolution observed in 2012
  - signs of charge trapping/incomplete charge collection
  - disadvantage of smaller Lorentz angle, but still larger than charge sharing pitch

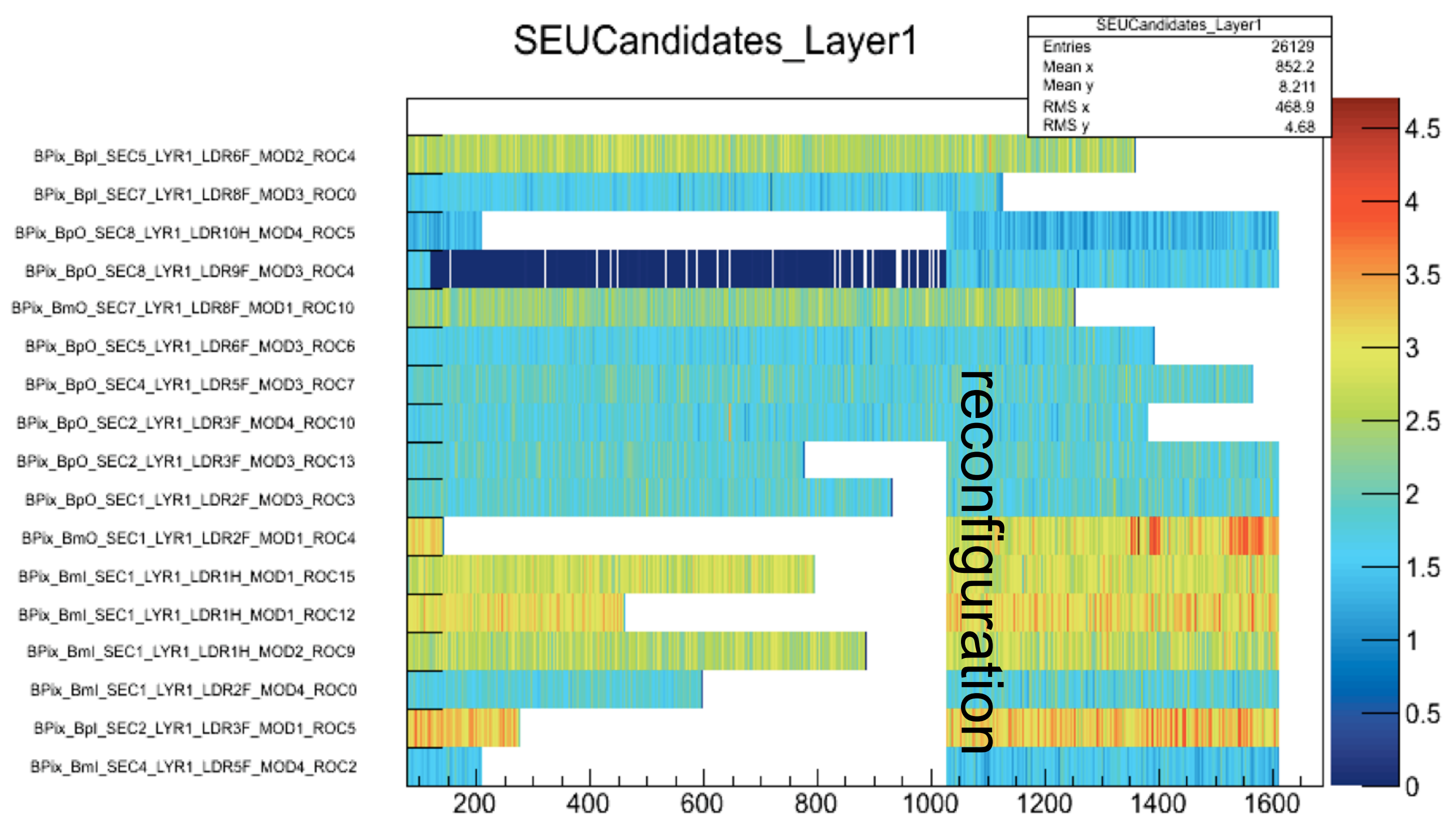


How to deal with high data rates and radiation?

- operate at lower temperature
- upgrade of the DAQ surface links
  - link after the slink, i.e. from the FRL, was changed from Myrinet to 10Gb ethernet
- centring of BPix w.r.t. beam pipe ➜ rates are more equal
- SEU recovery in place
- frequent re-calibrations

Single Event Upsets

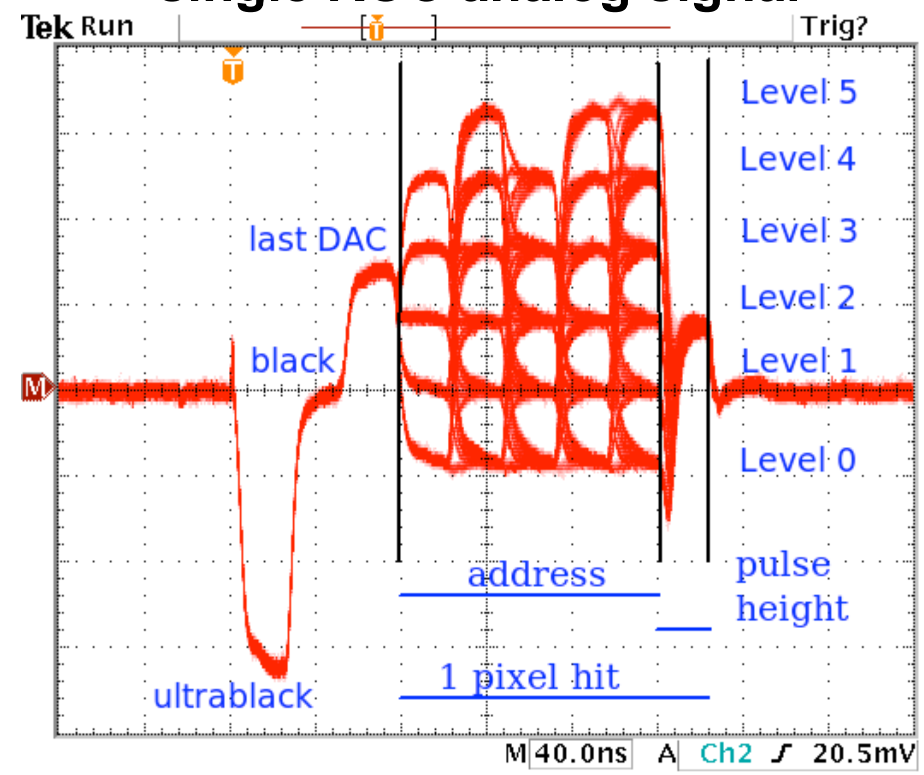
- Single Event Upset (SEUs): bit flip on detector electronics caused by irradiation
  - can affect control registers at different levels: from pixels to auxiliary electronics
  - no action needed if single pixel or ROC affected
  - immediate action taken if SEU stops data-flowing from a full module (>1‰)
  - happens ~every 73 pb^{-1}
- automatic SEU identification and recovery mechanism implemented
  - takes a few seconds (used to take ~3/4 minutes)
  - takes advantage of the recovery triggered by other systems to perform reprogramming



Pixel Detector readout calibration

- Pixel Detector functioning depends on readout chain settings
- optimal settings for readout system parameters must be used
- majority of settings unchanged until:
  - detector temperature changes
  - significant amount of radiation is accumulated
- for parameters more sensitive to environmental changes, recalibration performed on regular basis:
  - Front-End Driver(FED) opto-receiver offset adjustment (weekly)
  - set the signal baseline in the middle of ADC range
- address level calibration (monthly):
  - ensure good decoding of pixel address by FED

single ROC analog signal



pixel address level distribution