Contribution ID: **76** Type: **not specified**

ATLAS FTK: Fast Track Trigger

An overview of the ATLAS Fast Tracker processor is presented, reporting the design of the system, its expected performance, and the integration status. The next LHC runs, with a significant increase in instantaneous luminosity, will provide a big challenge to the trigger and data acquisition systems of all the experiments. An intensive use of the tracking information at the trigger level will be important to keep high efficiency in interesting events, despite the increase in multiple p-p collisions per bunch crossing (pile-up). In order to increase the use of tracks within the High Level Trigger (HLT), the ATLAS experiment planned the installation of an

hardware processor dedicated to tracking: the Fast TracKer (FTK) processor. The FTK is designed to perform full scan track reconstruction at every Level-1 accept. To achieve this goal, the FTK uses a fully parallel architecture, with algorithms designed to exploit the computing power of custom VLSI chips, the Associative Memory, as well as modern FPGAs. The FTK processor will provide enough computing power to reconstruct tracks with $p_T > 1$ GeV in the whole tracking volume. The tracks will be available at the beginning of all the trigger selections, allowing to develop new more pileup resilient strategies. The FTK system will be installed in 7 racks of high density electronics, with about 8000 AM chips and 2000 FPGAs, providing full tracking with an event rate of up to 100 KHz and an average latency of 100 μs. Preliminary studies on tracking and trigger performance will be presented, showing the overall tracking performance and the potential benefits in the selection of τ, b-jets, and primary vertex determination. The status of the final hardware prototypes and the installation schedule will be presented, as well as the possible evolutions for the HL-LHC.

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