VERTEX 2015

24th International Workshop on Vertex Detectors

BELLE II Pixel Detector

INSTITUTO DE FÍSICA CORPUSCULAR

Marçá Boronat on behalf of the DEPFET coll.

The DEPFET Collaboration.

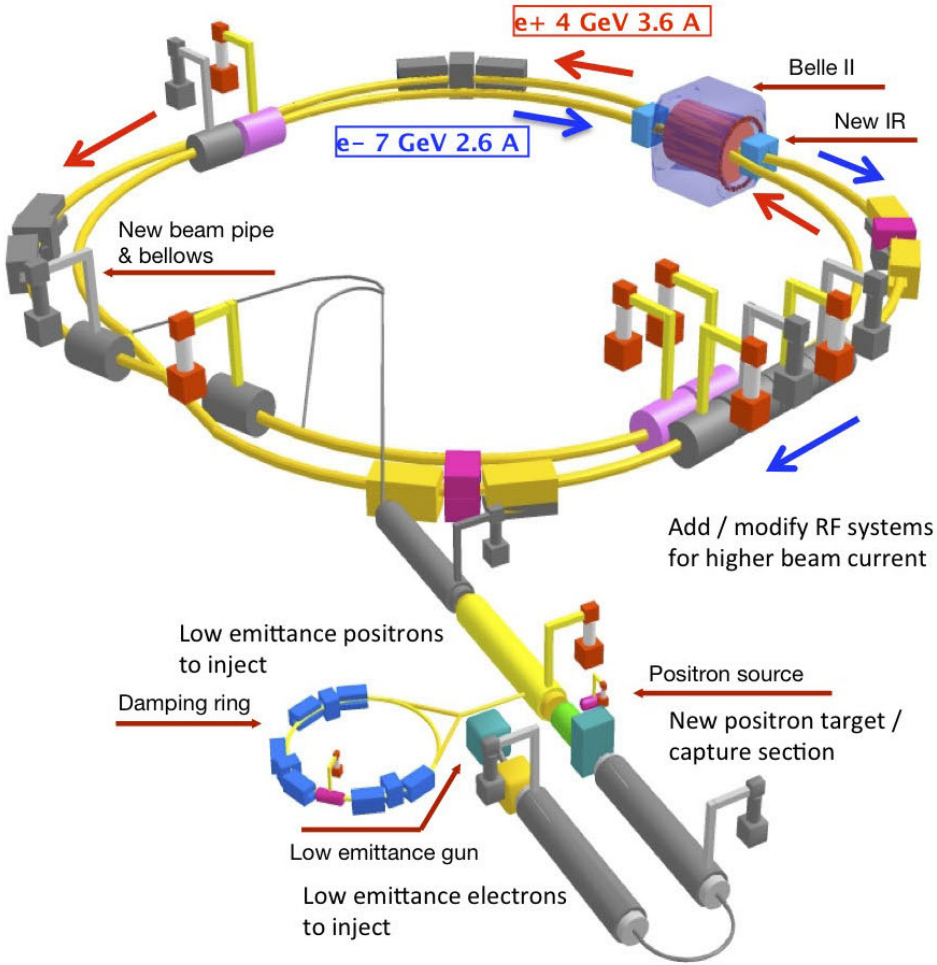
VTX15

- Charles University, Prague
- University of Mainz
- IFJ PAN, Krakow
- IFCA, Santander
- KEK-PF, Tsukuba
- IFIC, Valencia
- DESY, Hamburg
- IHEP, Beijing
- LMU, Munich
- MPI, Munich
- TUM, Munich
- HLL, Munich
- KIT, Karlsruhe
- University of Bonn
- University of Tabuk
- University of Giessen
- University of Göttingen
- University of Barcelona
- University of Heidelberg

Outline

- Belle II PXD
  - SuperKEKB & Belle II
  - Belle II Vertex Tracker
- DEPFET PXD Detector
  - DEPFET - DEpleted P-channel FET
  - Thinning Technology & Material Budget
  - Pixel Array Operation
  - Half Ladder
  - Off-Module Data Flow
  - PXD Detector
  - Mechanics
  - Cooling System
  - Gated Mode
- DEPFET Beam Test
- Status & Prospects

Belle II PXD
SuperKEKB



- Upgrade of KEKB using the same tunnel.
- Asymmetric e^-e^+ collider with E_{CM} at the $\Psi(nS)$ resonance.
- $L = 8x10^{34} cm^{-2} s^{-1}$ (x40 larger than in KEKB).

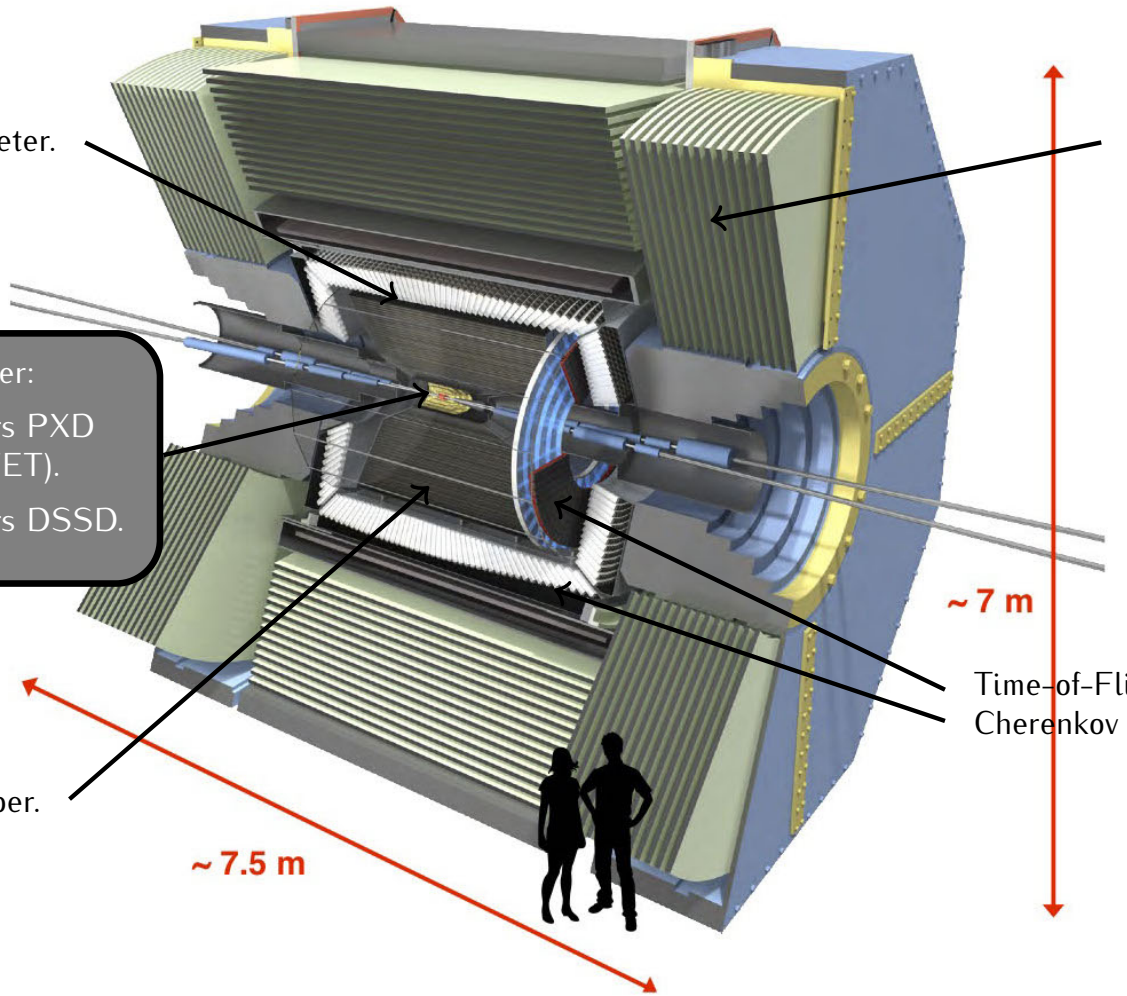
New beam scheme:

- Nano beam concept (10 μmx60 nm).
- Increase of the beam current ($x2$).

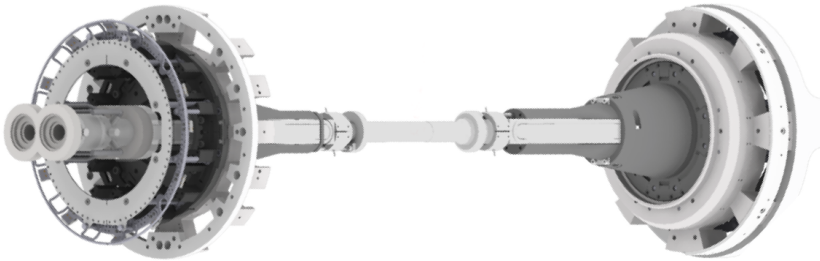
Higher background (x20): higher occupancy & radiation damage.
Higher event rate: faster trigger, DAQ...

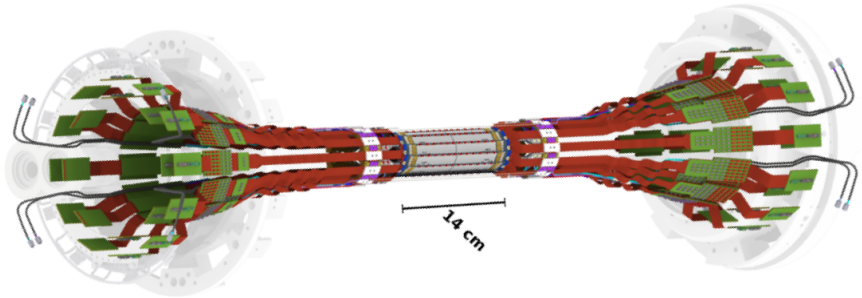
SuperKEKB: $\beta\gamma = 0.28 : e^-(7GeV)e^+(4GeV)$
KEKB: $\beta\gamma = 0.42 : e^-(8GeV)e^+(3.5GeV)$
Better vertexing reconstruction.

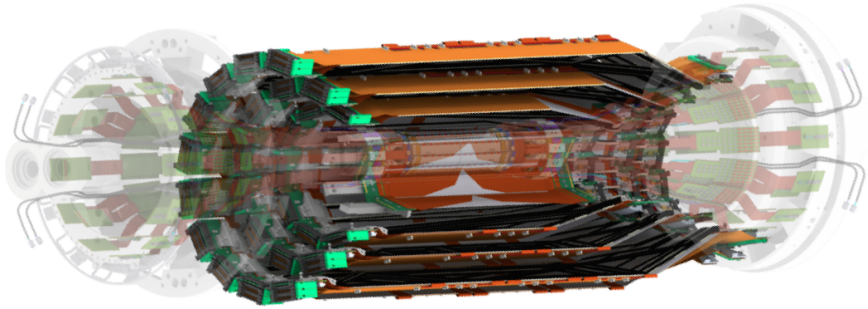
Belle II PXD
Belle II



Belle II PXD
Belle II Vertex Tracker







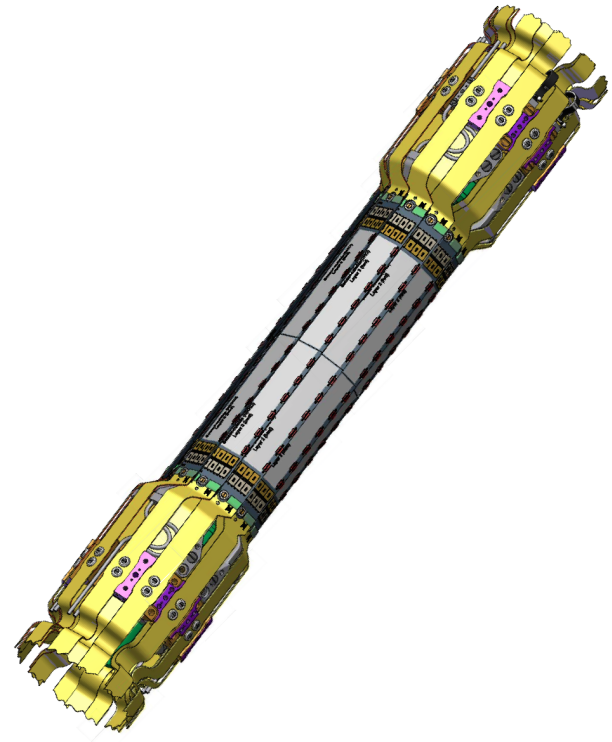
- Beryllium beam pipe:
  Radius: 10 mm.

- PXD:
  Pixel Detector
  2 layers Si Pixel at $R = 1.4$ & 2.2 cm
  DEPFET Technology
  Thickness: 75 μm

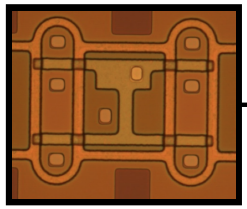
- SVD:
  Silicon Vertex Detector
  4 layers double sided Si strip detector
  $R = 3.8$, 8.0, 11.5 & 14 cm
  (See next talk)

Belle II PXD
Belle II Requirements

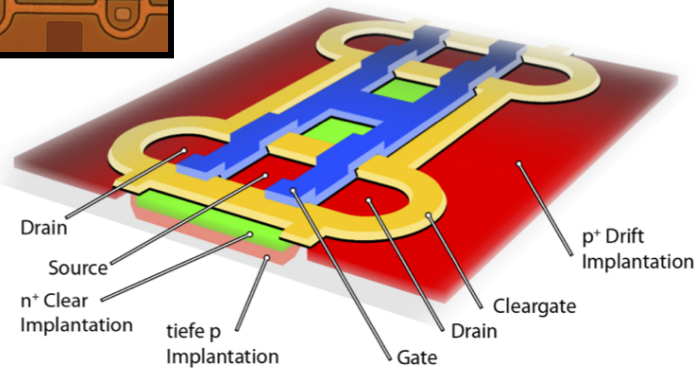
	Belle II
Occupancy	0.4 hits/μm^2/s (< 3%)
Radiation	2 Mrad/year
Duty cycle	1
Frame time	20 μs (cont r.o. mode)
Acceptance	17º-155º
Material budget	0.21% X_0 per layer
Resolution	15 μm (50x75 μm^2)



- Lower momentum range → ↑ Multiple Scatering ⇒ ↓ Material budget & ↑ Resolution.
- ↑ Background → ↑ Radiation damage ⇒ ↑ Radiation tolerance.
- ↑ Background ⇒ ↑ Readout Speed → ↓ Occupancy.

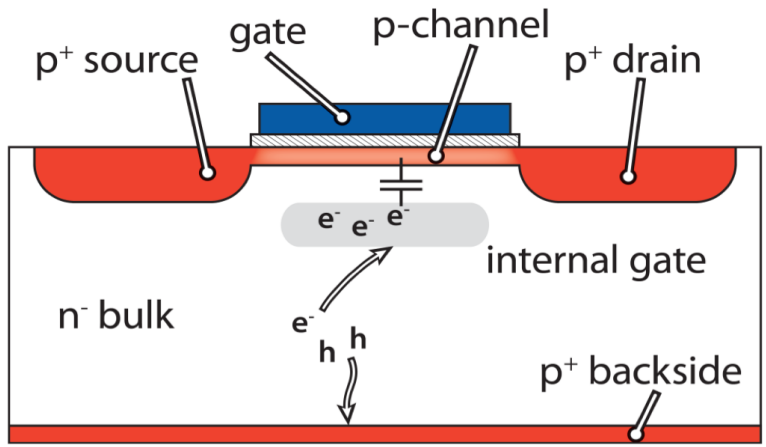


Micrometric structure



- Each pixel is a p-channel FET integrated in a completely depleted bulk.
- A deep n-implant creates a potential minimun for electrons under the FET gate (internal gate).
- Internal gate is capacitive coupled to the FET gate.
- The drain current is proportional to the number of electrons collected in the internal gate.

Internal gain: $g_q \sim 500 pA/e^-$

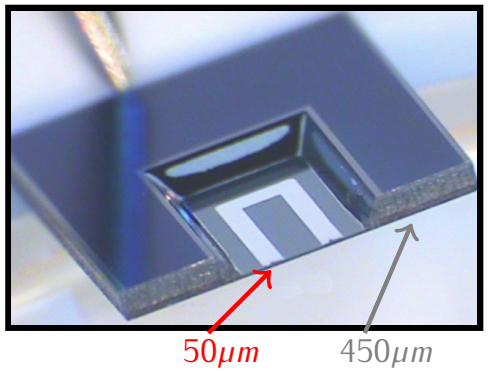


- Detection and internal amplification.
- Small intrinsic noise.
- Low power consumption.

DEPFET
Thinning technology & material budget

VTX15

Process backplane. Wafer bonding. Thinning of top wafer. Process top. Etching of handle wafer.



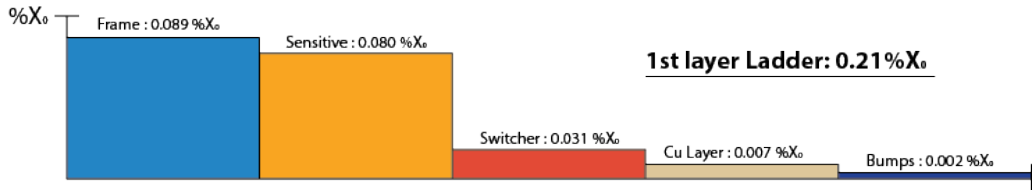
90 steps fabrication process:

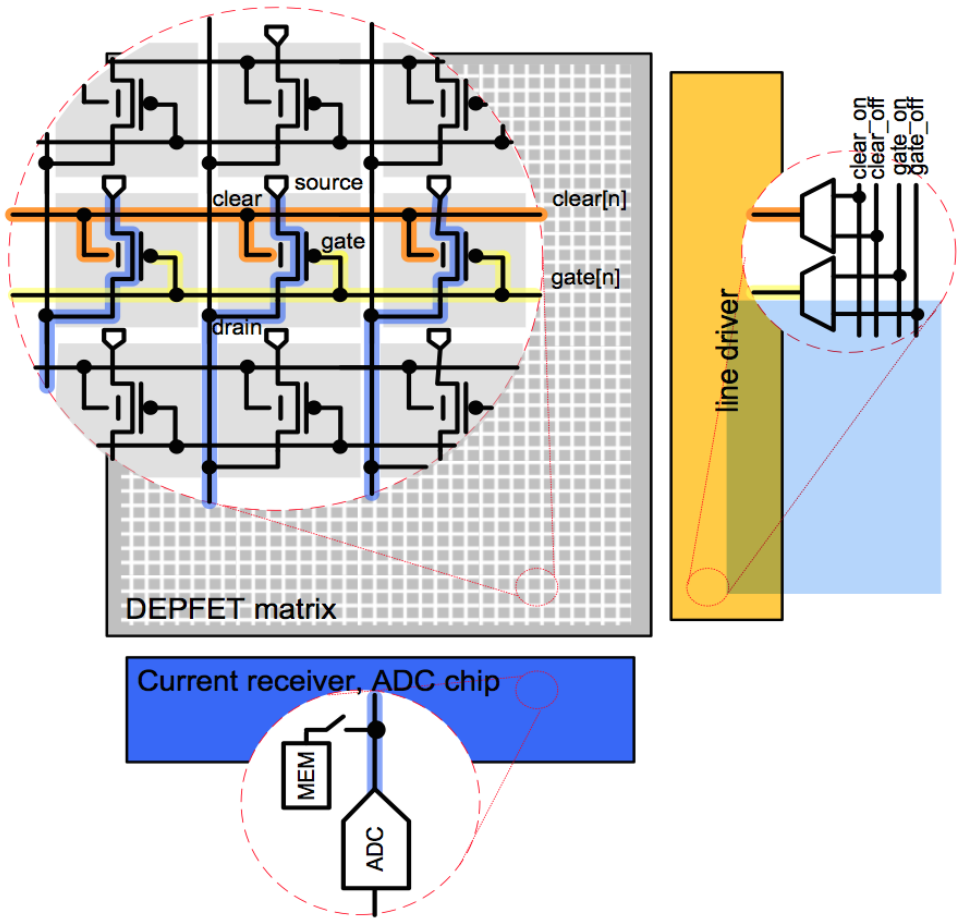
- 9 Implantations.
- 19 Lithographies.
- 2 Poly-layers.
- 2 Alu-layers.
- 1 Copper layer.
- Back side processing.

DEPFET material budget:

- Belle II Scenario: 0.21% X_0

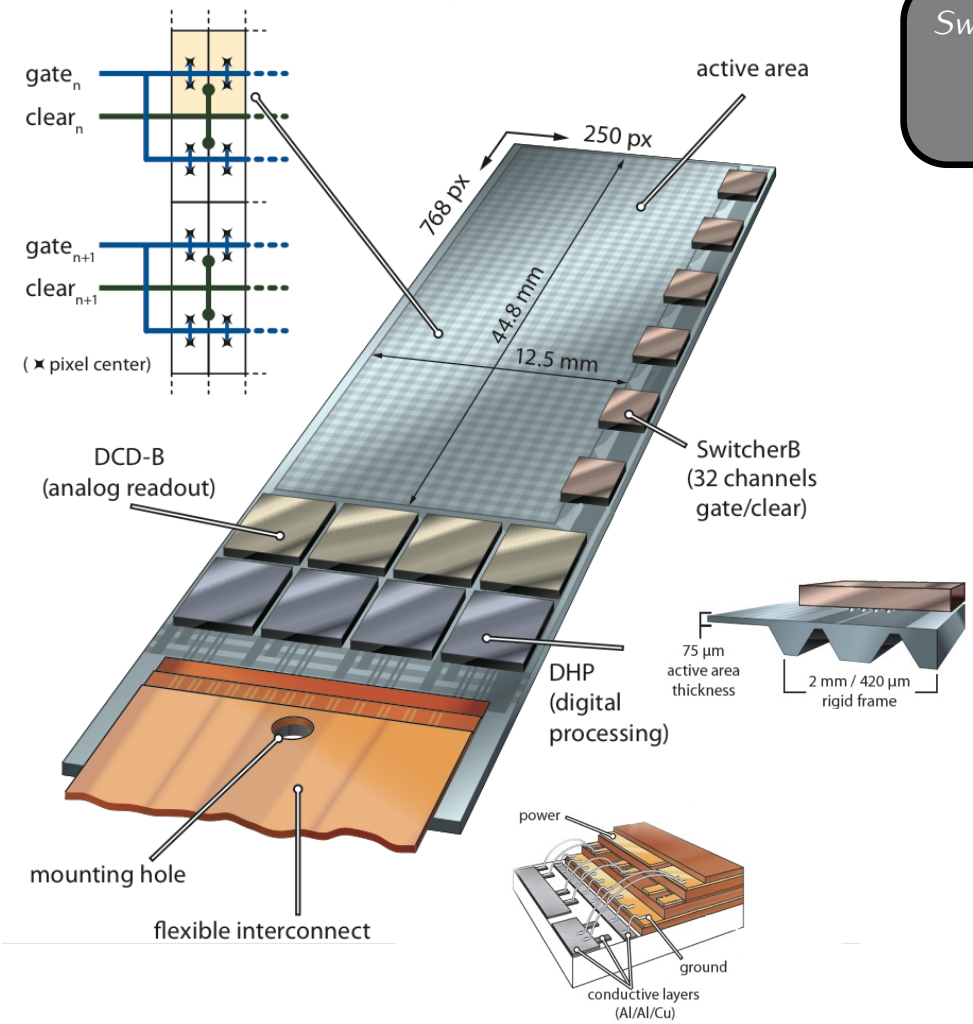
See also "*Spatial resolved radiation length (X/X_0) measurements of DEPFET pixel sensors using EUDET tracks.*" by Ulf Stolzenberg (University of Göttingen) - 16^{th} International Workshop on DEPFET Detector and Applications.





- Gate and Clear lines need switcher steering chip.
- Row-wise readout - 20 μs/frame - 100 ns/row (for Belle II 4 rows are read at time).
- Long drain read out lines keep most of the material out of the acceptance region.
- Only “activated" rows consume power.
  - The others rows are still sensitive to charge.
  - Low power consumption.

DEPFET
DEPFET half ladder



SwitcherB: Row Control

- Gate and clear voltages.
- 32x2 channels

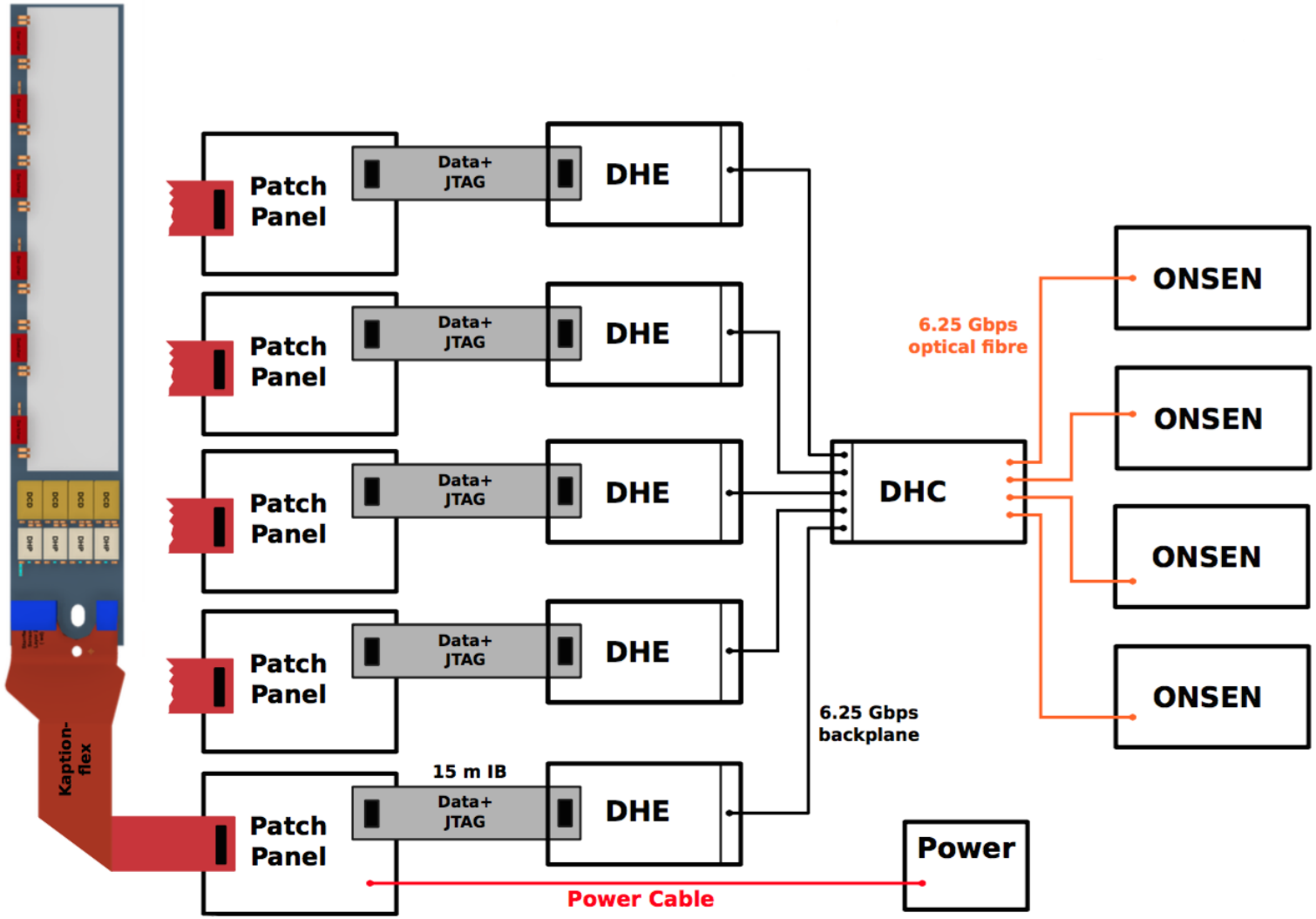
DCDB (Drain Current Digitizer):

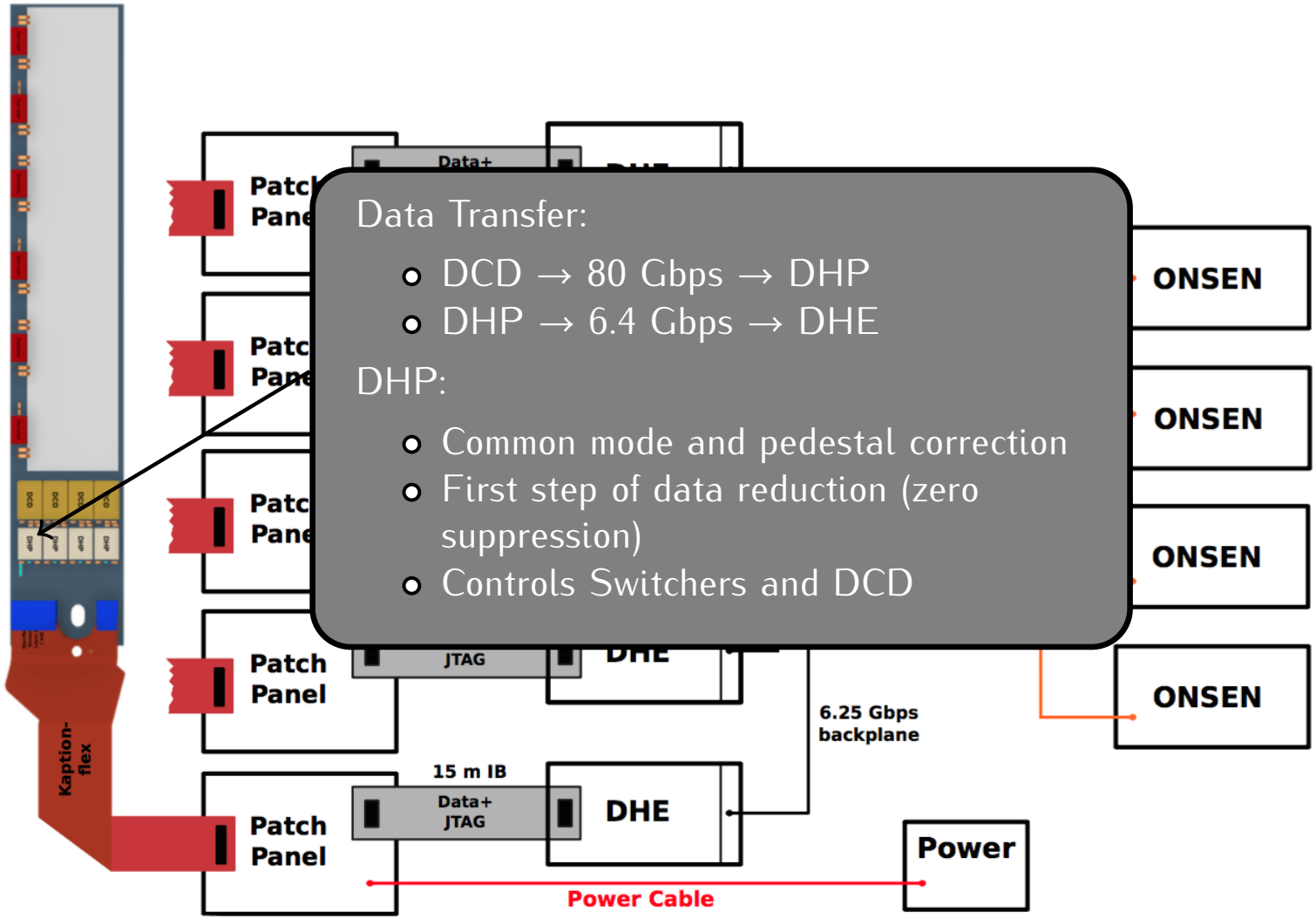
- Analog Frontend.
- Amplification and digitation of DEPFET signals.
- 256 input channels - 8-bit ADC/channel
- 92ns sampling time.

DHP (Data Handling Processor):

- First data compression
- Common mode & pedestal correction.
- Data reduction (Zero suppression).
- Timing and trigger control.

DEPFET
Off-module Data Flow



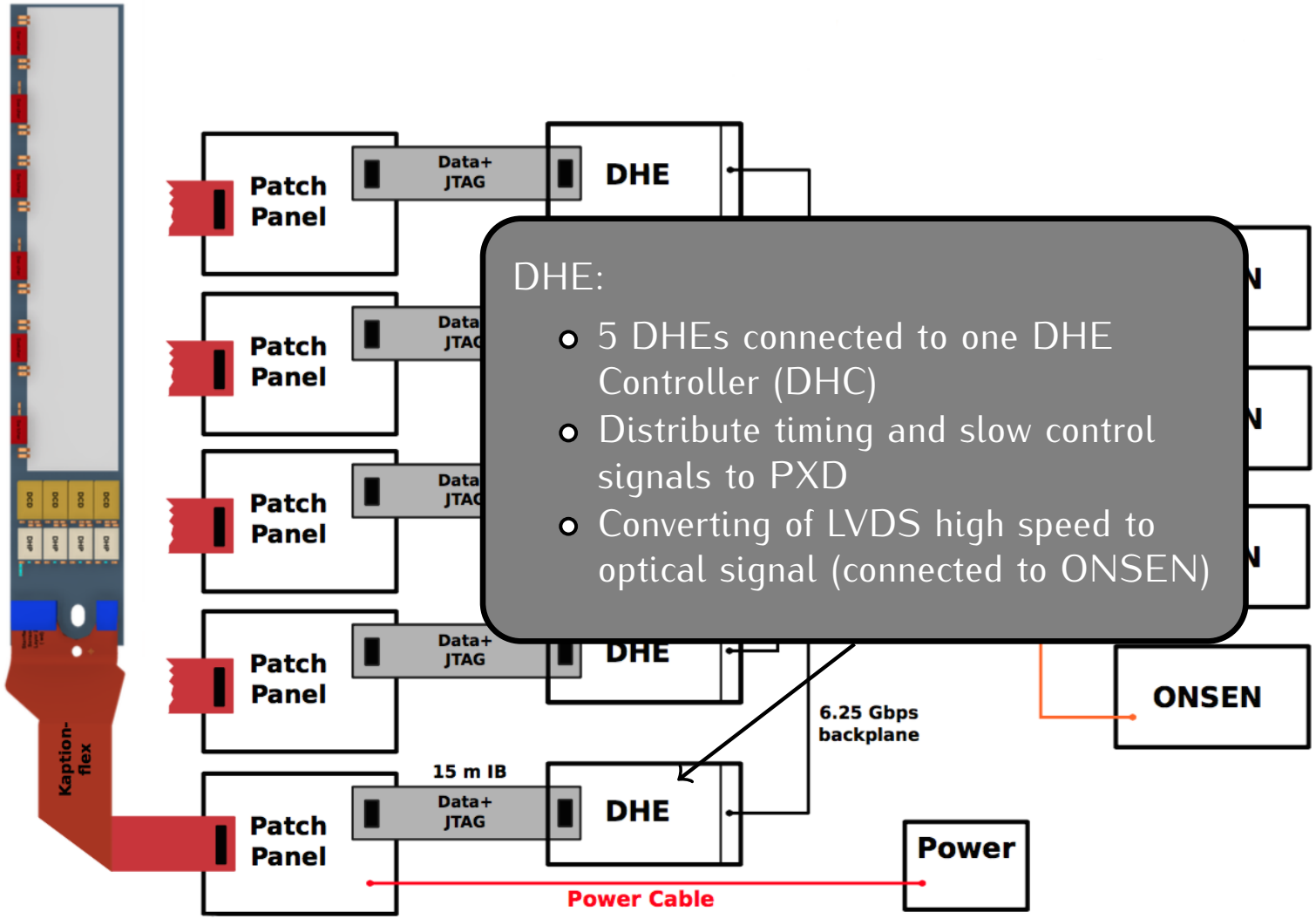


Data Transfer:

- DCD → 80 Gbps → DHP
- DHP → 6.4 Gbps → DHE

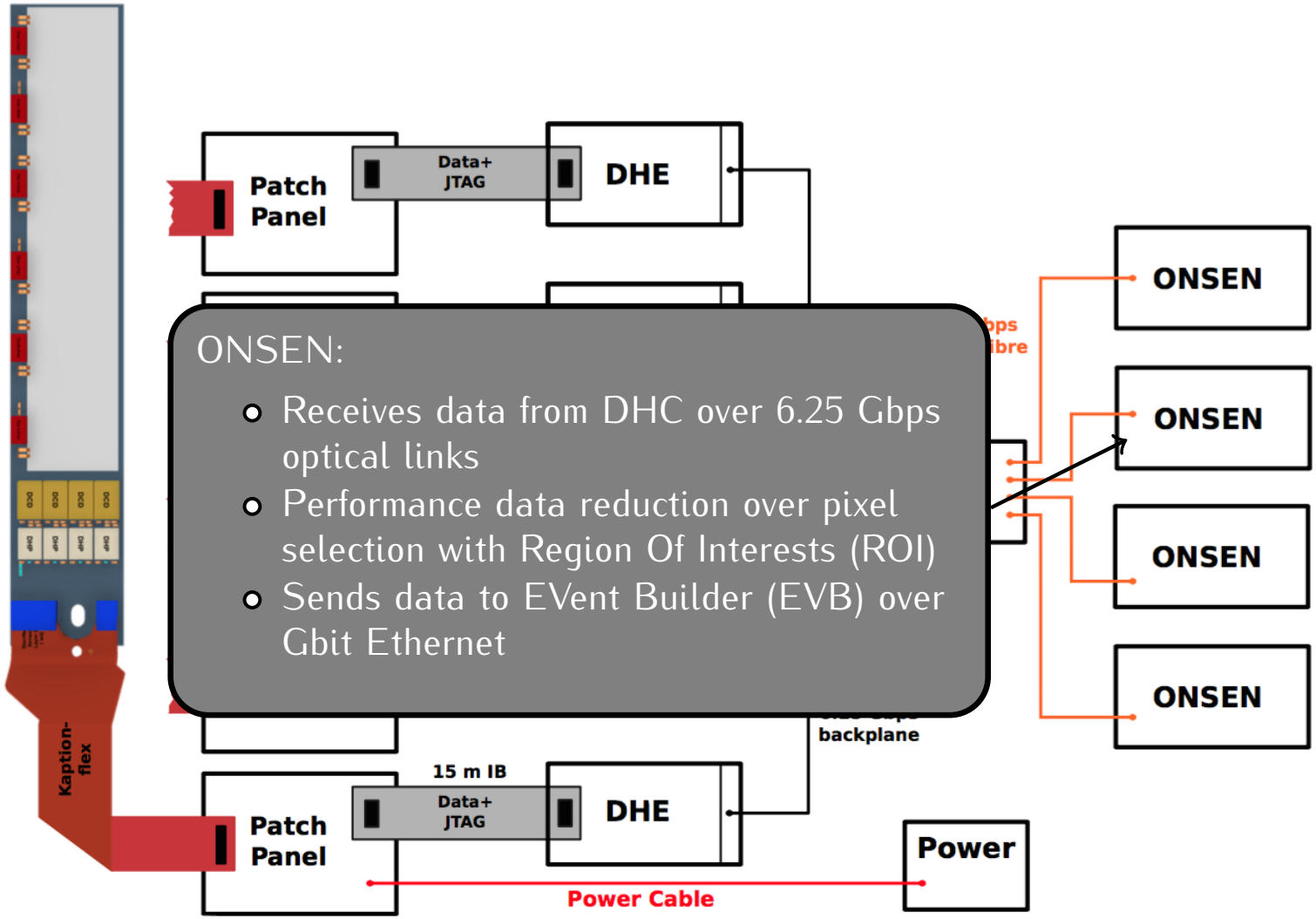
DHP:

- Common mode and pedestal correction
- First step of data reduction (zero suppression)
- Controls Switchers and DCD



DHE:

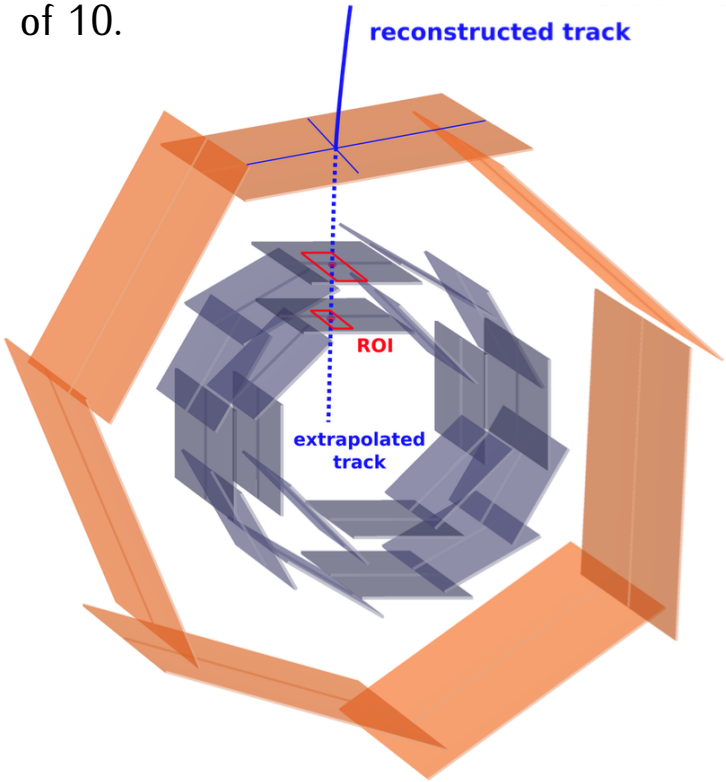
- 5 DHEs connected to one DHE Controller (DHC)
- Distribute timing and slow control signals to PXD
- Converting of LVDS high speed to optical signal (connected to ONSEN)

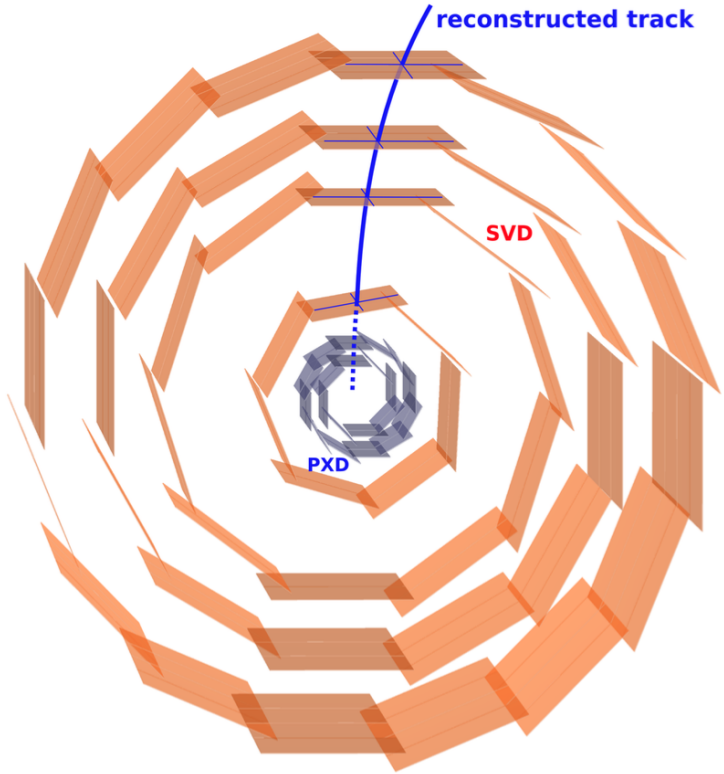


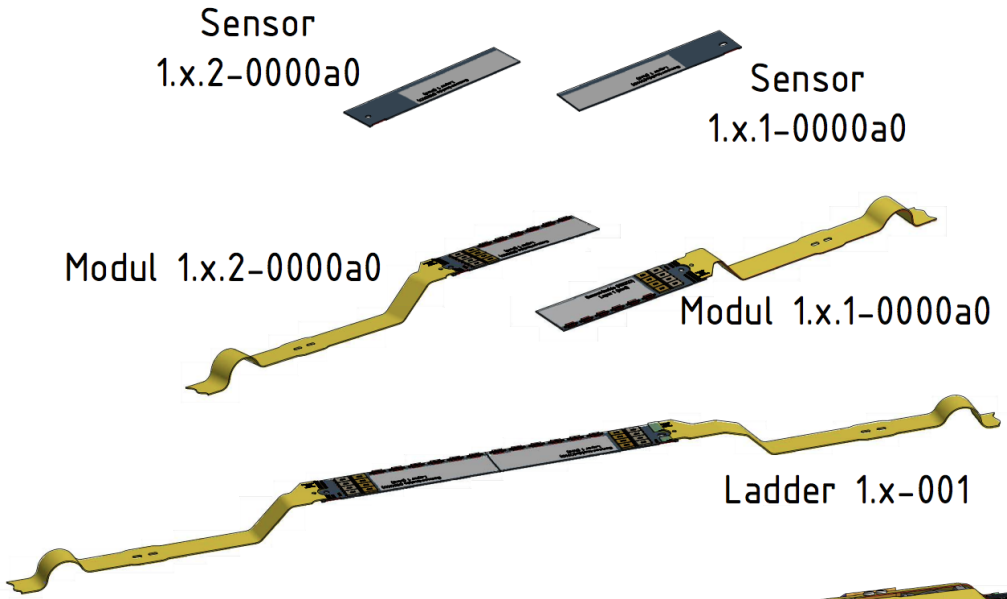
ONSEN:

- Receives data from DHC over 6.25 Gbps optical links
- Performance data reduction over pixel selection with Region Of Interests (ROI)
- Sends data to EVent Builder (EVB) over Gbit Ethernet

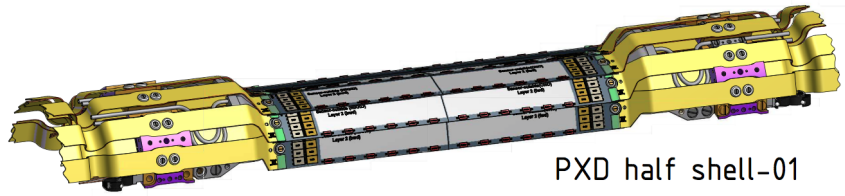
- ROI Selection: Use hits from the surrounding strip detector, find and fit tracks, back extrapolate on the PXD and create Region of Interest (ROI).
- Expected: Data reduction by a factor of 10.







- Sensors are processed & ASICs and SMDs soldered.
- Kapton flex cable is attached.
- Two half ladders are glued together.



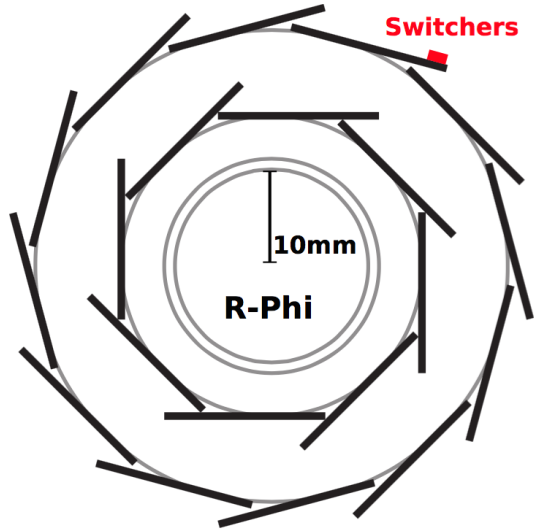
PXD half shell-01

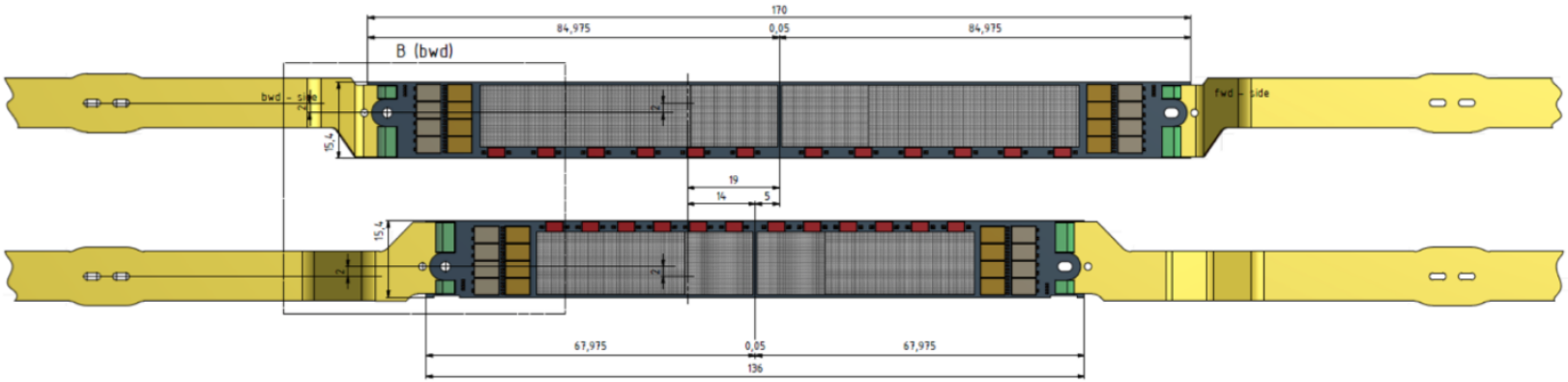
- Half detector shell is assembled separately.
- The two half detector shells are mounted together.

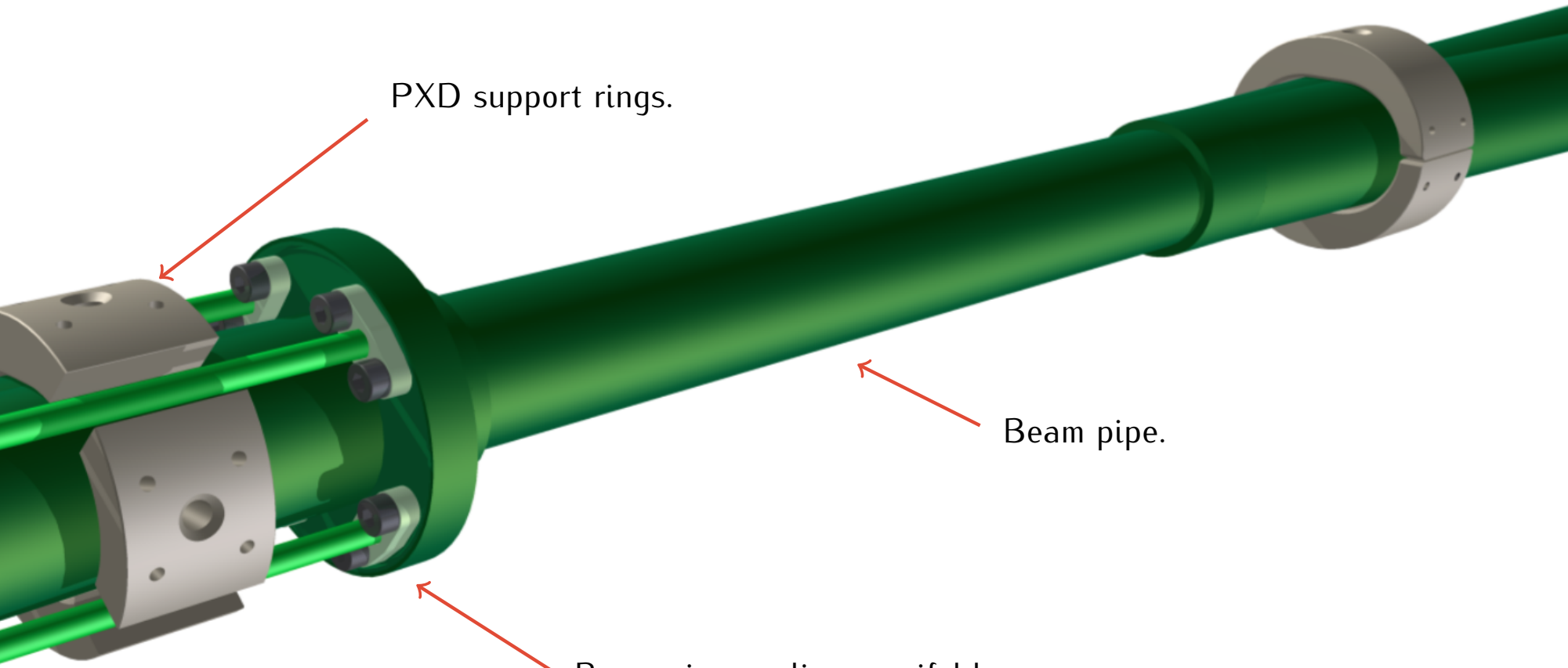
PXD full shell

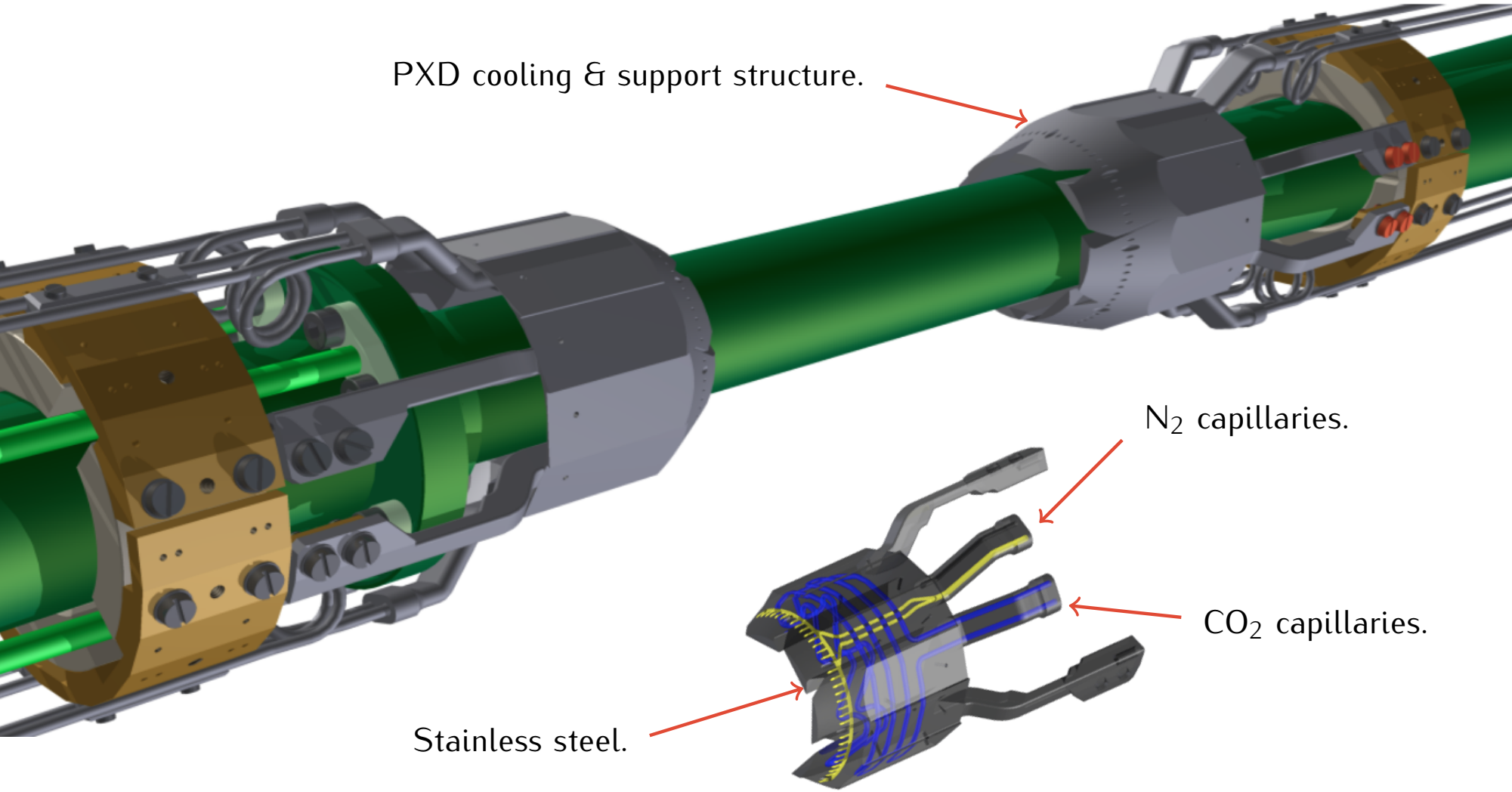
DEPFET
Complete pixel detector

	Layer 1	Layer 2
Module	8	12
Radii	14 mm	22 mm
Ladder Size	15x136 mm^2	15x170 mm^2
Pixel Size	50x55 μm^2 50x60 μm^2	50x70 μm^2 50x85 μm^2
Pixels	250x1536	250x1536
Thickness	75 μm	75 μm

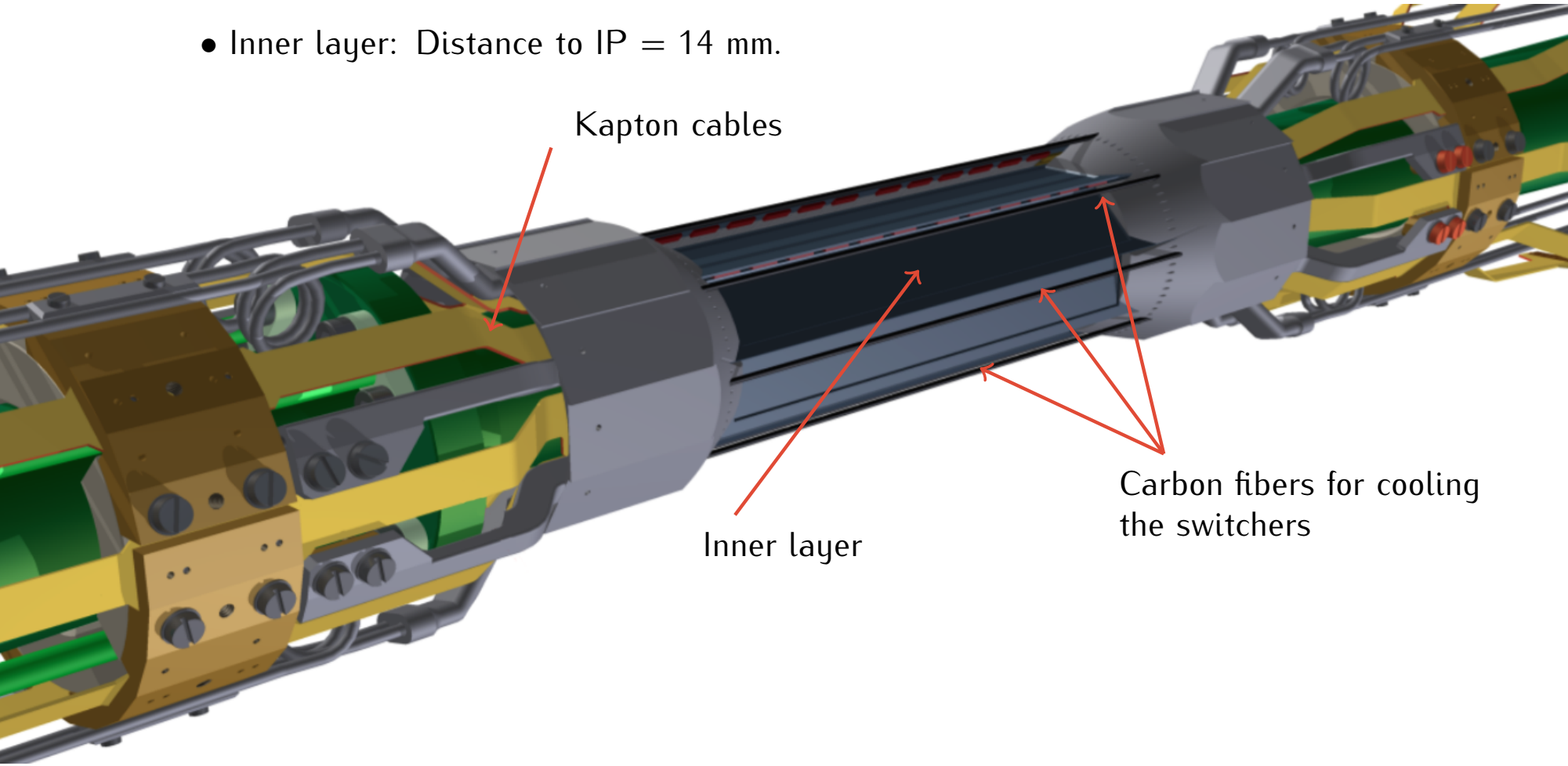





PXD support rings.
Beam pipe.
Beam pipe cooling manifold.

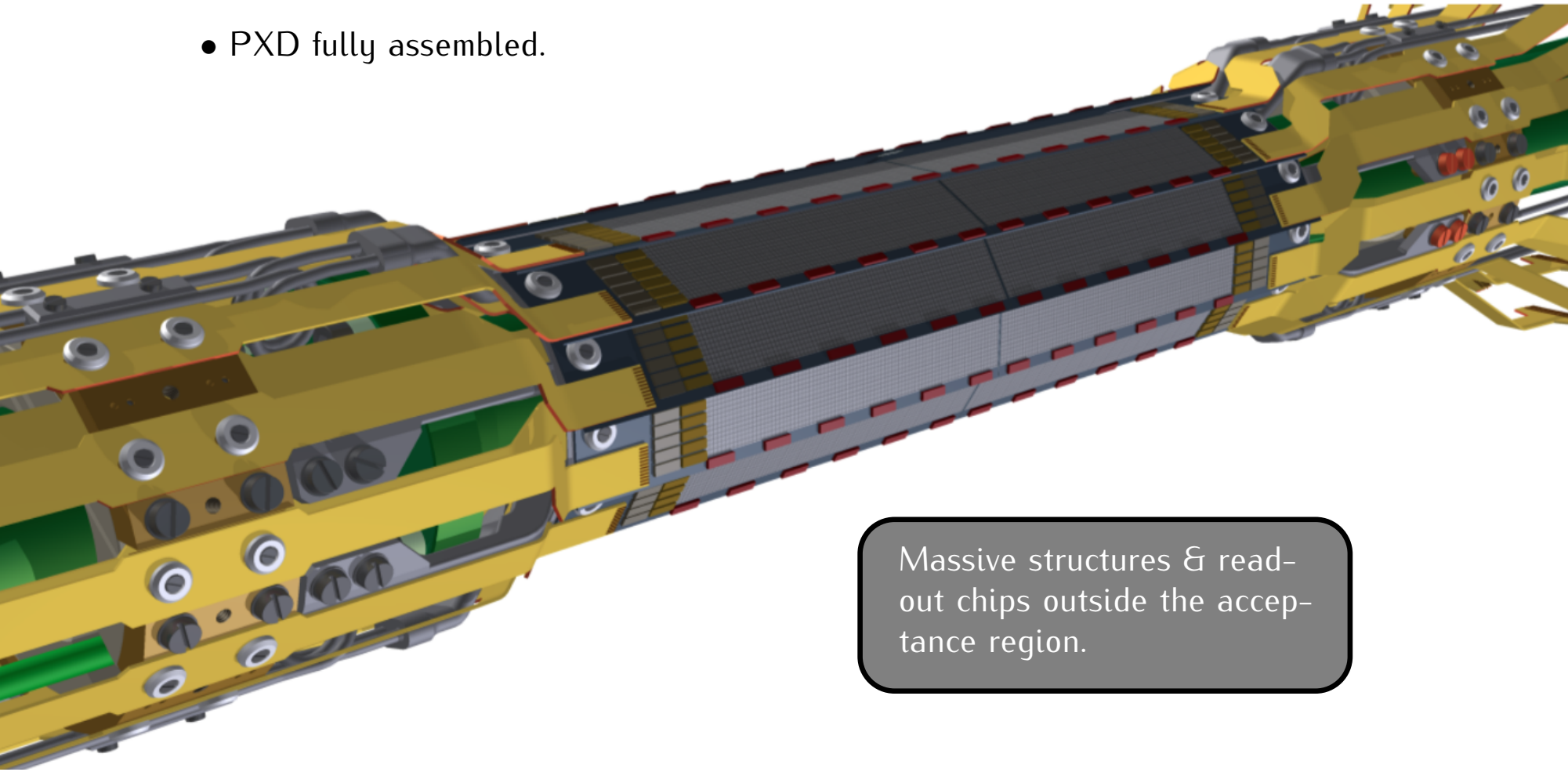

PXD cooling & support structure.
N_2 capillaries.
CO_2 capillaries.
Stainless steel.

- Inner layer: Distance to IP = 14 mm.

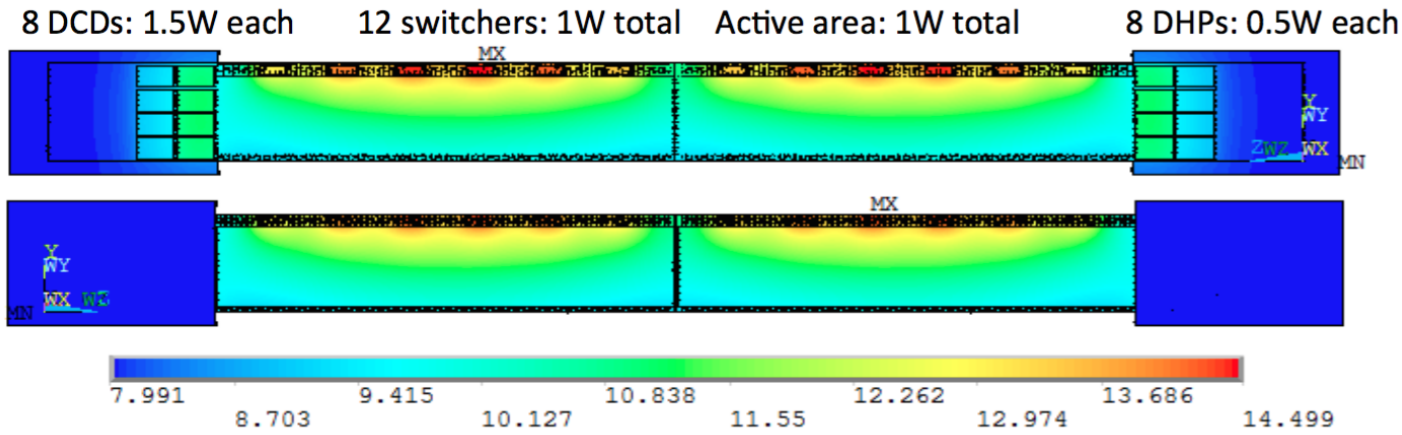


DEPFET
DEPFET Mechanics

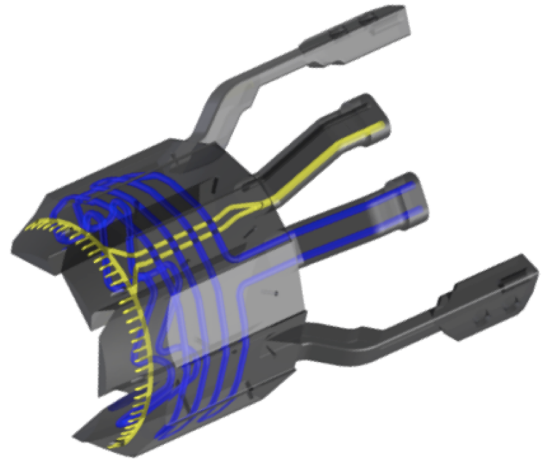
- PXD fully assembled.

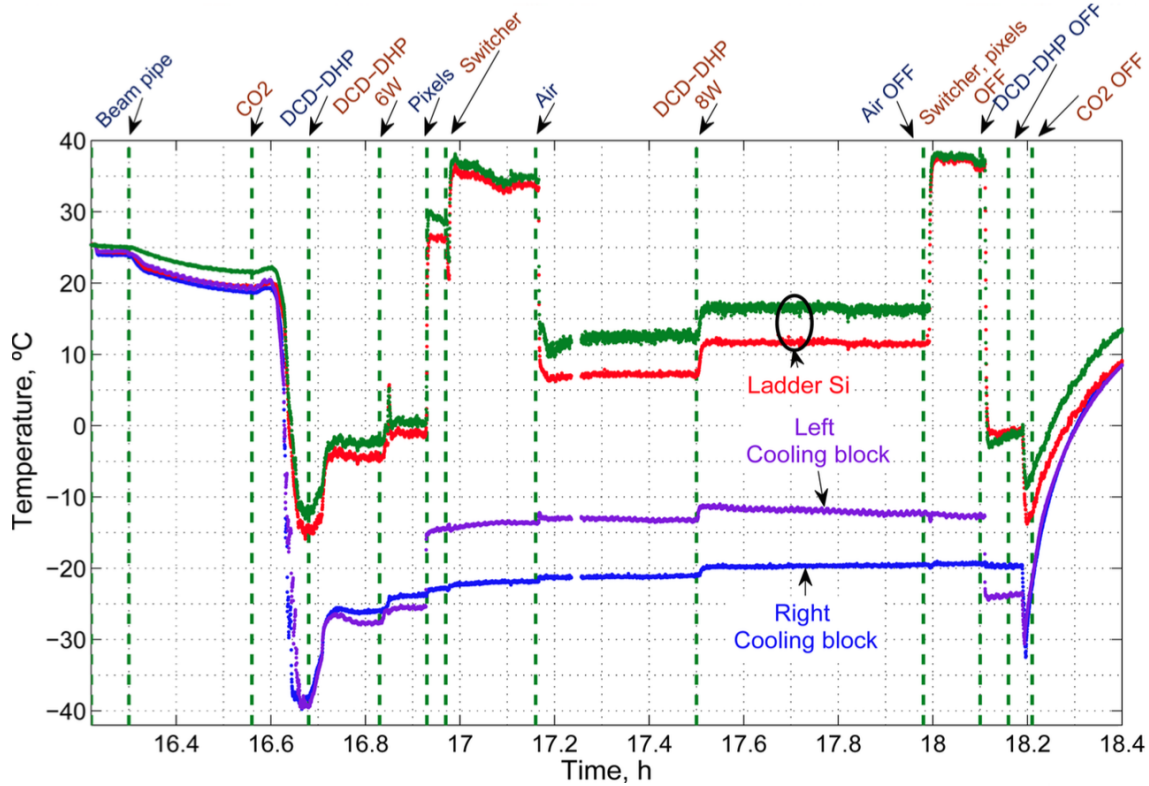


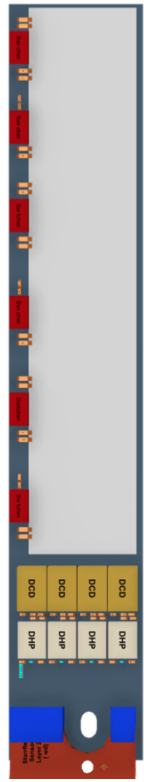
Massive structures & read-out chips outside the acceptance region.

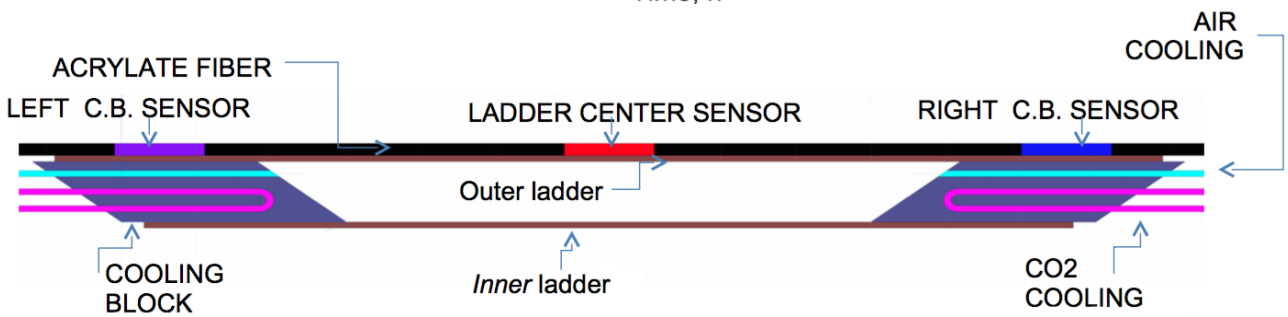


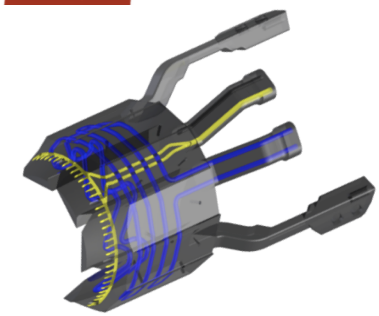
- Ladder: 18W → Full PXD: 360W.
- Cooling Blocks with CO_2 at $-30^{o}C$ & N_2 flow ($0^{o}C$) to decrease & homogenize the temperature distribution.

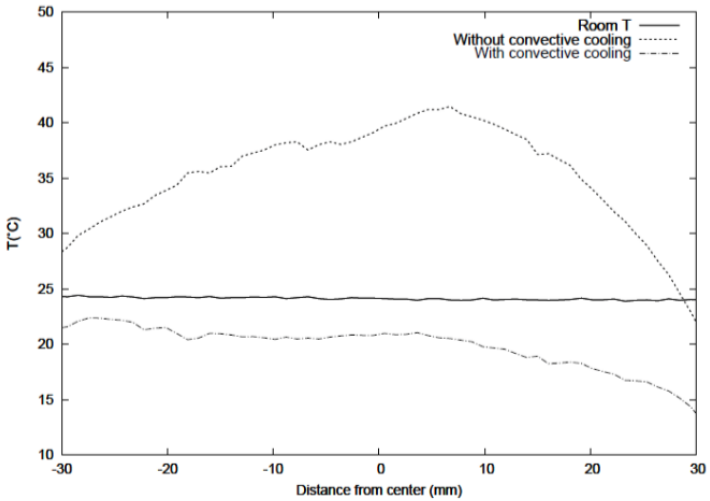


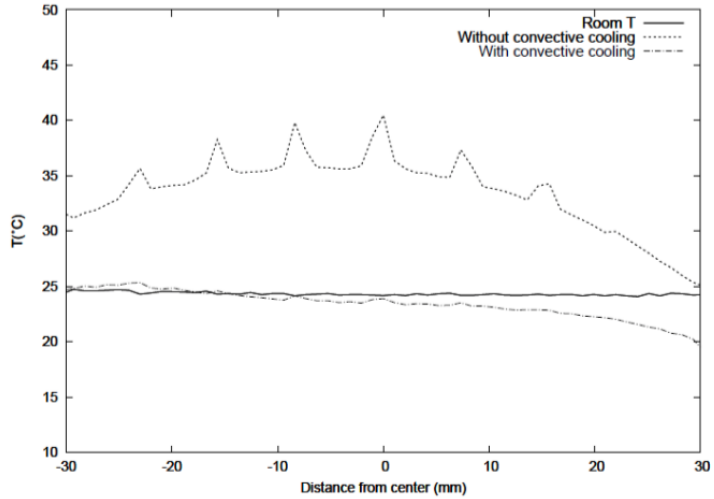

Beam pipe
CO2
DCD-DHP
DCD-DHP
6W
Pixels
Switcher
Air
DCD-DHP
8W
Air OFF
Switcher, pixels OFF
DCD-DHP OFF
CO2 OFF
Ladder Si
Left
Cooling block
Right
Cooling block
Temperature, °C
Time, h



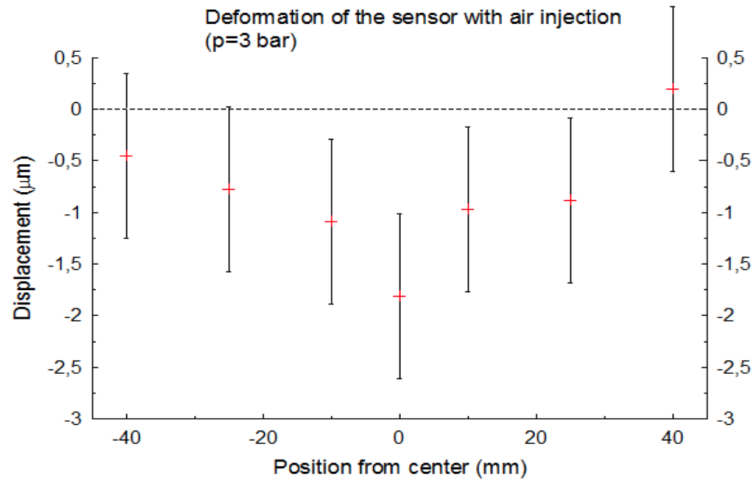

ACRYLATE FIBER
LEFT C.B. SENSOR
LADDER CENTER SENSOR
RIGHT C.B. SENSOR
AIR
COOLING
Outer ladder
COOLING
BLOCK
Inner ladder
CO2
COOLING

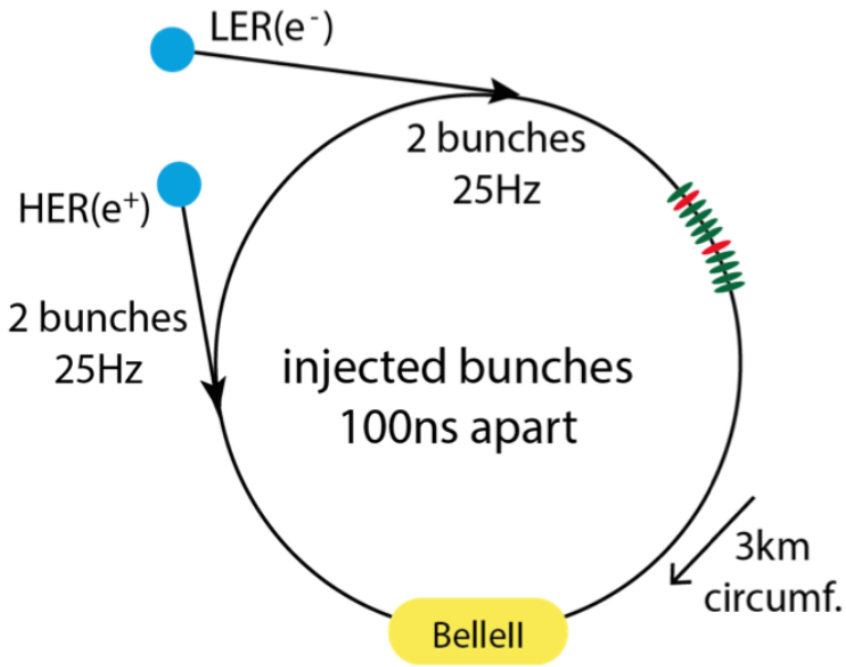


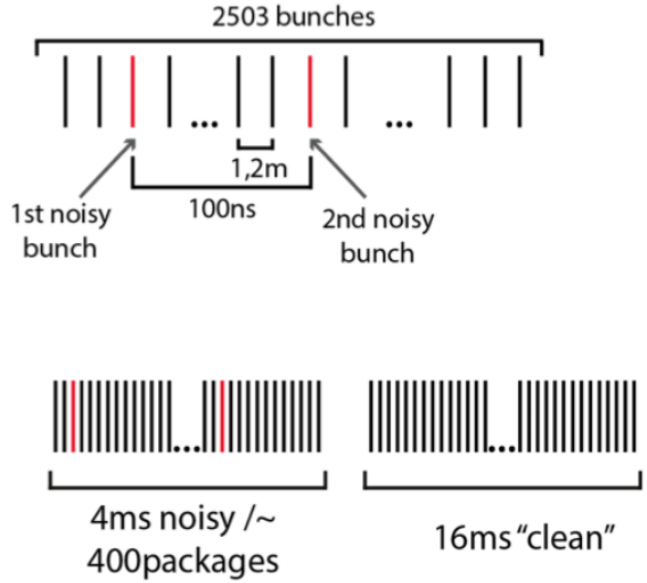




- Cooling attainable with a flow rate of 15 l/min, pressure 3 bar. This is below fundamental mode vibration conditions.
- Maximum deformation (center) $1.8 \pm 0.8\ \mu m$.



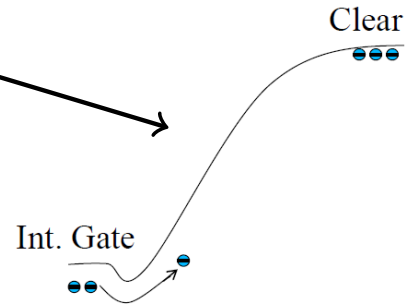




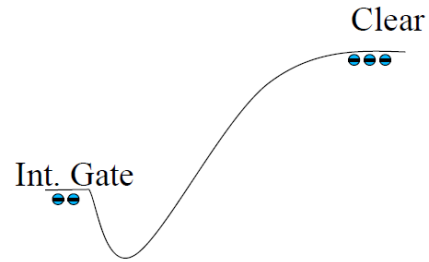
- "Noisy bunches" create (junk) electrons within the Pixel Detector (PXD).
- Mask "noisy bunches" → PXD deadtime = 20%.
- DEPFET option: Gate the sensor during the passage of the noisy bunches → PXD deadtime ∼ 0%.

External Gate in off state: Shifts the potential of the internal gate by capacitive coupling → larger potencial barrier.

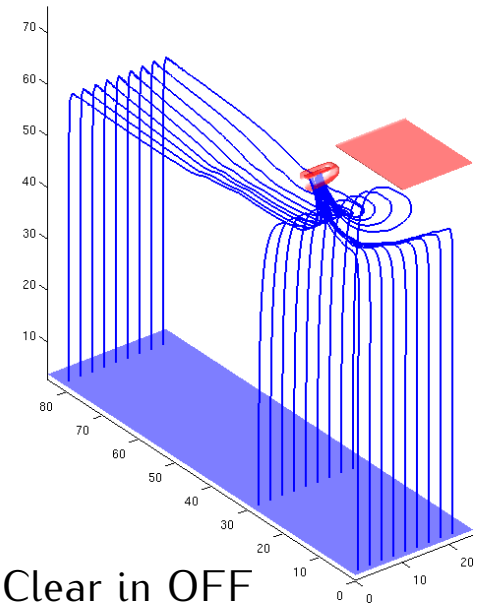
External Gate in ON state



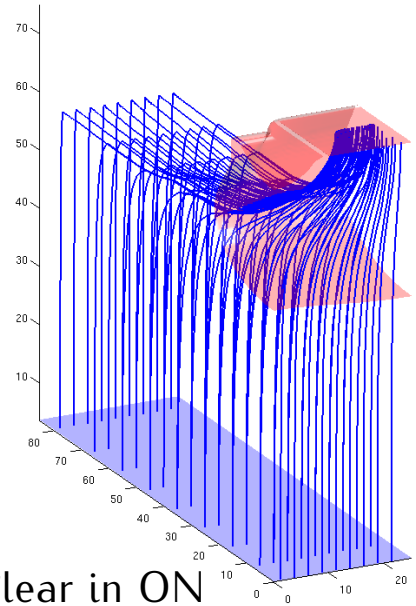
External Gate in OFF state



Clear in on state: Remove the new charge created in the bulk.

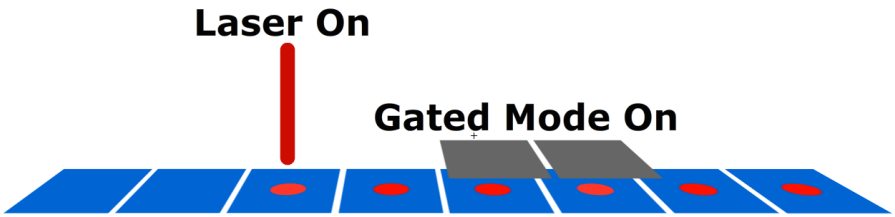


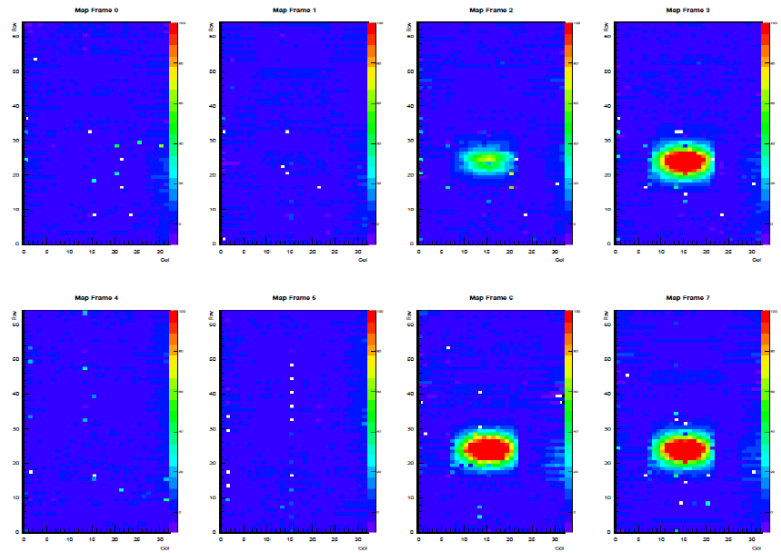
Clear in OFF state



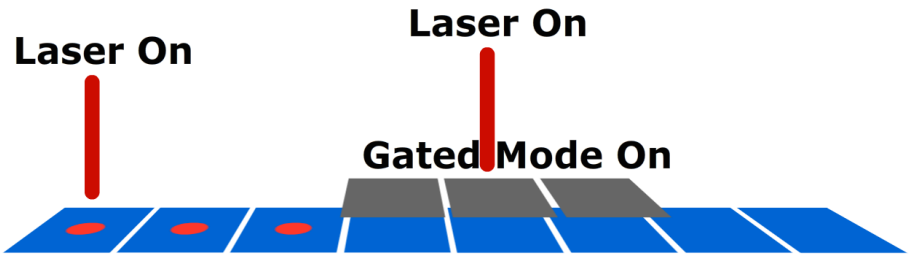
Clear in ON state

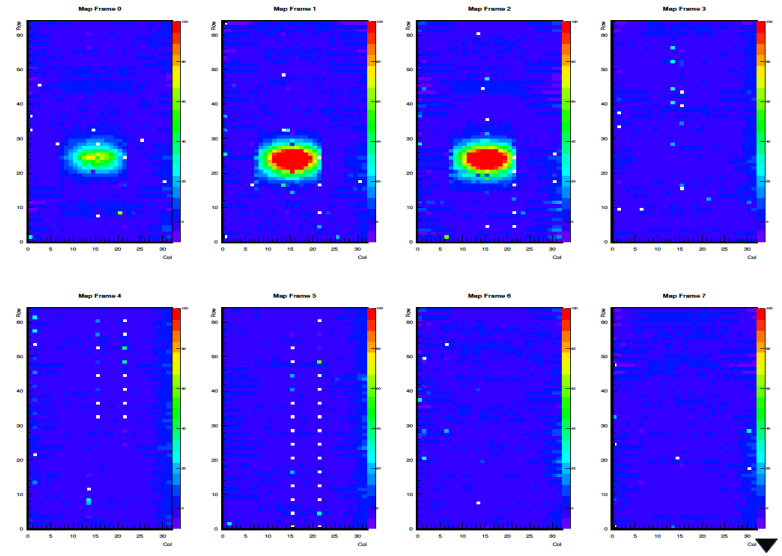
Signal Charge Restore:





Junk Charge Generation:





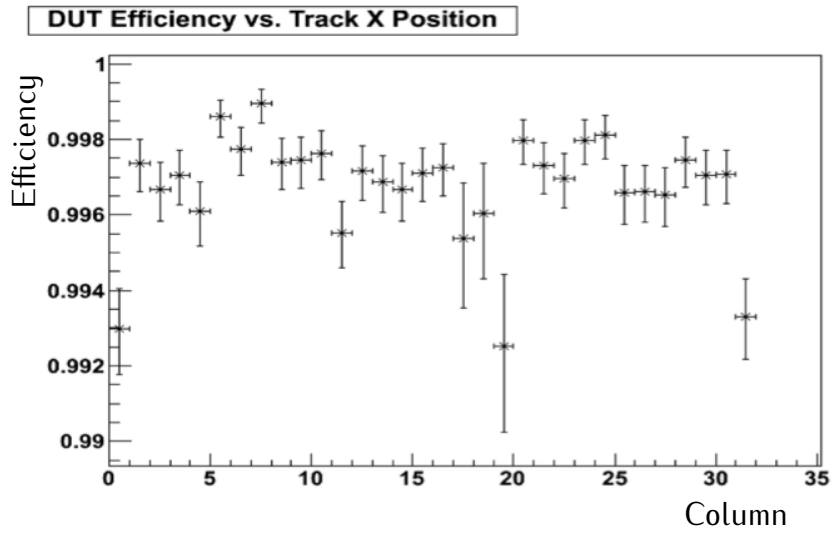
DEPFET Beam Test

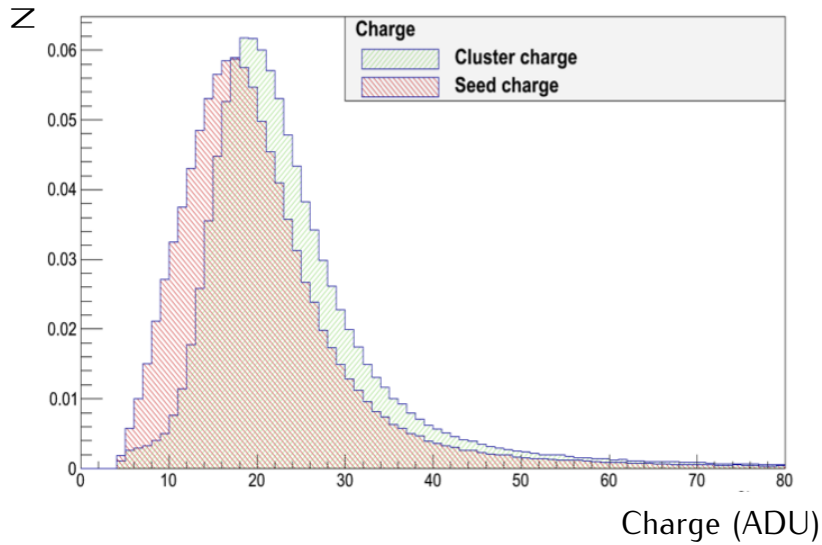
DEPFET PXD6 extensively tested:

- 120 GeV pions at CERN-SPS.
- 1-5 GeV electrons at DESY.
- Magnetic field.
- Sensor properties (Charge collection homogeneity, operating points, efficiency, angular scans, various pixel sizes, gate lengths, clear structures, drift regions and pixel designs).
- System related aspects (Power supply, prototypes DHH and ONSEN readout).

PXD6 Belle II design 50x75 μm^2 (50 μm thick):

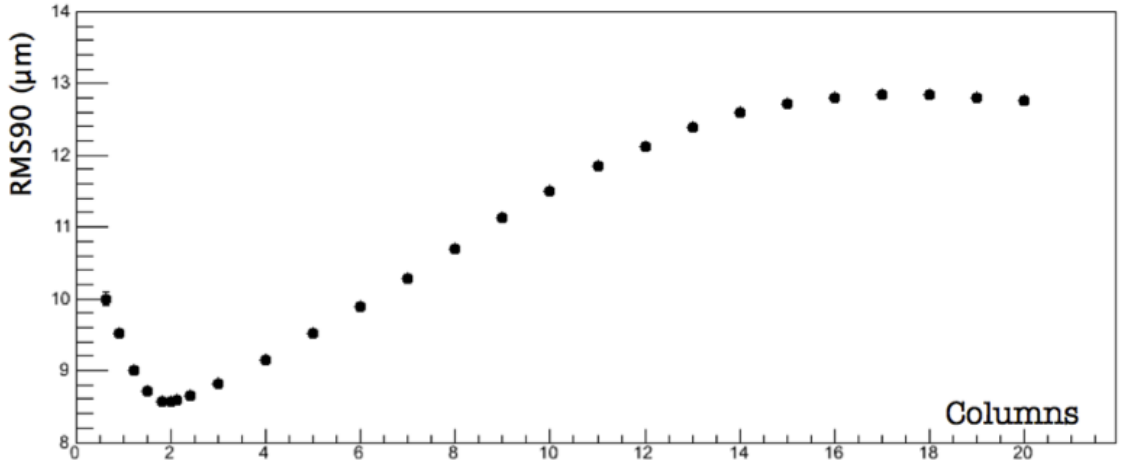
- DUT efficiency > 99.5%
- Signal ~ 21 ADU, Noise ~ 0.6 ADU - S/N ~ 40.





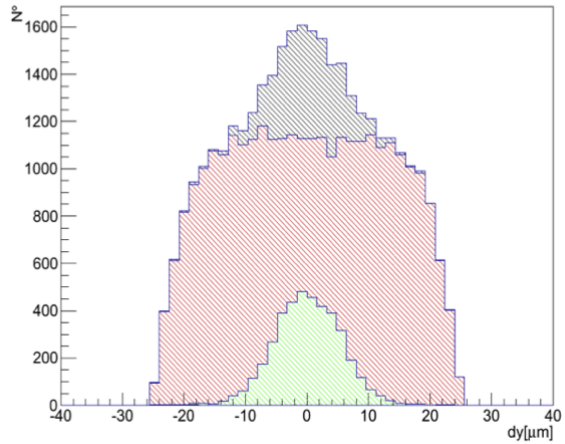
DEPFET Beam Test

DEPFET PXD6 Belle II design - test beam data (50 μm pitch and 50 μm thick).



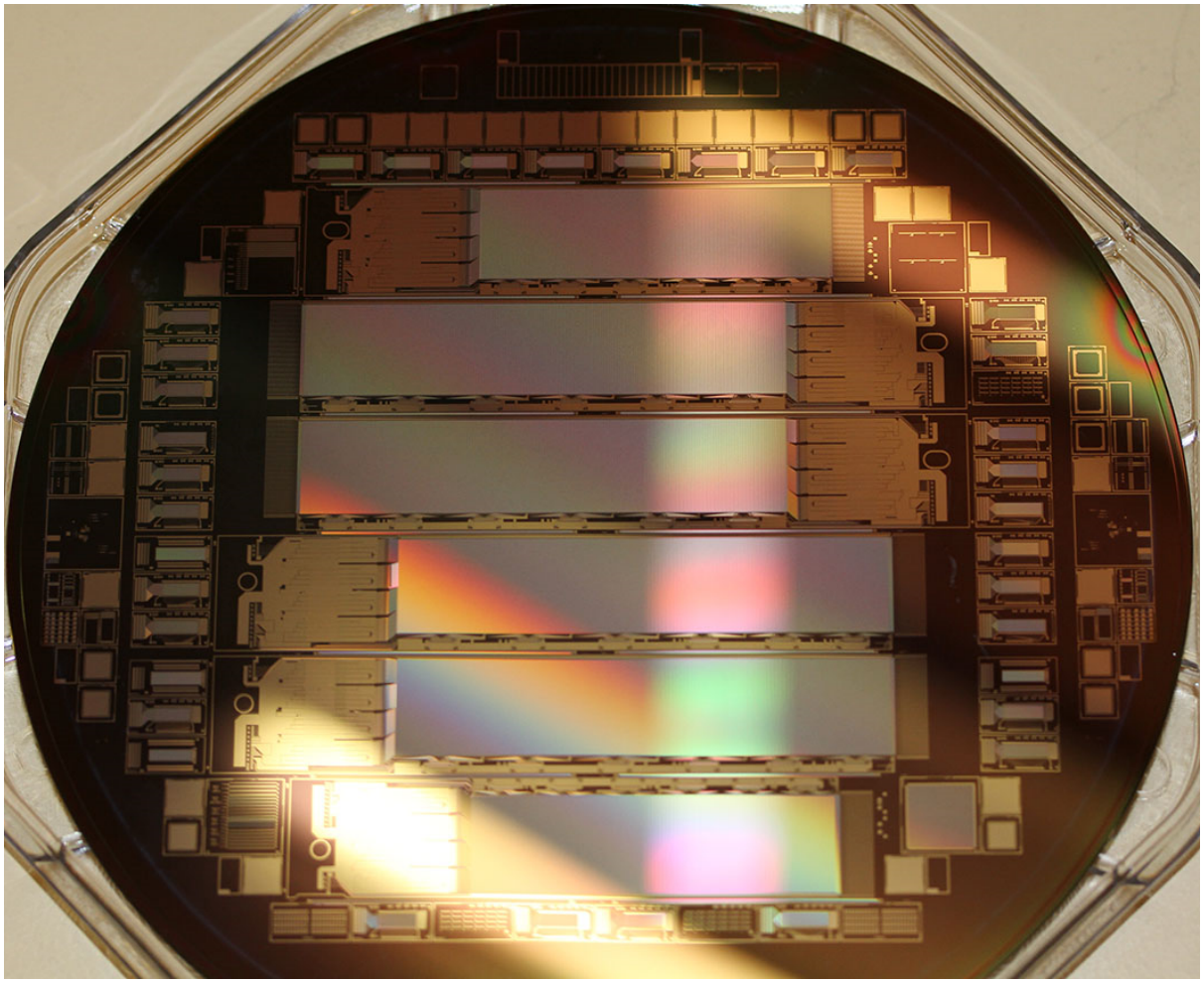
Max resolution 8.5 μm

- Belle II scenario $\sim$ 10 μm of resolution (test beam data).



See also: *DEPFET active pixel detectors for a future linear e^+e^- collider* - DEPFET Coll. - http://arxiv.org/pdf/1212.2160.pdf.

Status & Prospects
Next Step: Pilot Run



- Pilot Run: Final sensor prototype with PXD9 full matrix.
- First pilot run detectors, fully assembled expected by mid July.
- Debugging the ASICs and complete half ladder operation.
- Full detector characterization and test of quality control process.

- Pilot Run with first “hot wafers” (test by summer of 2015).
- DESY Thermal Test (includes PXD and SVD dummies) in 2015.
- Build 2 ladders (from Pilot Run) for DESY VXD Beam test (spring 2016), prepare Slow Control for VXD.
- Final ASICs by spring 2016.
- Finish PXD module / ladder production by spring 2017.

Summary

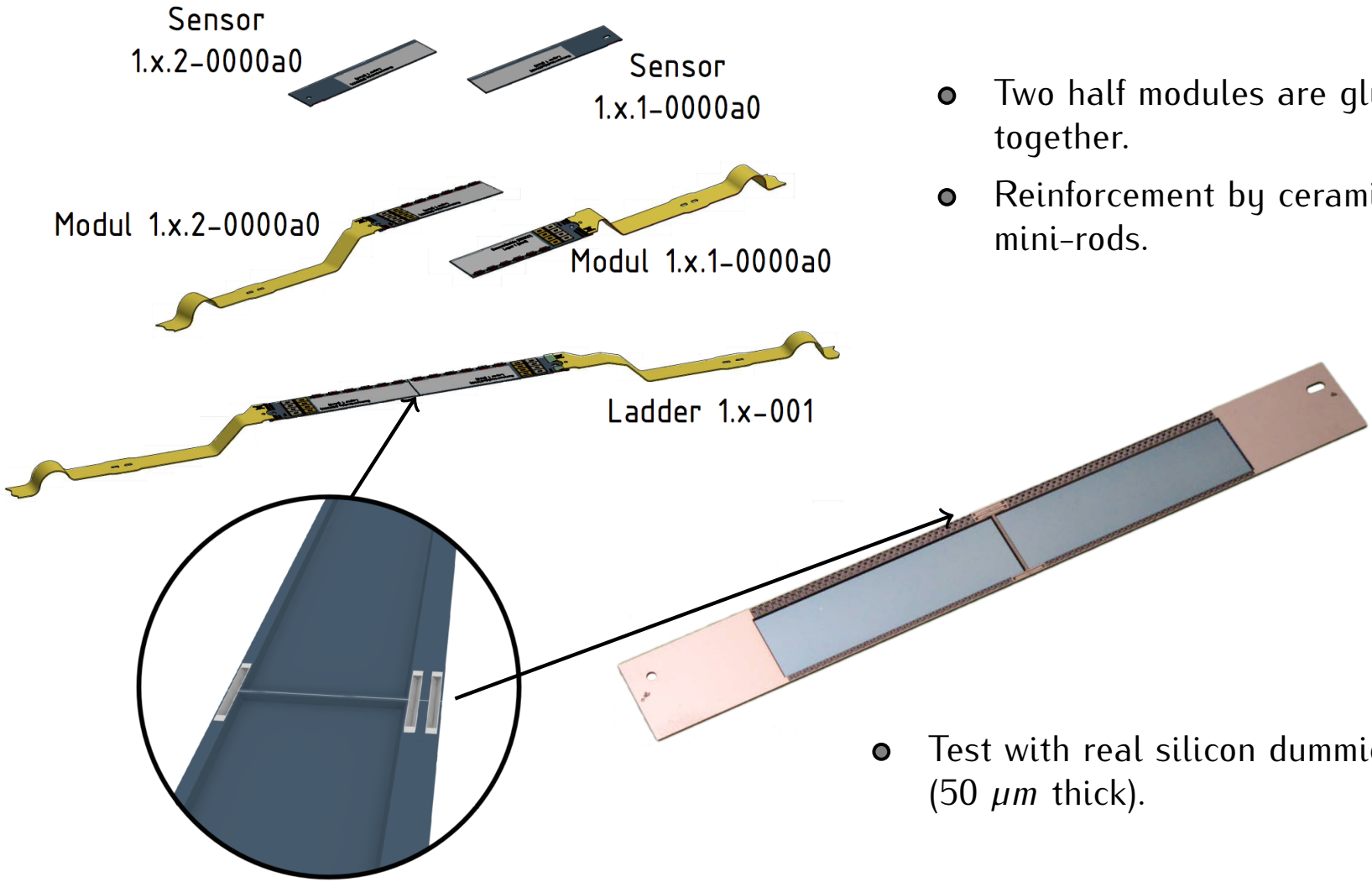
- Belle II requires a new inner Vertex detector to cope with increased luminosity and higher vertex reconstruction demands.
- The good performance of the DEPFET detector system in terms of SNR, spatial resolution, readout speed is demonstrated, fitting all the requirements.
- Every detail is being considered and planned (cooling, mechanics, DAQ...).
- With the pilot run, the final sprint have just started, finishing at spring 2017 when the Belle II PXD will become a reality.

Thanks

THANK YOU.

BACKUP

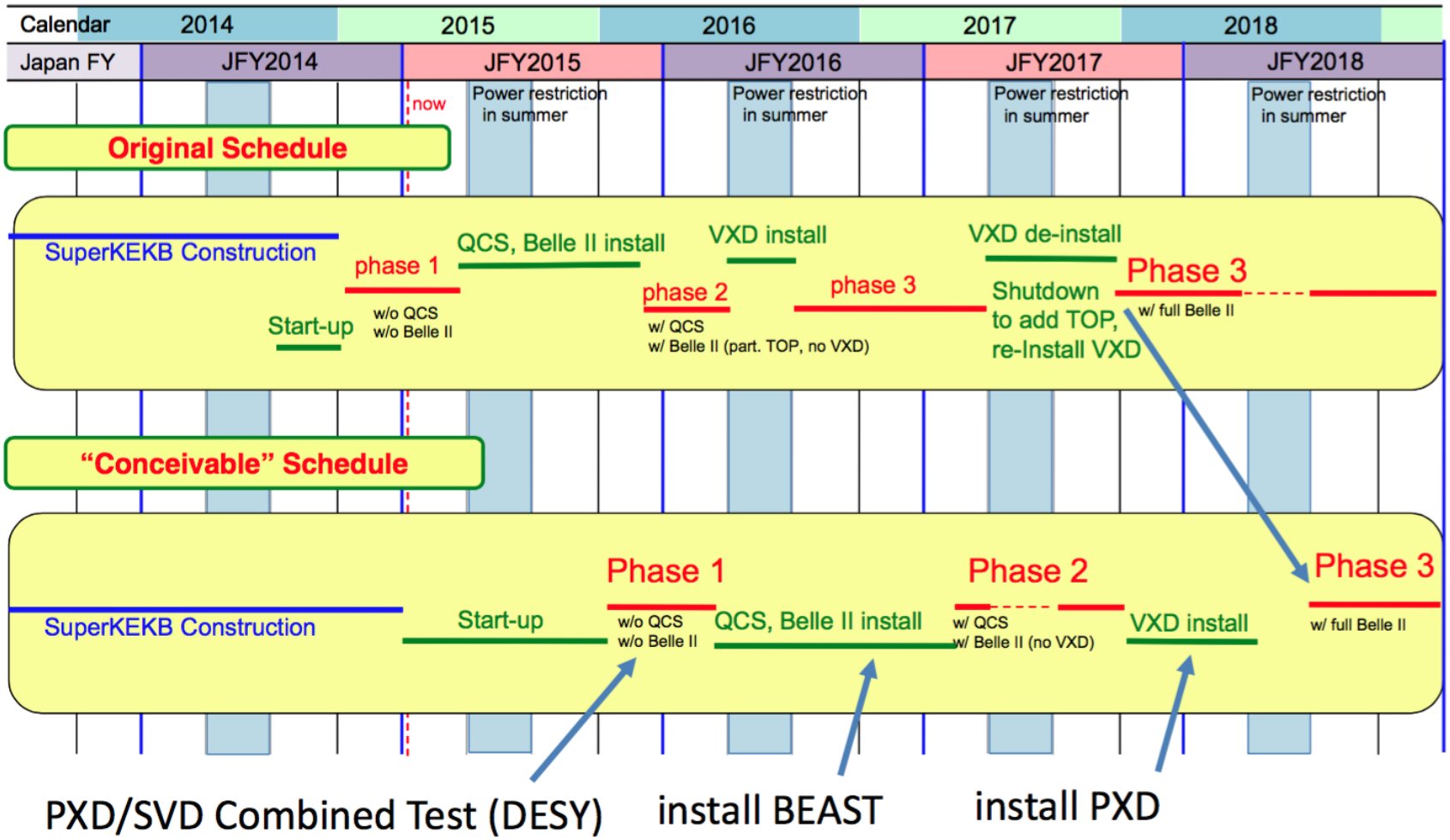
Backup



- Two half modules are glued together.
- Reinforcement by ceramic mini-rods.

- Test with real silicon dummies (50 μm thick).

Backup


Calendar
2014
2015
2016
2017
2018
Japan FY
JFY2014
JFY2015
JFY2016
JFY2017
JFY2018
now
Power restriction in summer
Power restriction in summer
Power restriction in summer
Power restriction in summer
Original Schedule
SuperKEKB Construction
Start-up
phase 1
w/o QCS
w/o Belle II
QCS, Belle II install
VXD install
phase 2
w/ QCS
w/ Belle II (part. TOP, no VXD)
phase 3
VXD de-install
Shutdown to add TOP, re-Install VXD
Phase 3
w/ full Belle II
"Conceivable" Schedule
SuperKEKB Construction
Start-up
Phase 1
w/o QCS
w/o Belle II
QCS, Belle II install
Phase 2
w/ QCS
w/ Belle II (no VXD)
VXD install
Phase 3
w/ full Belle II
PXD/SVD Combined Test (DESY)
install BEAST
install PXD

(Vertex 2014) The Belle II Pixel Detector for SuperKEKB - Michael Schnell.

Expected Background

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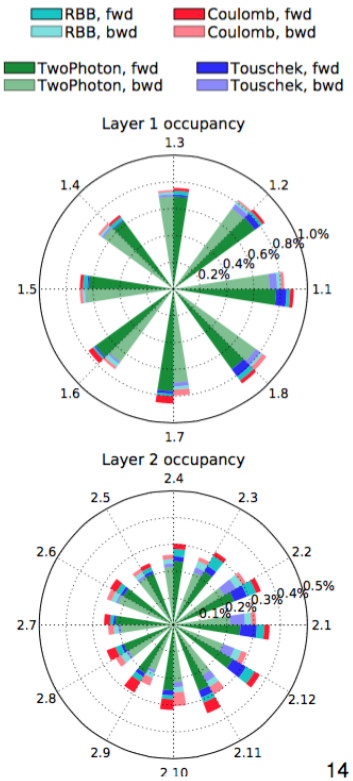
Background	Layer 1	Layer 2
QED	0.8 %	0.3 %
Touschek	< 0.03 %	< 0.03 %
Radiative Bhabha	< 0.13 %	< 0.13 %
Beam-Gas	< 0.01 %	< 0.01 %
Total	< 1.0 %	< 0.5 %

- Synchroton radiation studies ongoing
- An average $B\bar{B}$ event creates 10 tracks
- PXD is dominated by background hits!



Michael Schnell

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(Vertex 2014) The Belle II Pixel Detector for SuperKEKB - Michael Schnell.

Data Handling Processor

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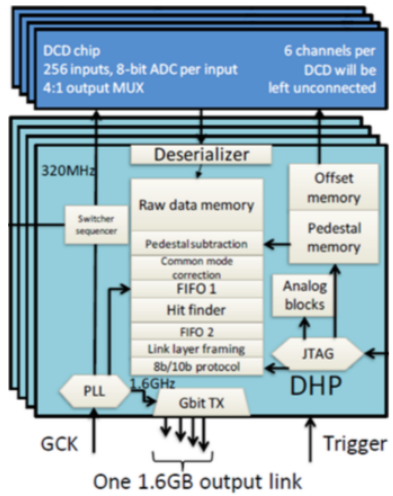
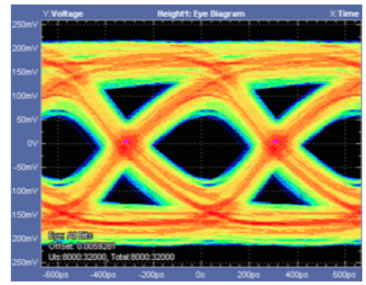
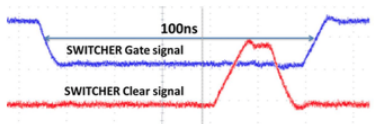
- Common mode and pedestal correction
- First step of data reduction (zero suppression)
- Data handling up to 2.6 % occupancy without loss
- Controls Switchers and DCD
- High speed data transfer with pre-emphasis link driver (50 cm Kaptonflex + 15 m Infiniband cable)







(Vertex 2014) The Belle II Pixel Detector for SuperKEKB - Michael Schnell.

DHH System

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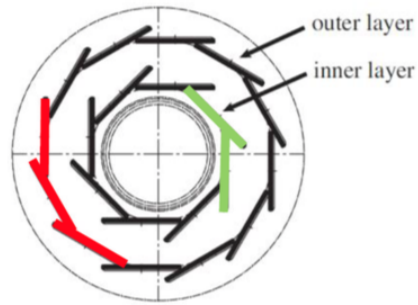
- 5 DHHs connected to one DHH Controller (DHHC)
- Load balancing: 3 layer 2 and 2 layer 1 per DHHC
- Built-on Virtex 6 FPGAs in ATCA standard
- Tasks of the DHH system:
  - Distribute timing and slow control signals to PXD FEE
  - Clustering of pixel data
  - Converting of LVDS high speed to optical signal (connected to ONSEN)



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(Vertex 2014) The Belle II Pixel Detector for SuperKEKB - Michael Schnell.

ONline SElector Node (ONSEN)

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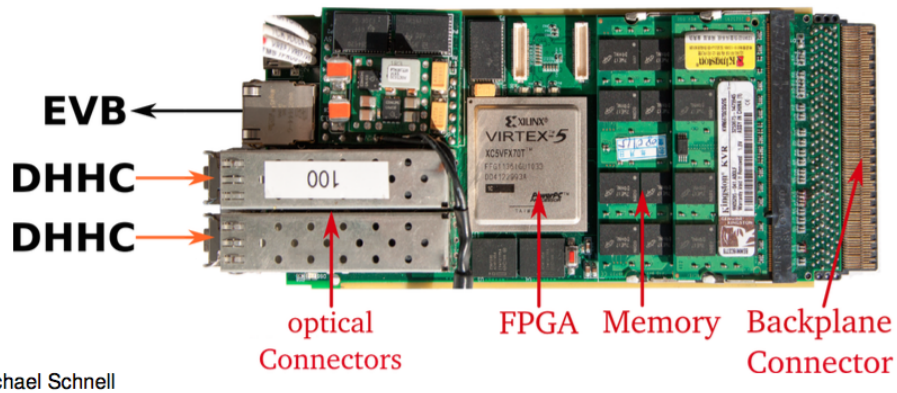
- Build on the xTCA standard
- Using Advanced Mezzanine Cards (AMC) with Virtex 5 FPGA
- Receives data from DHHC over 6.25 Gbps optical links
- Performance data reduction over pixel selection with Region Of Interests (ROI)
- Sends data to EVent Builder (EVB) over Gbit Ethernet.



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(Vertex 2014) The Belle II Pixel Detector for SuperKEKB - Michael Schnell.

New Testbeam Setup: To This!

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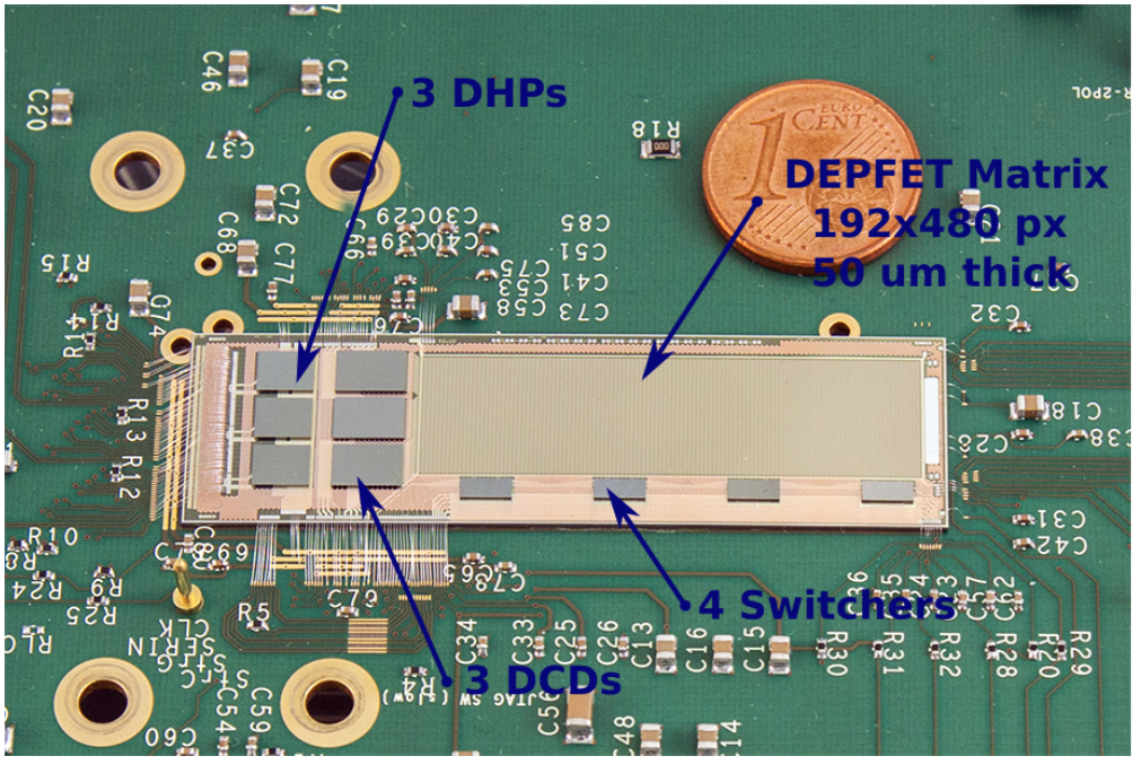
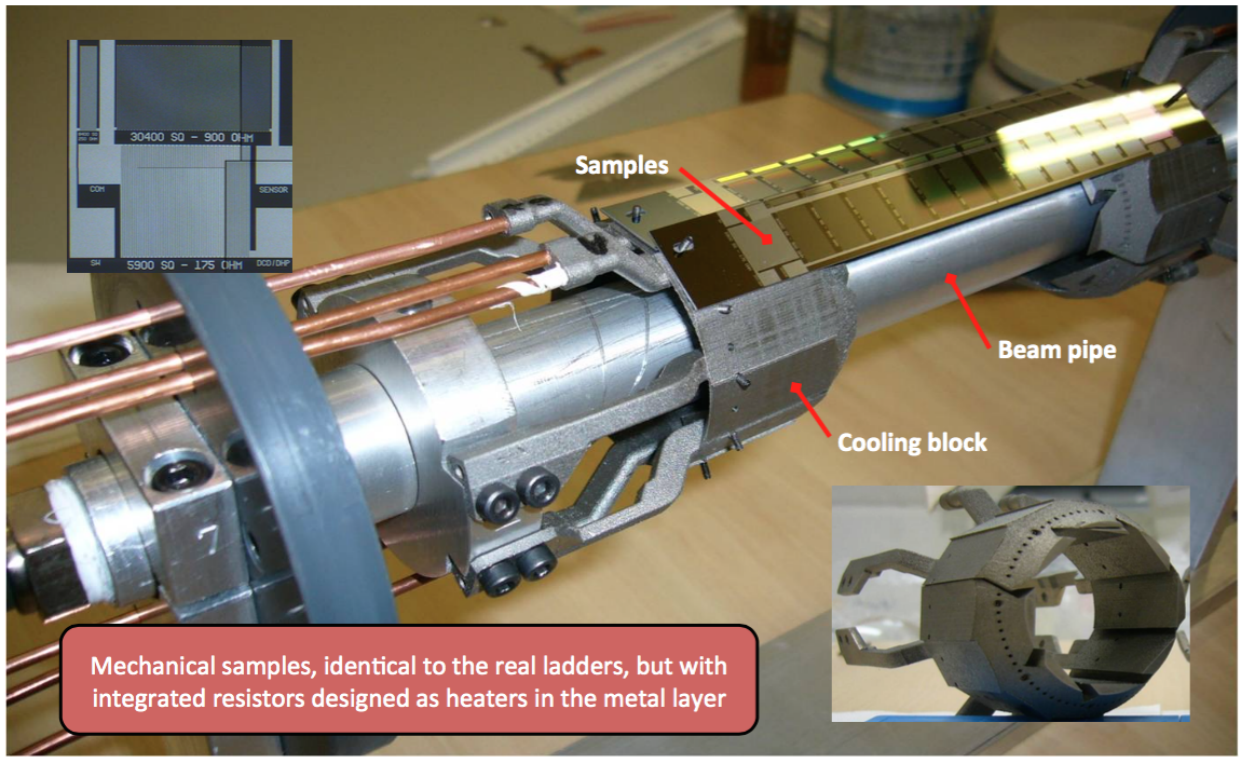


Michael Schnell 26 / 32

(Vertex 2013) The Pixel Detector for Belle II at SuperKEKB - Carlos Lacasta.

Thermo-mechanical measurements



Vertex 2013 Conference Carlos Lacasta 28

(Vertex 2013) The Pixel Detector for Belle II at SuperKEKB - Carlos Lacasta.

CO_2 cooling: MARCO

Multi-Purpose Apparatus for Research in CO_2

Collaboration between CERN, NIKHEF and MPI
Principles by CERN/NIKHEF, design and construction by MPI

Common commissioning at CERN,in July delivered to DESY for the combined PXD/SVD test

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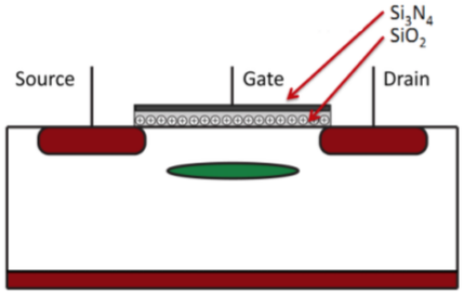
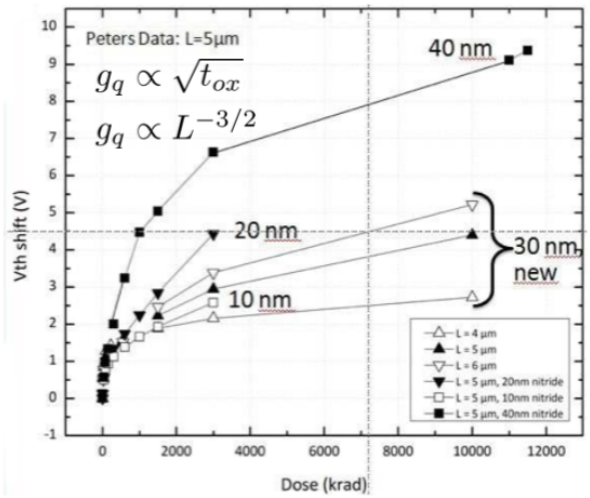
(Vertex 2013) The Pixel Detector for Belle II at SuperKEKB - Carlos Lacasta.

Radiation Tolerance

- ✓ PXD damage
  - ➔ Surface or oxide damage. Expected dose 1.9 Mrad/y
    - ↳ Change in operating voltage
    - ↳ SWB can cope with it.
  - ➔ Bulk damage Φ_{eq}=1.2x10^{13} cm^{-2} /y
    - ↳ Increase in leakage current
    - ↳ No type inversion expected until Φ_{eq}~ 2x10^{14} cm^{-2}~
- ✓ Can be operated for 10 year lifetime





Thinner gate oxide (SiO_2)
SiO_2 layer covered by an extra Si_3N_4 layer
Optimal oxide thickness is a trade of between:
- Threshold voltage shift and
- Internal amplification (g_q)

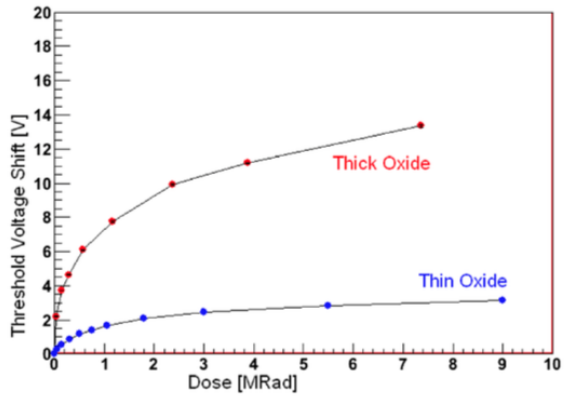
Vertex 2013 Conference Carlos Lacasta 15

Backup

(Heraeus Seminar 2013) The DEPFET Pixel Detector (PXD) for BELLE II - Paola Avella.

Radiation damages in DEPFETs

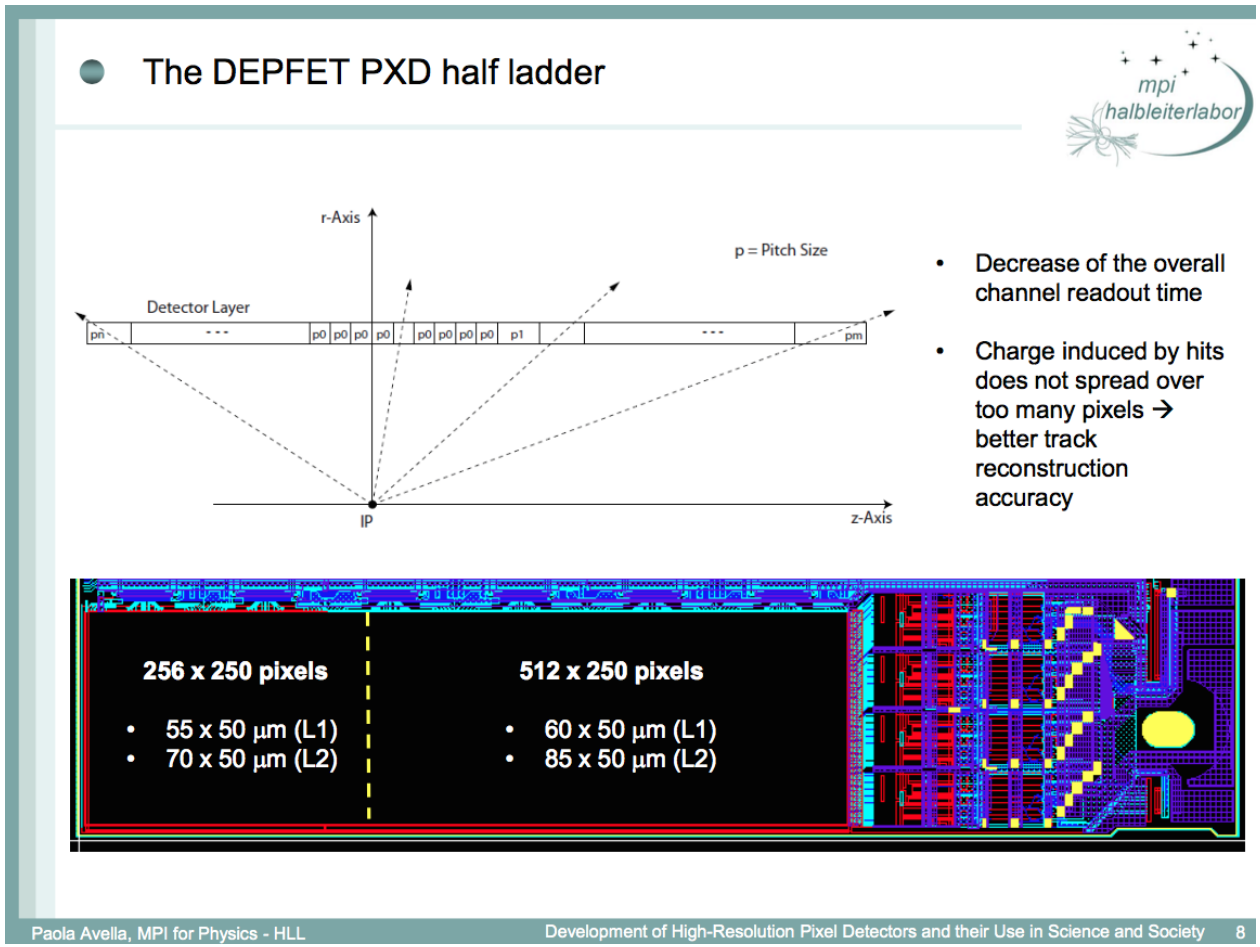
mpi halbleiterlabor



- The main cause of radiation damages in DEPFET detectors is due to *surface damages*
  → Increase of the threshold voltage → the electronics can cope with this!
- Bulk damages due to relatively low energy electrons could deteriorate the S/N → negligible effect

Paola Avella, MPI for Physics - HLL Development of High-Resolution Pixel Detectors and their Use in Science and Society 20

(Heraeus Seminar 2013) The DEPFET Pixel Detector (PXD) for BELLE II - Paola Avella.



(19th International Workshop on DEPFET - 2015) Pilot run production: yield outcome after 2nd metal - Paola Avella.

Combined* yield outcome after Al2

Yield (%)			
	W30	W35	W36
IF	75.0	100.0	100.0
OF1	100.0	100.0	100.0
OF2	100.0	100.0	100.0
OB1	99.8	99.4	0
OB2	99.6	0	99.8
IB	100.0	0	100.0
TOT	95.7	66.6	83.3

Yield calculated taking into account the following equation:

$$Yield(\%) = \frac{1}{10} \cdot (D - D_s)$$

With D the total number of drain lines (1000) and D_s the number of drain lines involved in the short.

Total number of

- perfect half ladders: 10 [6 outer (all OF) and 4 inner (2 IF + 2 IB)]
- not usable chips: 3 (1 IB + 2 OB)
- chips with faults in drain lines (as from production): 4 (all OB)
- chips damaged during testing: 2 (1 IF + 1 OB)

* After merging results from pre-tests on AC and Source and transfer characteristics

Seeon, 10-13 May 2015 P. Avella, MPP & MPG HLL 12