LHCC Poster Session - CERN, 4 March 2014

The Evolution of the Region of Interest Builder in the ATLAS Experiment at CERN

Abstract

ATLAS is a general purpose particle detector at the Large Hadron Collider (LHC) at CERN designed to measure the products of proton collisions. Given their high interaction rate (1GHz), selective triggering in real time is required to reduce the rate to the experiment's data storage capacity (1KHz). To meet this requirement, ATLAS employs a combination of hardware and software triggers to select interesting collisions for physics analysis. The Region of Interest Builder (RoIB) is an integral part of the ATLAS detector Trigger and Data Acquisition (TDAQ) chain where the coordinates of the regions of interest (RoIs) identified by the first level trigger (L1) are collected and passed to the High Level Trigger (HLT) to make a decision. While the current custom RoIB operated reliably during the first run of the LHC, it is desirable to have the RoIB more operationally maintainable in the new run, which will reach higher luminosities with an increased complexity of L1 triggers. We are responsible for migrating the functionality of the multi-card VME based RoIB into a single PCI-Express card in a commodity PC. In our testbed, we are reading out 12 channels with fragment size of 128 32 bit words at 150 KHz.

Trigger and Data Acquisition (TDAQ)

The role of the trigger and data-acquisition system is to select bunch crossings containing interesting interactions and to record the corresponding data on permanent storage. This is an extremely challenging task at the LHC because of the following:

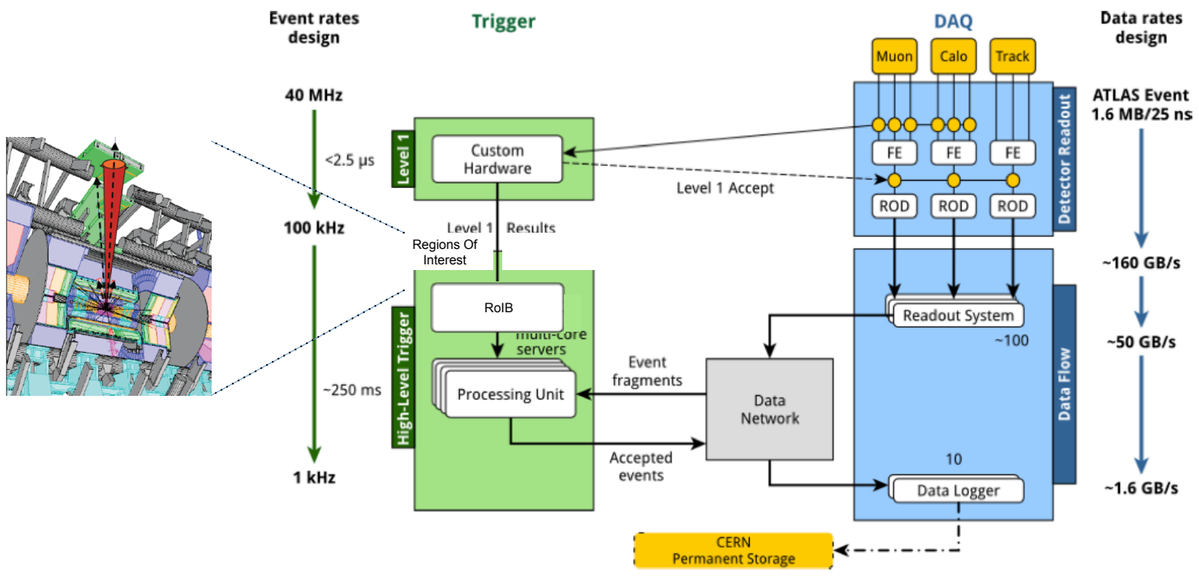
- Short bunch-crossing period (25ns): It is shorter than the time it takes particles travelling at the speed of light to traverse the detector.
- High rate of interactions per bunch crossing (pile-up): The pile-up events add to the volume of data to be read out and complicate the task of recognizing signatures of interesting interactions.
- Very high trigger selectivity: The interaction rate of 10^9 Hz (bunch crossing rate of 40 MHz) has to be reduced to 10^3 Hz to be recorded on permanent storage.
- Rare physics processes: The interesting events should be selected with high efficiency. For example, only about 1 interaction in 10^{13} would give rise to a Higgs boson decaying into four leptons.

ATLAS Readout Challenge

Property	Design Expectation (TDR)
Total channels to read out	100M
Bunch crossing rate	40MHz
Average event size	1.6MB
Data written to disk	1.6GB/s

The Trigger and DAQ performance is critical

ATLAS TDAQ System



In this readout architecture, the RoIB guides the HLT by building an event fragment with the RoIs used by the HLT to retrieve partial information from the Readout System (ROS) and thus eliminating the need to make a trigger decision based on the full detector readout which will be technically challenging and expensive at high rates.

Region of Interest Builder (RoIB)

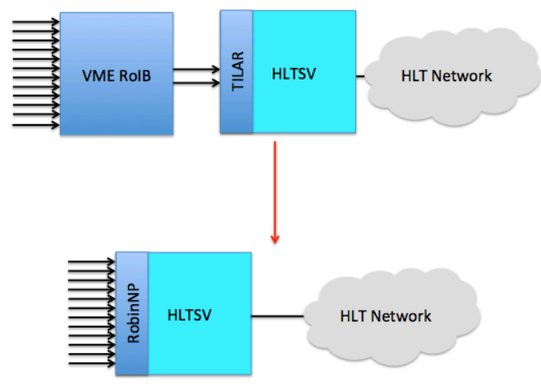
Custom RoIB:

- Custom electronics using VME bus system for data transfer.
- Backplane operates at 20 MHz and transfers 16 data bits per clock cycle for up to 12 inputs.
- Maximum data throughput: 40 MB/s per link.
- Requires 3 input cards, 2 builder cards (9U) mounted in the VME rack.

RoIB Evolution:

- RobinNP: PCI Express 8xlanes card with up to 200MB/s per link.
- 3 QSFPs: optical patch cords with 4 fiber pairs in each using the S-Link protocol.
- Guarantee the longevity of the system and facilitate its operation and scalability.
- Card widely used in the TDAQ system of ATLAS (ROS) and other LHC experiments (ALICE), broader expertise making maintenance simpler.

RoIB Evolution



HLTSV

HLT Supervisor (HLTSV) manages the HLT processing farm:

- Receives L1 results from the RoIB.
- Assigns events to HLT nodes and handles bookkeeping.
- Runs on a host PC.

Goals

Absorb the RoIB function in the HLTSV:

- Replace the custom made VME bus system of the RoIB with the RobinNP input PCIe card in the HLTSV.
- Achieve over 100 KHz readout rate with the full ATLAS TDAQ system.

Tasks:

- Test the input/output bandwidth limitation of the RobinNP using a high performance processor.
- Determine the HLTSV host PC specifications
- Test the performance of the HLTSV after the installation of the new RobinNP.
- Perform a full integration test of the ATLAS TDAQ system with the RobinNP.

System Specifications

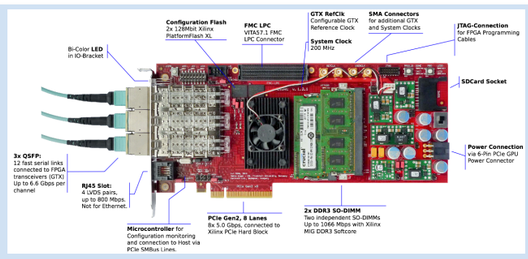
Host PC

PC configuration used for our tests:

- Intel(R) Xeon(R) CPU E5-1650 v2 @ 3.5GHz
- Memory: 16 GB
- Cache: 12 MB
- Cores: 6

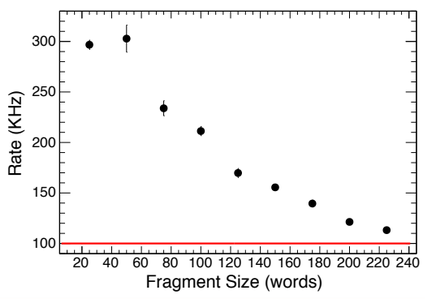
RobinNP

- ALICE CRORC with ATLAS firmware and software
- PCI Express 8xlanes
- FPGA: Xilinx Virtex-6 @ 125MHz
- Buffer memory: DDR3-1600 SO-DIMM RAM 2x4GB
- 12 Input channels

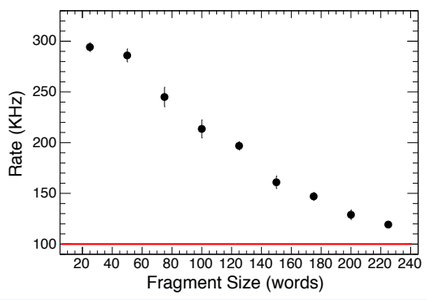


Results

Internal generation with 12 channels



External generation with 12 channels



- We are able to read out 12 channels at 150 KHz for fragments with a size of 128 32 bit words, the maximum expected size of an RoIB fragment, generated by an external source.
- The benchmarking machine used provides the needed performance.

Outlook

The new RobinNP based RoIB will add stability and flexibility to the ATLAS TDAQ system where cards can be replaced or added to increase the number of channels while maintaining high readout rates.
Currently, the RobinNP software is being included in the HLTSV framework in preparation for a full integration test of the readout performance. The final performance will be determined at point 1 with a realistic CPU and networking load.

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