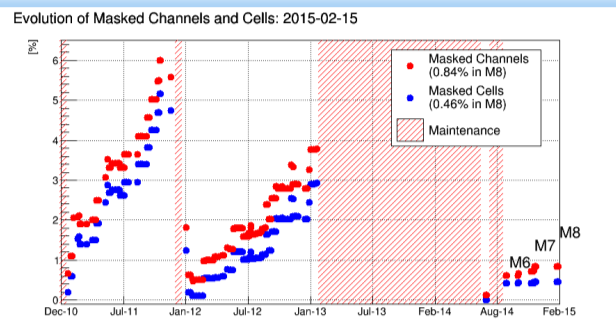


The ATLAS Tile Calorimeter for Run II and towards Phase II

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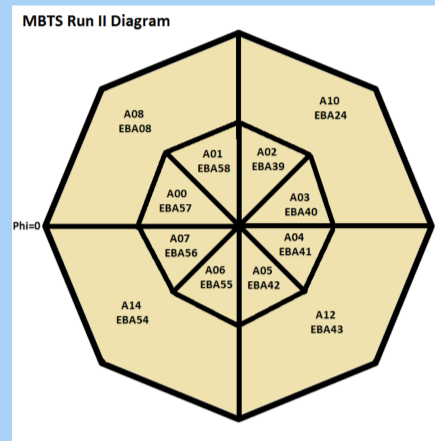
This is a presentation of the status of the ATLAS Tile Calorimeter at the beginning of the LHC Run II. TileCal is the hadronic central tile calorimeter of the ATLAS experiment of the LHC at CERN. It is based on a sampling technique using scintillating tiles as active material embedded in iron absorber plates. Consolidation during Long Shutdown 1 included the repair of masked cells and the replacement of Low Voltage Power Supplies. The Tile-Muon Trigger is scheduled to be ready for 25ns collisions and the entire Calibration System has been rerun. A new signal reconstruction that reduces out-of-time pile-up will be applied for Run II and the whole TileCal read-out electronics is being replaced in Phase-II.

CONSOLIDATION DURING THE LONG SHUTDOWN 1 (LS1)



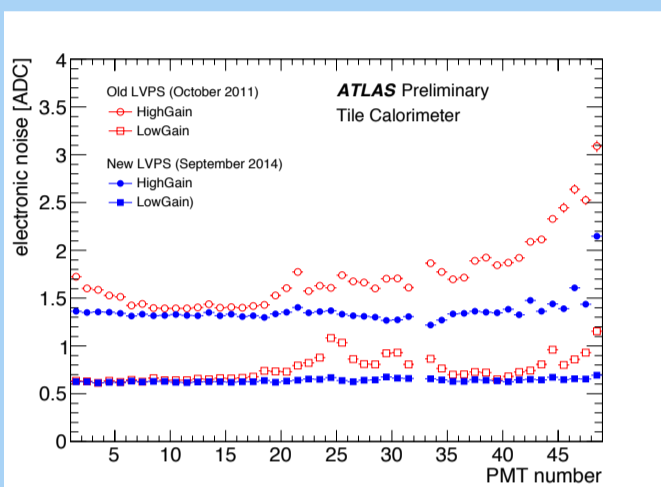
Masked Channels

- Consolidation Campaign successfully **repaired masked channels** of Run I
- The status during last weeks has stayed approximately constant
- The current level of masked channels is below 1%



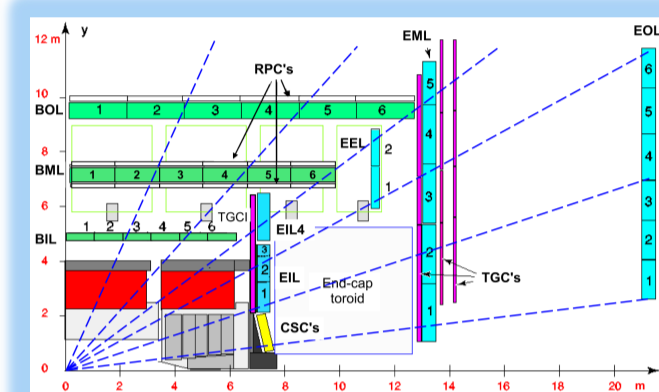
Minimum Bias Trigger Scintillators

- MBTS have been replaced**, due to irradiation during Run I
- Small increase of acceptance in η , $2.08 < |\eta| < 3.86$ (in Run I was 3.75)
- Reduced granularity** in outer counters to obtain full phi coverage of Tile Crack scintillators
- New light collection layout for a more homogeneous response from the tiles
- Installed in the experimental cavern in 2014



New Low Voltage Power Supplies

- New LVPS installed during LS1, which provide **greater robustness against power trips**
- Electronic noise has been reduced considerably (mainly non-Gaussian tails) from October 2011, when an older version of the LVPSs was present in the drawers, to September 2014, after the LS1 maintenance campaign and installation of newer LVPSs



Tile-Muon Trigger Project

- Coincidence of TGC inner chambers and Tile D-layer in $1.0 < |\eta| < 1.3$ to reduce fake triggers
- 82% fake reduction** for signals above 500 MeV deposits in Tile
- Tile-Muon Trigger in schedule to be ready for 25ns collisions with 16 boards (Extended Barrel)

CALIBRATION

Laser II System

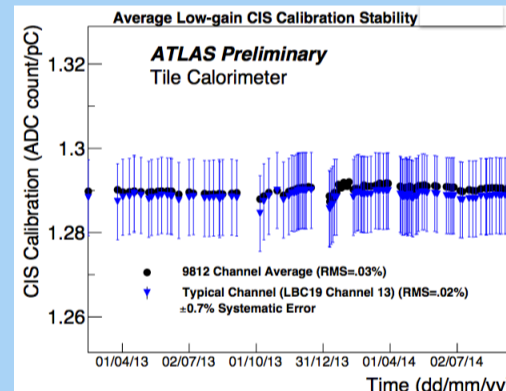
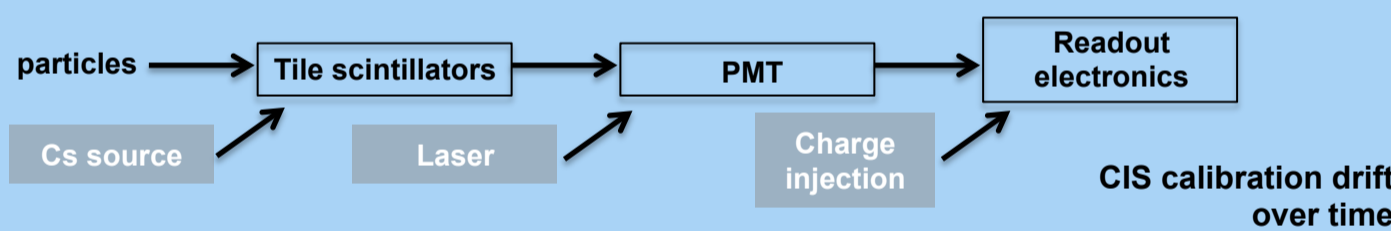
- Installation of a **new Laser system** in October 2014 in USA15: new source, optics and electronics
- Ongoing commissioning:
 - DAQ commissioning during last weeks
 - Good laser pulse-to-pulse **stability**: <3%
 - Focus on the stability of the photodiode response
- Close to study the PMT stability in time

Charge Injection System

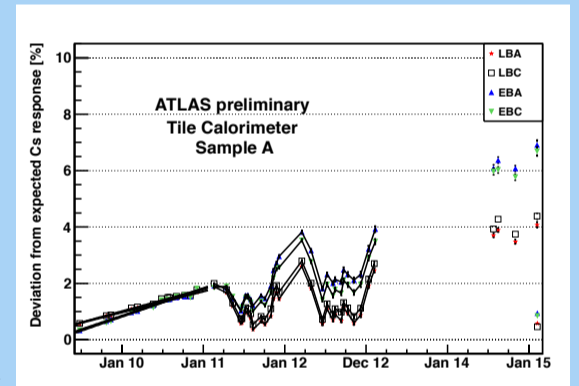
- CIS is used to define the ADC count to pC conversion for the High Gain and Low Gain readout
- Since the end of LS1 consolidation and maintenance period, vast majority of TileCal channels have been **stable** from a CIS perspective

Cesium Calibration System

- Newest Cs scan without magnetic field
- Results show **similar up-drift as in the past**
- First iteration to set the HV based on Cs (same procedure adopted before Run I)
- More Cs scans in the next week/months with full magnetic fields



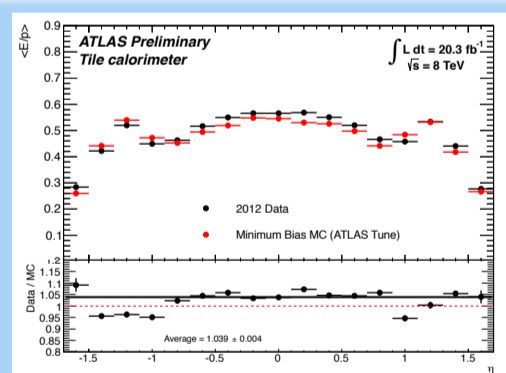
Deviation from expected Cs response over time for layer A



DATA PREPARATION AND PERFORMANCE

Response to isolated charged hadrons

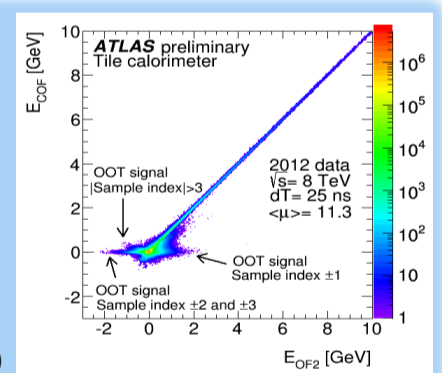
- This measurement can be used to place constraints on the systematic uncertainty for the jet and tau energy scales
- Comparisons 2012 data/MC are within few percent in all detector regions and are **compatible** with 2011 and 2010 measurements



New signal reconstruction for Run II

- Offline: **Constrained Optimal Filtering (COF)**. COF is a 2-step algorithm that aims to identify signals within the 7 bunch crossing read-out window
 - Better performance** than Optimal Filtering 2 (OF2) in high pile-up conditions
- Online: Optimal Filtering (OF1)

COF method (run II) vs OF2 method (run I)

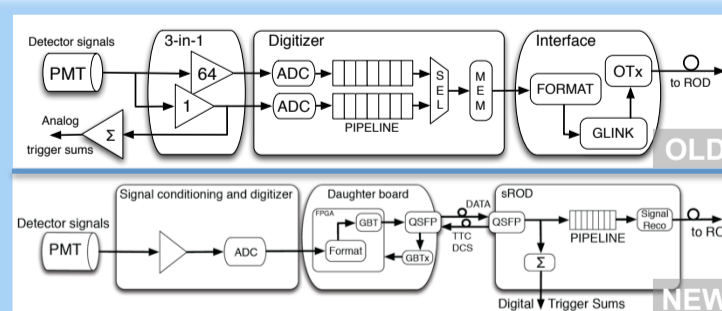


UPGRADE PHASE-II

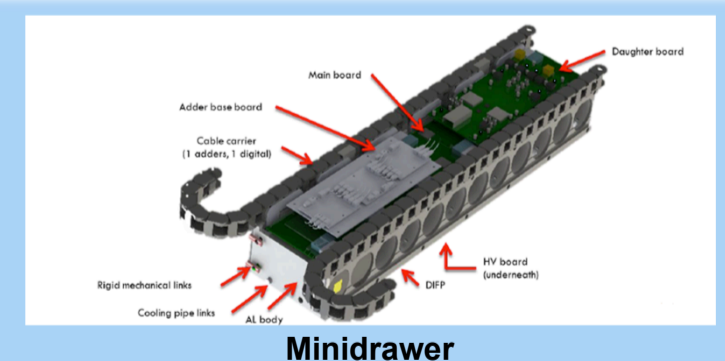
Introduction

TileCal plans a complete replacement of the read-out electronics in Phase-II (except the PMTs). The new read-out architecture will transfer full digitized data to the off-detector system requiring a total data bandwidth of 80 Tbps.

The **demonstrator project** aims to evaluate and qualify the new proposed read-out electronics. The validation program will include standalone beam tests and the insertion of the new electronics in part of the real detector.



Old and new architectures of the read-out electronics



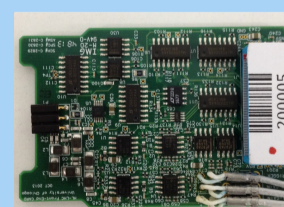
Minidrawer

On-detector electronics

Front-End boards

Three alternatives being evaluated:

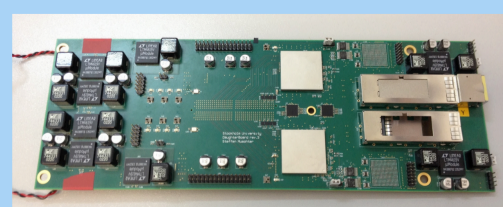
- The **modified 3-in-1** cards based on the current design using discrete components.
- The **QIE ASIC** is a Charge Integrator and Encoder based on a current splitter.
- The **FATALIC ASIC** solution is a current conveyor with pulse shaping and ADC functionalities.



New 3in1

Mainboard and Daughterboard

The **Mainboard** is the data and control interface between the very front-end boards and the Daughterboard. For each of the three alternatives a different type of Mainboard is required for the digitization of the signals of 12 PMTs. The **Daughterboard** provides high speed communication between on- and off-detector electronics. Each side of the board hosts a Kintex7 FPGA that receives the digitized data from the Mainboard and transmits it to the sROD.



Daughterboard

Off-detector electronics

sROD demonstrator module

- Interface between the detector and the L0/L1 trigger and DAQ systems.
- The module is equipped with Virtex7 and Kintex7 FPGAs. It is compliant with double AMC format to be in an Advanced Telecommunications Computing Architecture (ATCA) carrier.
- It includes four QSFP connectors which provide full duplex communication with four MiniDrawers.

