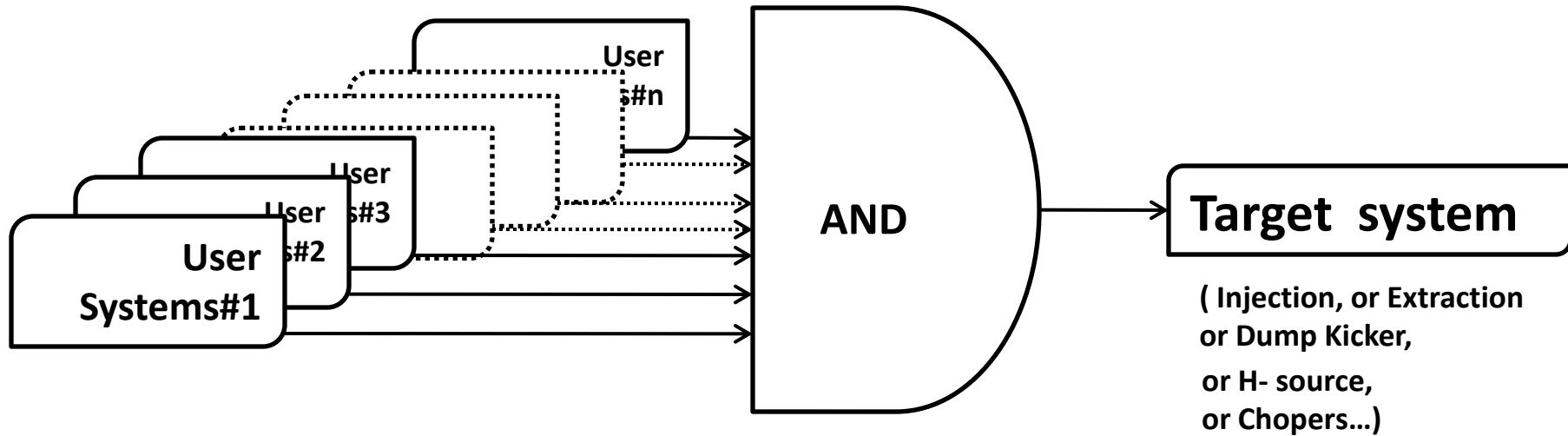**Technical Workshop
on the Beam Interlock System(s) for CERN and ESS
(3rd and 4th of February** 2015)

Quick Overview
of the
Beam Interlock System
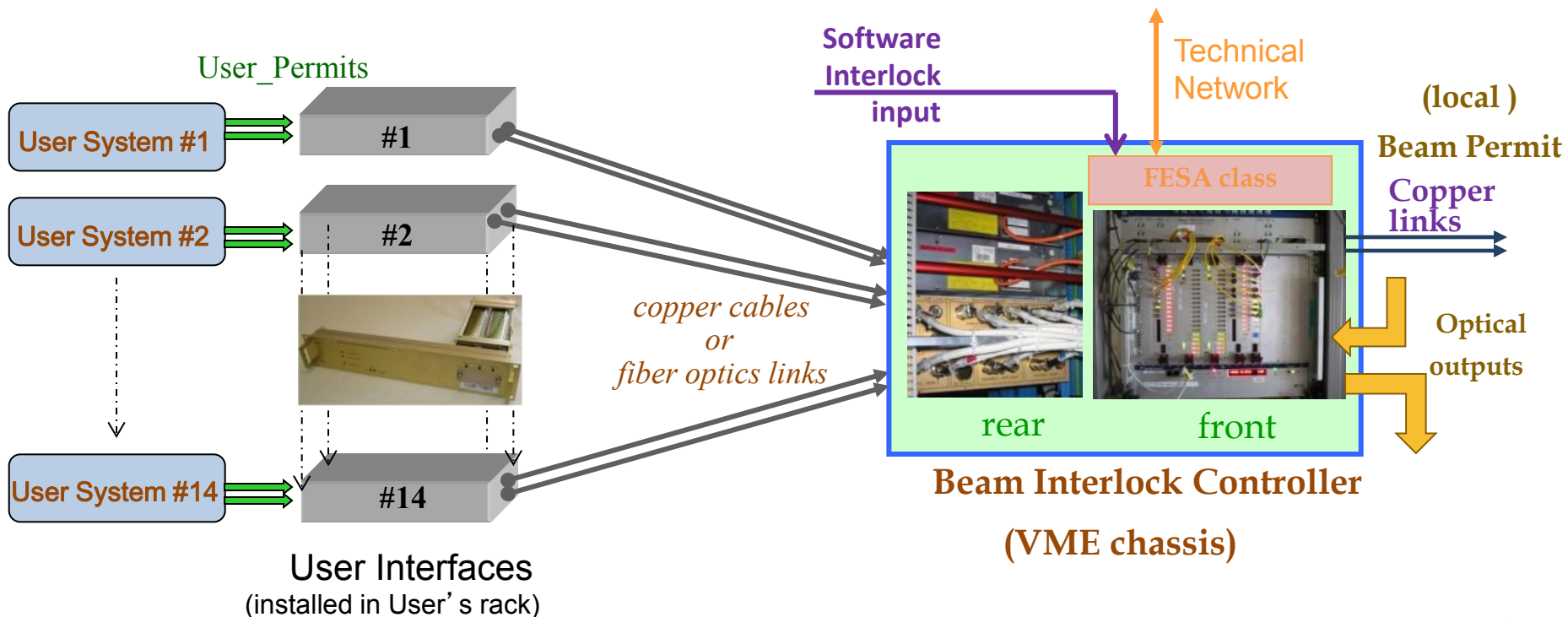# for LINAC4

Bruno PUCCIO
TE/MPE

BIS Principle

User Systems#1

User Systems#2

User Systems#3

User Systems#n

AND

Target system

(Injection, or Extraction or Dump Kicker,

or H- source,
or Chopers...)

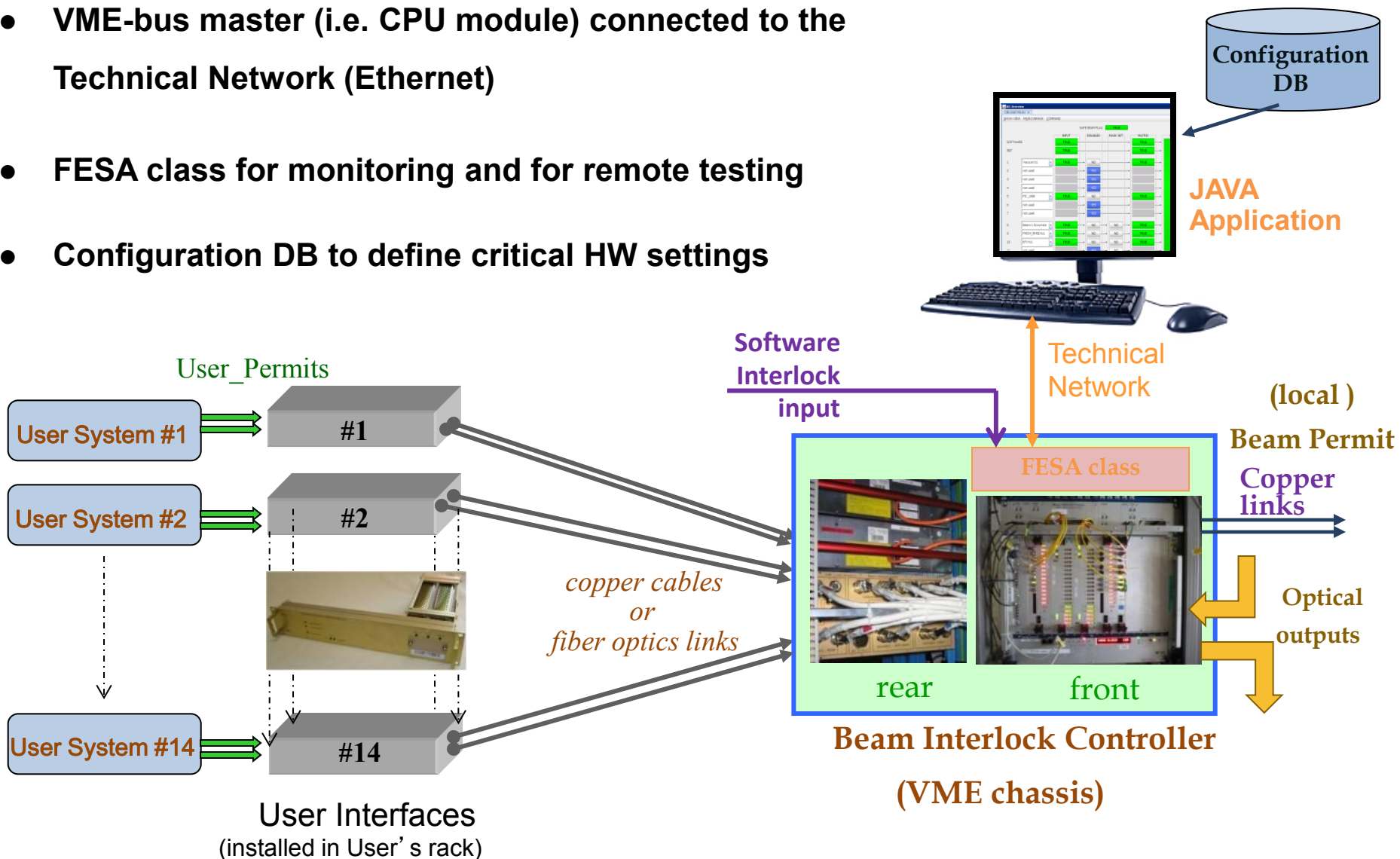$$\Sigma \text{ (User Permit } = \text{ « TRUE ») } \rightarrow \text{ Beam Permit } = \text{ « TRUE »}$$

Beam Interlock System : simplified layout

- ❑ **Remote User Interfaces safely transmit Permit signals from connected systems to Controller**

- ❑ **Controller acts as a concentrator,**
  - • **collecting User Systems Permits (14 HW + 1SW)**
  - • **generating local Beam Permit**

- ❑ **Controllers linked either in Tree or in Ring architecture**

User_Permits

User System #1 → #1

User System #2 → #2

User System #14 → #14

copper cables
or
fiber optics links

User Interfaces
(installed in User's rack)

Software Interlock input

Technical Network

(local) Beam Permit

FESA class

Copper links

rear   front

Optical outputs

Beam Interlock Controller

(VME chassis)

Bruno Puccio / Technical Workshop on the Beam Interlock System(s) for CERN and ESS (3rd and 4th of February 2015)

Beam Interlock System : simplified layout 1/2

- **VME-bus master (i.e. CPU module) connected to the Technical Network (Ethernet)**

- **FESA class for monitoring and for remote testing**

- **Configuration DB to define critical HW settings**

Configuration DB

JAVA Application

Software Interlock input

Technical Network

User_Permits

User System #1 → #1

User System #2 → #2

User System #14 → #14

copper cables or fiber optics links

User Interfaces
(installed in User's rack)

FESA class

rear   front

Beam Interlock Controller

(VME chassis)

(local) Beam Permit

Copper links

Optical outputs

Bruno Puccio / Technical Workshop on the Beam Interlock System(s) for CERN and ESS (3rd and 4th of February 2015)

BIS & SIS : the link with Software Interlocks

**thanks to a 15th input available on <u>each</u> Beam Interlock Controller,
the Software Interlock (SIS) is an input to the Hardware Interlock system**
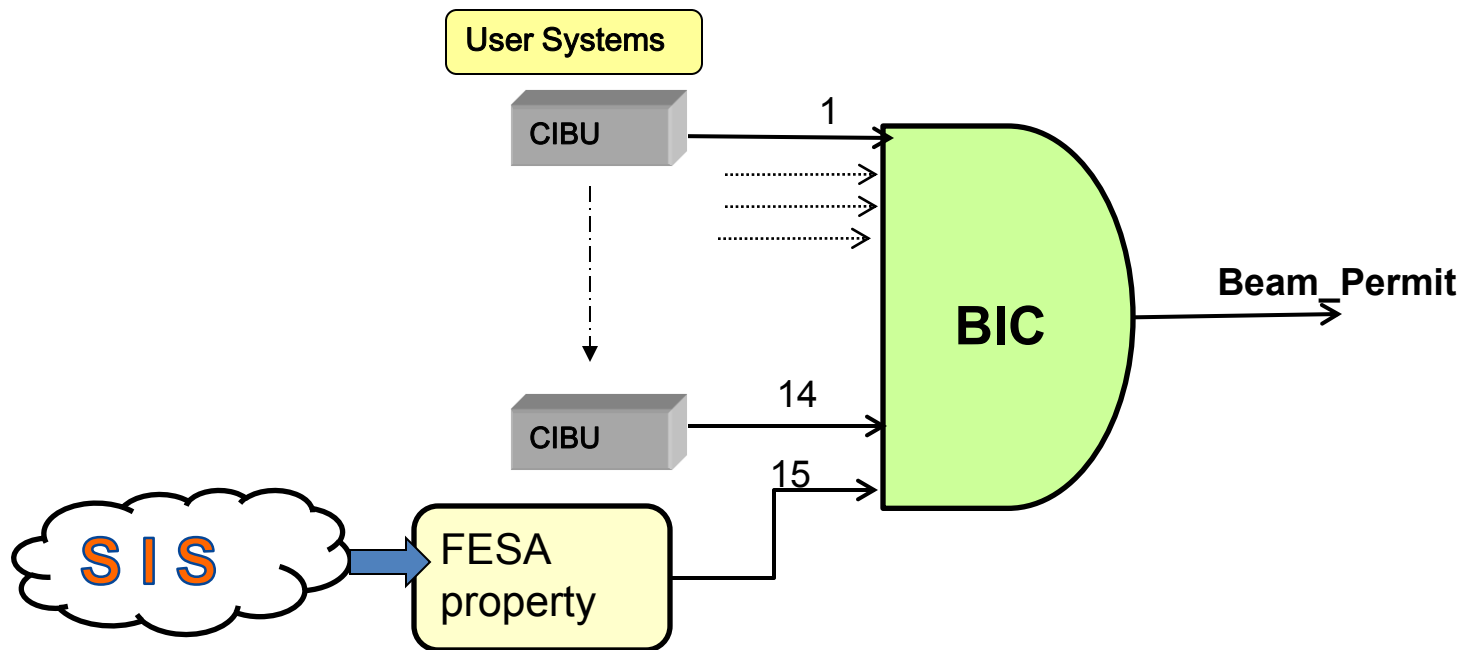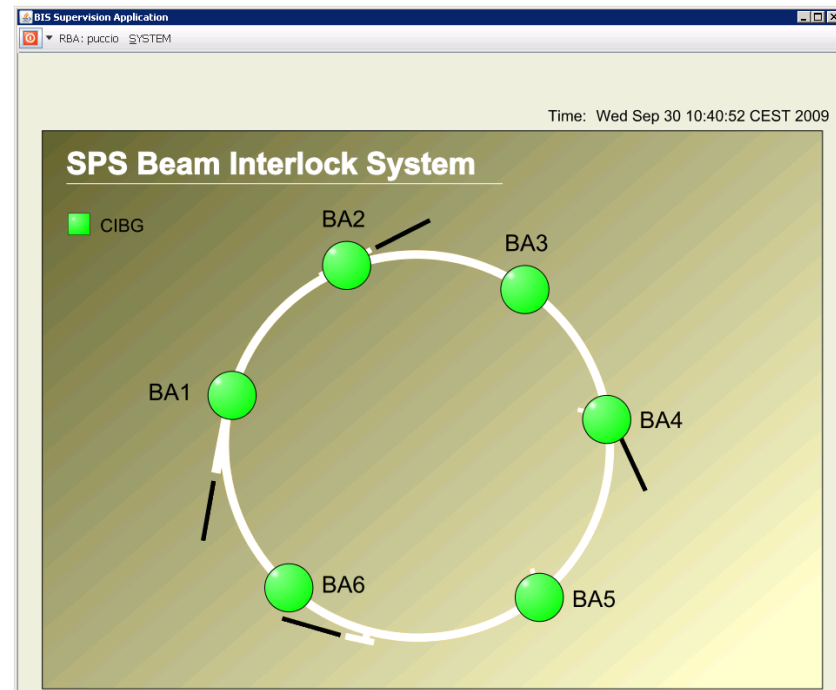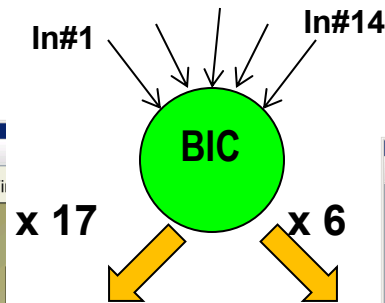

More details in next presentations

Scalability & Ring architecture
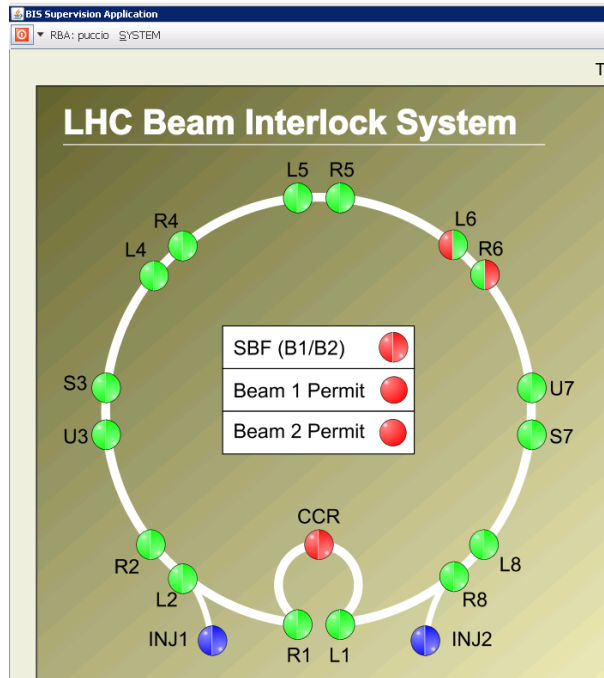

Screen shot of the Supervision application

Screen shot of the Supervision application

In the Ring Architecture: each Controller "shares" the redundant Beam Permit Loops.

Frequency signals passing through the different BICs and through the corresponding Kicker system.

Scalability & Tree architecture

– **Slave BICs**: AND operation of the max. 15 inputs
– **Master BIC**: AND and OR operations possible
  - Inputs: either outputs from Slave BICs or additional USER_PERMIT inputs

In the Tree Architecture, the (Local) Beam Permit signal is transmitted to the Master BIC via copper links
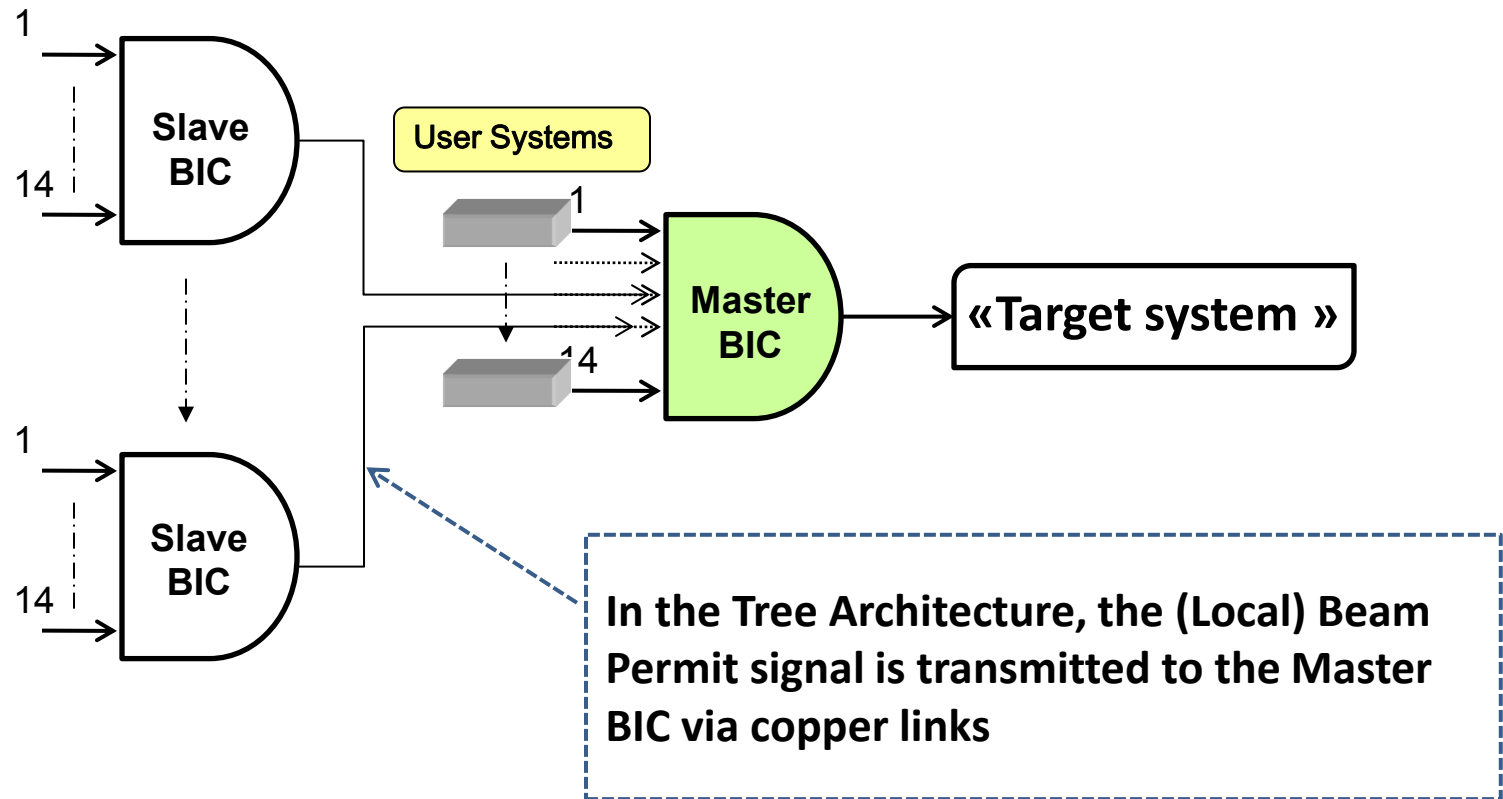
The Tree Architecture is currently used in both SPS-LHC Transfer lines and LINAC4

Master BIC : Matrix of AND and OR operation

Equations for the SPS Beam Extraction interlock

THE BIS Configuration DB

Oracle DB to describe critical HW settings.

Used for Pre-Operational & Post-Op. checks, also used for the BIS Application, etc…
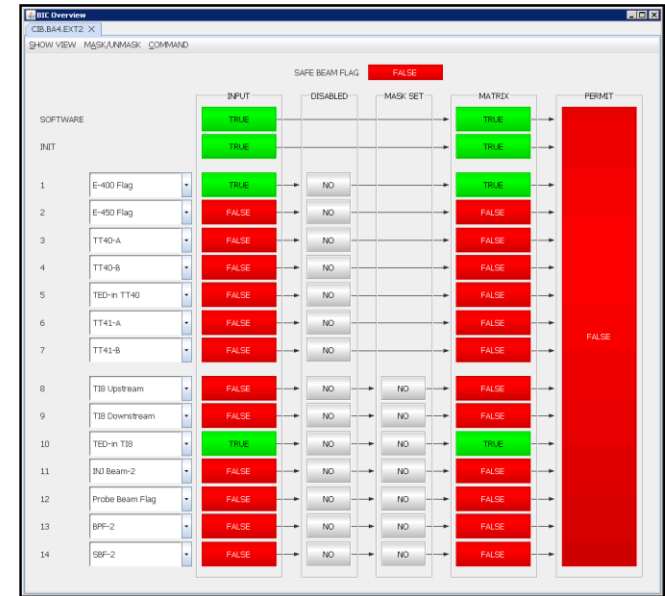
BIS Application : the I/O view

Active input

ID# of the corresponding CIBU unit

Hardware modules

More details in next presentations

User Interface

Redundant P.S.

Optical daughter cards
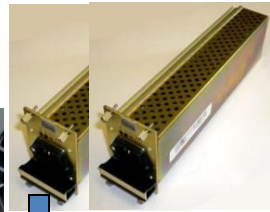
Manager

Test & Monitoring

F.O. variant of the User Interface
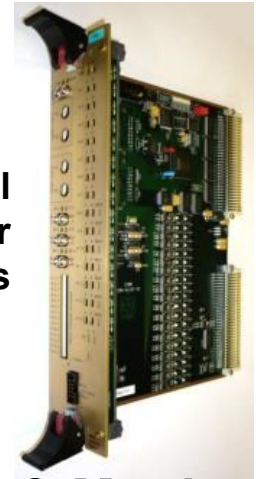
Back Panel

User system's side

Controller's side

BIS interface (CIBU)

Front view

rear view
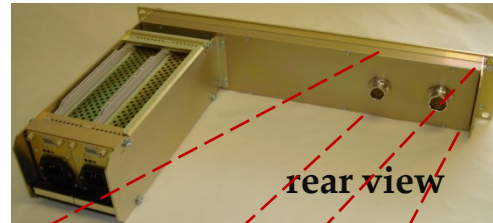
Unique HW solution for connecting any User System via a copper cable
[F.O. variant available for long link (>1.2km)]

User System

Could be PLC based, or VME based, or any type of electronics…

User_Permit_A+

User_Permit_A-

User_Permit state transmitted in RS485 format

to Controller
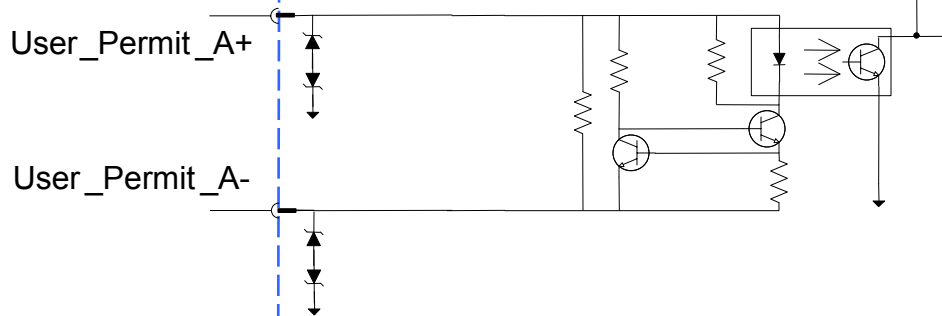
User_Permit = "FALSE" if Input current < ~10mA

More details in next presentations

BIS Reaction Time

(LHC case)
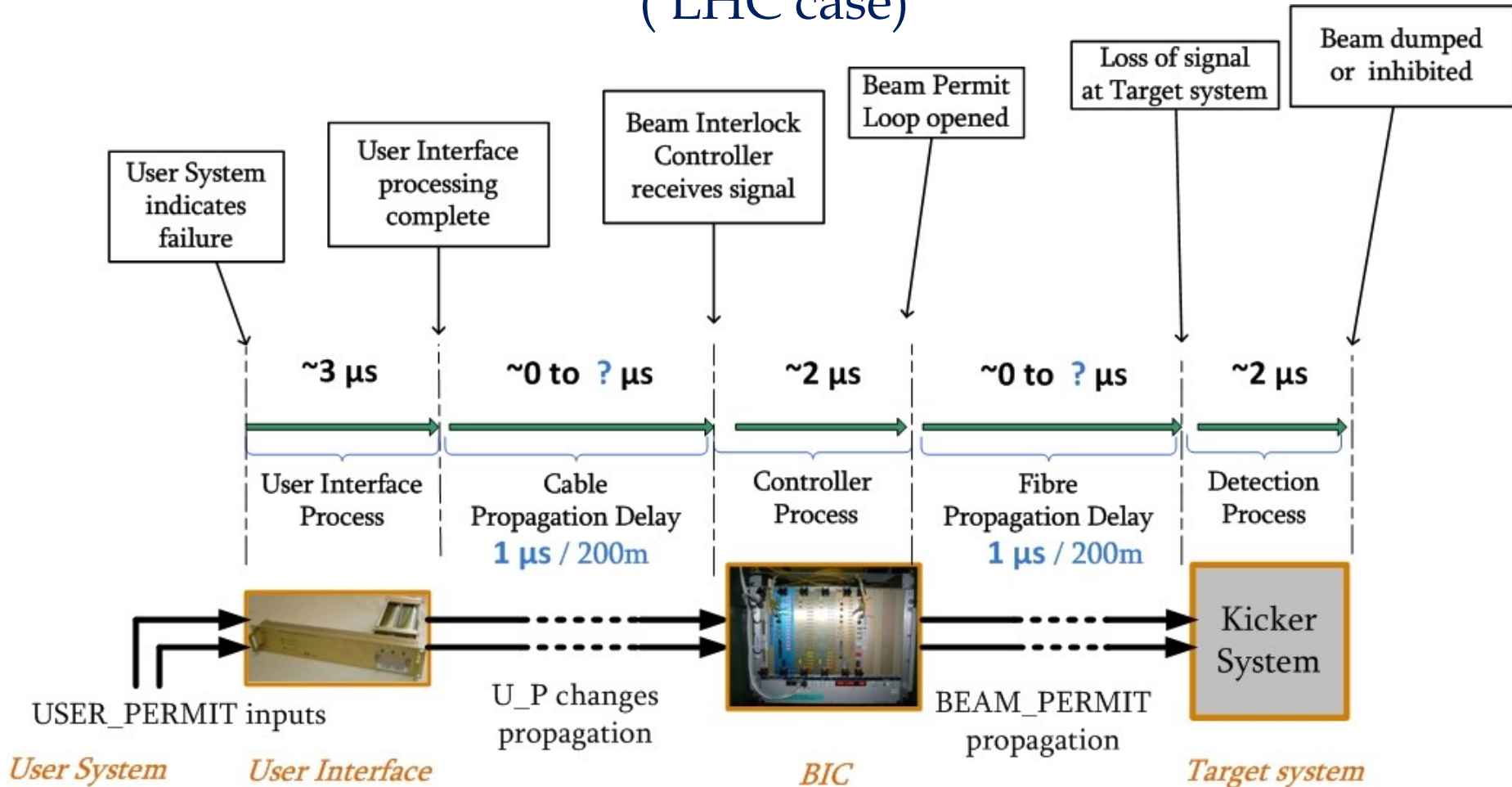
BIS layout for Linac4

BIS for Linac4 & PS Booster : the interlock zones

- ## Linac4 interlock zones
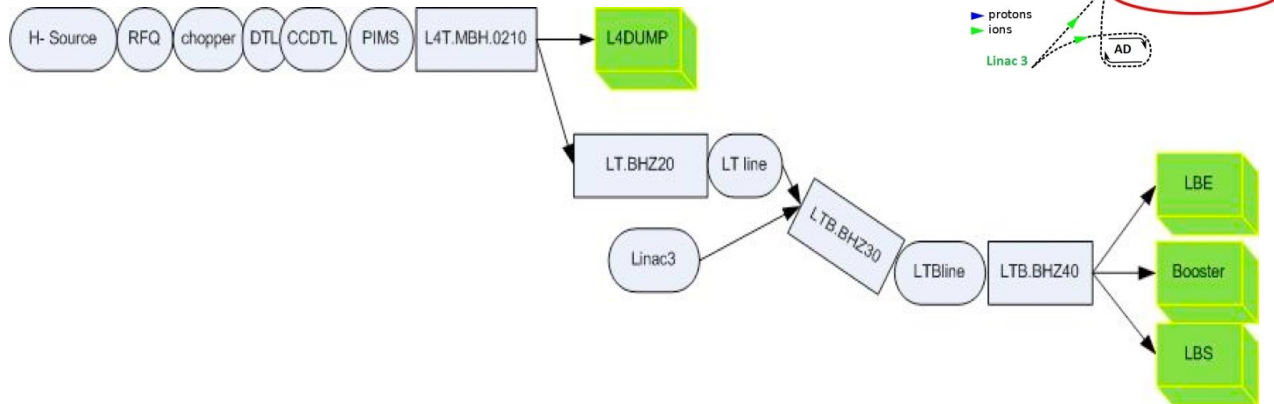
- ## PSB interlock zones
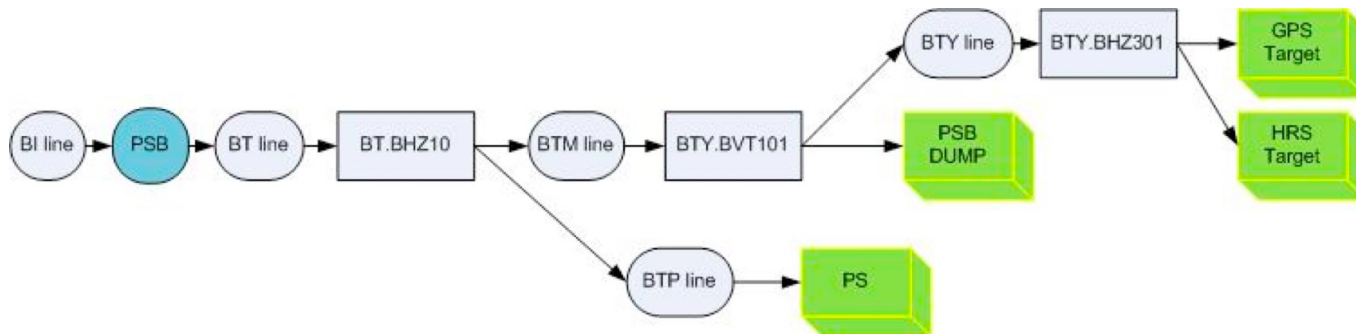
Beam Interlock System – Design Principle (1)

- Main constraints:
  - Multiple 'interlock zones' due to several destinations
    - Destinations for Linac4: L4DUMP, LBE, LBS, PSB and PS ring
    - PSB destinations: BDUMP, ISOGPS, ISOHRS, PS

  - PSB machine is (timing) master of Linac4
    - Maximize proton delivery to the experiments via '**External Conditions**'; the "user" (+beam destination) is calculated for the current cycle depending on some necessary conditions;

      This analysis takes up to 3 basic periods and yields the decision if the 'normal' or 'spare' (or none) cycle should be executed
    - Beam stoppers and bending magnet rise-time too slow

➔ BIS for PSB and BIS for Linac4 must be considered together

Courtesy B. Mikulec

BIS for Linac4 : Design Principle (2)

- Three main ingredients:

  1. Hardware interlock system (BIS): reliable, fast
     - For fast reaction times
     - If considered useful to avoid machine activation

  2. Software interlock system (SIS): flexible
     - For slow-changing parameters
     - If some more complex logic needs to be adopted

  3. External conditions (EC): for proton optimization
     - Consider user requests
     - Method also useful for ring-specific interlocks

Courtesy B. Mikulec

BIS for Linac4 : Design Principle (3)

- Hybrid beam interlock concept based on BIS, SIS and EC.

- Engineering Specification = EDMS # 1016233

    Timings and tolerance defined for each interlock condition (outside scope of this document)

CERN
CH-1211 Geneva 23
Switzerland

LINAC4 Project Document No
L4-CIB-ES-0001 rev. 1.0

CERN-Div/Group or Supplier/Contractor Document No
BE/OP

EDMS Document No
1016233

Date: 2013-08-14

Engineering Specification

BEAM INTERLOCK SPECIFICATIONS FOR LINAC4, TRANSFER LINES AND PS BOOSTER WITH LINAC4

Abstract

The beam interlock system for Linac4 and its transfer lines to the PSB will be based on a mixed system comprising hardware interlocks provided via the BIS (Beam Interlock System), software interlocks based on the SIS (Software Interlock System) and the concept of External Conditions used currently in the PS complex. This document summarises the beam interlock specifications to safely operate Linac4, the Linac4-to-PSB transfer lines and the PSB with Linac4 injection.

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Reminder: The Beam Interlock System does not include personnel safety systems !

BIS Layout of Linac4 and Booster
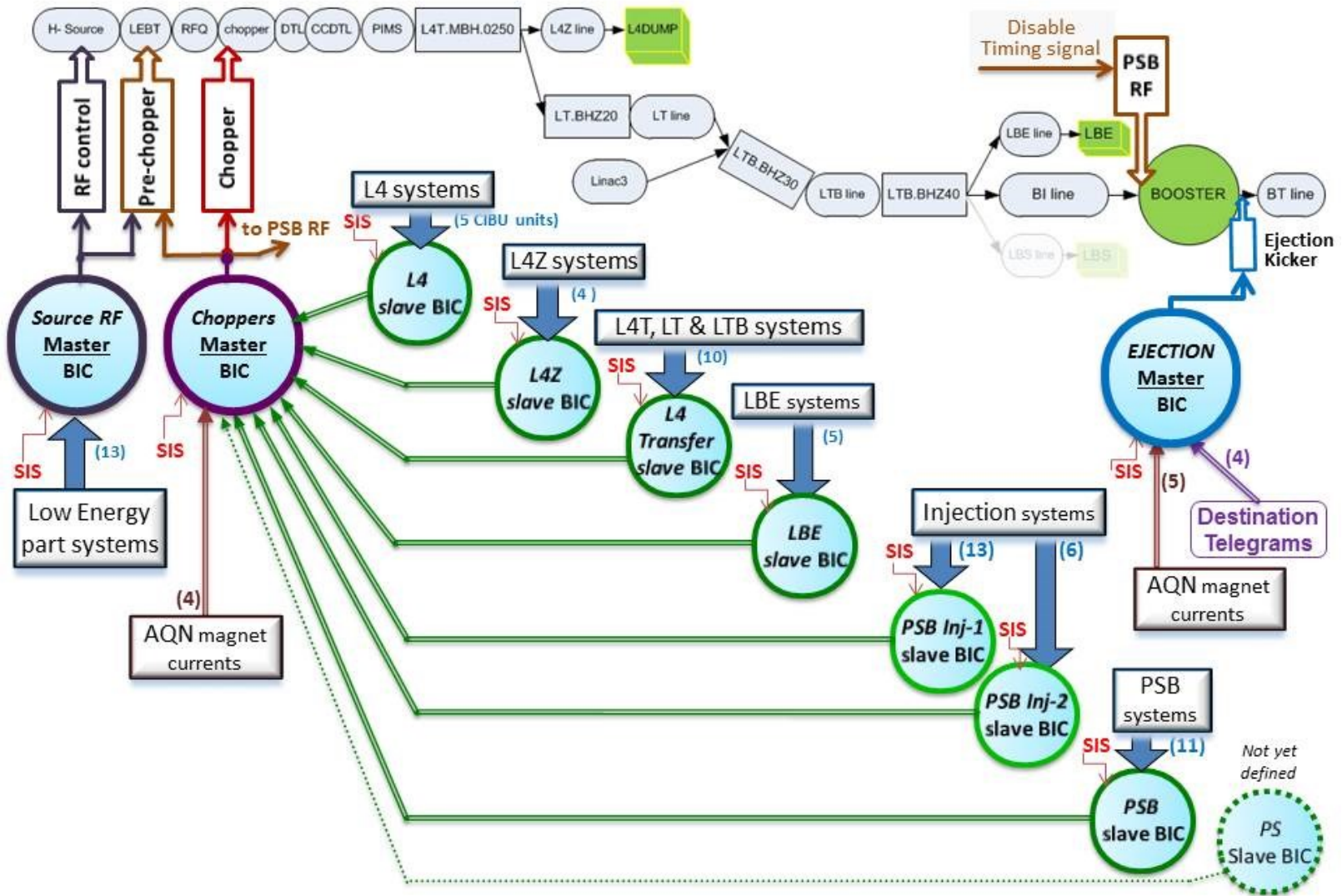
BIS Linac4 (1/4) : the Master BIC 'Source RF'
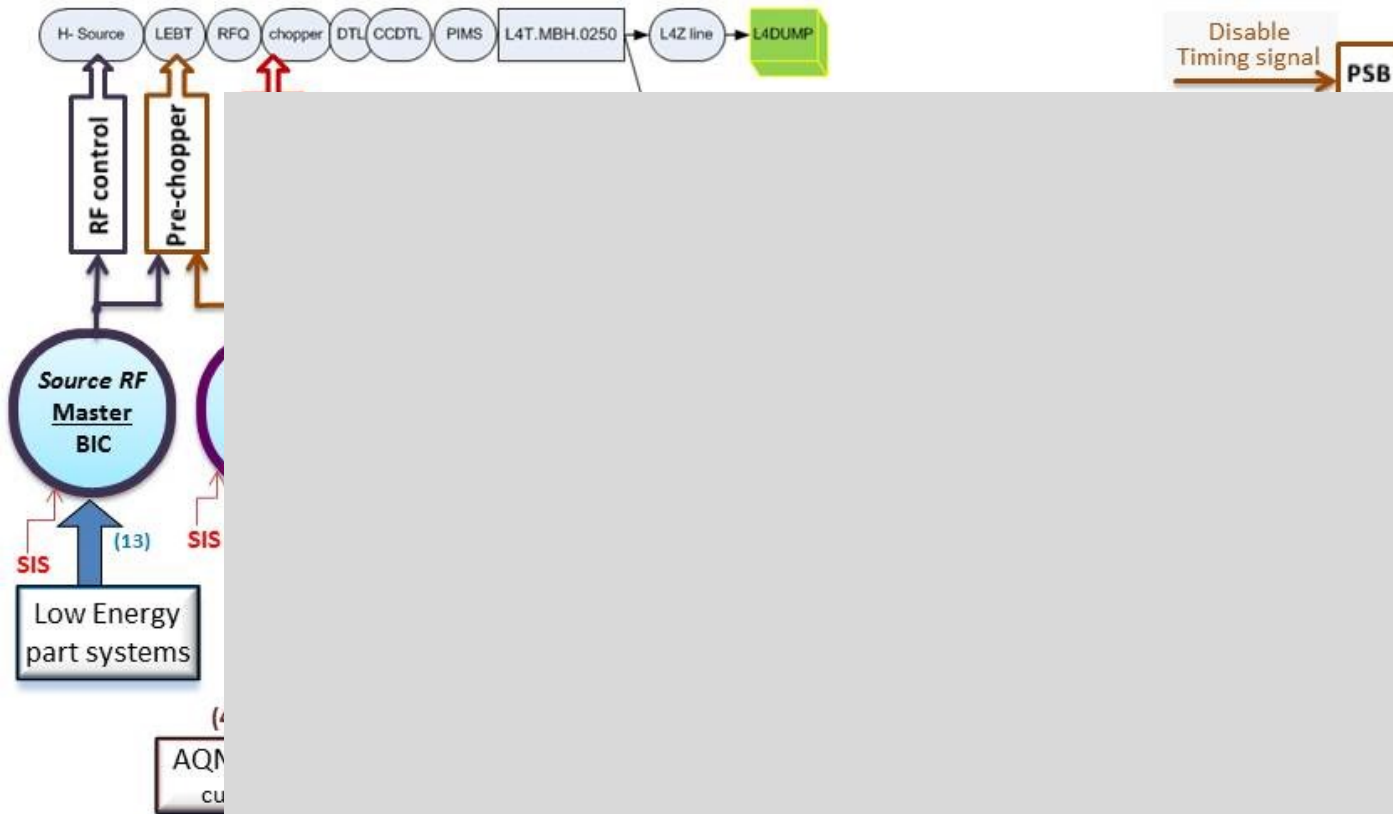
Master BIC 'Source RF'

Role: Manage interlocks from equipment that are installed <u>upstream of the DTL</u>.

Action:
- Switch off the RF of the H$^-$ source and
- Pulse the pre-chopper for redundancy reasons.

<u>Note:</u> In case of an interlock, an immediate repair action will be required.
During access or whenever the beam stopper will be inserted, the source needs to be pulsing continuously to guarantee beam current stability.

=> 2-line equation:
- Beam Stoppers are IN
- Beam Stoppers are OUT (or moving)

		Interlock Element	Ch.
↰	↰	SIS	0
↰	↰	Source Internal	1
↰	↰	Source HV	2
✕	↰	Pre-chopper	3
O	↰	Source Beam Stoppers Out/Moving	4
↰	O	Source Beam Stoppers In	5
✕	↰	Chopper	6
✕	↰	L4 Low-Energy Watchdog	7
✕	↰	L4 Low-Energy Vacuum Valves	8
✕	↰	AQN L4L.QUADS	9
✕	↰	RFQ	10
✕	↰	CCC Operator Veto	11
✕	↰	L4 Operator Veto	12
✕	↰	Not used	13
✕	↰	Not used	14
↰	↰	H$^-$ Source Beam_Permit	OUT

BIS Linac4 (2/4) : the Master BIC 'Choppers'

Bruno Puccio / Technical Workshop on the Beam Interlock System(s) for CERN and ESS (3rd and 4th of February 2015)
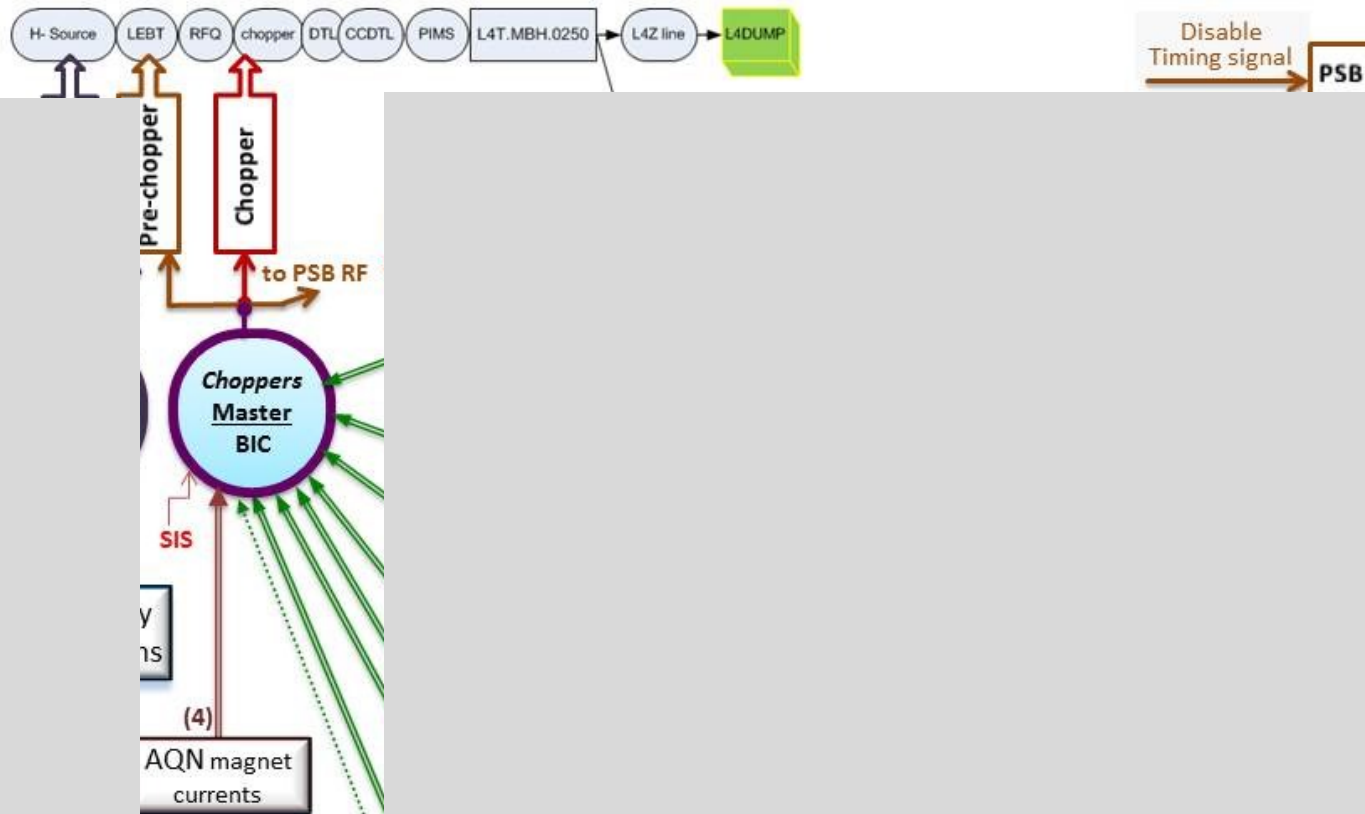
Master BIC 'Choppers'

Role: Assure valid conditions for all Linac4 destinations: Linac4 dump, LBE, LBS, PS Booster & PS ring.
To define these destinations, the magnet current acquisitions of the corresponding bending magnets is used.

⇒ **5-line equation**
(one per Linac4 destination)

Action:
- Pulse the pre-chopper and for redundancy reasons,
    Pulse chopper; a few ns rise-time and
    Disable start timing of PSB RF

Beam to PS	Beam to PSB	Beam to LBS	Beam to LBE	Beam to Dump	Interlock Element	Ch.
1	1	1	1	1	SIS	0
1	1	1	1	1	Linac4 OK	1
0	0	0	0	1	AQN L4T.MBH_DUMP	2
×	×	×	×	1	L4Z OK	3
1	1	1	1	0	AQN L4T.MBH_L4T	4
1	1	1	1	×	Linac4 Transfer OK	5
0	0	0	1	×	AQN LTB.BHZ40_LBE	6
×	×	×	1	×	LBE OK	7
0	0	1	0	×	AQN LTB.BHZ40_LBS	8
×	×	1	×	×	LBS OK	9
1	1	0	0	×	AQN LTB.BHZ40_PSB	10
1	1	×	×	×	PSB Injection OK	11
1	1	×	×	×	PSB OK	12
1	×	×	×	×	Destination PS	13
1	×	×	×	×	PS OK	14
1	1	1	1	1	Choppers Beam_Permit	OUT

BIS Linac4 (3/4) : Slave BIC 'Linac4 OK'
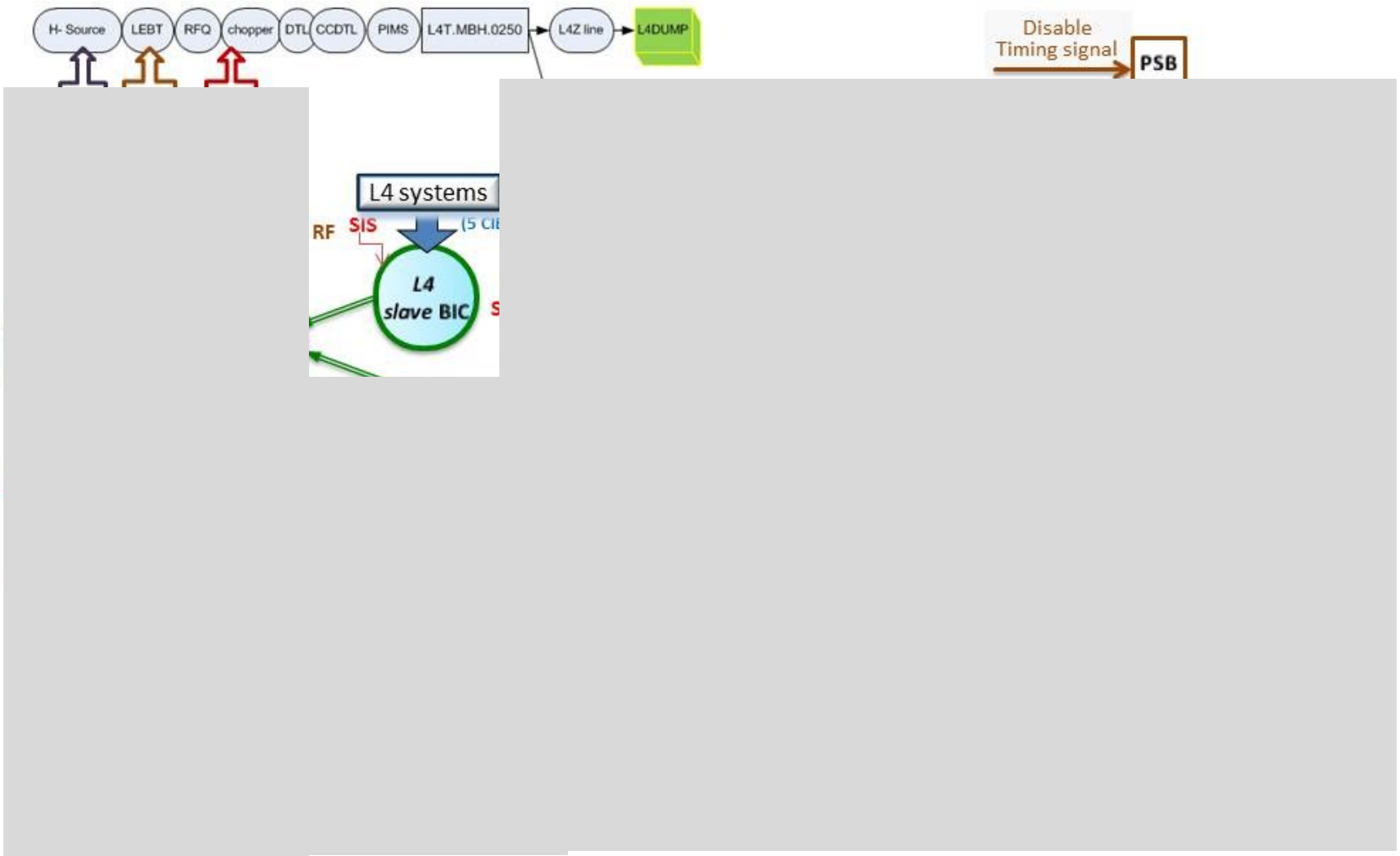
Slave BIC 'Linac4 OK'

Role: Gathers the valid conditions of the major elements installed from the DTL up to the 1st bending magnet.

Action:
- Input for Master BIC 'Choppers'

When its local BEAM_PERMIT is TRUE, this slave BIC issues the condition 'Linac4 OK', which is a necessary input condition for the 'Choppers' Master BIC.

This condition is required for any of the 5 Linac4 beam destinations.

	Interlock Element	Ch.
⅃	SIS	0
⅃	External Conditions (full pulse)	1
⅃	L4 Vacuum Valves + L4T.VVGS.0101	2
⅃	BLMs L4+L4Z	3
⅃	L4 RF	4
⅃	WIC L4	5
×	not used	6
×	not used	7
×	not used	8
×	not used	9
×	not used	10
×	not used	11
×	not used	12
×	not used	13
×	not used	14
⅃	Linac4 OK	OUT

24

BIS Linac4 (3/4) : Slave BIC 'L4Z OK'

Slave BIC 'L4Z OK'

Role: The **'L4Z'** slave BIC gathers the valid conditions for the elements installed after the 1st horizontal bending magnet up the Linac4 dump.

Action:
- Input for Master BIC 'Choppers'

When its local BEAM_PERMIT is TRUE, this slave BIC issues the condition 'L4Z OK'.
This condition is required for **only the 'Beam to Dump' destination**

	Interlock Element	Ch.
↱	SIS	0
↱	L4Z Dump OK	1
↱	L4Z Dump WD	2
↱	L4Z Vacuum Valve	3
✗	not used	4
✗	…	…
✗	not used	14
↱	L4Z OK	OUT

SIS conditions

SIS LINAC4
LINAC4

Equipment Name	Conditions
Cooling Linac4 Dump	L4 Dest: L4DUMP
Cooling LBS Dump	L4 Dest: LBS
Cooling LBE Dump	L4 Dest: LBE
Cooling LBS Slit	L4 Dest: LBS
Debuncher	L4 Dest: LBS, LBE, PSB
AQN LT.BHZ20	L4 Dest: LBS, LBE, PSB
AQN LT.BHZ30	L4 Dest: LBS, LBE, PSB

SIS BOOSTER INJECTION
BOOSTER, PS TRANSFER + ISOLDE

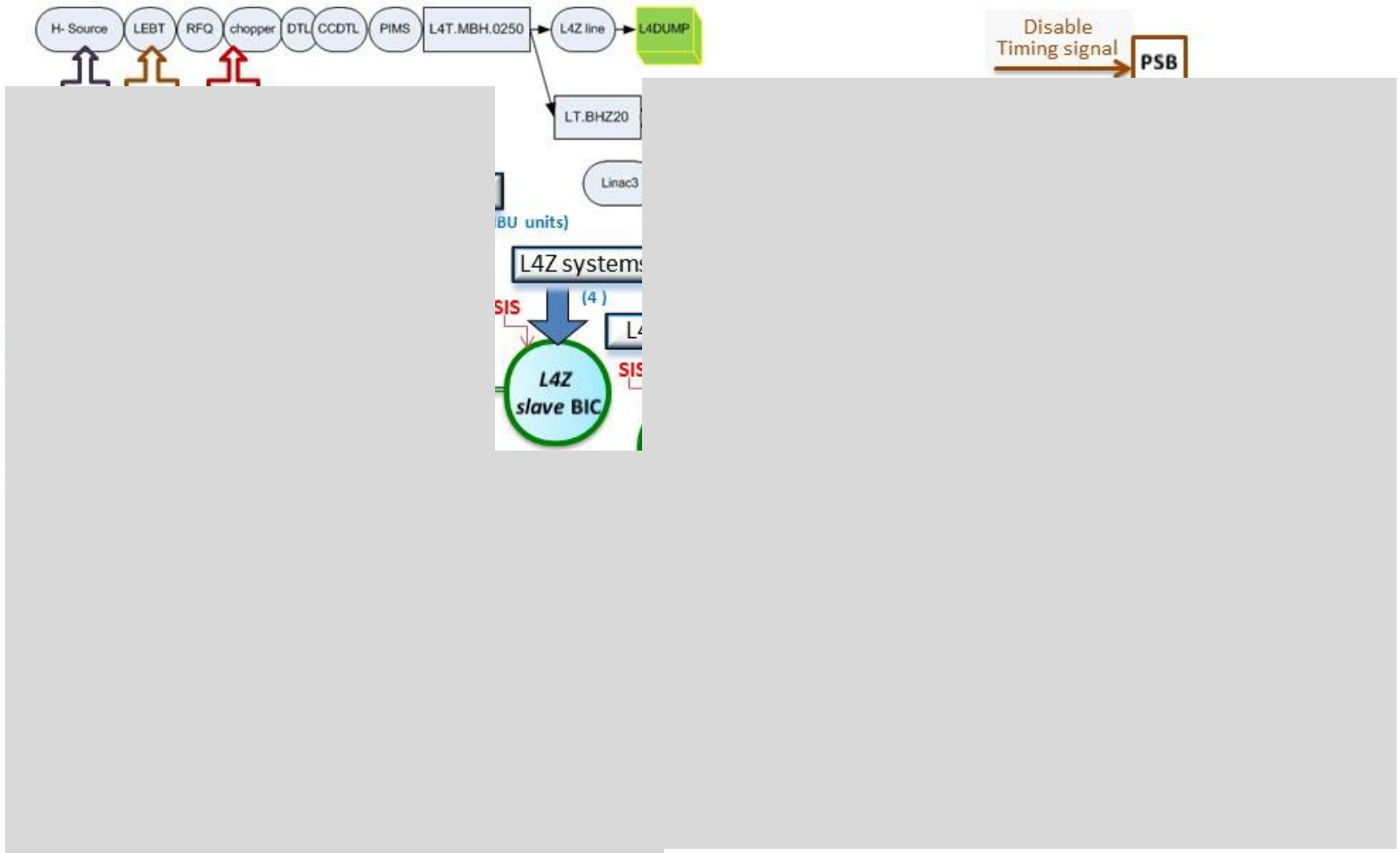| Equipment Name	Conditions	Threshold
Cooling H°/H⁻ Dump	L4 Dest: PSB	
Cooling head dump	L4 Dest: PSB	
AQN BI.DVT40	L4 Dest: PSB	
AQN BI.BVT	L4 Dest: PSB	
Cooling PSB Dump	PSB Dest: BDump	
AQN BT.BHZ10DUMP	PSB Dest: BDUMP, ISOGPS, ISOHRS	fixed dep. on energy
AQN BT.BHZ10PS	PSB Dest: PS	fixed
AQN BTY.BVT101DUMP	PSB Dest: BDUMP	fixed dep. on energy
AQN BTY.BVT101ISOLDE	PSB Dest: ISOGPS, ISOHRS	fixed dep. on energy
AQN BTY.BVT301GPS	PSB Dest: ISOGPS	fixed dep. on energy
AQN BTY.BVT301HRS	PSB Dest: ISOHRS	fixed dep. on energy
AQN BTY.BVT116	PSB Dest: ISOGPS, ISOHRS	editable
AQN BTY.BHZ308	PSB Dest: ISOHRS	editable
AQN BTY.QDE209	PSB Dest: ISOGPS	editable
AQN BTY.QFO210	PSB Dest: ISOGPS	editable
GPS Intensity averaged	PSB Dest: ISOGPS	editable
AQN BTY.DHZ211	PSB Dest: ISOGPS	editable
AQN BTY.DVT212	PSB Dest: ISOGPS	editable
AQN BTY.QDE321	PSB Dest: ISOHRS	editable
AQN BTY.QFO322	PSB Dest: ISOHRS	editable
HRS Intensity averaged	PSB Dest: ISOHRS	editable
AQN BTY.DHZ323	PSB Dest: ISOHRS	editable
AQN BTY.DVT324	PSB Dest: ISOHRS	editable

– Action depending on Master BIC affiliation

– Above lists not exhaustive!

BIS layout during the different Linac4 commissioning phases

The Linac4 basic architecture

Commissioning steps of the Linac4 BIS

- BIS will be deployed in accordance with the global Linac4 schedule which includes five commission phases: 3MeV, 12MeV, 50MeV, 100MeV and 160MeV.

- Defined in Engineering Specification (EDMS # 1310007)

- It describes the steps
  - to deploy the different beam interlock controllers
  - and to identify the connected systems which will be required for each phase of the commissioning.

CERN
CH-1211 Geneva 23
Switzerland

the Linac4 project

EDMS NO.	REV.	VALIDITY
1310007		

REFERENCE
L4-CIB-ES-0005

Date: 2014-02-24

Engineering Specification

THE COMMISSIONING STEPS OF THE LINAC4 BEAM INTERLOCK SYSTEM

ABSTRACT:

The beam interlock system for Linac4 and its transfer lines to the PSB will be deployed in accordance with the global Linac4 schedule which includes five commission phases: 3MeV, 12MeV, 50MeV, 100MeV and 160MeV.

This document describes the steps to deploy the different beam interlock controllers and to identify the connected systems which will be required for each phase of the commissioning.

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Example#1: the required configuration of the 'Source RF ' Master BIC for 12 MeV commissioning phase…

3.3.2 Availability of the USER_PERMITS for 12 MeV commissioning phase

For the 12 MeV commissioning phase the 'Source RF Master BIC' obviously needs to stay available (see Figure 8). As written above, instead of using the 'Choppers Master BIC' with the 'Linac4 BIC' as slave and as its only entry, it is proposed to install the 'Linac4 BIC' alone, whose BEAM_PERMIT should act on Pre-chopper and Chopper.

0	1	2	3	4	5	6	7	8	9	10	11	12
SIS	Source Internal	Source HV	Pre-chopper	Source Beam Stoppers Out/Moving	Source Beam Stoppers In	Chopper	L4 Low Energy Watchdog	L4 Low Energy Vacuum Valves	L4L. QUADS4Chopper	RFQ	Commissioning Dump status	L4 Operator Veto
1	1	1	1	1	0	1	1	1	1	1	1	1
1	1	1	x	0	1	x	x	x	x	x	x	x

Figure 8: The 'Source RF' Master BIC needs to stay available throughout all Linac4 commissioning phases.

Note: Inputs #1, #2, #6 and #11 of the 'Source RF' Master BIC were not available during the 3 MeV commissioning phase.

For the 12 MeV commissioning phase, the "Commissioning Dumps status" USER_PERMIT signal becomes essential and should be not anymore strapped.

Bruno Puccio / Technical Workshop on the Beam Interlock System(s) for CERN and ESS (3rd and 4th of February 2015)

Example#2 : the required readiness of interfaces with the Beam Current Transformers all along the commissioning phases

7.5.2 INTERFACES WITH THE BCT system

For each commissioning step, the following table lists the required readiness of the different USER_PERMIT links provided by the BCT system:

USER_PERMIT (short name)	BIC name	3MeV	12MeV	50Mev	100MeV	160MeV	comments
Low-energy watchdog	SOURCE RF (Master)	Y	Y	Y	Y	Y	the corresponding USER_PERMIT interface is required since the 3 MeV phase
Linac4 dump watchdog	L4Z	N					the corresponding USER_PERMIT interface is not required for the 3 MeV phase
L4T watchdog	L4 Transfer	N	N	N	N		" "
BI watchdog	L4 Transfer	N	N	N	N	N	the corresponding USER_PERMIT interface is not required for Linac4 commissioning
LBE watchdog	LBE	N	N	N	N		" "

Hardware modules used for the Linac4 (Tree Architecture)

The copper link between Slave BIC and Master BIC (1/2)

The CIBI module is used to transmit

the local Beam_Permit signals of the Slave BIC to the Master BIC
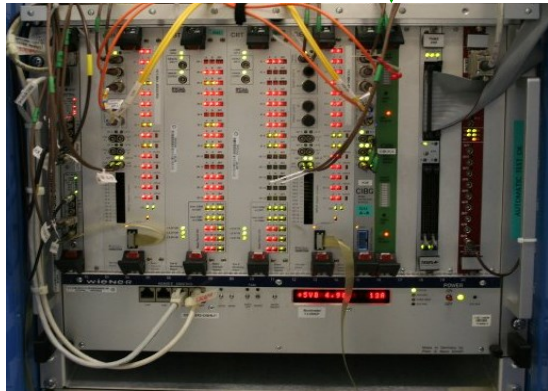
This CIBI board has been designed to receive a differential input signal and to convert this signal in a single ended voltage source with the appropriate output current.
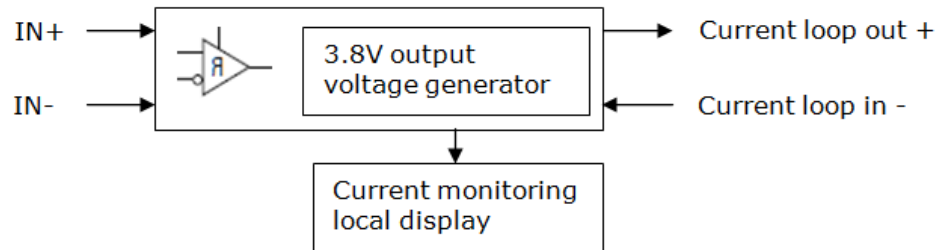
Figure 1 : CIBI functional bloc overview

The card is divided into 2 halves having totally identical functionality.

The "upper part" is used to generate USER_PERMIT_B and the "lower part" is used to generate USER_PERMIT_A.

The two LOCAL_PERMIT signals are routed on the P2 of the VME bus connector.

For redundancy reasons, LOCAL_PERMIT_A and LOCAL_PERMIT_B are individually routed.

CIBI INTERCONNECTION
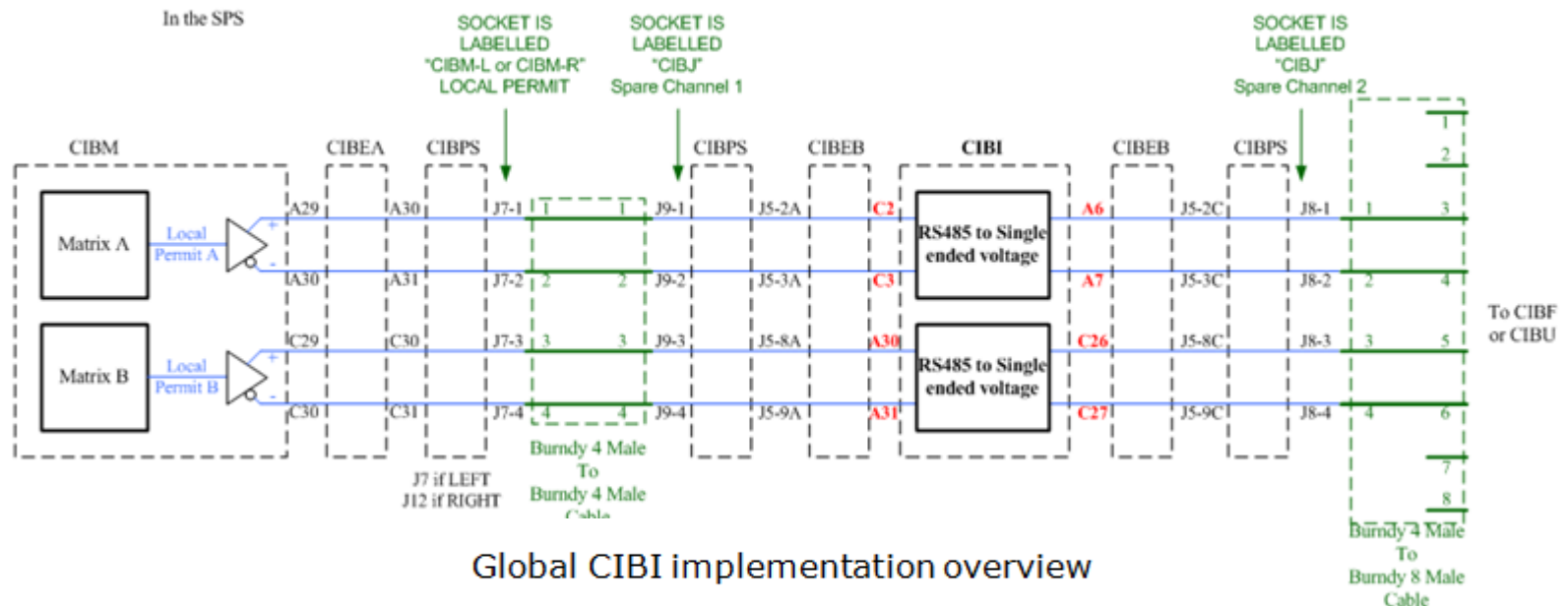
Global CIBI implementation overview

The CIBIT module is used to safely transmit the redundant Beam_Permit signals to **up to 4** Target Systems
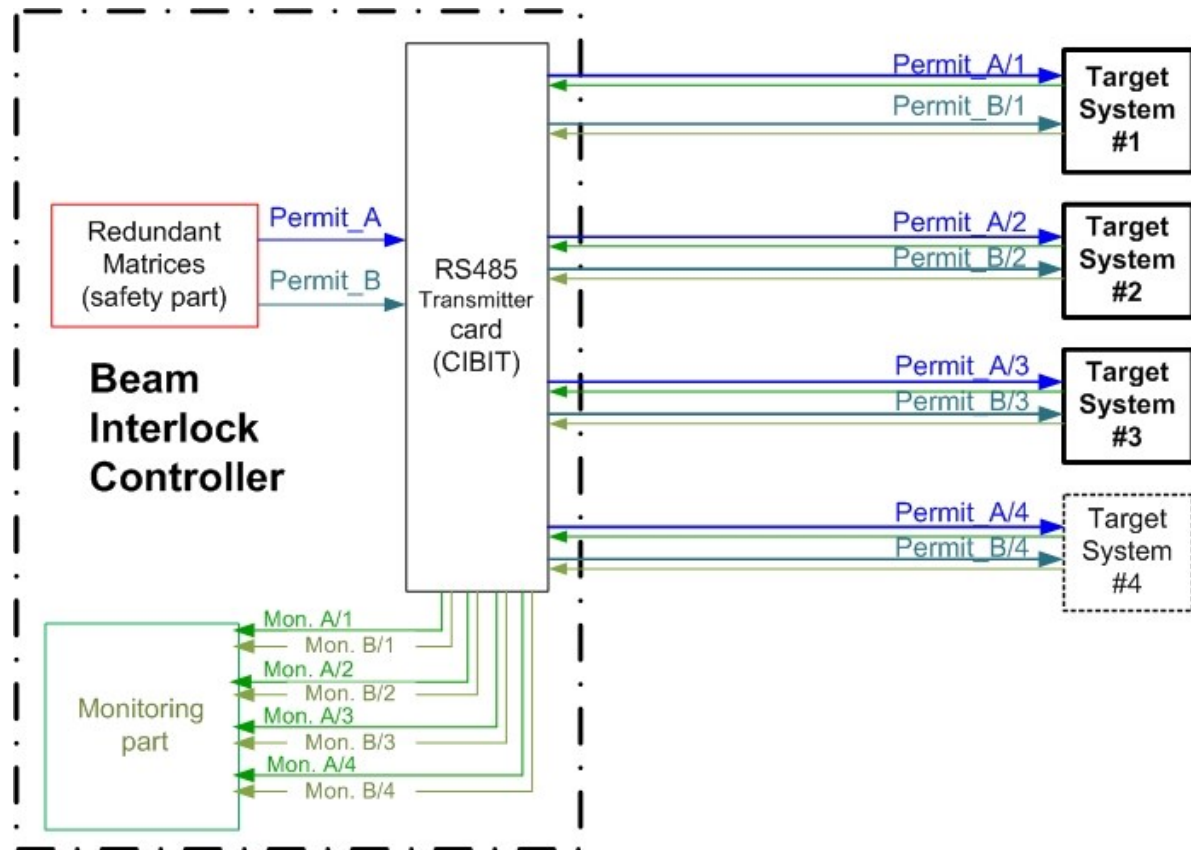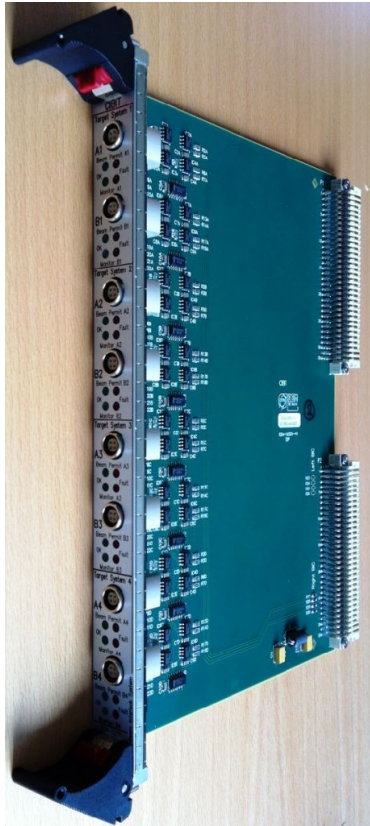
The 'star' topology is used to propagate the Linac4 Beam_Permit signals

Bruno Puccio / Technical Workshop on the Beam Interlock System(s) for CERN and ESS (3rd and 4th of February 2015)

The copper link between a BIC and Target System(s) (2/2)

The [CIBIR card](#) is used to safely receive the redundant Beam_Permit signals inside the Target System electronics

CIBIR IV2 PANEL
00-26908-e0-0004
CIBIR
1V2
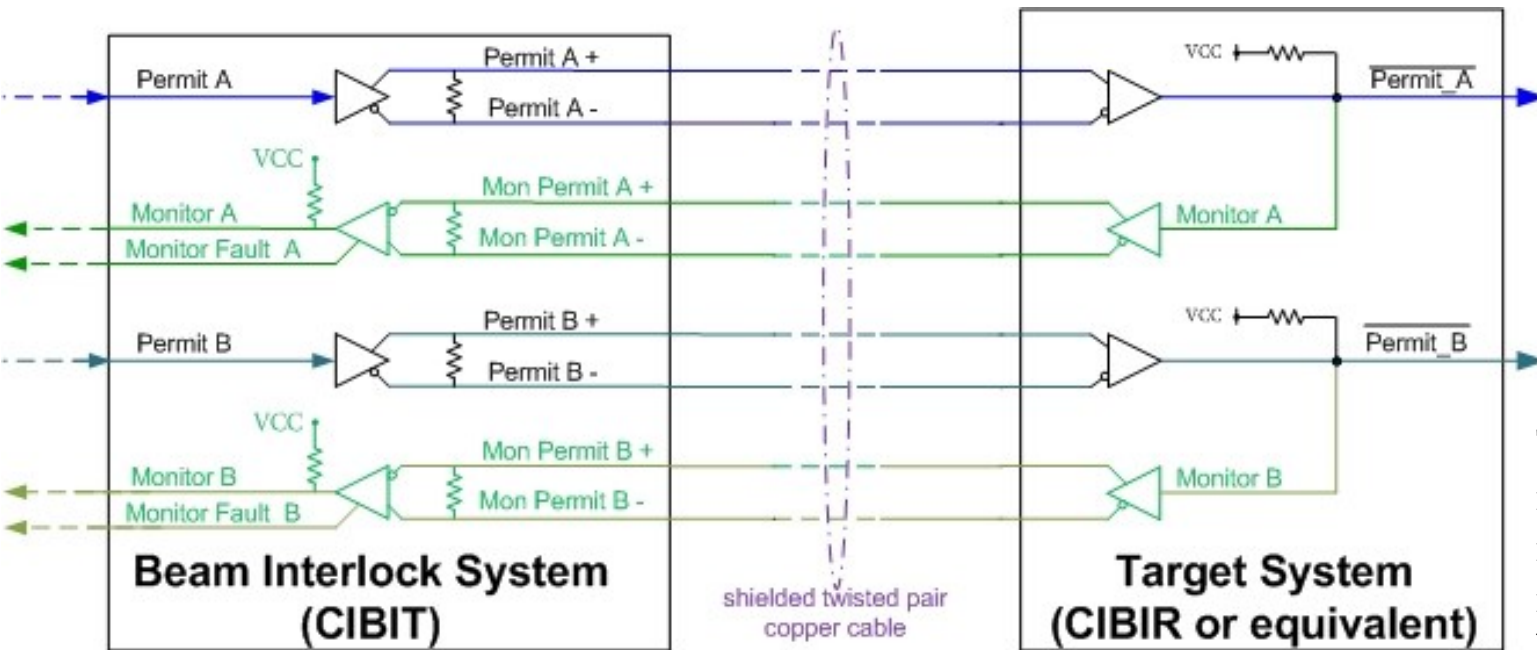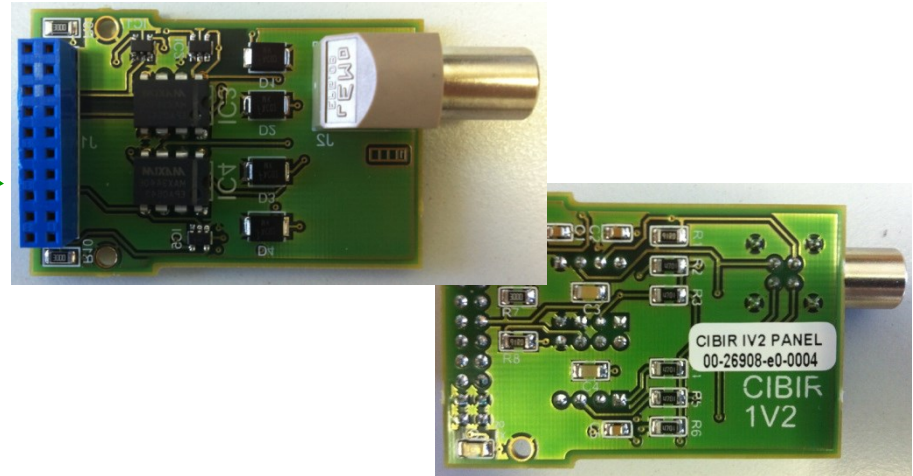
Simplified schematics of the Beam_Permit interface

The CIBIR is a mezzanine card mounted on a motherboard belonging to the *Target System*.

in summary...

BIS @CERN : the standard solution from LHC down to Linac4

❑ **Same Hardware:**

- Fast, Safe, Reliable (initially designed for LHC)
- Standardised interface (CIBU)
- Proven solution
- Cost-effective

❑ **Same Monitoring Software:**

- Unique application in CERN Control room
  for L4, Booster…. SPS, Transfer Lines, LHC
- 100% test coverage
  - Pre-operational checks
  - On–line monitoring
  - Post-operational checks

❑ **Operational flexibility**
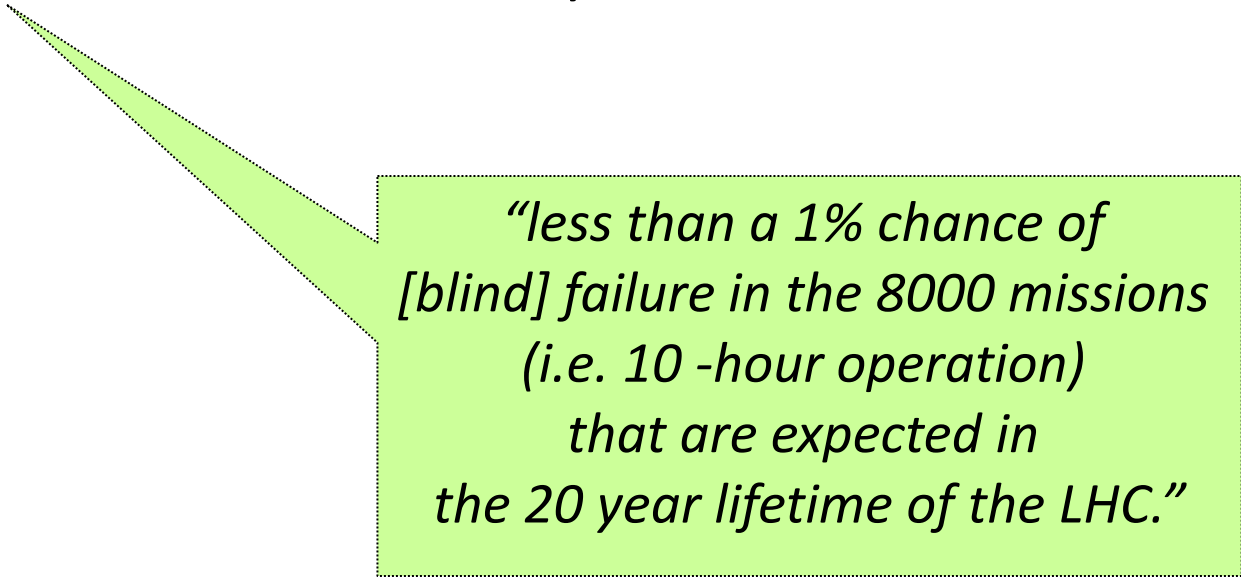
- Software Interlock Inputs
- External Condition signals used as User_Permits
- Masking available on half of input channels

> BIS is more than a safety system: Regarding past experience, it also improves the beam operation efficiency. and it reduces the beam activation as well

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Thank you for your attention

Additional slides

some BIC numbers...

■ **1** ▸ the number of electronic interface type
(CIBU is the unique interface for giving the User Permit)

■ **2** ▸ for twice.... because the BIS is fully redundant
(from User connection up to the Beam Dump triggering input)

■ **3** ▸ <u>SIL3</u> is the estimated safety level

*"less than a 1% chance of
[blind] failure in the 8000 missions
(i.e. 10 -hour operation)
that are expected in
the 20 year lifetime of the LHC."*

Interlocking of the Booster Ejection line

PS Booster

GPS target

HRS target

BTY.BHZ301

BT.BHZ10
BTY.BVT101

BI line

BT line

BTM

BTY line

PSB dump

PS

Ejection Kicker

EJECTION Master BIC

SIS

(7)

(4)

AQN magnet currents

Destination Telegrams

✋ *drawing not to scale*

(1) Beam to Dump
(2) Beam to GPS
(3) Beam to HRS
(4) Beam to PS

	TRUTH TABLE	(1)	(2)	(3)	(4)
0	SIS	T	T	T	T
1	**AQN BT.BHZ10_BDUMP**	T	F	F	F
2	**AQN BT.BVT101_BDUMP**	T	F	F	X
3	**Destination PSB Dump**	T	F	F	F
4	**AQN BT.BHZ10 _ISOLDE**	X	T	T	F
5	**AQN BT.BVT101_ISOLDE**	T	F	F	X
6	**AQN BTY.BHZ301 _GPS**	X	T	F	X
7	**Destination ISOGPS**	F	T	F	F
8	**AQN BTY.BHZ301_HRS**	X	T	T	X
9	**Destination ISOHRS**	F	F	T	F
10	**AQN BT.BHZ10_PS**	F	F	F	T
11	**Destination PS**	F	F	F	T
	Beam_Permit	T	T	T	T

Beam_Permit given to only the extraction kicker
The planned action is to disable it when the signal is "FALSE"

Master BIC 'PSB Ejection'

Role: Assure valid conditions for the 4 PSB destinations: PSB dump, ISOGPS, ISOHRS, & PS ring.

To define these destinations, the magnet current acquisitions of the corresponding bending magnets is used.

$\Rightarrow$ **4-line equation** (one per beam destination)

Channel	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	OUT
Interlock Element	SIS (currently not used)	Destination PSB Dump	Destination ISOGPS	Destination ISOHRS	Destination PS	AQN BT.BHZ10 DUMP	AQN BT.BHZ10 PS	AQN BTY.BHZ301 GPS	AQN BTY.BHZ301 HRS	AQN BTY.BVT101 DUMP	AQN BTY.BVT101 ISOLDE					PSB Ejection Permit
	1	1	0	0	0	1	0	x	x	1	0					1
	1	0	1	0	0	1	0	1	0	0	1					1
	1	0	0	1	0	1	0	0	1	0	1					1
	1	0	0	0	1	0	1	x	x	x	x					1

Action: Disable the PSB extraction kickers